GBT Receiver to VEGAS Bank Connection

D. Anish Roshi
NRAO, Green Bank, WV & NTC, Charlottesville, VA

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A block diagram of the VEGAS is shown in Fig. 1. It consists of 8 independent spectrometers working in parallel. Each spectrometer can process dual polarized signal with a usable bandwidth of 1.25 GHz. These spectrometers are referred to as BANKS in the data processing software (eg. GBTIDL) and are named A to H with the polarization input ports named as A1, A2, B1, B2 and so on. The spectrometers are connected to the Converter Racks outputs (port J9) of the GBT. For further details see Roshi et al. (2011).

The mapping of receiver to VEGAS Banks is given in Table 1 & 2. The receiver bandwidth (ie the maximum front-end bandwidth), IF bandwidth and the maximum bandwidth VEGAS can process with the present IF connectivity are given in Columns 1, 2 and 3 respectively. Where ever the processing bandwidth is less than 10 GHz, the IF/receiver system and/or the IF routing needs to be upgraded to utilize the full potential of VEGAS. The text shown in red are new connections to be made through IF router to get the full RF bandwidth processed digitally.

Reference

Roshi et al. 2011, `http://www.gb.nrao.edu/vegas/report/overalldoc.pdf`

Revision History

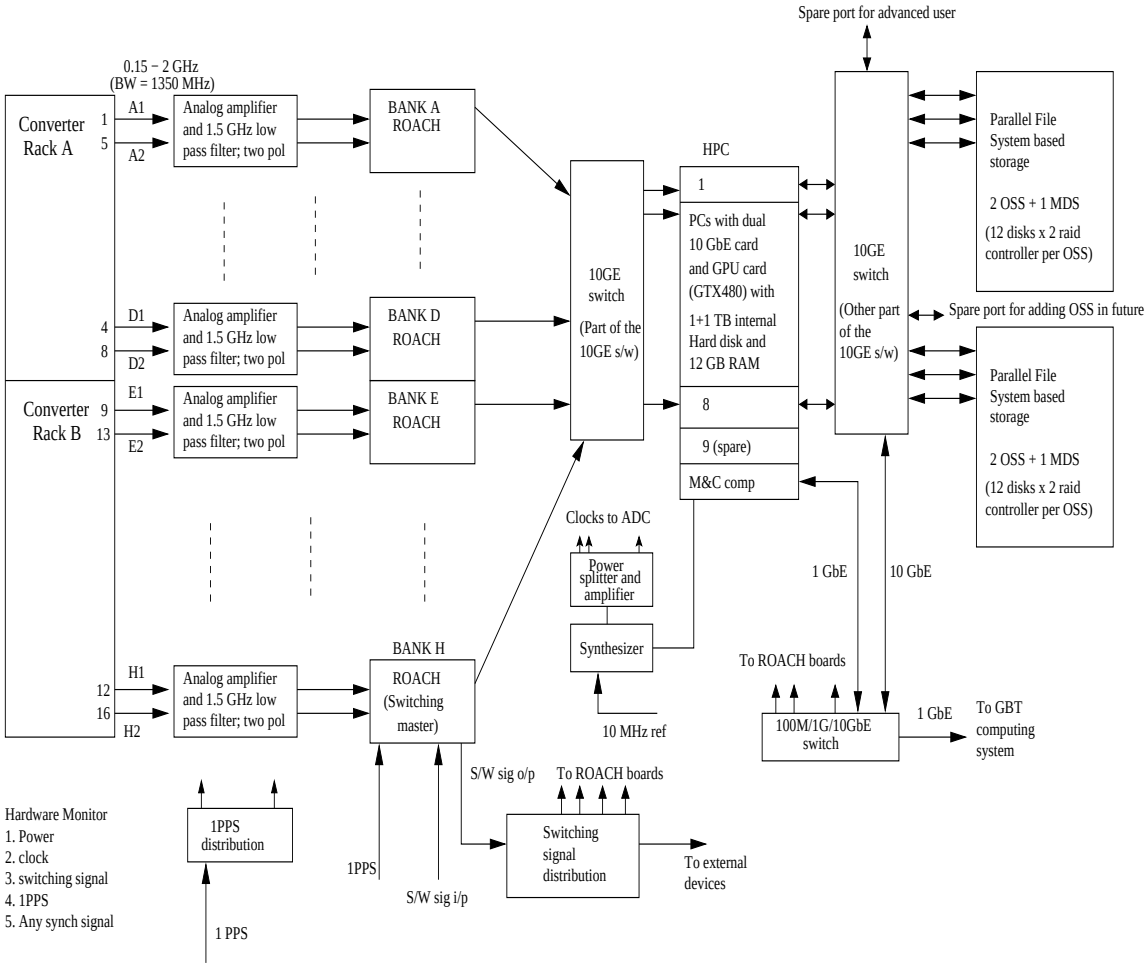

Figure 1: A schematic of the new GBT spectrometer

Table 1: Receiver, Converter Module and VEGAS Bank Mapping

Receiver	Rec BW	IF BW	Dig BW	Converter Module															
Name	(MHz)	(MHz)	(GHz)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PF1_340XL			10	A1	B1	C1	D1					E1	F1	G1	H1				
PF1_340YR			10					A2	B2	C2	D2					E2	F2	G2	H2
PF1_450XL			10	A1	B1	C1	D1					E1	F1	G1	H1				
PF1_450YR			10					A2	B2	C2	D2					E2	F2	G2	H2
PF1_600XL			10	A1	B1	C1	D1					E1	F1	G1	H1				
PF1_600YR			10					A2	B2	C2	D2					E2	F2	G2	H2
PF1_800XL	240		10	A1	B1	C1	D1					E1	F1	G1	H1				
PF1_800YR	240		10					A2	B2	C2	D2					E2	F2	G2	H2
PF2XL	320		10	A1	B1	C1	D1					E1	F1	G1	H1				
PF2YR	320		10					A2	B2	C2	D2					E2	F2	G2	H2
L_XL	650		10	A1	B1	C1	D1					E1	F1	G1	H1				
L_YR	650		10					A2	B2	C2	D2					E2	F2	G2	H2
S_XL	970		10	A1	B1	C1	D1					E1	F1	G1	H1				
S_YR	970		10					A2	B2	C2	D2					E2	F2	G2	H2
C_XL	2150		10	A1	B1	C1	D1					E1	F1	G1	H1				
C_YR	2150		10					A2	B2	C2	D2					E2	F2	G2	H2
X_YR	2400		10	A1	B1	C1	D1					E1	F1	G1	H1				
X_XL	2400		10					A2	B2	C2	D2					E2	F2	G2	H2
Ku_B1R	6000		5/10					A2	B2	C2	D2					E2	F2	G2	H2
Ku_B1L	6000		5/10	A1	B1	C1	D1					E1	F1	G1	H1				
Ku_B2R	6000		5													E2	F2	G2	H2
Ku_B2L	6000		5									E1	F1	G1	H1				

Table 2: Receiver, Converter Module and VEGA Bank Mapping

Receiver	Rec BW	IF BW	Dig BW	Converter Module															
Name	(MHz)	(MHz)	(GHz)	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
KFPA_R1	7500	1800	5													E2	F2	G2	H2
KFPA_L1	7500	1800	5									E1	F1	G1	H1				
KFPA_R2	7500	1800	5					A2	B2	C2	D2								
KFPA_L2	7500	1800	5	A1	B1	C1	D1												
KFPA_R3	7500	1800	5													E2	F2	G2	H2
KFPA_L3	7500	1800	5									E1	F1	G1	H1				
KFPA_R4	7500	1800	5					A2	B2	C2	D2								
KFPA_L4	7500	1800	5	A1	B1	C1	D1												
KFPA_R5	7500	1800	5					A2	B2	C2	D2								
KFPA_L5	7500	1800	5	A1	B1	C1	D1												
KFPA_R6	7500	1800	5					A2	B2	C2	D2								
KFPA_L6	7500	1800	5	A1	B1	C1	D1												
KFPA_R7	7500	1800	5													E2	F2	G2	H2
KFPA_L7	7500	1800	5									E1	F1	G1	H1				
KFPA_R1	7500	7500	5/10					A2	B2	C2	D2					E2	F2	G2	H2
KFPA_L1	7500	7500	5/10	A1	B1	C1	D1					E1	F1	G1	H1				
KFPA_R2	7500	7500	5													E2	F2	G2	H2
KFPA_L2	7500	7500	5									E1	F1	G1	H1				
Ka_M	13500	6000	5									E1	F1	G1	H1				
Ka_N	13500	6000	5													E2	F2	G2	H2
Ka_S (R)	13500	6000	5	A1	B1	C1	D1												
Ka_T (L)	13500	6000	5					A2	B2	C2	D2								
Q_R1	10600	4000	5					A2	B2	C2	D2								
Q_L1	10600	4000	5	A1	B1	C1	D1												
Q_R2	10600	4000	5													E2	F2	G2	H2
Q_L2	10600	4000	5									E1	F1	G1	H1				
W_X2	24000	6000	5									E1	F1	G1	H1				
W_Y2	24000	6000	5													E2	F2	G2	H2
W_LX1	24000	6000	5	A1	B1	C1	D1												
W_RY1	24000	6000	5					A2	B2	C2	D2								