

# Green Bank Instrumentation circa 2030

Dan Werthimer and 800 CASPER Collaborators

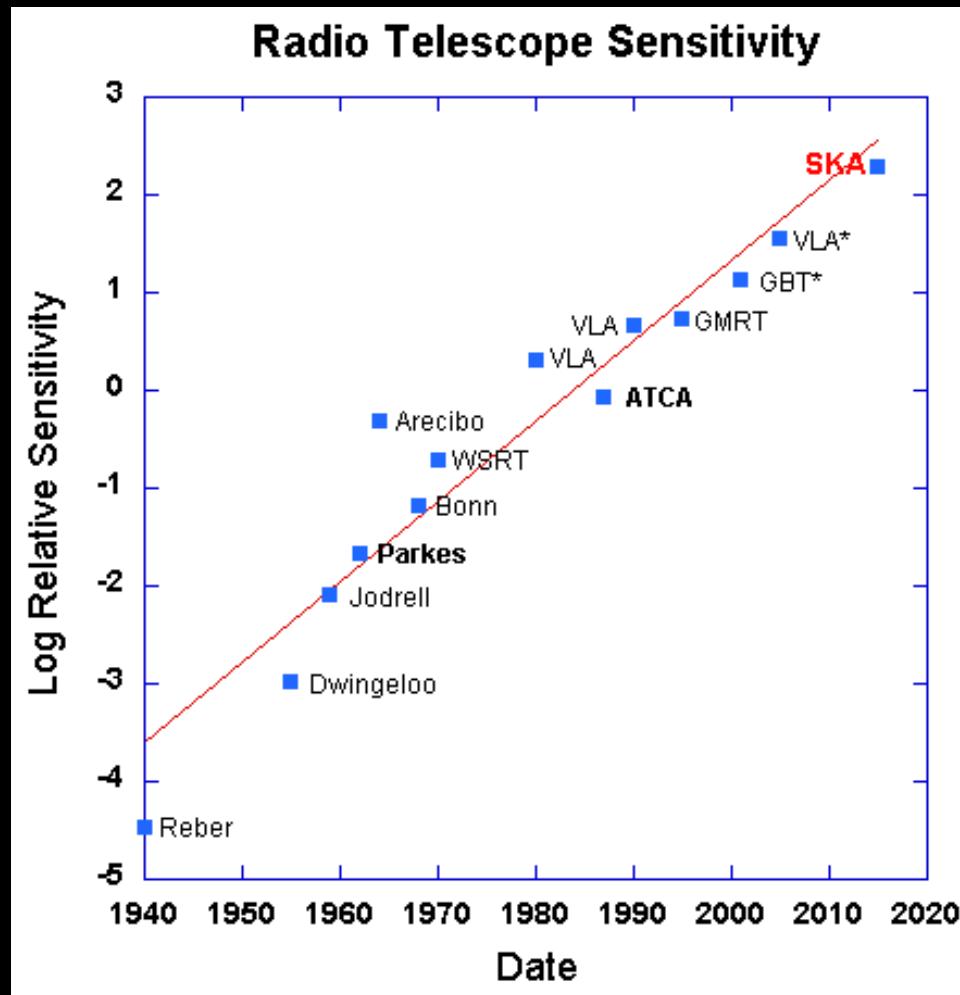
<http://casper.berkeley.edu>



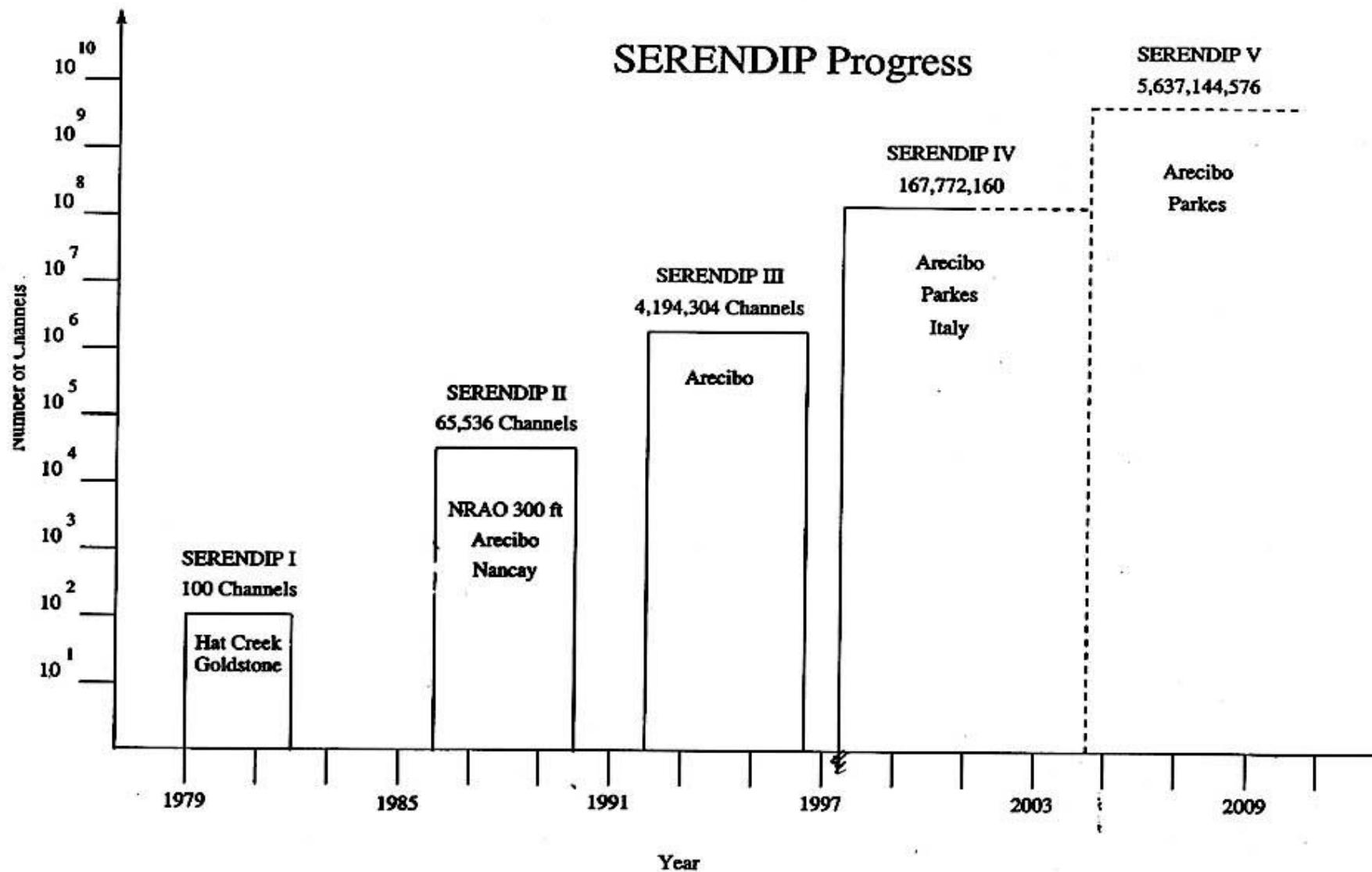
# Upcoming **Nobel Prizes** with Radio Instrumentation

- Gravitational Wave Detection (pulsar timing)  
(eg: this morning's LIGO announcement)
- Black Hole Physics (Event Horizon Telescope...)
- How did the First Stars and Galaxies Form ? (EOR)
- What causes FRB's ?
- Measure baryon density of universe using FRB's
- B mode polarization CMB
- Discover ET

# Radio Telescope Sensitivity doubles every 3.6 years



# Moores Law – Instruments using FPGA's: 2X per year (1,000,000 over 20 years)

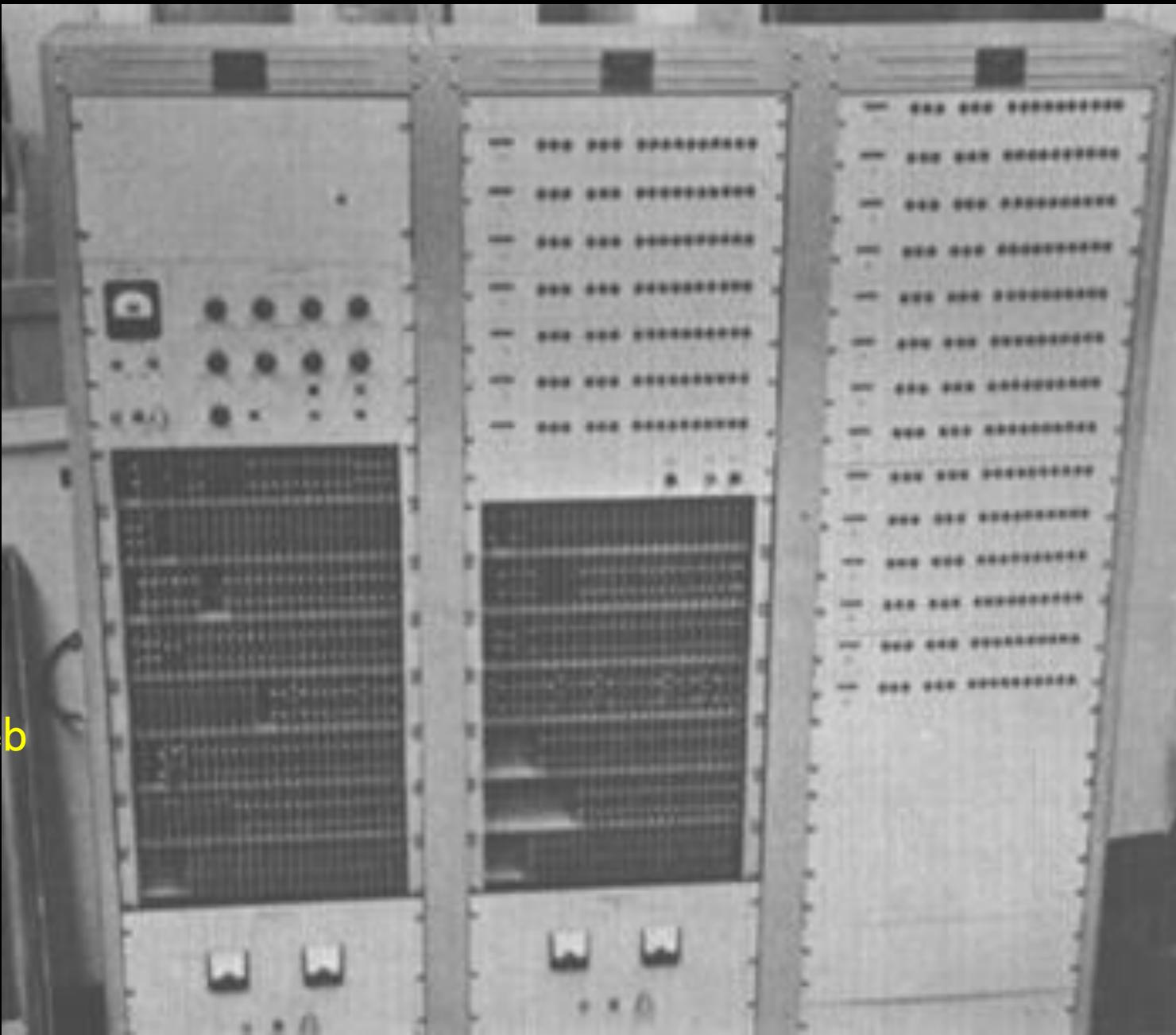


## 1960 – First Radio Astronomy Digital Correlator

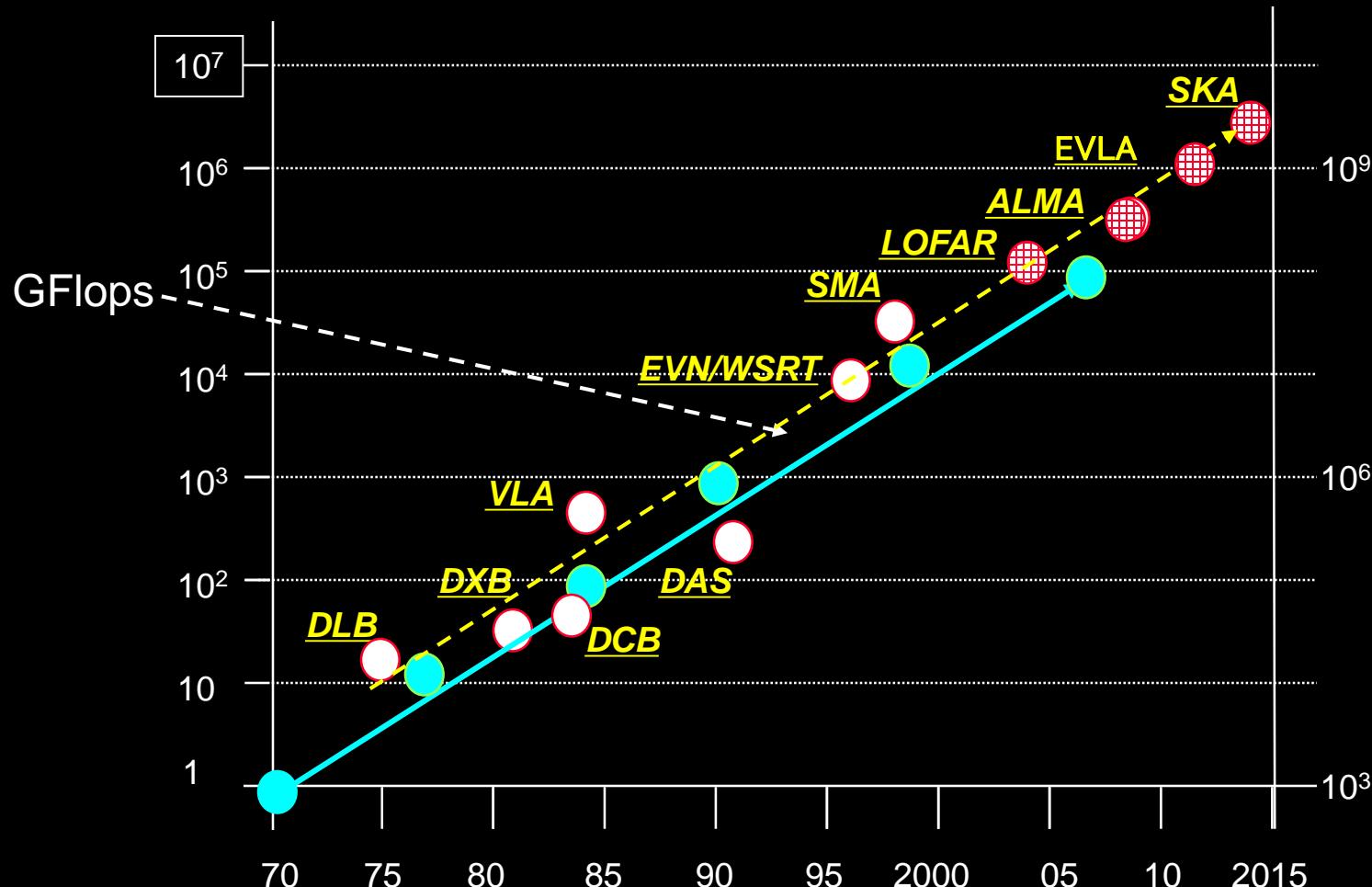
21 lags  
300kHz clock  
discrete transistors

\$19,000

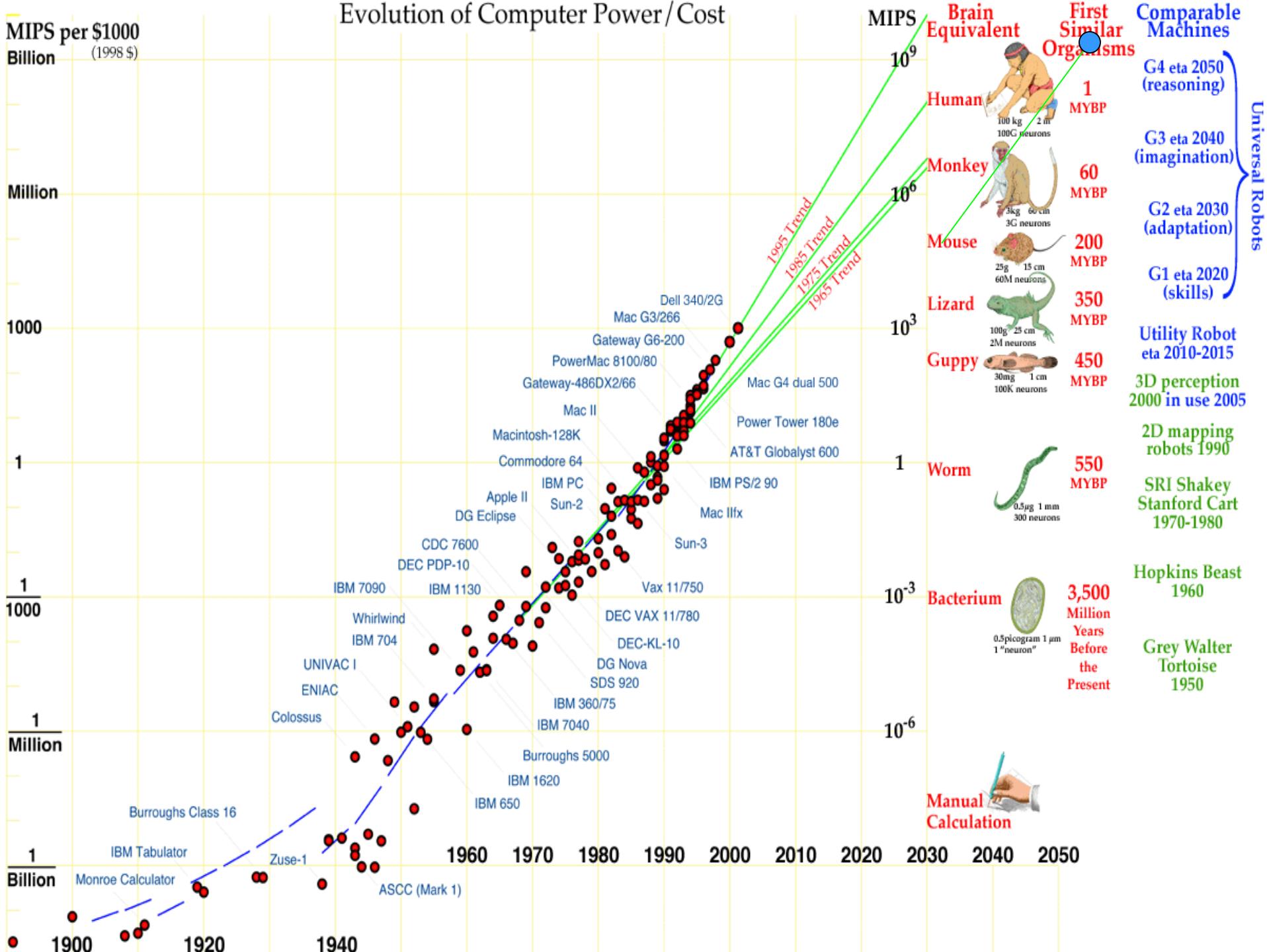
Sandy Weinreb



# *Correlator processing power*



source: Arnold van Ardenne



# CASPER Philosophy and Religion

## Design Observatories with Plan for Exponential Growth in Digital Processing

- Digital Backend should be replaced every 5 years (keep software, toss old - buy new hardware)
- DSP Part of Operating Costs, not construction costs

# expect (plan for)

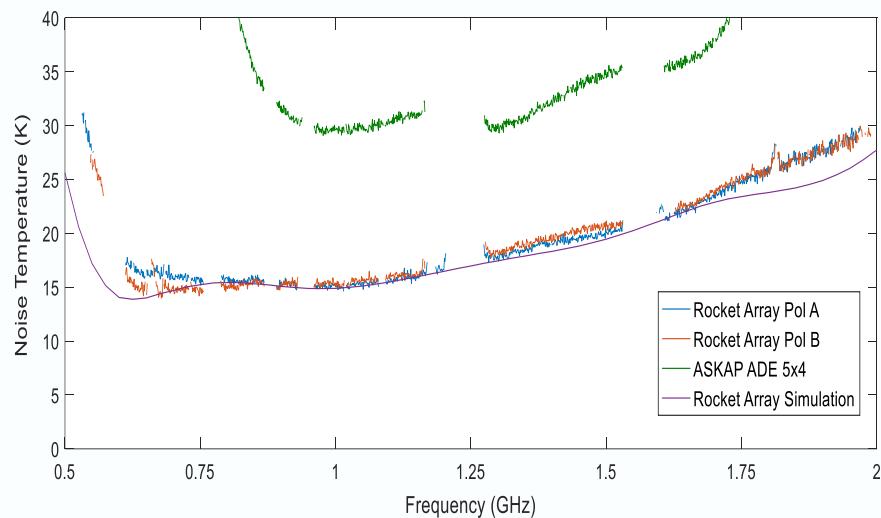
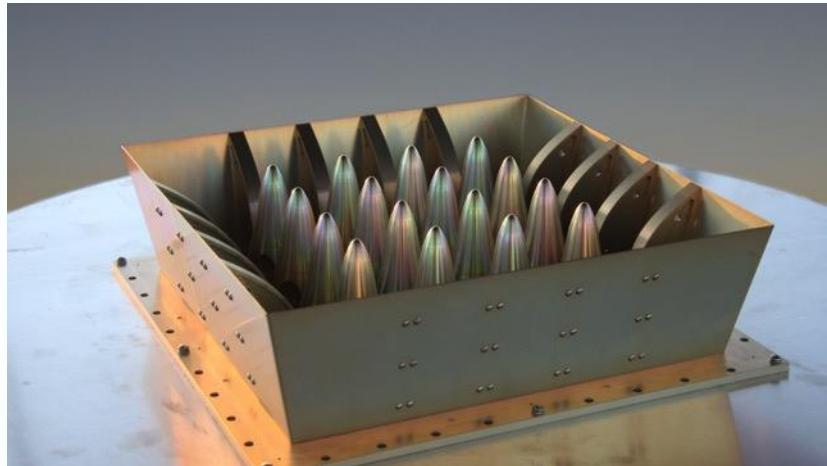
- 100 GHz bandwidth
- 1000 to 1M antenna arrays
- 1000 to 1M beams (commensal experiments)
- 6:1 or 20:1 ? Feeds and receivers
- phased array feeds with low Tsys ?
- Observatory removes RFI (part of instrument)

# GBO Receivers circa 2025

- 0.6 to 4 GHz 6:1 22K single beam
- 4 to 24 GHz 6:1 22K single beam
- 20 to 120 GHz 6:1 single beam
- 0.6 to 2 GHz Phased Array Feed 20K 1,000 beams
- 75 – 115 GHz 800 beam horn array (ultra-argus)

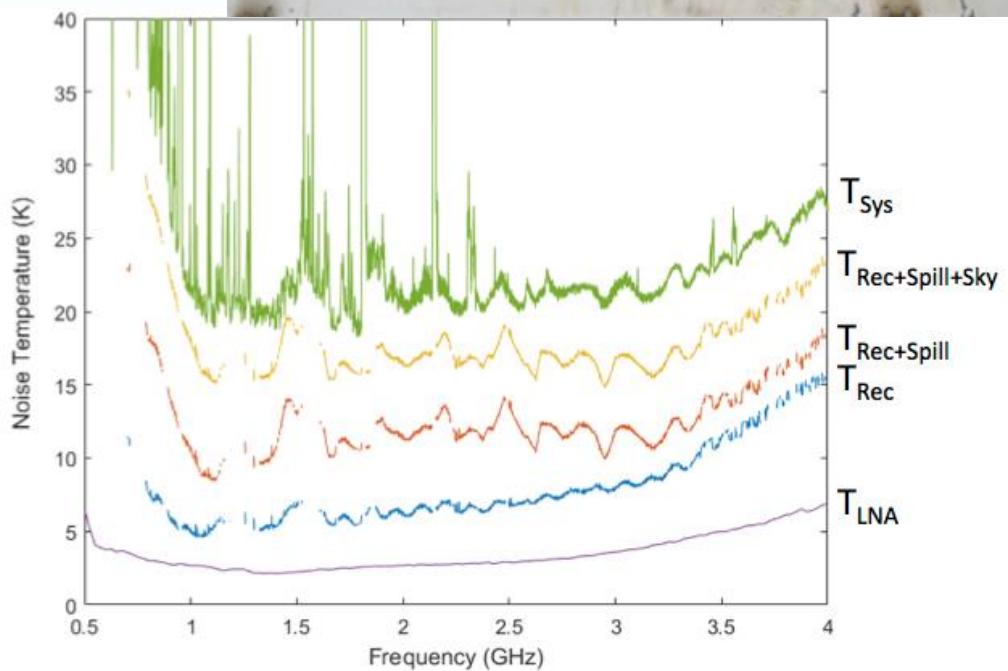
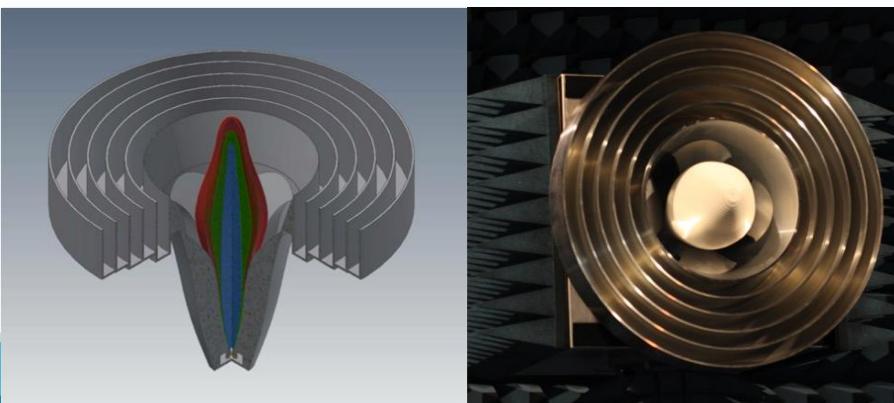
# “Rocket” PAF

- Next generation PAF
  - “rocket” elements; “edge” elements
- Superb matching with LNA
  - Key to improved performance
  - Noise Temp due to uncooled LNAs
- 4x5 prototype constructed
  - tested as aperture array
  - ~15K better than equivalent ASKAP tests
  - Tested on Parkes
    - Measurements affected by RFI
- Design better suited to cooling
  - → **CryoPAF funding proposal**
    - Full 94 dual-pol array + ASKAP back-end
    - Expected T<sub>sys</sub> <20K !?

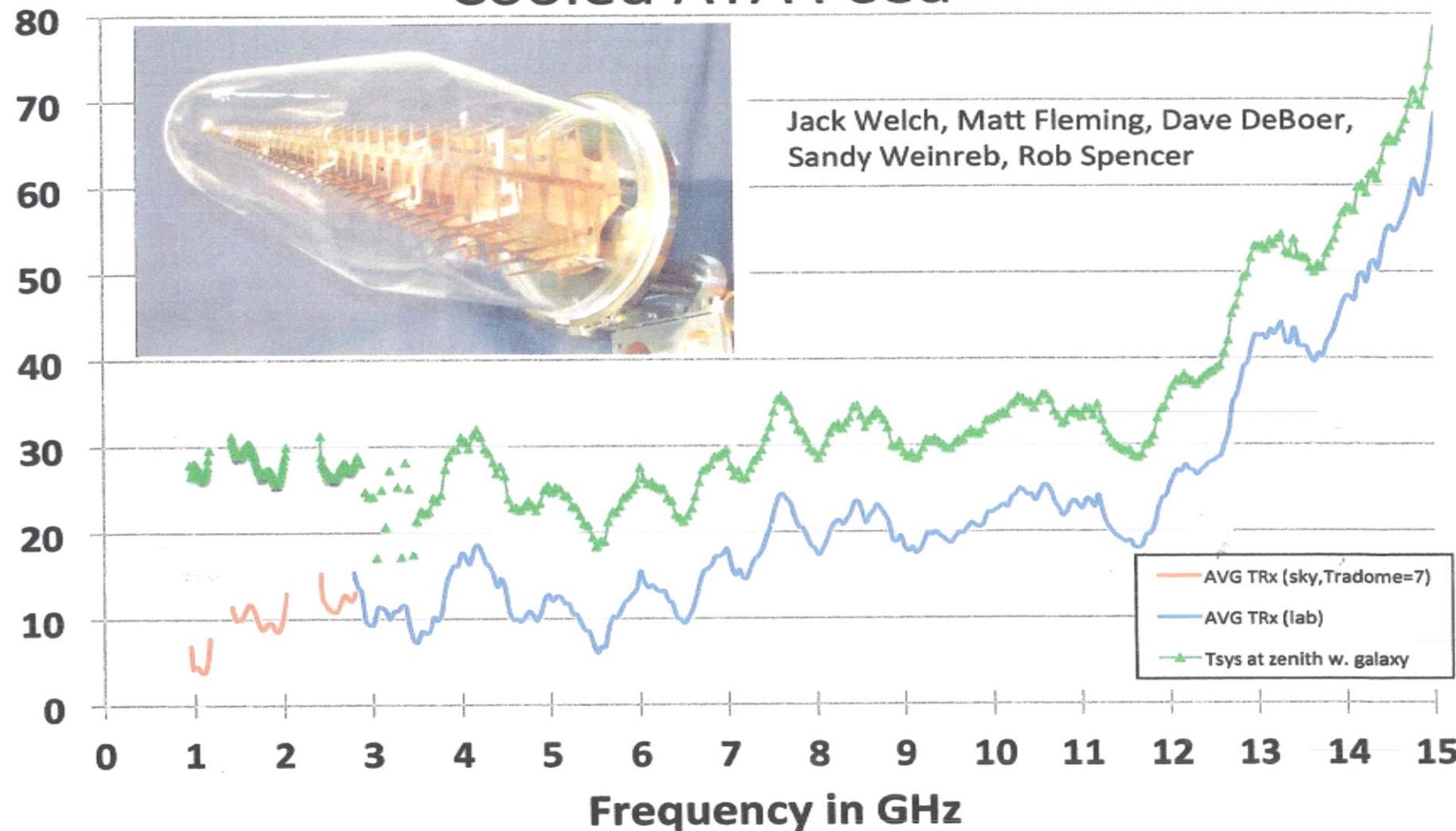


# Parkes UltraWideBand system

- Quadridge structure with dielectric spear
- 0.7–4.0 GHz, T<sub>sys</sub> ~22K, SEFD ~35 Jy
- First light Aug 2017, commission late 2017
- Sampler/digitiser and timing (Back-end)
  - 4 Gsps (2 GHz bands)
- Ethernet switch and GPU cluster
  - Installed 2016 & used PAF@Parkes
  - Software - collaborators
- RFI mitigation built-in – reference antenna



# Measured Receiver Temperature & Tsys at Zenith Cooled ATA Feed

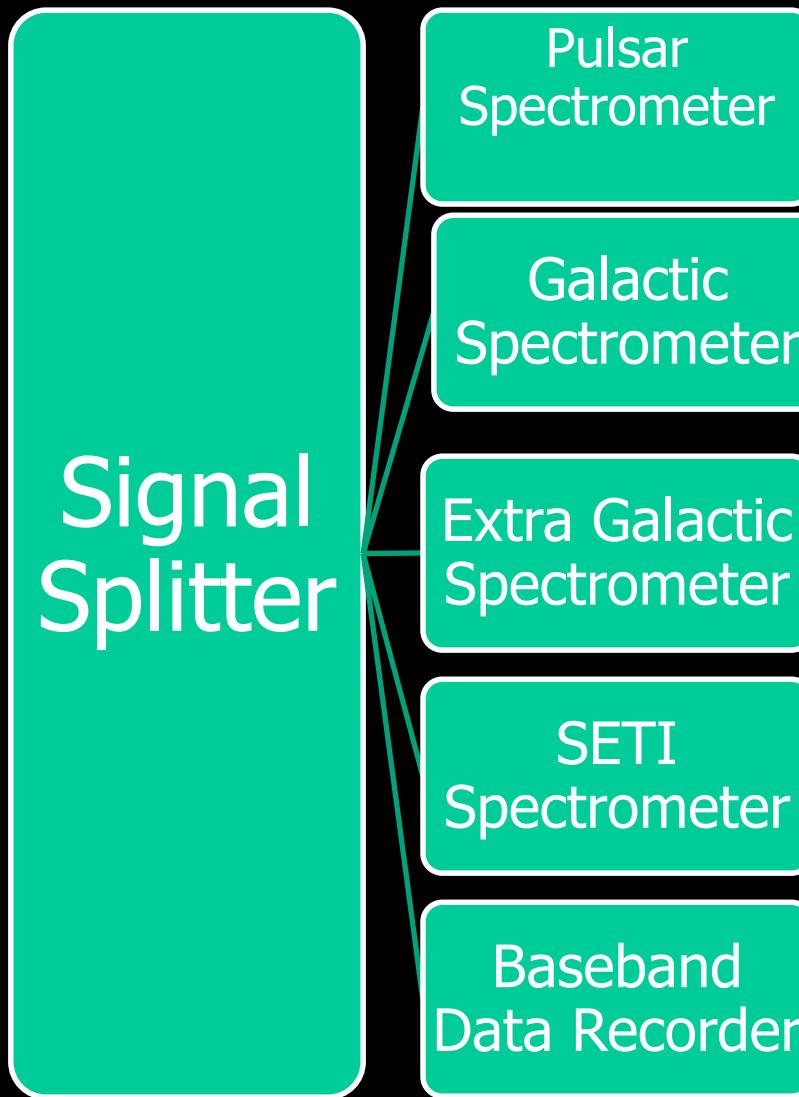


# Instrument Architectures

- Scalable
- Upgradeable
- Flexible
- General and Multi-Purpose
- Fault Tolerant

# Simultaneous Digital Backends

## Piggyback, Commensal, Sky Surveys



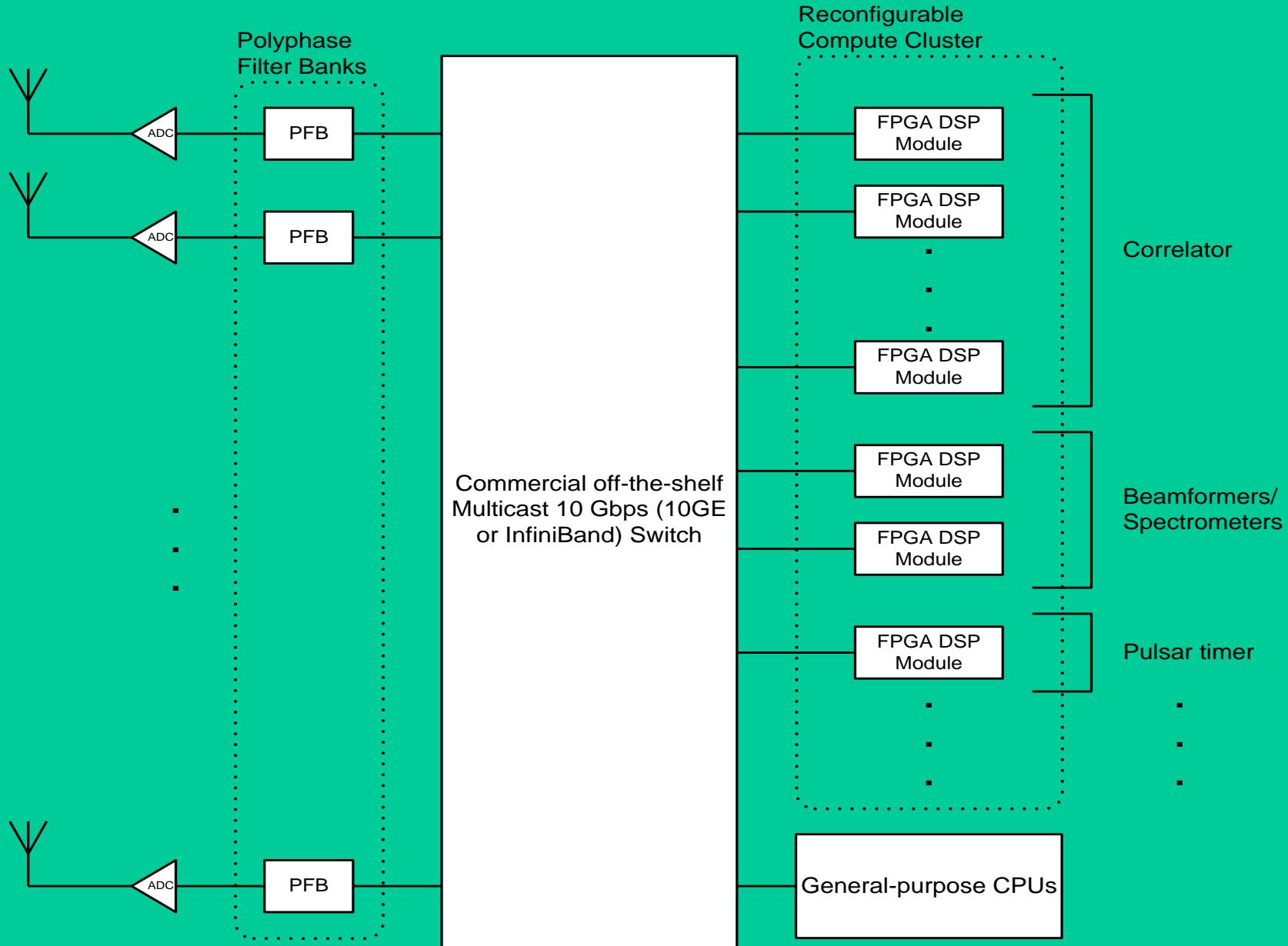
Analog Power Splitters

or

Digital Data Splitter

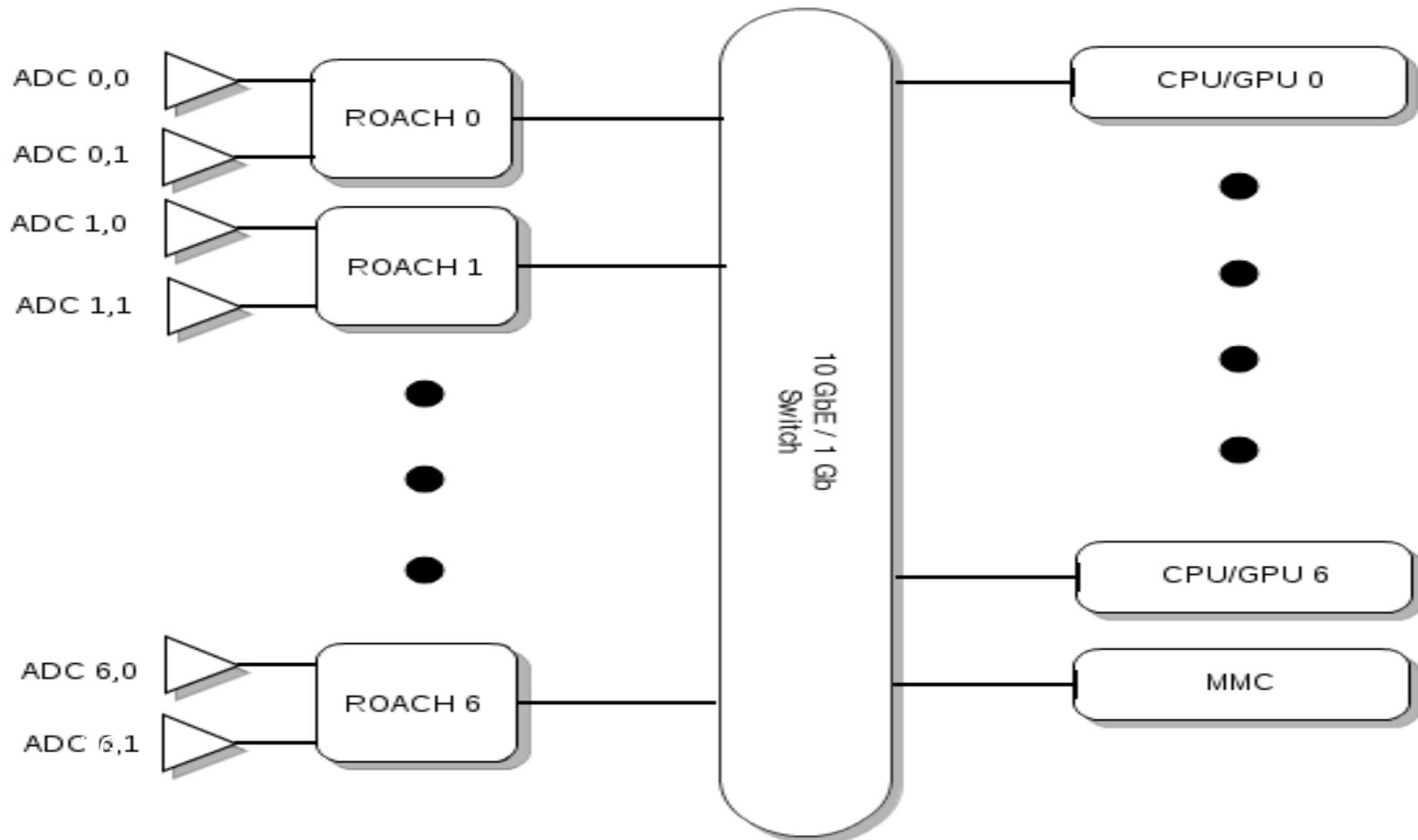
# CASPER General Purpose Architecture

## Dynamic Allocation of Resources, need not be FPGA based



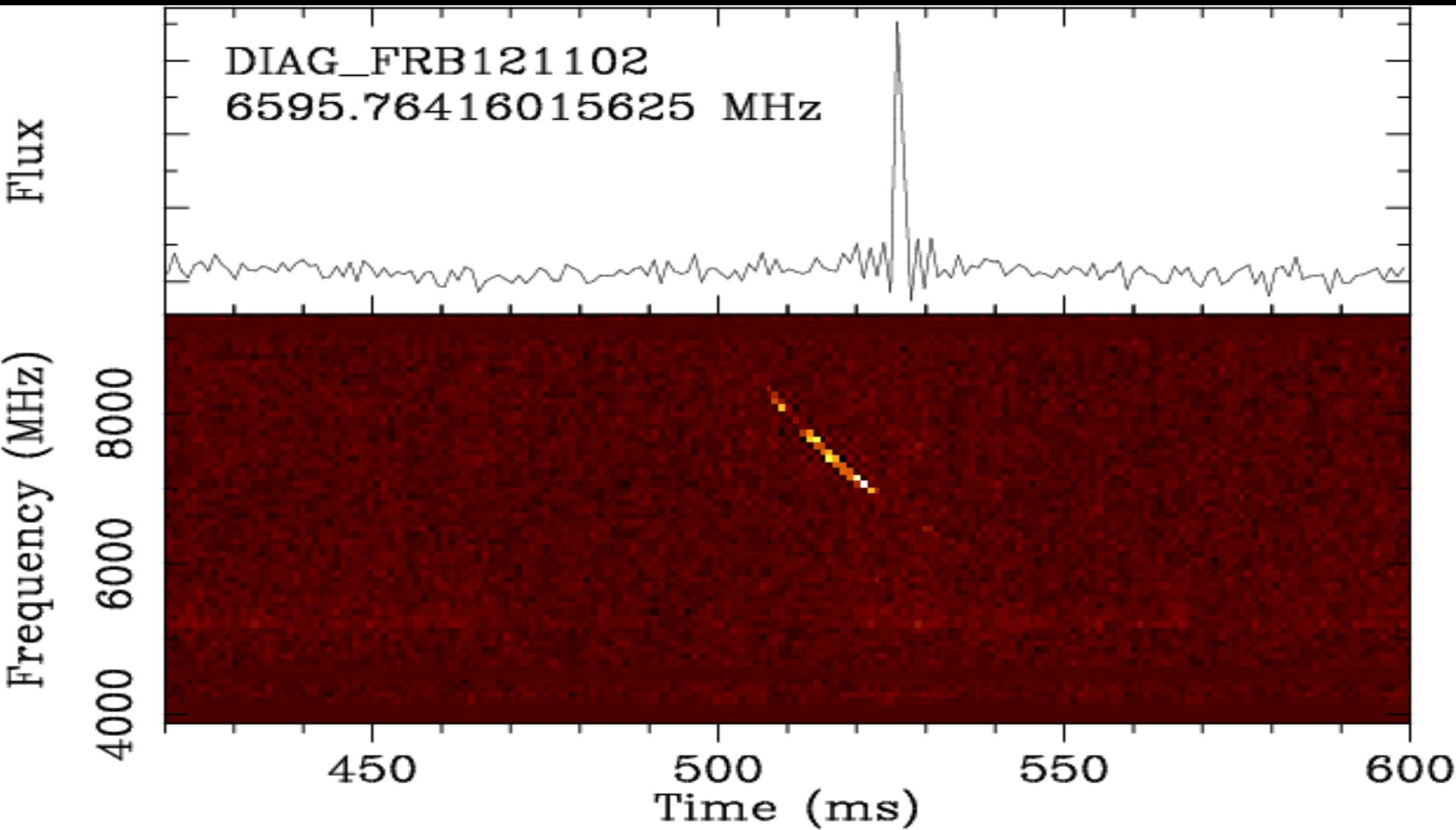
# VEGAS/DIBAS Multi-beam Spectrometer + Pulsar Timing/Search

John Ford, Dan Werthimer, David MacMahon, Richard Prestage

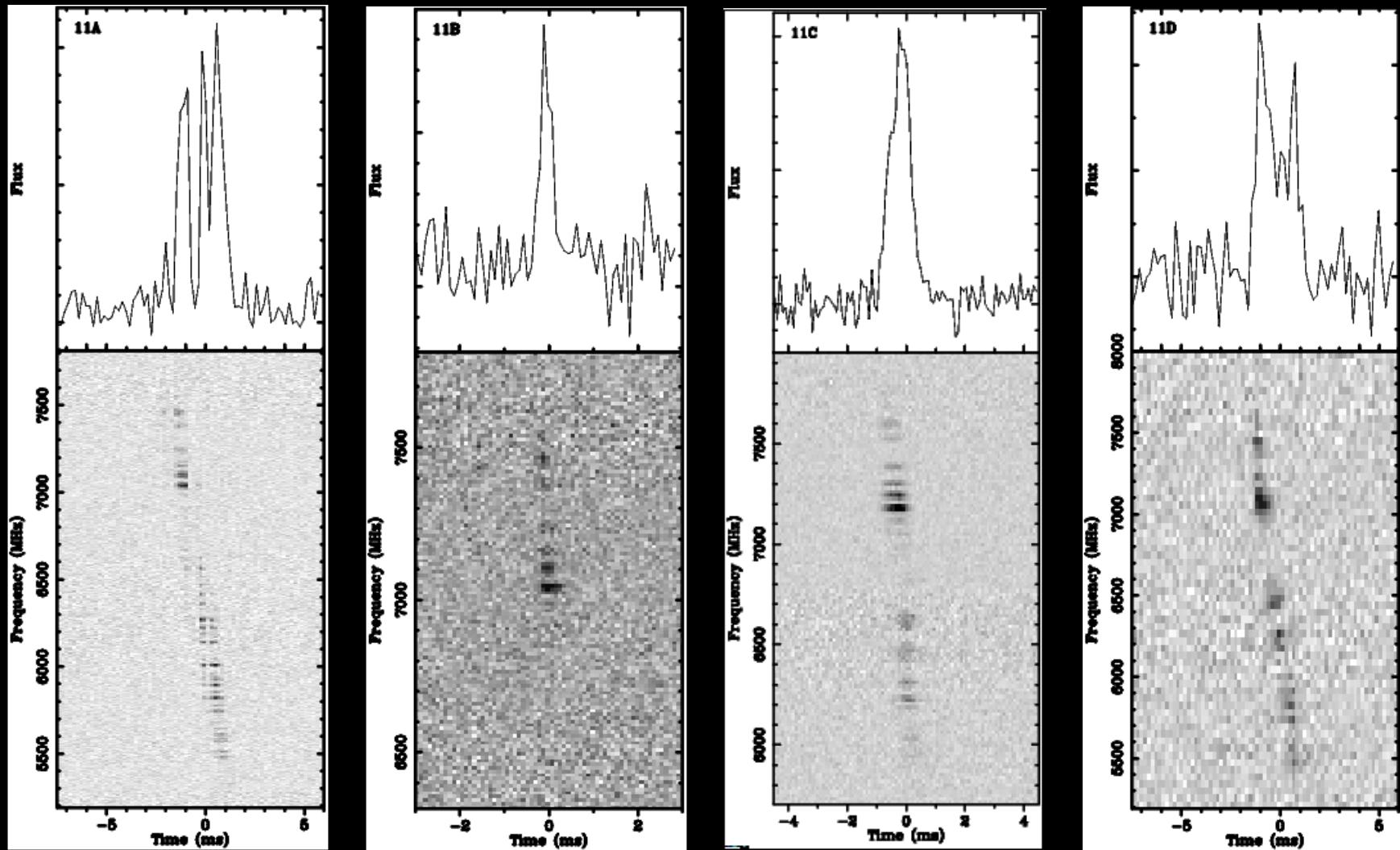


# FRB121102 (repeater)

Highest Frequency detection (4 – 9 GHz)  
widest bandwidth (5.4 GHz)



# Coherently dedispersed pulses

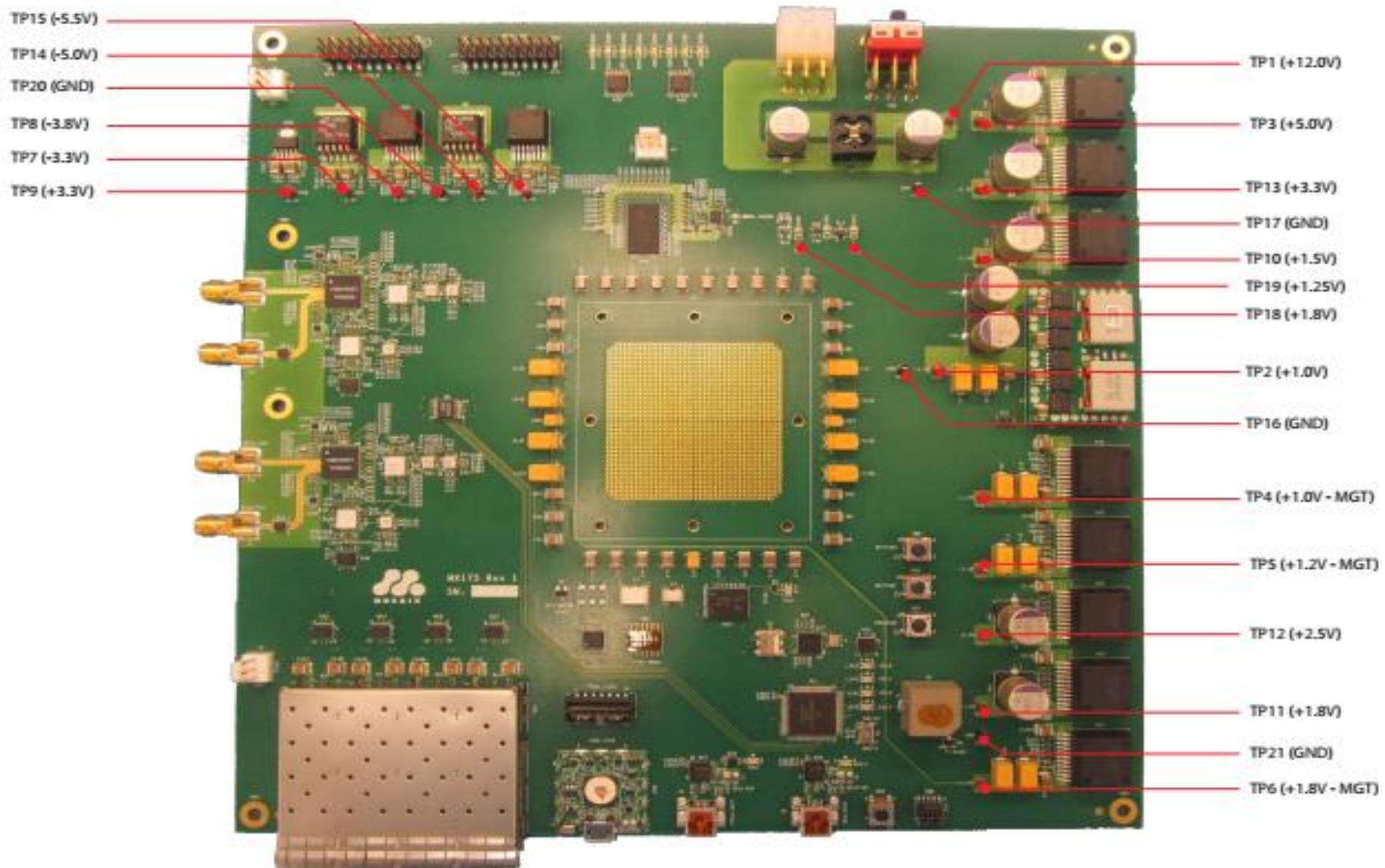


# Fast ADC's

<b>15 Gsps</b>	<b>4 bit</b>	<b>Adsantec</b>
<b>26 Gsps</b>	<b>3.5 bit</b>	<b>Analog Devices</b>
<b>55 Gsps</b>	<b>8 bit</b>	<b>Fujitsu</b>
<b>80 Gsps</b>	<b>8 bit</b>	<b>Berkeley</b>
<b>160 Gsps</b>	<b>8 bit</b>	<b>Keysight</b>
<b>240 Gsps</b>	<b>8 bit</b>	<b>Teledyne Lecroy</b>

# Dual 26 Gsps 3.5 bit ADC and FPGA

MX175R1 TESTPOINTS

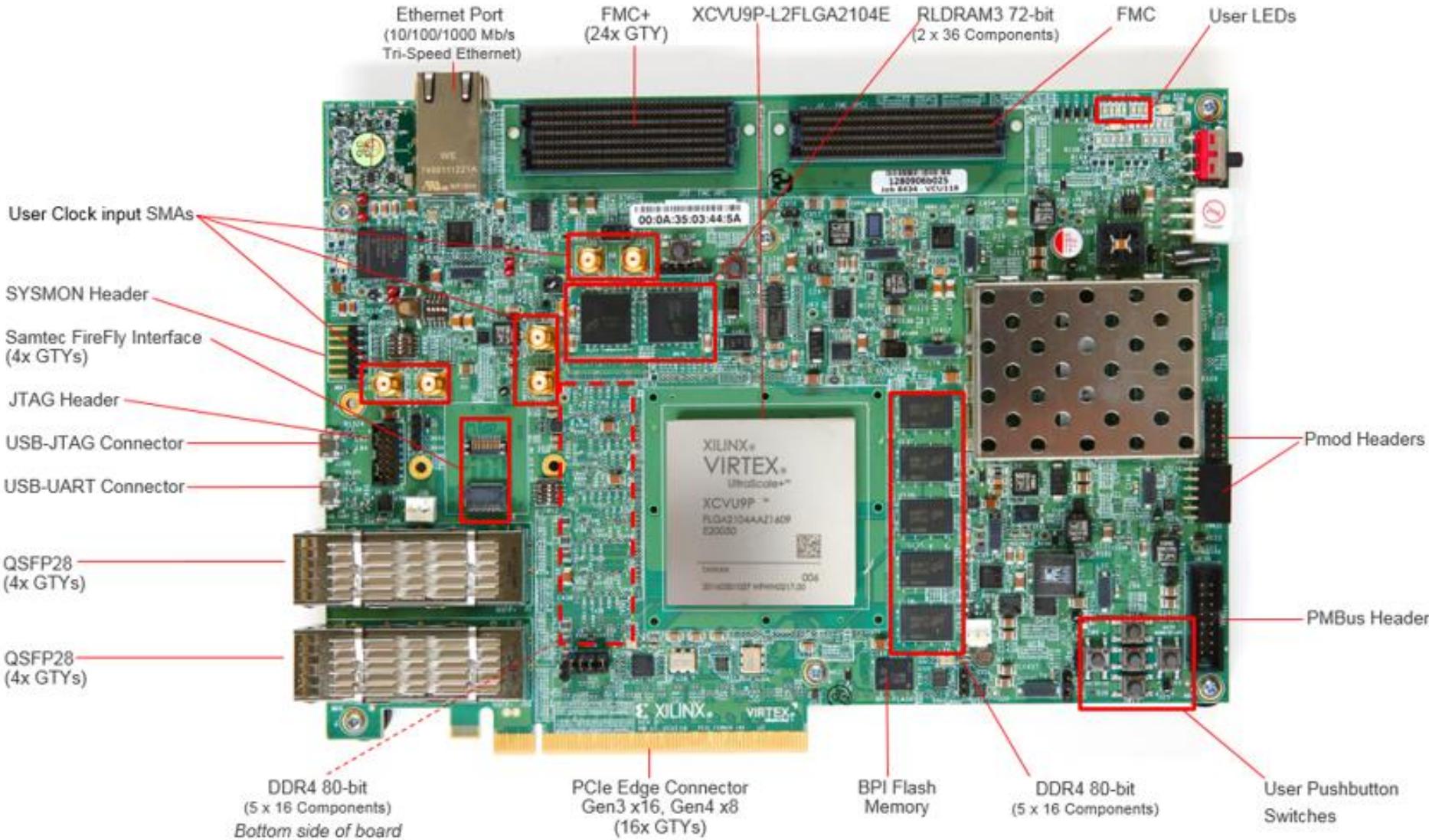


# Board Interconnect - Upgradable

- Problem: Backplanes are short lived  
(S100, Multibus, VME, ISA, EISA, PCI, PCIx, PCIe, PCIe2.0, compactPCI, compactPCIe, ATCA...)
- Solution: Use 10, 40 or 100 Gbit/sec Ethernet  
Ethernet since 1973 – likely to stay around !



# VCU118 5x100Gbit Ethernet ports



# Casper Commandments

Thou Shalt Share thy Knowledge

Thou Shalt Help thy Neighbor Casperite

Thou Shalt Covet thy Ethernet to Connect Everything

Switches are Free

# CASPER Real-time Signal Processing Instrumentation

- Rapid development
- Open-source, collaborative
- Reusable, platform-independent gateware
- Modular, upgradeable hardware
- Industry standard ethernet communication
- Use switches to interconnect FPGA/GPU/CPU
- Low Cost

# Tutorials

Introduction to Simulink and Roach (blink an LED)

Using 10 Gbit Ethernet

Spectrometer (400MHz, 2k channels)

Correlator (4 input, 400MHz, 1k channels)

Heterogeneous Computing ADC→ROACH→CPU/GPU

Intro to embedding Verilog/VHDL in Simulink

Yellow Block Creation

# Annual CASPER Workshops

morning: talks

afternoon: lab training, tutorials, working groups,  
get help designing an instrument....