NOTES ON PHASE DOWNLINK SIGNAL PROCESSING

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A simplified block diagram of the phase downlink signal processing planned for the Green Bank OVLBI earth station is shown in Figure 1. In this memo, several aspects of the design choices involved will be discussed. It will be assumed that the reader is familiar with the ystem design concepts previously described [1,2].

The overall objective is to make a precise measurement of the phase of the downlink carrier with respect to a quasi-sinusoid that represents the predicted downlink carrier. In our implementation, a double-conversion receiver using fixed-frequency LOs is used to bring the received signal to a relatively low frequency, near 10 MHz, where it is compared in a quadrature phase detector with the sine and cosine outputs of a high-resolution direct digital synthesizer (DDS). The latter will be programmed to generate the predicted carrier.

First Local Oscillator and First I.F.

The first conversion will be to an I.F. in the range 500–800 MHz. This is chosen to be compatible with the I.F. used in the VLBA, thus facilitating use of the antenna and receivers for radio astronomy when they are not engaged in spacecraft tracking. The I.F. band must be high enough in frequency to allow rejection of the image of the first mixer with filters of modest selectivity. It must also be wide enough in bandwidth to allow coarse tuning in the first LO, so as to facilitate a phase-stable design. Since the first LO is the only one at microwave frequencies, it is the most critical. We want to use only the most stable references available and to minimize the multiplication factors applied to them. We also want to use as much as possible of the VLBA design. These considerations lead to the use of a synthesizer that locks a VCO to a harmonic of the 500 MHz reference offset by $\pm$100 MHz. Recall that the 500 MHz reference is transmitted to the antenna-mounted package by a phase-corrected cable. The result is a synthesizer with tuning steps of 300 and 200 MHz, alternating. Any signal frequency can then be converted to a 300 MHz-wide I.F. band. For the specific frequencies planned for Radioastron (8.47296 GHz) and VSOP (14.200 GHz), we will use LOs at 7.9 and 13.6 GHz giving first I.F.s of 572.96 and 600.00 MHz, respectively.

Second Conversion

The second conversion is not strictly needed, since the phase detection could be done at the 500–800 MHz I.F. But the phase detector can be implemented much more accurately at a lower frequency, and this is a critical consideration. We choose a fixed-frequency LO for the second conversion, and again the tuning is only as fine as necessary. The step size is determined by the frequency range of the DDS that will be used for the phase detector reference. We have selected a silicon VLSI DDS (Stanford Telecom model 1277) because it provides very high resolution (32 bits) and some valuable features including dual outputs

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with independently programmable phases (nominally sine and cosine, but adjustable to correct for phase detector errors) and the ability to set the absolute phase with respect to a slow reference. This DDS has a maximum clock frequency of 60 MHz, and we expect to run it at 50 MHz, allowing output frequencies from 0 to about 22 MHz. Thus, the second LO synthesizer's resolution can be as coarse as about 10 MHz. To cover the full possible I.F. range, it should be capable of tuning from 490 to 790 MHz. [The detailed design of this synthesizer will be covered elsewhere. For practical reasons, its tuning range is expected to be limited to 540–780 MHz.]

An alternative for the second conversion might have been to include the fine-tuning for the predicted carrier phase in its LO and then to operate the phase detector at a fixed frequency, say 10 MHz. This could be done by using the 2–22 MHz DDS as an offset reference to a PLL, generating $Nf_r + f_d$ where $f_r = 10\text{MHz}$ and f_d is the DDS frequency. It could be argued that the phase detector can be more accurate if operated at a fixed frequency, but any advantage would be lost because a variable-frequency phase detector would be required in the offset PLL. Furthermore, it will be possible to calibrate and correct the phase detector errors nearly continuously in the digital signal processing, whereas measurements of the errors in such a PLL would be difficult. We therefore have selected a fixed-frequency, coarsely-tuned second LO and a variable-frequency, finely tuned phase detector.

Since the second I.F. (2–22 MHz) is less than the required tuning range, an image-rejecting mixer (IRM) is needed unless we are willing to sacrifice 3 dB of SNR. Although the worst-case SNR expected is very much in excess of our requirements (see Table 1), we prefer to maintain the best possible sensitivity as a hedge against future needs; and whereas the IRM can be easily fabricated from inexpensive components, we will include it.

For VSOP, the phase downlink signal will include the wideband data as QPSK modulation, so it is necessary to recover the carrier from the modulated signal. We plan to do this in a fourth-order Costas loop which accepts the I.F. signal as input and produces the recovered carrier and two baseband data signals as outputs. A convenient design, shown in Figure 1, uses the second LO to offset the Costas loop's VCO so that the second conversion is accomplished at the same time as the carrier recovery. The recovered carrier then comes out within the frequency range of the phase detector, 2–22 MHz. However, it may be that the Costas loop will be part of a demodulator that we procure commercially. In that case, we may not have so much flexibility and the recovered carrier may come out at I.F.; it can then be passed through the same converter as is used for Radioastron. In either case, the effective (noise) bandwidth at the phase detector input (B_3 in Figure 1) will be that of the Costas loop. Selection of the loop bandwidth is not critical, and is a compromise among acquisition time, false-lock immunity, and VCO phase noise requirements; a value in the range 3 kHz to 30 kHz seems feasible.

For Radioastron, the downlink signal is unmodulated and there is no need for a PLL prior to the phase detector. However, an offset PLL could be used to implement the second conversion for Radioastron also. This would have some advantages: (1) an IRM would not be required; and (2) if the loop bandwidth B_3 can be made small enough, then no sampling pre-filter (F4 in Figure 1) will be needed after the phase detector. For example, a 500 Hz loop bandwidth and 1 kHz sampling rate would allow elimination of F4. This might avoid some phase errors due to the delay through F4. But there are disadvantages: (1) the complexity of the added PLL more than makes up for savings in other components; and (2) the PLL requires a phase detector at 500–800 MHz with 20 dB dynamic range, and any d.c. offset in this detector produces an uncorrectable error in the measured phase. (The latter problem occurs for VSOP's Costas loop too, but there it is unavoidable because of the modulation, and must be minimized by careful design.)

Phase Detection

Some considerations of the phase detector design were discussed under Second Conversion above, and additional ones are included here.

We choose an analog quadrature phase detector based on double-balance mixers because of its inherent linearity and stability, especially at frequencies below 100 MHz. Errors in such phase detectors include d.c. offsets, amplitude imbalance, and phase quadrature error. The worst problem is the variation of d.c. offset with input level and temperature, especially in view of the fact that we want to operate over a 20-dB dynamic range (see below). We choose double balance mixers specifically designed for phase detection (Mini Circuits Lab model RPD-1); these have a high ratio of output voltage to d.c. offset (1000:1 at nominal levels, 100:1 with signal −20 dB from nominal). The amplitude and phase imbalance will be solved for in the digital signal processing of the quadrature outputs, on the assumption that these errors vary slowly compared with the signal phase being measured [the details of this will be covered in a separate report]. As mentioned earlier, any significant phase error can be corrected by programming the DDS; its two outputs, nominally in quadrature, can have independently-set phase offsets with 12-bit resolution.

The mixer outputs connect to simple RC filters and operational amplifiers producing a nominal output amplitude near 5 V (0.5 V at −20 dB from nominal) and a bandwidth near 500 kHz. If the orbit predictions are as good as expected, the rate of change of phase will be no more than 500 Hz, but during the early phases of each mission it could easily be much larger. In case it is too large to be handled by the digital processing that follows, we will provide a simple counter driven by the phase detector outputs to enable measurement of the average Doppler frequency. This counter will typically be latched and reset at 1-sec intervals under hardware control; the latched value will be available to the station computer. Even with a 500 kHz residual phase rate, a 24-bit counter will operate for 33 sec before it overflows.

Digitization

The two phase detector outputs will be digitized at the maximum rate at which the required digital signal processing can be carried out. This is still to be determined, but a minimum of 1 kHz sampling rate will be achieved. Something around 10 kHz should be possible with an inexpensive processor [to be discussed in a separate report]. Sampling will be done for the two signals simultaneously, and the sampling times should be accurate to a few nsec. Quantization to 12 bits per signal will be used (± 10 V range implies LSB=5 mV; at −20 dB from nominal level, effective resolution is 6.6 bits).

The pre-sampling filters F4 must limit the noise bandwidth to half the sampling rate or less, otherwise the effective SNR is reduced by aliasing. As we shall see shortly, the available SNR is very high and some aliased noise can be tolerated. Therefore, we set the 3-dB point of these filters at half the sampling rate and we do not require a sharp cutoff. To minimize phase errors as a function of phase rate, maximally-flat-delay filters will be used and the two filters for the quadrature channels will be carefully matched. Such errors are also minimized by having a high sampling rate, so that the phase rate is always much less than the filter bandwidth.

Signal-To-Noise Ratios and Dynamic Range

SNRs at various points in the signal processing have been calculated for the Green Bank station and the results are given in Table 1. The “best” case represents a near-perigee pass at high elevation, and the "worst" case represents a near-apogee pass at 5 deg elevation in poor weather.

It is apparent that the SNRs are extremely high. Even in the 20 MHz bandwidth of the second I.F., the SNR is never expected to be less than 0 dB. This means that the overall gain can be set according to the signal level and not the noise level without fear of saturation at any point in the signal processing.

The last line is Table 1 is the SNR in 5 Hz bandwidth, which is the final bandwidth planned for the phase measurements after averaging in the digital signal processor. It is this number that determines the noise contribution to the short-term coherence of the time transfer system. However, the SNR at the ADC input determines the phase error in any one sample, and this determines the probability of a cycle slip. It can be shown [see later report] that an SNR of 20 dB at this point is sufficient to keep this probability less than 10^{-8}, or 1 slip per 55 hours at 500 Hz, provided that the sampling rate is at least 3 times the phase rate (1.5 times Nyquist).

Not included in Table 1 is "noise" in the form of phase jitter induced by the data modulation due to non-ideal behaviour of the Costas loop (applies to VSOP only); nor quantization noise from the digitization (about -40 dB for the worst-case resolution of 6.6 bits).

The signal level covers a 26 dB dynamic range for each spacecraft, but it can only change by up to about 17 dB on any one tracking pass. We will provide gain adjustment in the I.F. amplifier in about 1-dB steps, but in order to avoid introducing phase errors this gain will remain fixed at a pre-computed value during each tracking pass. We therefore design for 20 dB dynamic range in the signal processing that follows. For Radioastron, this will be absorbed in the phase detector, and the effect of a 20-dB change in signal level has been noted in the discussions of phase detector performance above. For VSOP, this dynamic range will be absorbed in the Costas loop; there will be a variation with signal level in the effective phase detector gain and hence in the loop bandwidth (theoretically a factor of 10 in gain and 3 in bandwidth for a 20 dB change), but since the loop bandwidth is not critical this should be tolerable.

References

[1] L. D'Addario, "Green Bank Earth Station: System Design Principles," OVLBI-ES Memo No. 12, June 4, 1991.

[2] L. D'Addario, B. Shillue and D. Varney, "The Green Bank OVLBI Earth Station: Preliminary Design." NRAO, July 2, 1991.