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NATIONAL RADIO ASTRONOMY OBSERVATORY  
Green Bank, West Virginia

Electronics Division Internal Report No. 80

AUTOCORRELATION RECEIVER MODEL II:  
DIGITAL SYSTEM

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## PREFACE

This report is for maintenance personnel on the digital system of the NRAO Autocorrelation Receiver Model II. The system is of such complexity that a "build-up" type of approach is taken here. A description is given of a simplified block diagram, followed by a description of a more detailed block diagram; and then a thorough description is provided using the actual logic diagrams.

A complete coverage of every detail is not possible. However, an engineer or technician with a good knowledge of digital logic should be able to fill in the fine details by the use of the logic and timing diagrams.

Wherever it was considered helpful for quick reference, information has been restated in tabular form. Once this report has been read, most questions which arise while servicing can be answered by use of one of the tables.

To get a familiarity with the operation of the entire system, it is suggested that the NRAO Electronics Division Internal Report No. 75 be read. In addition to the data and drawings contained in this report, the following items - too bulky to be incorporated in this report - are available:

1. Wiring list of large card file.
2. Wiring list of small card file.
3. Cable wiring list.
4. Load and location chart.
5. Spare module and location tabulation.
6. Instruction manuals for core memory, power supplies, level converter and relay driver cards, and sensitive relays.

These items can be found in the Autocorrelation Receiver Service Center Cabinet which should always accompany the two receiver racks. Item 4 above is especially helpful in locating the origin and destination of any signal. All of the above are needed for any logic changes that would be contemplated.

Thanks are due to many people for help in completion of this project.

In particular, I express appreciation to the following:

Sander Weinreb for developing the digital autocorrelator theory;

Gart Westerhout of the University of Maryland for initiating the drive for a large autocorrelator;

Robert Mauzy for his excellent analog design, especially the clippers, samplers, and clock emitter followers which feed the digital system;

Raymond Hunter, who did every job imaginable, from wiring to design of Omni Comb units, through the entire project;

Wilbur Andrews and Jack Cochran for various mechanical and electrical designs and construction; and

Henry Light for all the drafting and logic checks.

I thank all of these people for going along with me and not doing it the WRONG WAY nor the RIGHT WAY, but the SHALL-O-WAY.

AUTOCORRELATION RECEIVER MODEL II DIGITAL SYSTEM

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# AUTOCORRELATION RECEIVER MODEL II DIGITAL SYSTEM

A. M. Shalloway

## I. Introduction

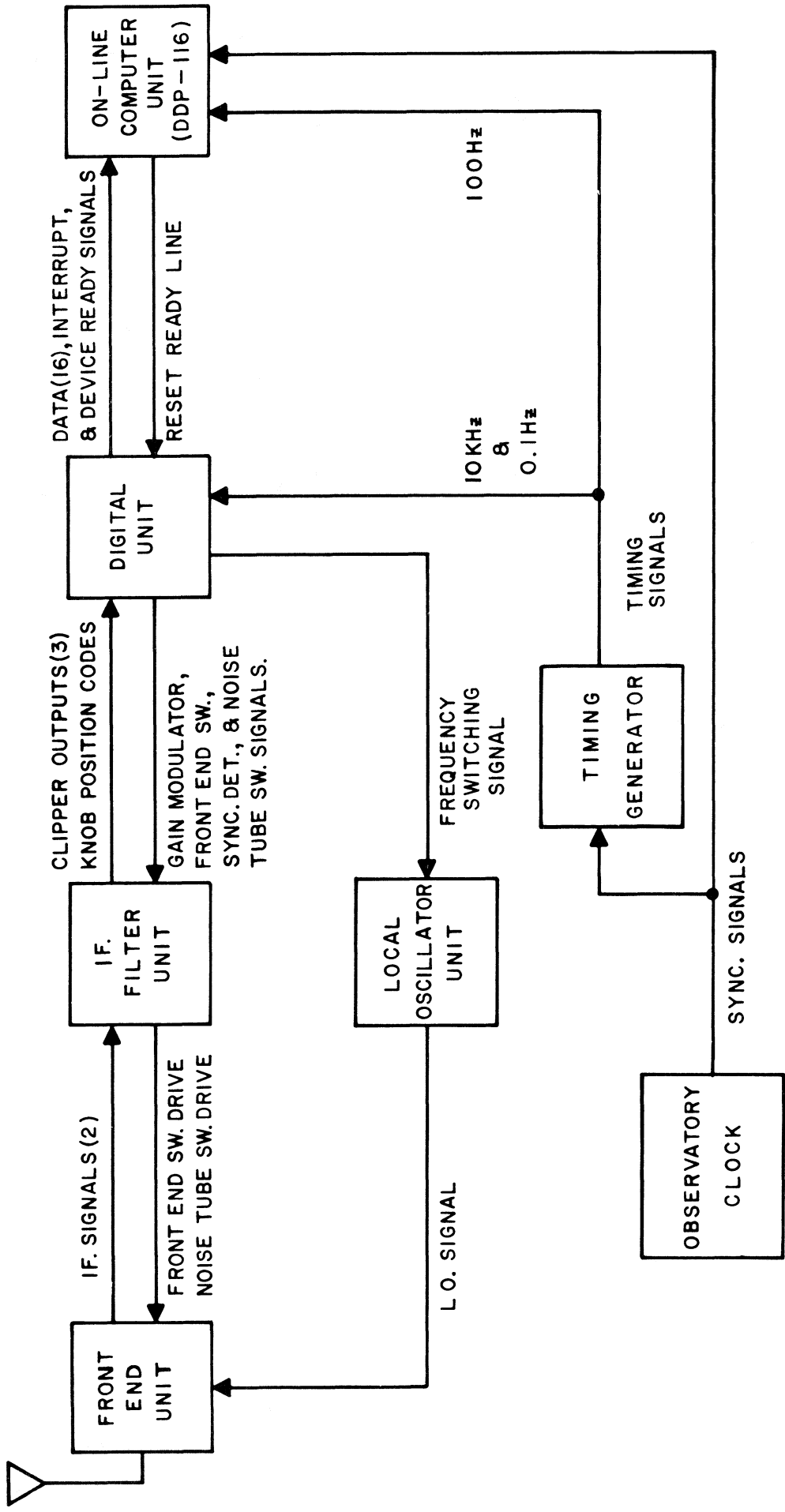
The NRAO Autocorrelation Receiver Model II is a specialized receiving system for observation of spectral lines. It is the equivalent of a multi-channel spectrum analyzer. A block diagram of a complete system using the correlation receiver is shown in Figure 1.

The process consists of filtering out a selected bandpass centered at a desired spectral-line frequency and heterodyning it down to the video-frequency range with one side of the bandpass being at zero frequency. This signal is clipped to provide a rectangular waveshape of fixed amplitude. The only correspondence between the clipped and unclipped signal is that they both cross zero at the same time. The clipped signal is sampled at a frequency equal to twice the bandwidth and the sampled data is used to generate two autocorrelation functions with 192 points or one with 384 points.

The integrated autocorrelation function is processed by an on-line computer. The computer performs a Fourier transform to generate a power spectrum. The computer data is available as an on-line graph on a storage oscilloscope, as a printed-tabular output, and as an output on magnetic tape which can be further processed by an off-line computer.

## II. Operational Description

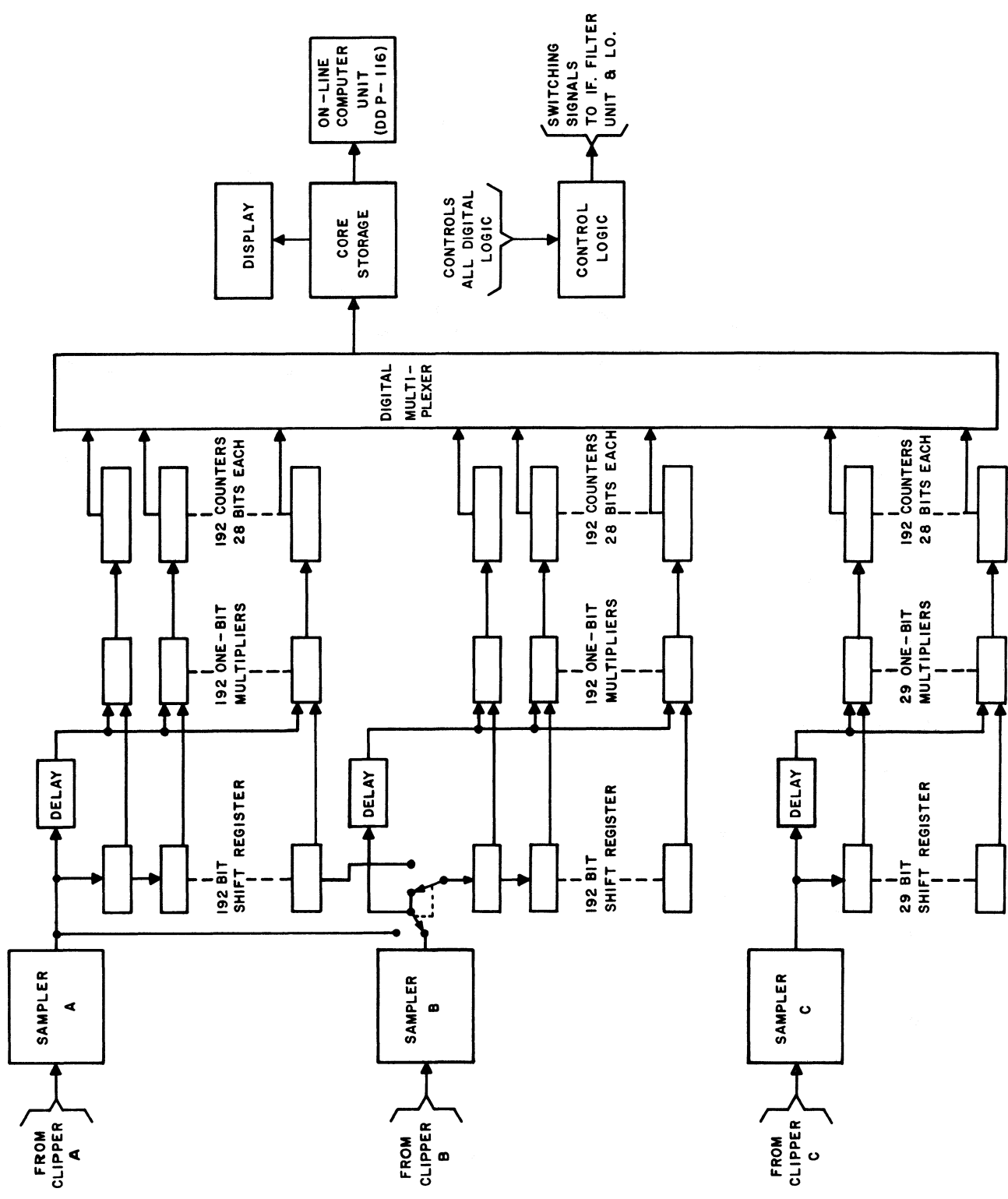
Reference should be made to the block diagram of Figure 2. The clipper output, which has been previously described as a rectangular waveshape containing the frequency information of the original received signal, is sampled at a rate equal to twice the filter bandwidth. The sampler provides a compatible digital output which is synchronized to the digital system clock.



SYSTEM BLOCK DIAGRAM

Figure 1





BLOCK DIAGRAM  
DIGITAL UNIT

Figure 2

The sampled data is continuously stored in a 192 bit shift register which is updated at every clock (sample) pulse. Each shift register stage feeds a one bit multiplier. The other input to the multiplier is the "present" (latest) data out of the sampler. This provides a correlation comparison between the present sample and the previous 191 samples, each spaced  $\tau$  seconds behind the adjacent sample; where  $\tau$  is the sampling period.

If the two samples sent to a multiplier correlate, the multiplier provides a 1 to the associated counter; if not a 0 is provided. After the appropriate integration time the counters represent 192 points on the autocorrelation curve of the integrated signal. The first channel always correlates, as it multiplies the present sample times itself. This provides a record of the number of sample pulses used during one integration period. In terms of the NRAO Autocorrelation Receiver Model I, this is what was referred to as  $2V_0$ .

The digital unit keeps the signal and reference data in separate memory locations of its core memory until dump time (every second or every 10 seconds), at which time the signal and reference data for all channels are sent to the on-line computer. Also sent to the computer are the signal and reference total power measurements for the three receivers. All knob positions are then sent to the computer. The knob positions sent to the computer are determined in the last half switching cycle prior to dump time.

There are 28 bits in each autocorrelation counter. The eight least significant bits are discarded prior to transmittal of the data to the computer. These eight bits are equal to or less than the RMS variations, and thus nothing is lost. There are 20 bits in the total power counters and they are all transmitted to the computer. A detailed description of data transferred to the computer is given in Appendix I.

The digital rack is an RFI shielded rack to prevent transmission of the many signals generated by the digital logic. Therefore, except to change

knob positions or to service the instrument, the front and rear doors should always be closed securely.

Figure 3 is a photograph of the digital rack. Power can be controlled from either box on top. The push buttons are normally used. If a long down-time is expected (more than a day) the toggle switch is also moved to the off position. A switch on the small card file with the display tests the display lamps. All other controls are on the digital autocorrelator chassis panel (large card file). A brief explanation of these follows:

#### Dump Period

The Dump Period is the integration time (1 or 10 seconds) in the correlator before dumping data into the computer.

#### Switching Rates

Switching rates between 1 Hz and 10 Hz can be selected. The signal/reference duty cycle can also be changed. The allowed combinations of switch rate and duty cycle are:

1 Hz - 50%/50%  
5 Hz - 50%/50%  
10 Hz - 50%/50%  
1 Hz - 90%/10%  
5 Hz - 75%/25%

As an example, "1 Hz - 90%/10%" means that 0.9 second is spent on signal and 0.1 second is spent on reference. This mode will improve sensitivity by approximately a factor of 2 if the reference data is integrated in the computer 100 times longer than the signal data. The usual setting is "1 Hz - 50%/50%".

#### Noise Tube Duty Cycle

In normal operation the noise calibration signal is automatically turned on for every other dump period (50%/50%) or for every tenth dump period (10%/90%).

6043

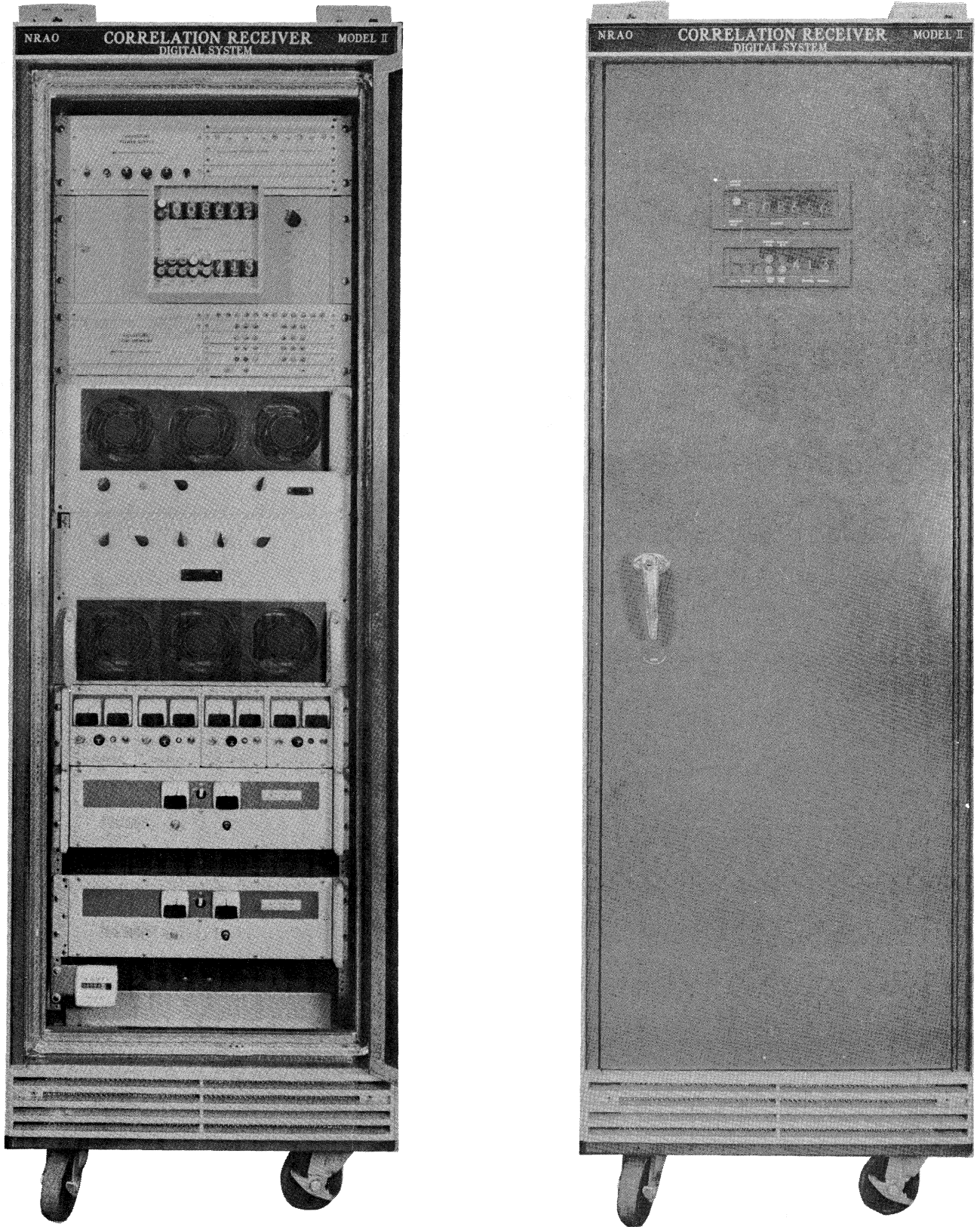


Figure 3. Digital Rack - Door Open & Closed

When the noise calibration signal is on, it is not on continuously - it is so modulated that it is on during the signal period and off during the comparison period. The usual setting is 50%/50%.

#### Blanking Time

Blanking time is a "dead" time at the beginning of each signal or reference period. A small amount of blanking time is needed to clear various registers in the correlator. A longer blanking time can be switch selected to allow front-end or LO switching transients to die out of both analog and digital portions of the system. The allowed blanking time is 4 to 26 ms in steps of 2 ms.

#### Display

A description of the displays and associated knobs follows:

Channel Data: Indicates data obtained for a particular channel during the previous dump period.

Channel Number: Indicates number of channel whose data is being displayed.

LAMP-DU: Data/Update - Whenever this lamp is on the channel data information is updated every dump time.

LAMP-CD: Computer Data - This lamp goes on as soon as the data is available for the computer at the beginning of each dump period. As soon as the computer has removed the data, the light goes out. A continuously burning light indicates that the computer is not taking data. If the cable between the Digital Unit and the Computer Unit is disconnected, the light will act as though the computer is removing data.

LAMP - +24 V: +24 volt power supply on-off indicator. +24 volts used on clock crystal oscillator circuit, lamps, and relays.

LAMP - +5 VB: +5 volt power supply on-off indicator +5 volt B is used on the lower half of the correlator chassis.

LAMP - +5 VA: +5 volt power supply on-off indicator. +5 volt A is used on the upper half of the correlator chassis.

LAMP S-R/I: Signal-Reference Integration. Light on indicates signal is being integrated. Off indicates reference being integrated. This assumes first half of each switching cycle is signal.

LAMP S-R/D: Signal-Reference Display. Light on indicates the channel being displayed is signal data. Light off implies reference. This assumes first half of each switching cycle is signal.

LAMP - -15 V: -15 volt power supply on-off indicator. -15 volts is used on clock amplifiers and sampler circuits.

LAMP - +15 V: +15 volt power supply on-off indicator. +15 volts is used on clock amplifiers and sampler circuits.

LAMP - -18 V: -18 volt and -6 volt power supplies on-off indicator. -18 and -6 volts are used on the input and output level converters.

LAMP - NT: Noise Tube. Light on indicates noise tube on.

LAMP - DT: Dump Time. Light goes off at beginning of dump period. Light goes on when dump period is half over.

KNOB - Light Test: Clockwise rotation turns all lamps except power supply indicators on.

KNOB - Display and Advance Rate: When the Display and Advance (Sw. 4) knob is in the Display and Advance position, this knob controls the rate of advancing from one channel to the next. The rate varies from approximately 0.8 Hz to 3.5 Hz.

KNOB - Display Mode (Sw. 3):

Display Update - Channel number remains constant. Data display is updated at every dump time.

Display & Advance - Channel is advanced at rate determined by Display & Advance Rate knob. As each new channel number appears the data display changes to show the data in that channel.

Advance 10 Ch/s, 50 Ch/s, and 250 Ch/s - Advances the channel display at the rate indicated. The Channel Data Display is inoperative.

TOGGLE SWITCH - Display and Advance (Sw. 4): Up is a locked position. Down is a spring return position. If the toggle is up or down, the Display Mode Knob (Sw. 3) is activated for all positions except Display Update. Display Update does not require the use of this toggle switch.

### Testing

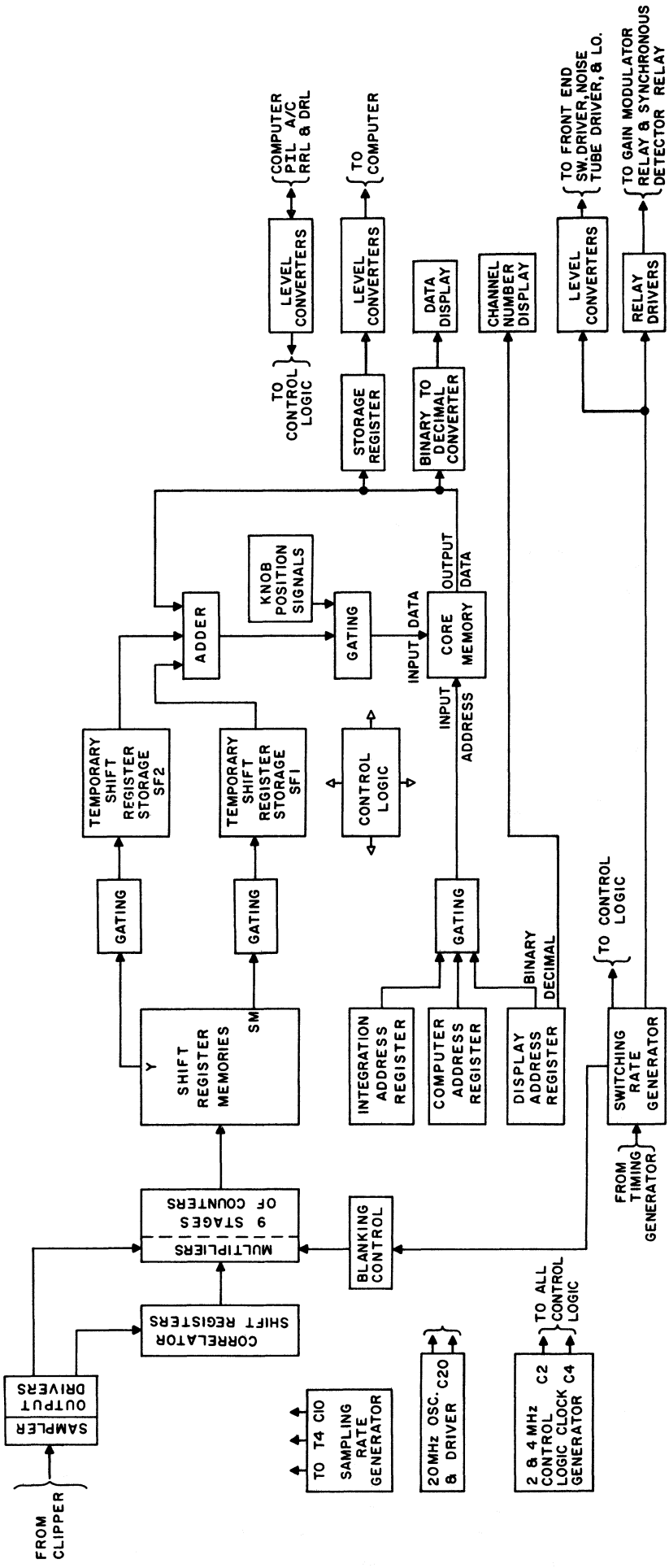
Square waves can be sent into the clippers by positioning the desired test toggle switch on the IF filter rack and choosing the desired frequency on the Test Signal Switch (Sw. 9) on the digital rack.

The crystal oscillator clock frequency can be checked by disconnecting the test signal cable between the digital rack and the IF-filter rack - top of the rack. Put the test signal switch on 10 MHz and feed the test output from the digital rack to a stable counter. Multiply the reading by 2. An error of  $\Delta f$  in this oscillator causes an expansion of the frequency scale so that a point at one end of the spectrum is shifted by  $\Delta f \cdot B/20$  where B is the spectrum bandwidth in MHz.

### III. Block Diagram Description

(Refer to Figure 4)

The CONTROL LOGIC consists of many small logic groups throughout the system. Each block in the diagram is associated with several of these logic groups to control the block's timing, gating, etc.



DETAILED BLOCK DIAGRAM

Figure 4.



The 20 MHz CLOCK is a crystal controlled oscillator from which all clocking pulses are derived. The oscillator has a stability of 20 PPM per 10 seconds and per 24 hours over a temperature range of +20° to +50°C, and can be set to within a few cycles of 20 MHz. In addition to using the 20 MHz directly, a divider provides a 4 MHz and 2 MHz clocks for clocking the lower speed sections.

The SAMPLING RATE GENERATOR is a dividing and timing system which, combined with the 20 MHz CLOCK, generates the correct sampling, shifting and multiplying rate.

The SAMPLER, described in the IF and Filter Section, receives the clipped noise signal at its input. A clock pulse is provided the SAMPLER to indicate when a sampling should be made. The SAMPLER output consists of a flip-flop which can only change state at the clock pulse time. It stores a one or a zero, until the next clock pulse, depending on whether the clipped noise signal is above or below zero at the sample time. The SAMPLER output is transferred to drivers with sufficient power to drive the first stage of the SHIFT-REGISTER and the 192 MULTIPLIERS.

The SAMPLER, SHIFT REGISTER and MULTIPLIERS operate at the clock rates indicated in Table I for the various bandwidths.

Two signals are received from the telescope Timing Generator: 10 KHz and 0.1 Hz. These are used to drive the SWITCHING RATE GENERATOR which controls the following:

1. Blanking Time
2. Dump Time
3. Front End Switching Rate
4. Noise Tube Switching Rate
5. Gain Modulator Switching Rate
6. Synchronous Detector Switching Rate

The BLANKING CONTROL holds up operation of the multipliers during the blanking time. During this time the data in the COUNTERS is transferred to the core memory and the old SHIFT REGISTER data is replaced by new data.

TABLE I

PARAMETER VALUES  
FOR VARIOUS VALUES OF BANDWIDTHS

BANDWIDTH	W8	W4	W2	W1	T0	C10	T4*	PULSE RATE	
								Sampler & Shift Register	Multipliers
10 MHz	0	0	0	0	1	1	1	20MHz	20MHz
5MHz	0	0	0	1	0	10MHz	1	10MHz	10MHz
							<u>Pulse</u>		
2.5MHz	0	0	1	0	0	10MHz	5MHz	5MHz	10MHz
							<u>Pulse</u>		
1.25MHz	0	0	1	1	0	10MHz	2.5MHz	2.5MHz	10MHz
625KHz	0	1	0	0	0	10MHz	1.25MHz	1.25MHz	10MHz
312.5KHz	0	1	0	1	0	10MHz	625KHz	625KHz	10MHz
156.25KHz	0	1	1	0	0	10MHz	312.5KHz	312.5KHz	10MHz
78.125KHz	0	1	1	1	0	10MHz	156.25KHz	156.25KHz	10MHz
39.0625KHz	1	0	0	0	0	10MHz	78.125KHz	78.125KHz	10MHz

\*T4 positive pulse width is 100ns and brackets C10 at gates where used.

See Figure 23.

The SHIFT REGISTER MEMORIES are an extension of the counters. They contain the 9th through the 16th least significant bits of the total 28 bits which are counted. The 9th bit exists both in the last stage of the COUNTERS and the first stage of the SHIFT REGISTER MEMORIES. Stages 16 through 28 are contained in the CORE MEMORY. A detailed explanation of the operation appears in Section IV. This arrangement greatly reduces the total number of components, both in the form of flip-flop counters required and gating required between the COUNTERS and the CORE MEMORY.

The ADDER is used in the process of extending the counters in to the CORE MEMORY, and, as mentioned above, covered in Section IV.

The CORE MEMORY is accessed for three purposes:

1. Integration and storage of the autocorrelation function, i.e. the counter numbers.
2. Removal of the data for transfer to the ON LINE COMPUTER.
3. Removal of the data for visual display.

These three processes are interleaved; each being allowed a specific time in which it may operate. This is accomplished by the use of three ADDRESS REGISTERS: INTEGRATION, COMPUTER and DISPLAY. The DISPLAY ADDRESS REGISTER is duplicated in decimal form to display the channel of the data being displayed.

A STORAGE REGISTER is used to hold one computer word until removed by the computer.

A BINARY-TO-DECIMAL CONVERTER provides the necessary output for the DATA DISPLAY.

The output signals of the autocorrelator, to the COMPUTER and switch drivers, pass through LEVEL CONVERTERS for adapting the positive logic level swings of the correlator integrated circuits to the negative swings required by the CCC S-PAC germanium circuits used in the external devices.

During the detailed description of Section IV, an occasional look at the block diagram of Figure 4 will help locate ones thinking in the overall picture.

#### IV. Descriptive Terminology

##### A. Location Terminology (Refer to Figures 5 and 6)

Wherever possible, all components can be located by an alphanumeric coding system. To reduce reading errors, the codes generally alternate between alphabetical and numerical indications e.g. B2K12. The codes travel from larger to smaller module as read from left to right. In the above example, B indicates the digital rack, 2 indicates the second chassis from the top of the rack (in this case the small card file), K indicates the tenth printed circuit connector position from the left as viewed from the wiring side of the file, and 12 indicates connector pin number 12.

An understanding of the location codes is necessary, particularly when servicing the equipment by use of the logic diagrams. The following notes will be helpful in deciphering the codes:

1. Rack A = IF-Filter Rack  
Rack B = Digital Rack  
Rack C = DDP-116 Computer Input-Output Rack
2. Plugs on the end of a cable are always referred to with the letter P. Jacks on a panel surface are referred to with the letter J.
3. Chassis B4 folds out. The two parts - upper and lower - are referred to as sub-chassis A and B, these letters entering into the location code. There are three files in each of these sub-chassis which are numbered 1, 2, and 3 from back to front. These numbers also enter into the location code, e.g. B4B2G15 would refer to the digital rack (B), the large card file (4), the lower sub-chassis (B), the middle file (2), the seventh connector from the





left (as viewed from the front of the chassis) (G), and the fifteenth pin on the connector (15).

4. In some drawings the rack indication B is left off. Also, in some cases, the chassis designation 2 or 4 is left off in which B2 or B4 is assumed. However, this is done in such a manner that an ambiguity as to what is meant, should not exist.

B. Identification Terminology (Refer to Figure 7 and Figures 10 through 22)

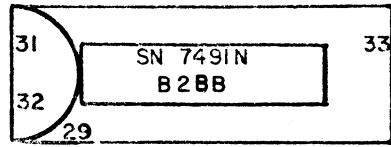
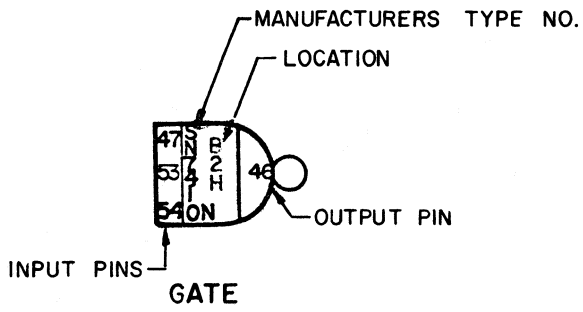
Figure 7 illustrates and identifies all of the logic symbols.

All flip-flops in the logic diagrams are given an F number. If the flip-flop is a part of a counter, register, or closely associated with other flip-flops in logic operation, they are given dash numbers, e.g. F18-10, which would be referred to as the 10th bit of the F18 counter. These F numbers refer to the output of the flip-flops and are barred for the complement (lower) output, e.g.  $\overline{\text{F18-10}}$ .

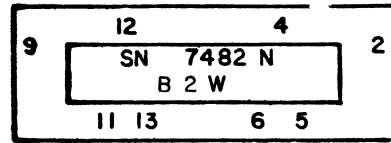
Gates and other logic elements do not have a designation other than location. Reference is made to gates by listing their location with the output pin. When an output line from any logic element is not continuous on the drawing to its input point, it is given an identification code. The code consists of a letter followed by a number and the general classifications are shown in Table II.

Some abbreviations which are used are as follows:

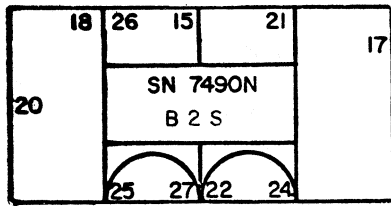
A/C - Autocorrelation (receiver)  
Ch - Channel  
DRL - device ready line - to computer  
Gain mod - gain modulator  
I.C.- Integrated circuit  
L.O.- local oscillator  
LSF - least significant bit



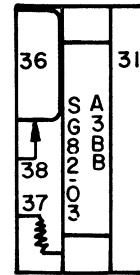
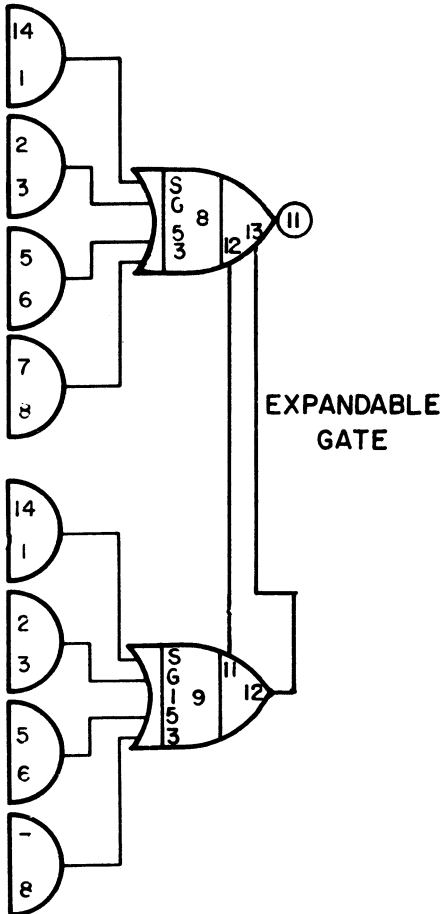
8-BIT SHIFT REGISTER



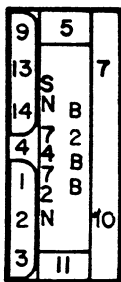
2-BIT BINARY FULL ADDER



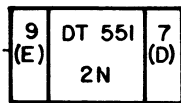
COUNTER



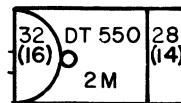
DELAY MULTIVIBRATOR



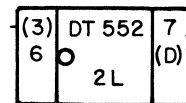
FLIP-FLOP



INPUT LEVEL CONVERTER



OUTPUT LEVEL CONVERTER



OUTPUT DRIVER

LOGIC SYMBOLS

Figure 7



TABLE II

SIGNAL IDENTIFICATION CODES

CODE	GENERAL CLASSIFICATION	EXAMPLE
C	Clocks	C4 4MHz clock
IA	Core Memory Address Selection	IA0 1st bit of input address
ID	Core Memory Input Data	ID1 1st bit of input word
M	Counter Control Matrix	M5 6th output of matrix
N	Core Memory Input Data Selection Matrix	N0 1st input word
OD	Core Memory Output Data	OD1 1st bit of output word
SF	Control Section Shift Registers	SF1 1st control shift register
SM	Sampled Output of Shift Register Memories	SF5 Sampled output of 5th shift register memory
T	All other signals not covered by other codes	T3 Blanking signal
W	Bandwidth code from IF-filter rack	WA1 Least significant bit of code from receiver A
Y	Parallel Output of Shift Register Memories	Y0A Least significant bit from shift register memory section A
$\Sigma$	Adder Output	$\Sigma$ 1 Least significant bit output of adder

When a signal code is followed by an A or B (e.g. C4A or C4B) it generally means they are the same signal logically, but from different sources, such as two separate drivers.

MSB - most significant bit  
M.I.- mode indicator - knob position signals sent to the computer  
N.T.- noise tube  
O.C.- omni-comb  
PIL - priority interrupt line - to computer  
ref - reference  
RRL - reset ready line - from computer  
sig - signal  
SR - shift register  
SRM - shift register memory  
SW - switch  
syn det - synchronous detector  
V/f C - voltage-to-frequency connector

### C. Timing Chart Terminology (Refer to Figures 23 through 27)

The timing charts are self-explanatory and are used in the detailed logic description. They are drawn as though there were no delays in any of the logic elements through which the various signals must pass. However, to indicate the possible delay, the small numbers mixed in with each plot indicate the maximum delay possible assuming the worst case from the integrated circuit manufacturer's specifications. A barred number indicates the complements signal maximum delay. If only a true or a complement delay is given, the other one is the same or no signal exists for the other one.

The two states available in the logic are zero volts (nominally 0 to 0.5 V) and a plus volt (nominally 3 to 4 V). Within the A/C 0V is a logical zero and the plus voltage is a logical 1. In further discussion, only the terms 0 and 1 will be used.

## V. Logic Description

### A. Location Code

In this section a detailed description will be given of the logic,

following in general, the same order of items as in Section III. Figures 14 through 22 are the nine control drawings and are entitled CONTROL LOGIC NO. 1 through 9. When reference is made to a particular piece of logic, a code will be noted in parenthesis to indicate the drawing location of the logic. The first item in the code will be a number between 1 and 9 to indicate the control logic drawing. The second item will be one or more of four letters; A, B, C, or D. They each refer to one quarter of the drawing, thus:

A	B
C	D

If only a number is contained in the parenthesis, it indicates reference to all four quadrants.

#### B. Synchronous System

The entire logic system is operated synchronously. Every flip-flop is operated in synchronism with either the 20 MHz clock, the 4 MHz clock, the display oscillator or the timing generator signal. Although these four clocks are not in synchronism with each other, whenever a signal is passed from a logic element controlled by one clock to a logic element controlled by another, it passes through an asynchronous to synchronous element.

Delay multivibrator circuits have been kept to a minimum and are used only for shaping and delaying the C10 clock signals. Along with the synchronous design, counters have been designed such that they cannot remain in an unused or undesirable logic state. This eliminates the need for a

reset switch on the control panel. About 20 seconds after applying power, the system should be synchronized and operating properly.

#### C. 20 MHz Clock

The clocking system (Figure 8) must generate all of the signals listed in Table I plus a 4 MHz and 2 MHz pulse for the control logic. All clock pulses originate on the 20 MHz crystal control oscillator board. The oscillator drives two emitter follower amplifiers, the total load being divided between the two amplifiers. The 20 MHz is distributed as a sine wave over unmatched but constant impedance transmission lines which are the same length within about  $\pm 6''$ .

On each board the 20 MHz sine wave is then converted into a pulse waveshape by a 1 K ohm resistor feeding a gate. The width of the pulse is controlled by a DC level set on each emitter follower on the clock board. They are normally set to produce a positive pulse width of approximately 21 or 22 nanoseconds into the clock input of the flip-flop.

#### D. Sampling Rate Generator

Except in logic drawings 8A and 8B the 20 MHz sine wave traverses four gates (7) to produce the required clock signal for sampling, shifting, and multiplying. When 20 MHz is required out of the four gates, T0, C10, and T4 are all 1. For 10 MHz; T0 is 0, C10 is a 10 MHz pulse, and T4 is a 1. For lower frequencies, T0 and C10 are the same as for 10 MHz and T4 is a control signal of such shape as to gate through every other C10, or every fourth C10, or every eighth C10, etc.

Counter F20 (8A) generates outputs at 10 MHz, 5 MHz, etc. - to 39.0625 KHz. When operating at 10 MHz bandwidth, the W (8A, 8C, 8D) signals are all 0. This produces: T0 = 1, C10 = 1, and T4 = 1, and all correlating



(sampling, shifting, and multiplying) circuits (7C, 7D, and Figure 10) are clocked at 20 MHz.

At lower than 10 MHz bandwidth, C20 continues to be distributed as a 20 MHz sine wave; however T0, C10, and T4 control the correlating circuits as shown in Table I.

A study of the table, control logic drawing 8A, B, C, and D, and timing diagram (Figure 23) illustrate how all of the high speed timing pulses are generated.

The two delay multivibrators (8D) with F20-1 input and  $\overline{\text{F20-1 AM}}$  (M for modulated) output, are to provide as symmetrical a signal as possible for the "test signal to clipper" (9C), and also to provide some delay for the proper phasing of the C10 signals with respect to the T4 signals.

The remainder of the delay multivibrators (8A, B, C, and D) are for shaping C10 to an approximate 30ns positive pulse and aligning all C10's in phase.

The C4 generator (8B) is an instantaneous divide by 5 counter. The output is taken from F3-2 to provide a pulse of 100ns positive and 150ns at ground. If the counter takes up an unused state when power is turned on, it will cycle around to its normal operation without the need of a reset. No phase relation need exist between C4 and C20 or C10.

C2 is generated (5B) by F33 driving C4. F33 controls the B2X41 gate, allowing every other C4 pulse through. This provides a C2 of 100ns positive duration and 400ns ground duration. The input to pin 92 of F33 is to synchronize C2 and C4 properly.

#### E. Sampler

In the following explanation of the SAMPLERS, CORRELATORS, COUNTERS, and SHIFT REGISTER MEMORIES, it will be assumed the incoming control signals

are available as required and their generation by the control unit will be explained later.

The SAMPLERS, (7C and D) - covered in NRAO Electronics Division Internal Report No. 77 - receive a signal from the associated clipper. A clock pulse - whose frequency is twice the bandwidth - is fed to the sampler. The sampler output changes approximately 25ns after the leading (positive going) edge of the clock pulse. The purpose in the many additional gates, through which the clock pulse must travel prior to reaching the sampler, is to provide the proper phasing of the sampler output changes with respect to the clocking pulse on the F22 flip-flop. Changes occur in the middle of the clock down time. The F22, F23, and F24 flip-flops are all fed the sampler data as shift registers. The F24 data shifts into the first shift register of the correlator boards. Note that it is one clock time behind the F23 data. The F23's shift into the multiplier drivers, and three per receiver are required to obtain the required drive. Receiver C uses only one F23, but the sampler card is the same to reduce spare stock requirements.

When serial operation is performed, T28 is 0 and  $\overline{T28}$  is a 1. Under this condition, the F23A's and F23B's receive the data from receiver A SAMPLER and receiver B SAMPLER is not used. T30 and  $\overline{T30}$  switch the inputs to F23A and C between the sampler outputs for normal operation (T30=1) and the test switch ( $\overline{T30}$ =1) for test operation with a 1 or 0 input signal. This test is only for Receiver A and C. It cannot be applied to B.

#### F. Correlator

The correlator logic consists of 416 channels. Figure 10 illustrates the logic contained on one printed circuit board. It consists of 16 channels of shift registers, multipliers, first two stages of counters and drive circuits. There are 26 of these cards. The operation of the shift registers requires no

explanation. The gates which multiply are contained in one integrated circuit with a flip-flop which is the first stage of the counter: The multiplication process is really one of comparison as per the following truth table:

INPUT FROM SHIFT REGISTER	PRESENT SAMPLE INPUT	MULTIPLIER OUTPUT TO COUNTER
0	0	1
0	1	0
1	0	0
1	1	1

As can be seen, this merely says that if the present sample and the previous sample, being correlated, are the same we enter a 1 into the counter - if not we enter a 0. This is a complemented exclusive "or" circuit and is accomplished by the "and-or" gates on the J and K inputs of the SF-213 flip-flops. The second stage of the counter is a straight forward type of flip-flop. Both types of flip-flops are set as there is no reset on them. This is counteracted by taking the carry off the complement of each flip-flop. Reset occurs during blanking time.

The SF-120 flip-flops are connected as shift registers and are used to obtain enough drive power and to obtain the correct phase at the input to the multipliers.

A review of the SG-220 gates will show that they are connected in the standard method as used to drive the sampler circuit with two exceptions. The last two gates are in two sets - to allow for the two different clocking rates, one for the shift registers and one for the multipliers. Also, during the blanking time we stop the multipliers from operating with signal T3, but allow the shift registers to continue shifting out the old data and shifting in the new data. The last gate on each of the two clocks is quadrupled to obtain sufficient drive.



### G. Counter

The COUNTER card logic is illustrated in Figure 12. Each card contains seven counter stages for each of eight channels. These are fed from the correlator board counter outputs. The integrated circuit modules contain three binary counting stages plus one independent flip-flop. The left over flip-flops from each two modules are connected to form the eighth channel. Reset occurs during blanking time. The spare SN7440N gate is used in the control logic. The count outputs are gated together by the SG-53 and SG-153 gates. There are 52 COUNTER cards and these are grouped in pairs to form a unit of 16 counters to feed one SHIFT REGISTER MEMORY card. The M0 through M15 signals select which one of the counters is to be gated out.  $\overline{T10}$  resets the SN7472N flip-flop just prior to activating the M signal which transfers the state of the last flip-flop into the SN7472N flip-flop.

The last of the three 416 counter channels are used for power measurements on the three receivers. This is accomplished by the last counter board being special, as indicated in the dashed exploded view of the V/f convertor inputs.

### H. Shift Register Memory

Figure 13 is the SHIFT REGISTER MEMORY logic diagram. Prior to an explanation of this logic, a few remarks on the overall system will be helpful.

To this point we have covered nine counter stages per channel - two on the correlator board and seven on the counter board. The overall system is equivalent to 28 stages of counters. In the worst case, of 10 Hz switching rate, the RMS variation is more than the count contained in the eight least significant bits. Therefore, we can safely discard these eight bits. We actually discard the bits contained in the nine counter stages

described so far. However, as will be seen, the last stage is redundant and is repeated as the first stage of the SHIFT REGISTER MEMORY. Thus, we discard the eight least significant bits.

At this point it is desirable to accomplish three tasks:

1. Reduce the number of counter flip-flops required ( $416 \times 28 = 11,648$ ) and thus reduce the total module count, power required, and rack space required.
2. Provide a storage medium to hold the autocorrelator function until the computer can remove the data.
3. Reduce the tremendous gating structure required between the counters and the storage medium (total number of gates would exceed considerably the  $416 \times 20 = 8,320$  count of flip-flops whose data must be removed).

The SHIFT REGISTER MEMORIES and CORE MEMORY accomplish these results. Since we do not require the first eight bits we arrange to shift out the ninth counter bit into the SRM more often than it can change at maximum count rate. A synchronous cycle system is set up for the removal of this data. Each SRM card acts as an eight bit counter for 16 channels; therefore, there are 26 of these cards. If the multipliers are being clocked at 20 MHz the minimum time between changes of the ninth counter bit is 12.8 microseconds. The cycle time of the SRM is such that it removes the data from the ninth counter bit of any one channel every 12 microseconds. In order to cover sixteen channels, the SRM operates for 750ns on each channel.

Reference should be made to logic diagram (Figure 13) and timing diagram (Figure 24). The cycle can be described as follows:

$\overline{T10}$  goes to 0 for 100ns and resets the output flip-flop, SN7472N on the counter board.

M0 goes to a 1 for 250ns and transfer the ninth bit of the 0 channel into the SN7472N flip-flop. The complement of this flip-flop is applied to "counter input 1" of the SRM. This applies the true value to the J and the complement to the K input of the first flip-flop in the SRM counter. The counter in the SRM consists of the A2, A3, A7, A8, B1, B2, B6, and B7 flip-flops.

During any 750ns period, the SRM counter acts as the counter for one of the sixteen channels associated with it. The channel data is shifted from the SN7491N shift registers into the counter, a count made and the number reinserted into the shift registers.

$\overline{T5}$  and  $\overline{T8}$  go to 0 and transfer the eight bits at the output of the shift registers into the counter. This represents the eight bits for channel 0 as integrated up to the particular time we are speaking.  $\overline{T8}$  goes to a 0 before  $\overline{T5}$  and back to a 1 before  $\overline{T5}$  to prevent incorrect data transfer.

T6 goes to a 1 for 100ns and transfers the eighth bit counter data to the first counter bit of the SRM. If the data changes the A2 flip-flop from a 1 to a 0 there is a carry down the counter.

T7 goes to a 1 for 100ns and shifts out from the SR the old channel 0 and shifts into the top of the SR the new channel 0 from the counter.

$\overline{T9}$  remains at 0 during this process.

$\overline{T2}$  changes similar to  $\overline{T5}$  and  $\overline{T8}$  except that it goes to 0 first and goes to a 1 last. A 0 on the flip-flop reset will not prevent a transient pulse on its output when a negative going signal hits the clock input. The purpose

in the use of  $\overline{T2}$  is to prevent this transient. That is also the purpose of the J and K input signals to flip-flops A3 and B2.

### I. Core Memory

Figure 9 is a block diagram to indicate the overall operation of the SRM's and the CORE MEMORY.

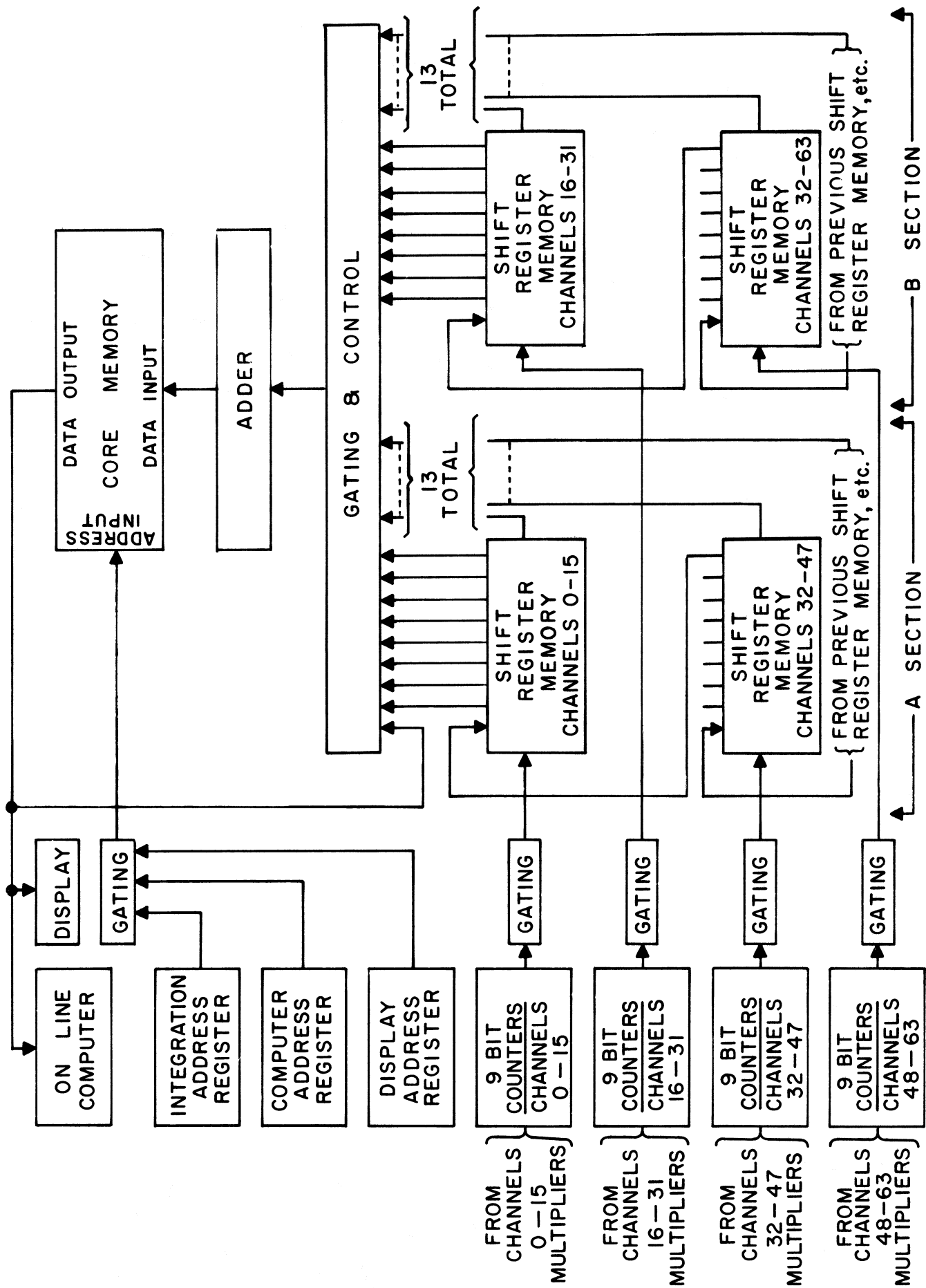
1. Each SRM picks up the data from the COUNTERS at the rate of 750ns per counter - 12 microseconds per 16 counters. Since all 26 SRM's run in synchronism, in 12 microseconds all of the counters have been looked at once by the SRM's.

2. In a similar manner, the CORE MEMORY picks up the most significant bit data from each of the 16 counters in each of the 26 SRM's.

3. During blanking time, the core memory picks up all eight of the 16 counters in each of the 26 SRM's.

Item 1 has been described above. Items 2 and 3 will now be covered; again with the assumption that the required control signals are available and leave their generation for later discussion.

The gates (1C) being fed by the various F12's provide a selection matrix for which SRM most significant bit is to be picked up next. F12 is the core register address counter for integration purposes. Therefore, when it selects a particular SRM it is also selecting a group of 16 associated words in core memory. This matrix continues with the gates (1D) fed by the SM's from the SRM's. This all culminates in the SM of one SRM being applied to the SF1 shift register. The timing is such that the MSB of the first 8 channels is stored in SF1. These are removed one at a time and added to the data of the corresponding channel. This data was transferred to the output register of the core in the read mode. The SM bit and channel data are added in the SN7482N (1A,B) adders. The SM bit represents the 8th bit



DATA FLOW - SHIFT REGISTER MEMORY TO CORE MEMORY

Figure 9

and is added in at that point. However, the sum of the 8th adder is stored (3D) in position 24 during integration and (3A) in position 8 during blanking time. This makes the latest data available in position 8.

During the first part of the blanking time, the eight bits of the SRM are transferred out of the SRM's, as previously explained, into core memory. They are taken out eight channels at a time into temporary storage in shift registers SF2. From here they are added one channel at a time to the associated data from core and this new data re-entered into core.

Data to be entered into core must go through (3) diode selection gates into temporary storage in register F10. F10 output is applied to the core memory data input lines through SN7440N gates for buffering and line driving purposes. The selection gates are controlled by the matrix N which selects counter data for the first 416 positions of the address register F12. For the next 16 positions it selects control (knob) settings.

Data to be sent to the COMPUTER is gated from the CORE MEMORY to the COMPUTER WORD STORAGE REGISTER (2D). Transfer into the register is accomplished by  $\overline{T18}$  clocking the F17 flip-flops. The COMPUTER can accept a maximum of 16 bits, whereas the A/C receiver words are 20 bits long. Therefore, the A/C words are sent into two parts, first 15 bits and then 5 bits. This is done by taking each word out of the CORE MEMORY twice and breaking it up into two parts with selection gate signal (20) F13-0 and  $\overline{F13-0}$ . F13 is the first bit of the COMPUTER ADDRESS COUNTER whose operation is covered in a later section.

Bit A/C  $I_1$  is the sign bit of the COMPUTER. It starts as a 1 at the beginning of each transfer of data between the A/C and COMPUTER. In each successive word it alternates back and forth between 0 and a 1. This is used as a check by the COMPUTER that no words are missed.

## J. Blanking Time

BLANKING TIME occurs at the end of each integration period - every half cycle of the switching frequency. It is required in order that the counter stop counting while the data is removed from the SRM's to the CORE MEMORY. It is also required so that the old data in the correlator SHIFT REGISTERS can be cleared out (signal or reference) and new data (reference or signal) can be shifted in. Thus, during BLANKING TIME, the COUNTERS and SRM's are reset after their data is transferred to the CORE MEMORY. Also, during this time, the correlator SHIFT REGISTERS continue to operate while the MULTIPLIERS are stopped by gating off their clock.

This is all controlled by T3 (see timing diagram, Figure 25). T3=1 during integration; T3=0 during BLANKING TIME. BLANKING TIME starts when F47-1→1. This is the SWITCHING SIGNAL SYNCHRONIZER (9A), which indicates the completion of half of a switching cycle. F47-1 allows the clock to flip F7 (8B) and cause T3→0 when the output of F7 is shifted into F8, the T3 drivers.

The length of the BLANKING TIME is determined by the setting of switch 7 between 4 and 24ms in 2ms steps. The switch input is provided by counter F6 (9A) which receives a pulse every 2ms. The switch in combination with gate B3T21 decodes the counter to provide a signal T29 which goes to a 1 after the required number of milliseconds have passed. T29 feeds the J input of F7 (8B) to put an end to the blanking time and drive T3 back to a 1.

## K. Control Signals

### 1. Switching Signals

Switching signals are the various F's, T's, etc. which have been assumed in previous discussions. These will be discussed in the order of their generation, as many depend on previously generated signals for their timing.

All switching rates are determined by the telescope timing generator which supplies the A/C receiver with 10 KHz and 0.1 Hz (see timing diagram, Figure 25). The 10 KHz (9A) drives a divider which provides all switching rates required from 0.1 Hz up. The 0.1 Hz timing generator signal synchronizes the divider with real time 10 second periods. F-46-1&2 provide a 500ns reset pulse to the F5 divider.

Synchronizer F47 provides a pulse to the blanking time generator (8B) to start the blanking time (T3→0). The "Sw. Rate Generator" gates (9D)-in conjunction with SW1, SW8 and associated level converters (DT-552)-generate the switching signals for the front end, local oscillator, gain modulator and synchronous detector.

## 2. Counter & SRM Control

The counter and SRM control generation logic is contained on one drawing (6). Refer to timing diagram of Figure 24 for the following explanation. F1 is a three state counter whose outputs F1-1 and F1-2 and their complements are used to generate many control signals. The generation of T5, T6, T8, and T10 are obvious. F2(6A) is a shift register counter whose count is as follows:

```
00000000
00000001
00000011
00000111
00001111
00011111
00111111
00111111
01111111
11111111
11111110
11111100
11111000
11110000
11100000
11000000
10000000
00000000
```



This is an ambiguous code with only one bit changing at a time. It also requires only two bits to decode any state. This is used in the decoding matrix (6A&B) to form the M control signals. Gates BlX and BlT feeding the J input on F2-1 prevent the counter from getting locked upon a count not listed in the table above. The BlX gates feeding the reset inputs of F2 are to synchronize the counter with other control signals so that the ANDED functions F2-1·F2-8, etc., are as shown on the timing diagram of Figure 26. The shift pulse T12, is a power version of F1-2. The strobe pulse T13 is a power version of F1-1 (6D). The remaining signals on this drawing must wait for an explanation of T7 and F11-1&2.

### 3. Address Registers & Controls

The CORE MEMORY is addressed by three address registers (4) which are time shared as shown by the START pulses on the timing diagram of Figure 26. During a 6 microsecond period, one "computer" start and one "display" start pulse can occur if called for. During the next 24 microseconds period, sixteen "integrate" start pulses occur. These sixteen pulses are to "read-modify-write" the data for eight of the sixteen channels on a SRM board. The next 30 microseconds repeats this 6 and 24 microsecond cycle, this time integrating the next eight channels of the SRM.

The INTEGRATION ADDRESS REGISTER is used as a control in many places besides addressing memory. It counts and controls the removal of the SM data from the SRM's to temporary storage during integration and also controls removal of the 8 channels of 8 bits of data each from the SRM's to temporary storage during blanking time. These two removal operations occur during the 6 microseconds in which the core memory is used for "computer" and "display"; and require that the first three stages of the counter go through eight states. This is accomplished by holding the J-K inputs of the fourth counter stage at

0 for the 6 microseconds with  $\overline{F31-2}$ . Thus, if T14 is properly generated, F12-1,2, and 3 can count from 000 to 111 and back to 000 without a carry and without a change in address during the 6 microseconds. During the 24 microseconds period of integration, the counter operates normally with  $\overline{F31-2}=1$  and counts in two modes determined by F9 and the gates controlling F9. One mode is during integration when the count is from 0 to 415 for the 416 channels. The other mode is during the first portion of blanking time when the count is from 0 to 431. The extra 16 counts picks up the A/C receiver control (knob) settings and stores them in core. During this 0 to 431 count, the SRM data is transferred to core and reset as previously described. The system then switches from signal to reference or vice versa. F12-10 changes the sub-sector of core being address to signal or reference, as the case may be. The change occurs at the end of the 431 count as controlled by the inputs to F12-10; SW-1B, the switching rate, and F11-3 which indicates the end of the 0 to 431 count and will be covered later.

The sector of memory being addressed by the INTEGRATION ADDRESS REGISTER is controlled by counter F14-1 which changes state every dump time. F14-1 is controlled by F35 being driven to a 1 by SW-2A (every 1 second or 10 seconds). F35 is NEEDED with F11-3 to switch F14-1 at the end of the 0 to 431 count which occurs at dump time.

When the COMPUTER or DISPLAY ADDRESS REGISTER are to control the core, the sector is changed for 6 microseconds by F31-1 $\rightarrow$ 1 and  $\overline{F31-1}\rightarrow$ 0. This 6 microseconds is divided into two 3 microsecond periods, the first for the computer and the second for the display. These are controlled by F58 and F59.

The COMPUTER ADDRESS REGISTER must transfer the 416 channels of signal data, the 416 channels of reference data, and the KNOB POSITIONS to

the computer. The KNOB POSITIONS are recorded in both the signal and reference sub-sectors, but only those in the reference sub-sectors are transferred to the COMPUTER. Each A/C receiver word must be removed from the CORE MEMORY twice in order to send it out in two parts of 15 bits and 5 bits each. F13-0 accomplishes this by dividing the input clock pulses to the COMPUTER ADDRESS REGISTER by 2. Therefore, the count for the COMPUTER ADDRESS REGISTER is controlled to be 0 to 831 for one sub-sector and 0 to 863 for the other by F25 and its controlling gates.  $\overline{T24}$  resets the register each dump time to be sure it is in synchronism with the remainder of the system.

The DISPLAY ADDRESS REGISTER is only used for channel data and thus counts from 0 to 415. When it resets to 0, F36-10 automatically flips and changes sub-sectors. The sub-sector, signal or reference, is indicated by the lamp L7. A decimal display indicating the channel number of the data being displayed is required. This is obtained by simultaneously counting in decimal with F45. Both F36 and F45 are reset simultaneously to prevent loss of synchronization.

#### 4. Miscellaneous Controls

Refer to timing diagram (Figure 26) and control logic drawing number 5. A table of cycle times will be helpful in understanding and keeping in mind all of the control signals:

OPERATION	CYCLE TIME
Transfer of data - one counter channel to SRM	750ns
Transfer of data - 16 counter channels to SRM	12 $\mu$ sec
Transfer of 8 channels of data from SRM to temporary storage	6 $\mu$ sec
Transfer of 8 channels of SRM data from temporary storage to CORE MEMORY	24 $\mu$ sec
Transfer of 416 channels of SRM data to CORE MEMORY	1560 $\mu$ sec
Transfer of 16 words of knob position to CORE MEMORY	60 $\mu$ sec
Transfer of data from CORE MEMORY to storage register for COMPUTER after RRL signal	30 $\mu$ sec max.

During one cycle of F12-1,2,&3, the core is in full cycle-read mode. During the next cycle the core is in half cycle read-modify-write-mode. The half-full cycle is determined (5A) by F12-3A controlling F31-1. F31-1 controls F31-2 which locks the core on read or lets it read or write as directed by F32-2. The two gate paths from F31-1 to the J of F31-2 are because  $F2-1 \cdot F2-8$  occurs at the beginning of one 6 microsecond cycle and  $\overline{F2-1} \cdot \overline{F2-8}$  occurs at the beginning of the next 6 microsecond cycle. As can be seen from the timing diagram, T14 must produce 8 pulses during the 6 microsecond period and 8 pulses during the 24 microsecond period. These two different frequency rates are controlled by the gates on the output of F31-2. F32-1 and F32-2 control the read-write cycle time allowing 1.5 microsecond for each.

The CORE MEMORY "start" pulse is generated by one of three logic units (5A&C): (1) INTEGRATE START GENERATOR, (2) COMPUTER START GENERATOR, and (3) DISPLAY START GENERATOR. The INTEGRATE START GENERATOR produces a start pulse every 1.5 microseconds for 24 microseconds out of every 30 microseconds when data is transferred from the temporary storage to the CORE MEMORY. One start pulse is required for read and one for write in the read-modify-write mode.

The COMPUTER START GENERATOR produces one start pulse when required during the first 3 microseconds of the 6 microseconds period when the SRM data is going into temporary storage. These start pulses are required when dump time occurs and new data is ready to be sent to the COMPUTER. This procedure is started by  $\overline{T24} \rightarrow 0$  and applying a 1 to the J input of F40-1 (5C). Immediately after the read cycle is completed,  $T18 \rightarrow 1$  and a PIL A/C (Priority Interrupt Pulse) is sent to the COMPUTER.

The second requirement for a COMPUTER START PULSE is each time the COMPUTER has removed the data word on its lines and signifies the need for the next word by sending an RRL (Reset Ready Line). The RRL through F40-2 and F41 generates a start pulse. There are a total of 416 signal words + 416 reference words + 10 knob position words (6 are not used) = 842 words A/C receiver words. When these have all been transferred to the COMPUTER, this fact is detected by T37 and T18 controlling F40-3 which then prevents F40-2 from accepting any further RRL's until the next dump time T24+1.

The DISPLAY START GENERATOR will be covered at the same time the display is explained.

The F-11 counter has five states. The counter assumes each of these states, except the zero state, at the same point in the 60 microsecond cycle. The purpose of this counter is to control the transfer of data from COUNTER to SRM to CORE MEMORY immediately after the start of BLANKING TIME until all the data is transferred.

As soon as BLANKING TIME starts we must allow the SRM to complete the 12 microsecond cycle it is in (0 state). We then make sure it goes through one more of these cycles to pick up all of the counter carries (1 state). Then we wait for the core memory to complete the 1560 microsecond cycle it is in (2 state). The next 1620 microsecond cycle is used to transfer the data from the SRM's and the knob position to the CORE MEMORY (3 state). The system is then allowed to start integrating again (4 state) even though the blanking is not over. At the completion of BLANKING TIME, the F11 counter returns to the 0 state.

The following table will be a helpful reminder of the F11 counter operation:

STATE	TIME SPENT ON STATE	MAIN SIGNALS DRIVING COUNTER	OPERATION
0 = 000	Leaves 0 after T3 at beginning of 12 $\mu$ sec cycle		
1 = 001	12 $\mu$ sec	$\overline{T3} \cdot M0$	One complete cycle-counter to SRM data
2 = 010	0 to 1560 $\mu$ sec	$\overline{T3} \cdot M0$	Waiting for beginning of 1560 $\mu$ sec SRM to CORE MEMORY cycle
3 = 011	1620 $\mu$ sec	F9	Transfer data SRM to CORE MEMORY
4 = 100	Blanking time minus sum of above times	F9	Waiting for end of blanking time
0 = 000	1/2 Switching cycle plus 0-12 $\mu$ sec	T3	Integrating

The maximum time that the F11 counter can be off of zero is from the above table:

$$12 + 12 + 1560 + 1620 = 3204\mu\text{sec} = 3.204\text{ms}$$

Therefore, the minimum blanking time has been set at 4ms.

The CORE MEMORY must be reset, just prior to the start of integration, in the sector which has been dumped into the COMPUTER. This reset is controlled by the CORE MEMORY RESET GENERATOR (5D).

The four state counter F44 is controlled by T24 and F9 to start reset immediately after transfer of data from the SRM's to CORE MEMORY at dump time - F11-3 $\rightarrow$ 1 then T24 $\rightarrow$ 1. It resets the signal half of the sector of memory which has been sent to the COMPUTER. The reset process is stopped by F9 which is the reset for the INTEGRATION ADDRESS REGISTER. At the end of the first half of the switching cycle following dump time, F9 starts the reset of the reference half of memory. F9 then stops the reset process upon completion of the reference

reset and counts the F44 counter back to 00. A table showing the process is listed on drawing 5D below the F44 control gates.

T7 is controlled by five main gates (5B) B2Y49, B2Y80, B2Y90, B2Y91, and B2X60. (See timing diagrams, Figures 24 and 26). During integration T7 is determined by B2X60 and follows in the proper sequence after T5 and T6. When  $\overline{T9} \rightarrow 1$  and the data is to be transferred from the SRM's to CORE MEMORY, the other four gates are used. In this case we must produce 16 pulses in two groups of 8 to T7A. The 8 pulses are spread over 6 microseconds and separated from the second 8 pulses by 24 microseconds. Then while T7B goes through the same process, T7A must generate 112 pulses. This process continues until all of the data is shifted out of the SRM's and into CORE MEMORY.

The SRM SHIFT SLEW CONTROL starts the F30 counter at the beginning of each of the above cycles and gate B2Y21, feeding the K input of F29-1, detects a 111 count on F30 and F29-1 stops and resets F30 at a count of 112. Thus F29-1 controls T7 for 112 pulses through gates B2Y90 and B2Y80. Gates B2Y49 and B2Y91 with their NANGED inputs control T7 for the 16 pulses. Gate B2Z52 prevents the 16 T7A pulses being generated when the last 112 T7B pulses are being generated.

During this process,  $\overline{T25}$  must be a rectangular wave which changes state every 16 T7 pulses. This is accomplished by the F48 and F49 counters.

TEST SIGNALS are controlled by SW9 (9,C,D) and toggle switches on the IF-Filter rack. There are three toggle switches on the IF-Filter rack which control the A,B,and C receivers. Unless at least one of them is in "test" position no TEST SIGNALS are fed to the system except for positions 10 and 11 of SW9. T34 is controlled by these toggle switches and controls the test gates (9C) producing the "Test Signal to Clipper" on B4A-J3. This test signal is a selectable square wave from 39.0625 KHz to 10 MHz for positions 1 through 9 of SW9. The delay multivibrators A3BB31 & 32 (8D) insure a square wave

shape at 10 MHz. Positions 10 and 11 provide a 1 and 0 respectively directly to the drivers on the output of the sampler. These two positions are only applicable to receiver A and C and do not apply to the second 192 channels even in serial operation.

Position 12 of SW 9 produces  $\overline{T32}$  which controls a square wave sent to the SRM's "test input" (6D). SW11 selects two different frequencies. In position 1 a 24 microsecond period square wave is generated. This is the maximum rate of input acceptable by the SRM's and is helpful in troubleshooting the SRM's. This rate produces an output from the SRM's which is faster than the core can accept. Position 2 provides a square wave of 60 microseconds for an output acceptable to the CORE MEMORY.

The NOISE TUBE DUTY CYCLE is controlled by SW5 and F60. In the 50%-50% position 1, the noise tube is on during the first half of each switching cycle for every other dump period, and off for the second half of each switching cycle for that same dump period. During the "in between" dump periods, the noise tube is off for the entire period. On the 10%-90% position 2, the dump period in which the noise tube cycles on and off is one out of every ten.

A switch on the IF-Filter rack controls relay K3 (9D) which selects the PARALLEL or SERIES mode. In the SERIES mode, sampling, shifting and multiplying rates of the second 192 channels are determined by the bandwidth switch - WA- on the A receiver.

The following table lists all of the switching signals and associated data. Gain modulator B and synchronous detectors B and C can be made in or out of phase with A by the connection of "observers option", as indicated on the drawing (9B):



SIGNAL	DESCRIPTION
Front End Switch	Two square waves at switching rate, 180° out of phase. Signal = 0V Reference = -6V.
Noise Tube Switch	Two square waves at switching rate, 180° out of phase during switching, in-phase when not switching. Noise tube off = 0V Noise tube on = -6V.
Local Oscillator Switch	One square wave at switching rate. Signal = 0V Reference = -6V.
Gain Modulator Relay	Two square waves - in or out of phase as chosen by wiring in SCF(9B) - at switching rate. Signal = open Reference = gnd. +24V at approximately 200mA.
Synchronous Detector Relay	Same as Gain Modulator, except: A $\approx$ 44mA      B&C $\approx$ 88mA.

A "TEST LIGHTS" switch, SW10, applies ground to one side of all lamps except power supply lamps to test lamp operation.

#### L. Display

Two displays (2) are provided, both in decimal form. One is Channel Data for the 416 signal channels and the 416 reference channels. The other indicates the channel number of the data being displayed and whether it is signal or reference.

The controls are as follows:

#### SW-3 - Display Mode

Position 1 - Display Update: Channel number remains constant. Data display is updated at every dump time.

Position 2 - Display & Advance: Channel is advanced at rate determined by Display & Advance Rate Knob. As each new channel number appears the data display changes to show the data in that channel.

Positions 3, 4, & 5 - Advance 10 Ch/s, 50 ch/s, and 250 Ch/s: Advance the channel display at the rate indicated. The Channel Data Display is inoperative.

SW-4 - Display & Advance

Up is a locked position. Down is a spring return position. If the toggle switch is up or down, the Display Mode Knob (SW3) is activated for all positions except Display Update. Display update does not require the use of this toggle switch.

Rheostat-Display and Advance Rate

[Connected to pin 95 of A3BB oscillator in DISPLAY CONTROL (2B)]. When the Display and Advance (SW4) knob is in the Display and Advance Position (position 2), this rheostat controls the rate of advancing from one channel to the next. The rate varies from approximately 0.8 Hz to 3.5 Hz.

Reference should be made to timing diagram (Figure 27). The divider F50 (2B) provides the advance and display frequency of 0.8 to 3.5 Hz. Advance is controlled through F38-3 to  $\overline{T20}$  when advancing only, and through F38-1 to  $\overline{T20}$  when displaying and advancing. They are interlocked so that advance cannot start in the middle of a display binary to decimal conversion.

In displaying, the channel selected is in the DISPLAY ADDRESS REGISTER and as previously described, is also stored in a decimal counter whose contents are displayed on the channel number display.

At the beginning of a display cycle the DISPLAY BINARY COUNTER F18 - which counts down - is in the zero state and the DISPLAY DECIMAL COUNTER F19 and DISPLAY STORAGE COUNTER F43 contain the data from the last conversion.

A 1 on the J input of F38-1 is transferred through F38-2 to counter F37 setting T21 to a 1.

T21 resets the Decimal Counter to zero, and through the ZERO DETECTOR gating (2A) enters one pulse into the DISPLAY BINARY COUNTER which causes it to go to all ones.

The next C2 pulse on Counter F37 (2B) drives T22 to a 1. T22 through F34 generates a DISPLAY START PULSE and at the completion of the core memory

read cycle causes  $T19 \rightarrow 1$  for 750ns (5A,B). T19 transfers the core memory output to the DISPLAY BINARY COUNTER. T19 also allows the F37 counter to advance on the next C2 to generate a 1 for T23. This opens the ZERO DETECTOR (2A) gate B2U91 so that as soon as  $\overline{F34}$  returns to a 1, C4 pulses are fed through to the F18 and F19 counters until the F18 counter reaches 0. At that time the F19 counter contains the desired number in decimal form and  $\overline{T26}$  goes to a 1. This allows F38-2 (2B) to be set to a 0 by C2, which resets the F37 counter allowing  $\overline{T23} \rightarrow 1$  and  $T26 \rightarrow 0$ .  $T26 \rightarrow 0$  transfers the data in counter F19 to storage register F43 from whence it is displayed.

APPENDIX I

LIST OF CONTROL SIGNALS

In the following the true form of each signal is listed, even though in some cases, only the complement exists. Differentiating letters are not listed, e.g. C4 is listed but not C4A. Dash numbers are not listed when many flip-flops have the same main number, unless the modules perform different tasks. Because of the many uses of some signals, only the main logical functions are listed.

- C2 2 MHz clock
- C4 4 MHz clock
- C10 10 MHz clock
- C20 20 MHz sine wave clock
  
- F-1 Count of 3 binary counter. Associated with SRM controls.
- F-2 Count of 16 shift counter. Generates M0 through M15.
- F-3 Count of 5 binary counter. Generates C4.
- F-4 Not used.
- F-5 Decimal counter. Generates switching rate frequencies.
- F-6 Count of 16 binary counter. BLANKING TIME counter.
- F-7 Start-stop flip-flop. BLANKING TIME control.
- F-8 BLANKING TIME control drive.
- F-9 Reset INTEGRATION ADDRESS REGISTER.
- F-10 Storage register. Stores data from ADDER and knob indicators for CORE MEMORY input.
- F-11 Count of 5 binary counter. Controls transfer of data during BLANKING TIME from counters to SRM to CORE MEMORY.
- F-12 Count of 832 or 864 binary counter. INTEGRATION ADDRESS COUNTER.
- F-13 Count of 1684 binary counter. COMPUTER ADDRESS COUNTER.
- F-14 Count of 10 decimal counter. Provides noise tube duty cycle logic with count of 10 dump time. F14-1 selects memory sector; integration data or computer data.
- F-15 Not used.
- F-16 Not used.
- F-17 Storage register. Stores data from CORE MEMORY to COMPUTER.

- F-18 Count of 1,048,576 binary down counter. DISPLAY BINARY COUNTER.
- F-19 Count of 1,000,000 decimal counter. DISPLAY DECIMAL COUNTER.
- F-20 Count of 512 binary counter. Sampling rate frequency generator.
- F-21 Not used.
- F-22 SAMPLER output drivers.
- F-23 SAMPLER output drivers-to multiplier drivers.
- F-24 SAMPLER output drivers-to CORRELATOR shift registers.
- F-25 Reset COMPUTER ADDRESS REGISTER.
- F-26 Count of 2 binary counter. Rec. A power counter buffer.
- F-27 Count of 2 binary counter. Rec. B power counter buffer.
- F-28 Count of 2 binary counter. Rec. C power counter buffer.
- F-29 SHIFT REGISTER MEMORY. Serial shifter control.
- F-30 Count of 112 binary counter. Controls advance of SRM serially to 112 shifts during transfer of SRM to CORE MEMORY.
- F-31 Selects pulse rate at which to advance INTEGRATION ADDRESS REGISTER and temporary storage shift register.
- F-32 Generates read and write mode signals and start pulse for CORE MEMORY.
- F-33 Generates C2.
- F-34 Stores T21 to generate display start pulse to CORE MEMORY.
- F-35 Dump time buffer.
- F-36 Count of 832 binary counter. DISPLAY ADDRESS COUNTER.
- F-37 Count of 4 binary counter. Display control.
- F-38 Display controls.
- F-39 Prevents false T18 and T19.
- F-40-1 Controls PIL A/C and first computer start signal after dump time.
- F-40-2 Controls RRL generated computer start signal.
- F-40-3 Stops COMPUTER ADDRESS REGISTER (RRL's from computer) after 1683 computer words.
- F-41 Stores and synchs RRL A/C and PIL. Generates DRL. Controls computer start pulse.
- F-42 Controls reset of DISPLAY ADDRESS REGISTER.
- F-43 Display storage register.
- F-44 Count of 4 shift counter. Controls CORE MEMORY reset.
- F-45 Count of 832 decimal counter. Display address register - binary to decimal converter counter.
- F-46 Synchronizing control for 0.1 Hz signal from timing generator.
- F-47 Synchronizing control for switching rate. Starts BLANKING TIME.

- F-48 Count of 32 binary counter. Generates shift input signal (T25A) for reset of SRM's.
- F-49 Count of 32 binary counter. Generates shift input signal (T25B) for reset of SRM's.
- F-50 Count of 256 binary counter. Divides variable oscillator frequency for display and advance rate.
- F-51 Count of 2 binary counter. Generates 12  $\mu$ sec test square wave for SRM's.
- F-52 Not used.
- F-53 Not used.
- F-54 Controls length of  $\overline{T8}$ .
- F-55 Controls length of  $\overline{T2}$ .
- F-56 Lengthens F34 true output to prevent transient into T18 and T19.
- F-57 Increases width of PIL to 4  $\mu$ sec.
- F-58 Controls gating of COMPUTER ADDRESS REGISTER to CORE MEMORY.
- F-59 Controls gating of DISPLAY ADDRESS REGISTER to CORE MEMORY.
- F-60 Delays signal to noise tube switch and determines phase.
- M Matrix. Selects one of sixteen counters, on each set of two counter cards, whose most significant bits will be transferred to the SRM's.
- N Matrix. Selects integration or knob information word to store in CORE MEMORY input data register.
- OD Output data from CORE MEMORY.
- SF Shift registers. Temporary storage between SRM's and CORE MEMORY.
- SM Most significant bit outputs from SRM's.
- T0 Controls 20 MHz clock. T0 = 1 for 20 MHz sampling rate. T0 = 0 for all other sampling rates.
- T1 Not used.
- T2 Prevents carry in SRM's.
- T3 BLANKING TIME control. Inhibits multiplier clock during BLANKING TIME.
- T4 Controls gates passing C10 to generate lower frequency clock rates.
- T5 Transfer data from SR's to counter in SRM's.
- T6 Transfer MSB's from counters to SRM's.
- T7 Clock for SR's on SRM's.
- T8 SRM's counter reset input control.
- T9 SRM's counter set input control. T9 = 1 during integration time. T9 = 0 during transfer of SRM data to core memory (1620  $\mu$ sec at beginning of dump time).
- T10 Reset on synchronizing storage flip-flops on outputs of COUNTERS.
- T11 Resets COUNTERS.

- T12 Advances matrix M counter (F2).
- T13 Strobes matrix M to produce M0 through M15.
- T14 Advances INTEGRATION ADDRESS REGISTER and shift register temporary storage registers (SF2).
- T15 Not used.
- T16 Clock for CORE MEMORY input data storage register (F10).
- T17 Not used.
- T18 Clock for CORE MEMORY output data storage register (F17) feeding the computer.
- T19 Strobe pulse, transfers CORE MEMORY output data into DISPLAY BINARY DOWN COUNTER.
- T20 Advances DISPLAY ADDRESS REGISTER.
- T21 Reset for DISPLAY DECIMAL COUNTER. Controls display start pulse to CORE MEMORY. Adds a one to the DISPLAY BINARY DOWN COUNTER prior to conversion.
- T22 Controls display start pulse to CORE MEMORY.
- T23 Controls start of display binary to decimal conversion.
- T24 Indicates CORE MEMORY is ready to be dumped into COMPUTER. Controls PIL A/C, first computer start pulse after dump time, reset of CORE MEMORY, etc.
- T25 Produces, 1,0,1,0----pattern to reset SRM's during transfer of data from SRM's to CORE MEMORY.
- T26 Clock pulse for DISPLAY STORAGE REGISTER. Transfers in new display data.
- T27 Reset on F10 CORE MEMORY input data display register. Provides reset of CORE MEMORY at dump time.
- T28 Controls selection of serial (2 ea. 192 channels) or parallel (1 ea. 384 channels) operation through reed relays and SAMPLER output drive gating.
- T29 Controls BLANKING TIME length - stops BLANKING TIME.
- T30 Selects input to SAMPLER output drivers: SAMPLER or 1,0 test signal.
- T31 Indicates to COMPUTER when noise tube is on.
- T32 SRM test control.
- T33 1,0 test signal into SAMPLER output drivers.
- T34 Indicates if test controls on IF-Filter rack is on Test (T34 = 1) or operate (T34 = 0). Controls test signal logic.
- T35 Complement of computer start pulse. Controls F39 and resets F29 (reset flip-flop on COMPUTER ADDRESS REGISTER).
- T36 One of two clock on integration temporary storage shift register (SFI) between SRM's and CORE MEMORY. Clocks SFI when data goes from SFI to CORE MEMORY. T7 clocks from SRM to SFI.

- T37 Controls computer start pulses at end of transfer of data to computer such that no further computer start pulses can be generated until the next dump time.
- W Three four bit BCD codes from IF-Filter rack which indicate the bandwidths of receivers A, B, and C. Controls sampling, shifting, and multiplying frequencies.
- Y Channel numbers 0 to 15 (A) and 16 to 31 (B) SRM's shift register outputs.
- $\Sigma$  Output of adders.



APPENDIX II

CONTROL LOGIC NUMBERING GUIDE

IC TO CARD CONNECTOR

IC #1	Card Pin No.	IC #2	Card Pin No.	IC #3	Card Pin No.	IC #4	Card Pin No.	IC #5	Card Pin No.	IC #6	Card Pin No.	IC #7	Card Pin No.
1	12	1	26	1	40	1	54	1	68	1	82	1	94
2	11	2	25	2	39	2	53	2	67	2	81	2	95
3	13	3	27	3	41	3	55	3	69	3	83	3	92
4	14	4	28	4	42	4	56	4	70	4	84	4	96
5	9	5	23	5	37	5	51	5	65	5	79	5	93
6	10	6	24	6	38	6	52	6	66	6	80	6	90
7	8	7	22	7	36	7	50	7	64	7	78	7	78
8	7	8	21	8	35	8	49	8	63	8	77	8	91
9	1	9	15	9	29	9	43	9	57	9	71	9	85
10	2	10	16	10	30	10	44	10	58	10	72	10	86
11	3	11	17	11	31	11	45	11	59	11	73	11	87
12	4	12	18	12	32	12	46	12	60	12	74	12	88
13	5	13	19	13	33	13	47	13	61	13	75	13	89
14	6	14	20	14	34	14	48	14	62	14	76	14	76

CARD CONNECTOR TO IC

Card Pin No.	IC #1	Card Pin No.	IC #2	Card Pin No.	IC #3	Card Pin No.	IC #4	Card Pin No.	IC #5	Card Pin No.	IC #6	Card Pin No.	IC #7
1	9	15	9	29	9	43	9	57	9	71	9	85	9
2	10	16	10	30	10	44	10	58	10	72	10	86	10
3	11	17	11	31	11	45	11	59	11	73	11	87	11
4	12	18	12	32	12	46	12	60	12	74	12	88	12
5	13	19	13	33	13	47	13	61	13	75	13	89	13
6	14	20	14	34	14	48	14	62	14	76	14	90	6
7	8	21	8	35	8	49	8	63	8	77	8	91	8
8	7	22	7	36	7	50	7	64	7	78	7	92	3
9	5	23	5	37	5	51	5	65	5	79	5	93	5
10	6	24	6	38	6	52	6	66	6	80	6	94	1
11	2	25	2	39	2	53	2	67	2	81	2	95	2
12	1	26	1	40	1	54	1	68	1	82	1	96	4
13	3	27	3	41	3	55	3	69	3	83	3		
14	4	28	4	42	4	56	4	70	4	84	4		

APPENDIX III

COMPONENT LIST

The following list of components may be helpful in obtaining required data. Each item is followed by its purchase order (P.O.) number or numbers, which will also be helpful in locating specifications or a source of more data on the component.

BNC to SUBMIN COAX: Seaelectro Corp.; Type 58-010-000 Panel Mount. P.O.22051.

CABLE CONNECTORS: Elco Corp. P.O.20693.

CARD HOLDERS: Elco Varipak II type. P.O.19903.

COOLING FANS: Rotron venturi Sentinel type. P.O.19863, 20757.

CRYSTAL OSCILLATOR: McCoy Electronics Co. P.O.20303.

ELAPSED TIME METER: General Electric Co. Type 236. P.O.22794.

FEEDTHROUGH CAPACITORS: Cornell Dubilier 0.1 mfd. 100V Part No. 3-NFT-3H-1P-1L-10-10; 0.1 mfd. 600V Part No. 3-NFT-3H-6PIL-10-10. P.O.21086, 22054. Sprague 0.01 mfd. 100V

FERRITE BEAD CHOKES: National Radio Co.; Part No. R-45-8. P.O.21084, 23022.

FILTER CAPACITORS: Ceramic Disc Type HY-520 and HY420 Sprague. Electrolytic Type 150D 106 X 0020B2 Sprague. P.O.20458, 21657, 21970, 23462.

HEAT SINKS: Thermalloy Type 2211C and Wakefield-Engineering Type NF204. P.O.22741.

LAMPS: Type 381 (6.3V,200mA) for +5V. Type 382 (14V, 80mA) for  $\pm$  15V, Type 327 (28V, 40mA) for +24V. P.O.22741.

LAMP DISPLAYS: Dialight Corp. Type 134-3830. P.O.22562.

LEVEL CONVERTOR & POWER DRIVER CARDS: Data Technology Corp. Type 550, 551, & 552. P.O.22391.

MEMORY: Decision Control, Inc. (now Varian Data Division); Part No. 2VS-4096/24-RA-N; 4096 words, 24 bits/word, random access address register, NPN interface, 0.9  $\mu$ sec access time, 1.5  $\mu$ sec half-cycle time, 2  $\mu$ sec full cycle time, 2.5  $\mu$ sec read-modify-write cycle time. Power supply part No. MPS-701-3 includes auto data guard and memory tester. P.O.19567, 24072.

OMNI COMB TEST UNIT: Elco Corp.; Per NRAO Drawing Nos. DP-2916-1 & 2 and DP-2914A. P.O.21968.

PISTON CAPACITORS: JFD type MC623Y. P.O.21757, 23023.

POWER CONTROL DETECTION RELAYS: Sensitak Instruments Corp.; Model Nos. S16A3 and S16A1P. P.O.24069.

POWER CONTROL POWER RELAYS: Magnecraft Electric Co.; Model No. W88DX-3.  
P.O.24070.

POWER SUPPLIES: Lambda Electronics Corp.; +5V - Part No. LM-G5-OVM; +15V -  
Part No. L M-261 with metered panels No. MP-5-LM-261; +24V-  
Part No. LM-CC24 with metered panel No. MP-5-LM-CC24; Rack  
Adapter Part No. LRA-6. P.O.20433.  
Trygon Electronics Inc.; +200V - Type PS200-100F. P.O.22141.  
Lambda Electronics Corp.; +5V Part No. LMG 5-OVM, Metered  
panel for +200V Trygon supply, Part No. MP-5-LM-B150.  
P.O.22286, 24071.  
Acopian Corp.; -6V and -18V Model No. E6B70U-12B70U. P.O.22973.

PRINTED CIRCUIT BOARDS: National Circuits Inc.; Timonium, Md. P.O.20510, 20689,  
20688, 20761, 20946, 21108, 21328, 21487, 21486, 21840,  
22105, 22415, 23156.

PRINTED CIRCUIT CONNECTORS: Hughes Aircraft Co.; 44 & 96 contact jackpin type.  
P.O.20429, 22425, 22849.

RACK: Cabtron Corp.; RFI rack; Frame Part No. RFCB-20DD-1961-30; Rear Door  
Part No. RDF-1961-LH; Front Door Part No. RDF-1961-RH; 500CFM Blower  
Part No. RBL-500-1930; 4" Swivel Casters Part No. CA-600S. P.O.19830.

READ-OUT DISPLAY: National Electronics, Inc.; Decoder-Driver type NL-M101  
with NL-8422/5991 Readout tube. P.O.21196.

REED RELAYS: Magnecraft Electric Co.; Part No. 104EPX-4. P.O.22581.

RFI DISPLAY WINDOW: Metex Corp.; Pola-Vu Window, Part No. 09-0301-0367.  
7"x1 3/4" with polarized filter for Nixie tube viewing.  
P.O. 21229.

SILVER & GOLD PLATING ON BUS BARS: C. R. Hudgins Plating, Inc.; Lynchburg,  
Virginia; 500 x 10<sup>-6</sup>"silver, 100 x 10<sup>-6</sup>"  
gold. P.O.21865

TOGGLE SWITCHES: Mil Spec Type MS35059-31. P.O.22808.

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T30	- 25
T32	- 42
T34	- 41
T37	- 39
W1	- 12
W2	- 12
W4	- 12
W8	- 12,22



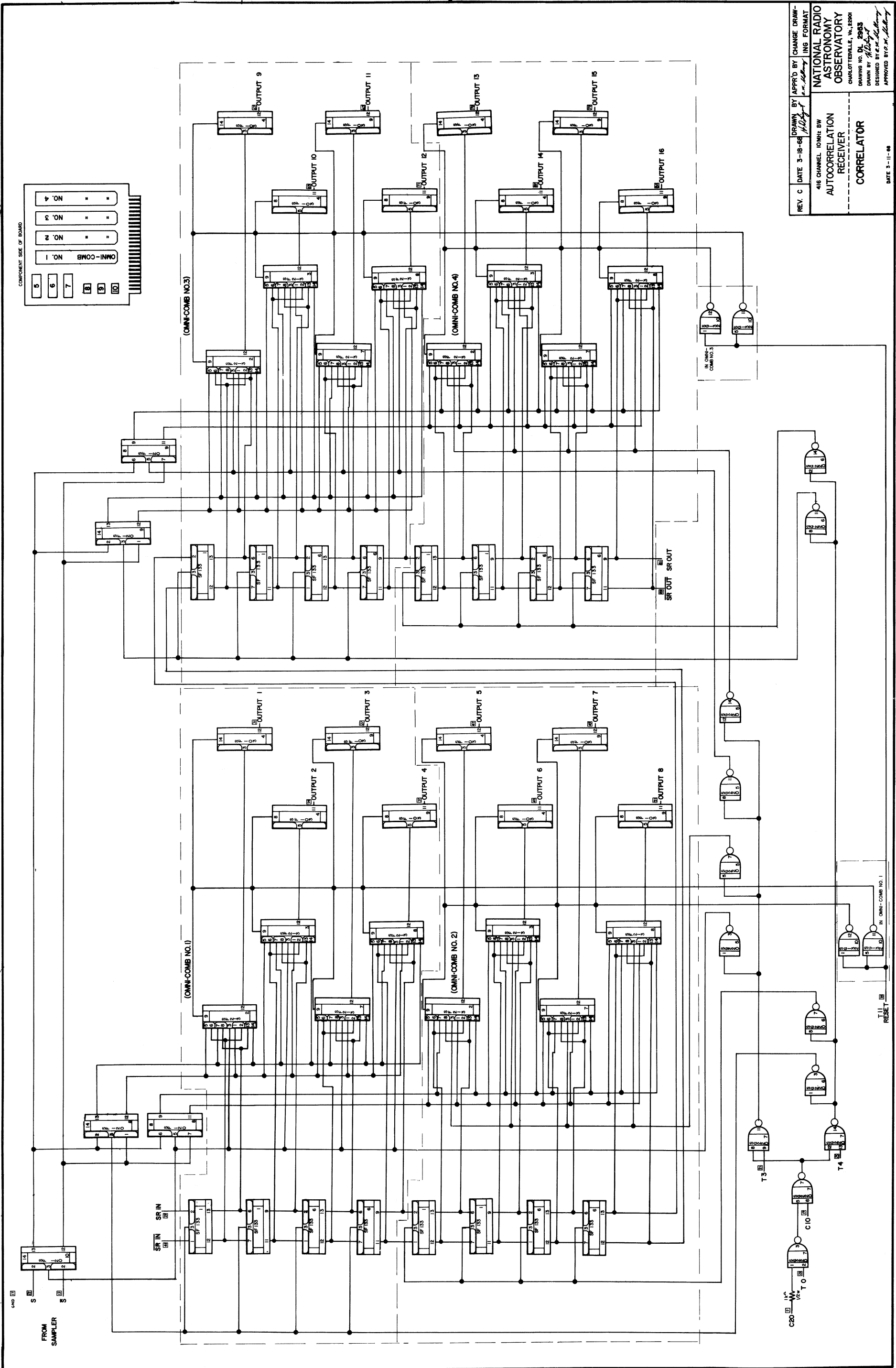
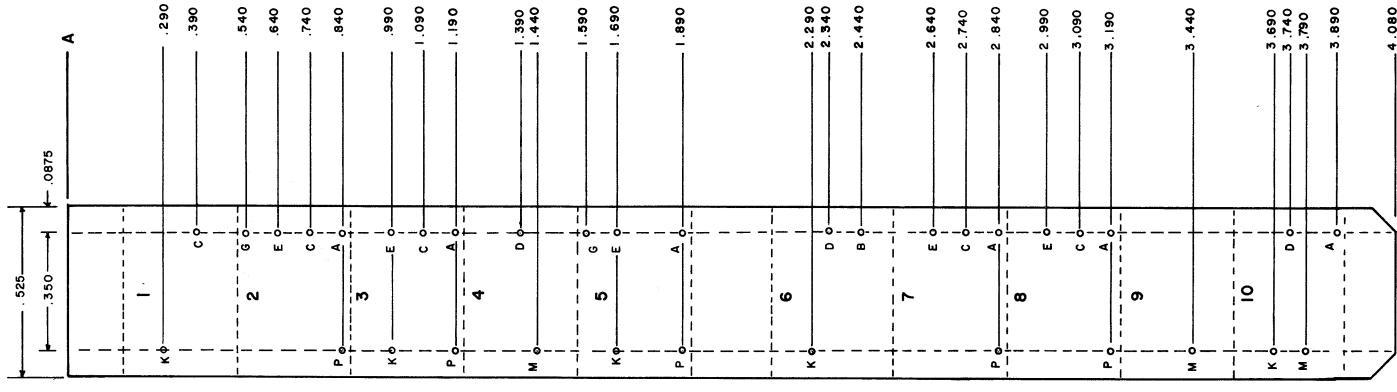
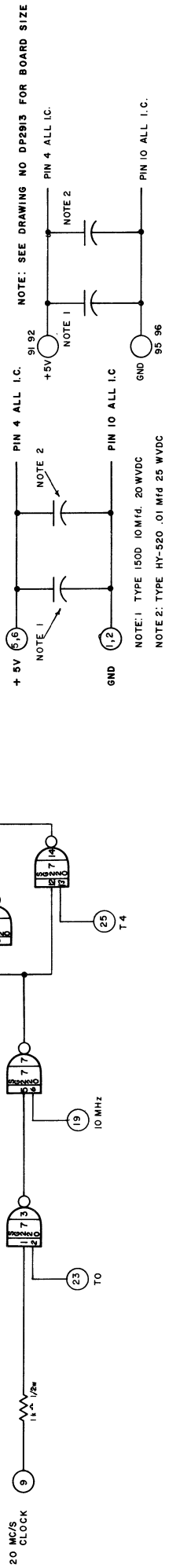
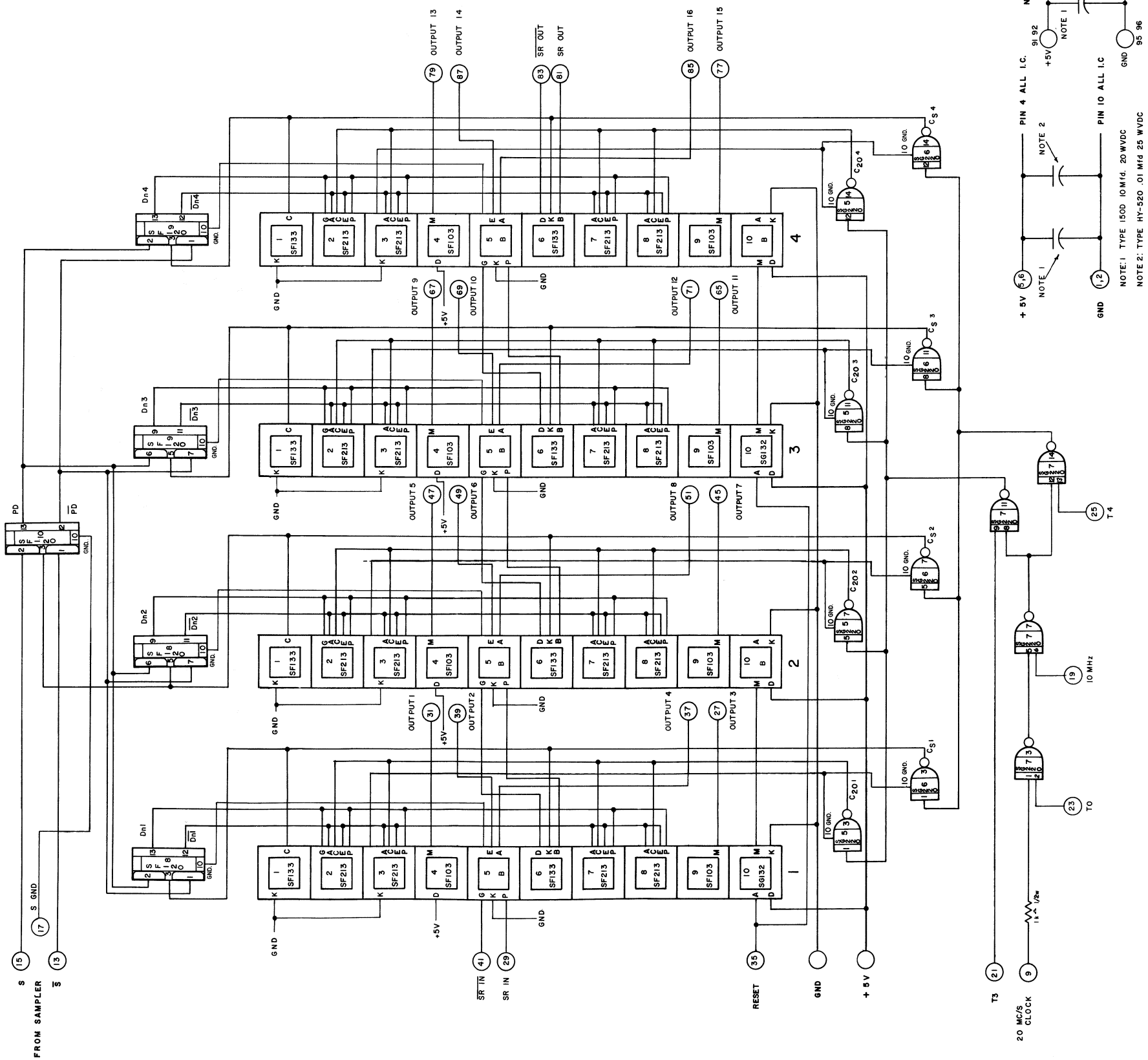


Figure 10

ELCO OMNI-COMB UNIT  
TOP VIEW



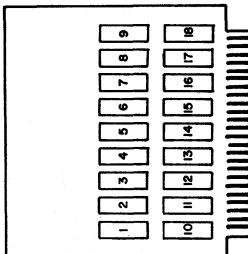
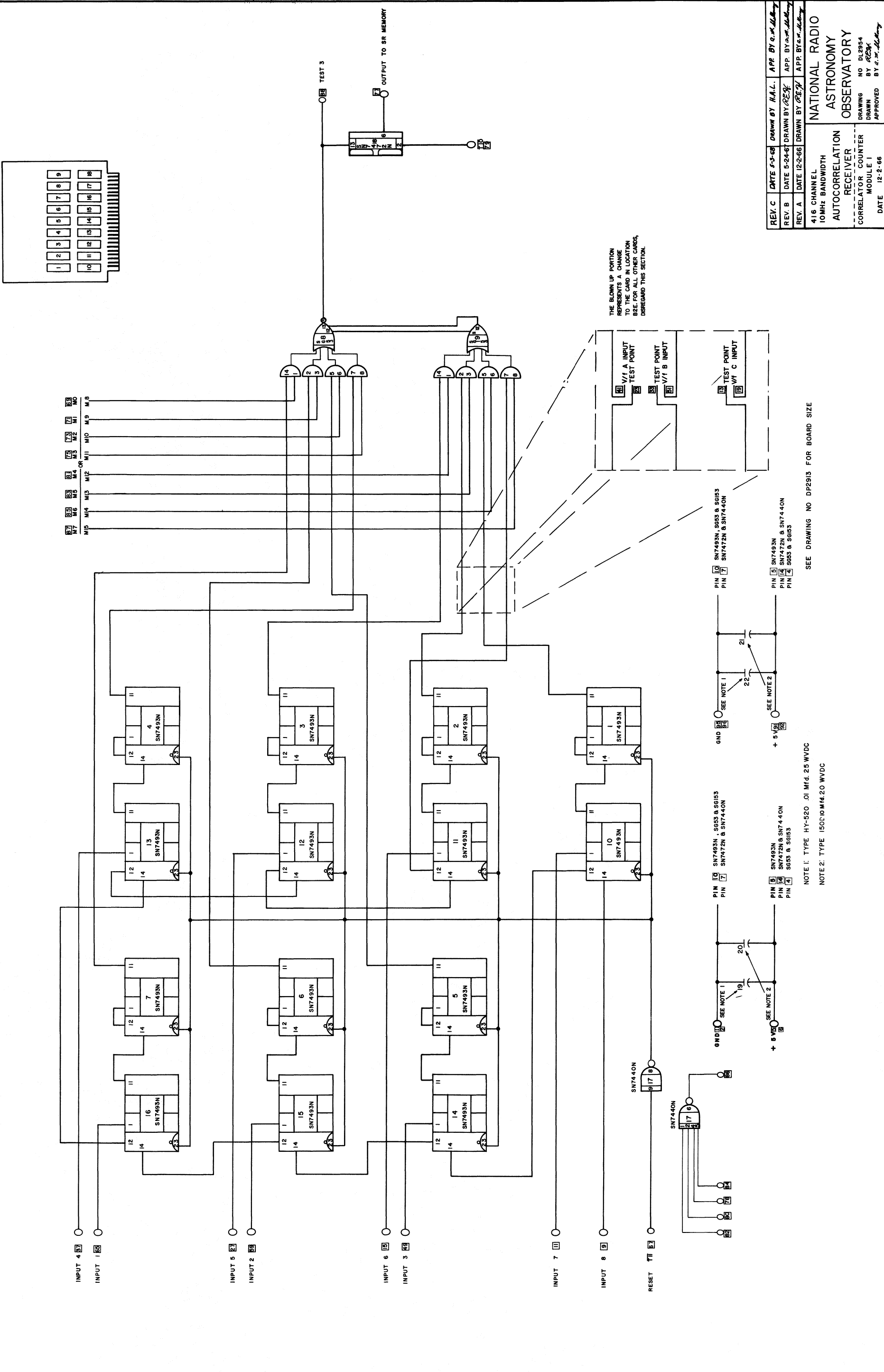
NOTE: DIMENSIONS IN INCHES REFERENCED TO SURFACE A  
TOLERANCE = .005, SOLDER PINS = .020 SQUARE



NOTE: SEE DRAWING NO DP2913 FOR BOARD SIZE  
NOTE 1: TYPE HY-520 .01 Mfd 25 WVDC  
NOTE 2: TYPE HY-520 .01 Mfd 25 WVDC

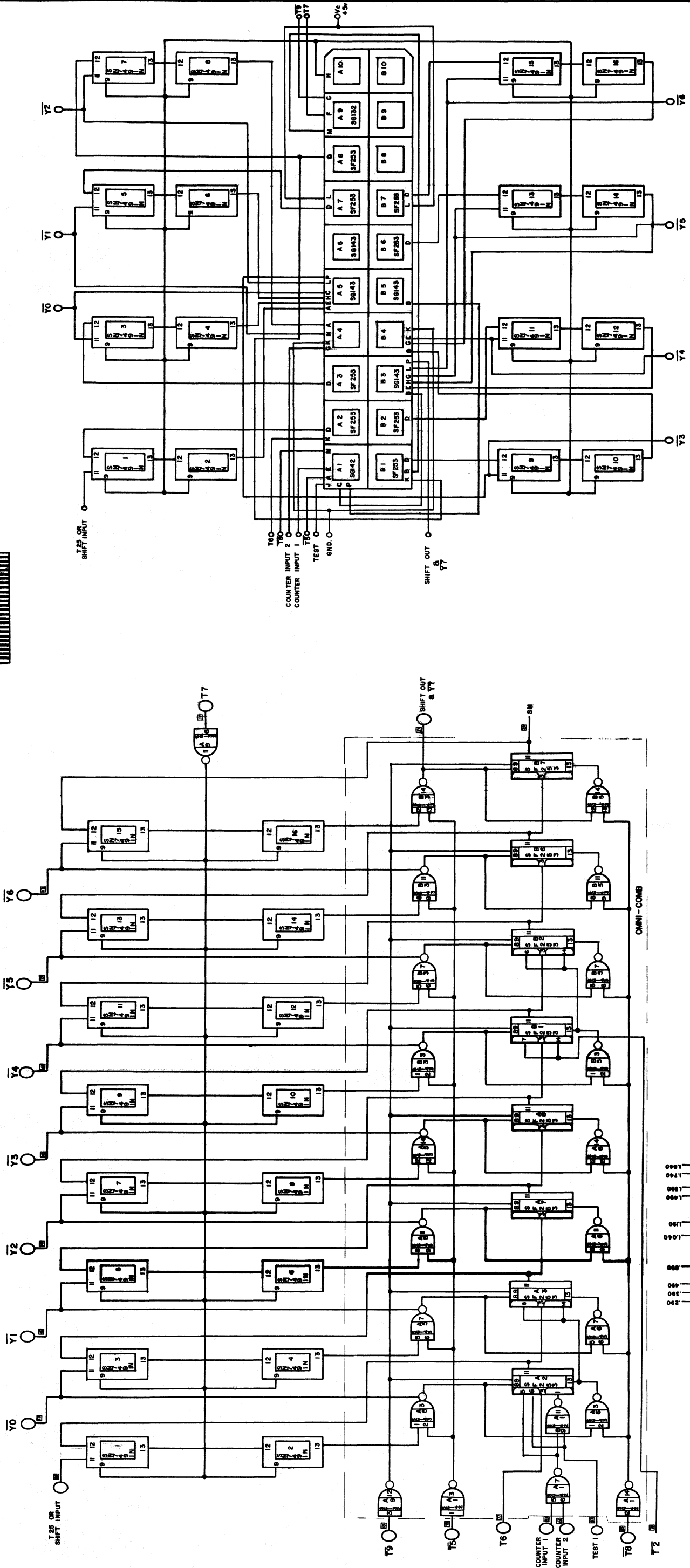
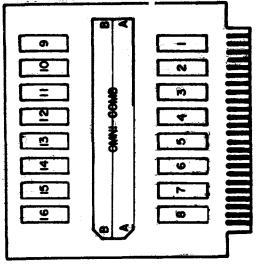
REV B	DATE 5-31-67	DRAWN BY HBY	APP BY E.M. Kelly
REV A	DATE 1-10-67	DRAWN BY HBY	APP BY E.M. Kelly
416 CHANNEL 10 MHZ BANDWIDTH AUTOCORRELATION RECEIVER CORRELATOR			
DATE 12-14-66			
NATIONAL RADIO ASTRONOMY OBSERVATORY			
DRAWING NO DP2913 DRAWN BY HBY APPROVED BY E.M. Kelly			

Figure 11

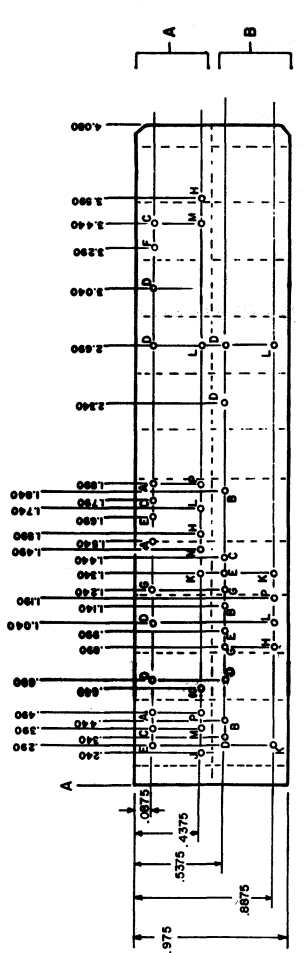
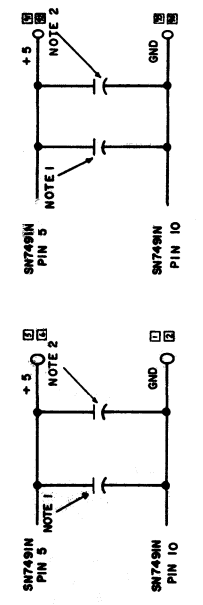


REV. C	DATE 5-5-66	DRAWN BY H.A.L.	APP. BY e.m. Hally
REV. B	DATE 5-24-66	DRAWN BY G.E.K.	APP. BY e.m. Hally
REV. A	DATE 12-2-66	DRAWN BY G.E.K.	APP. BY e.m. Hally
NATIONAL RADIO ASTRONOMY OBSERVATORY AUTOCORRELATION RECEIVER CORRELATOR - COUNTER MODULE 1 DRAWING NO. DL2954 DRAWN BY G.E.K. APPROVED BY e.m. Hally DATE 12-2-66			

Figure 12



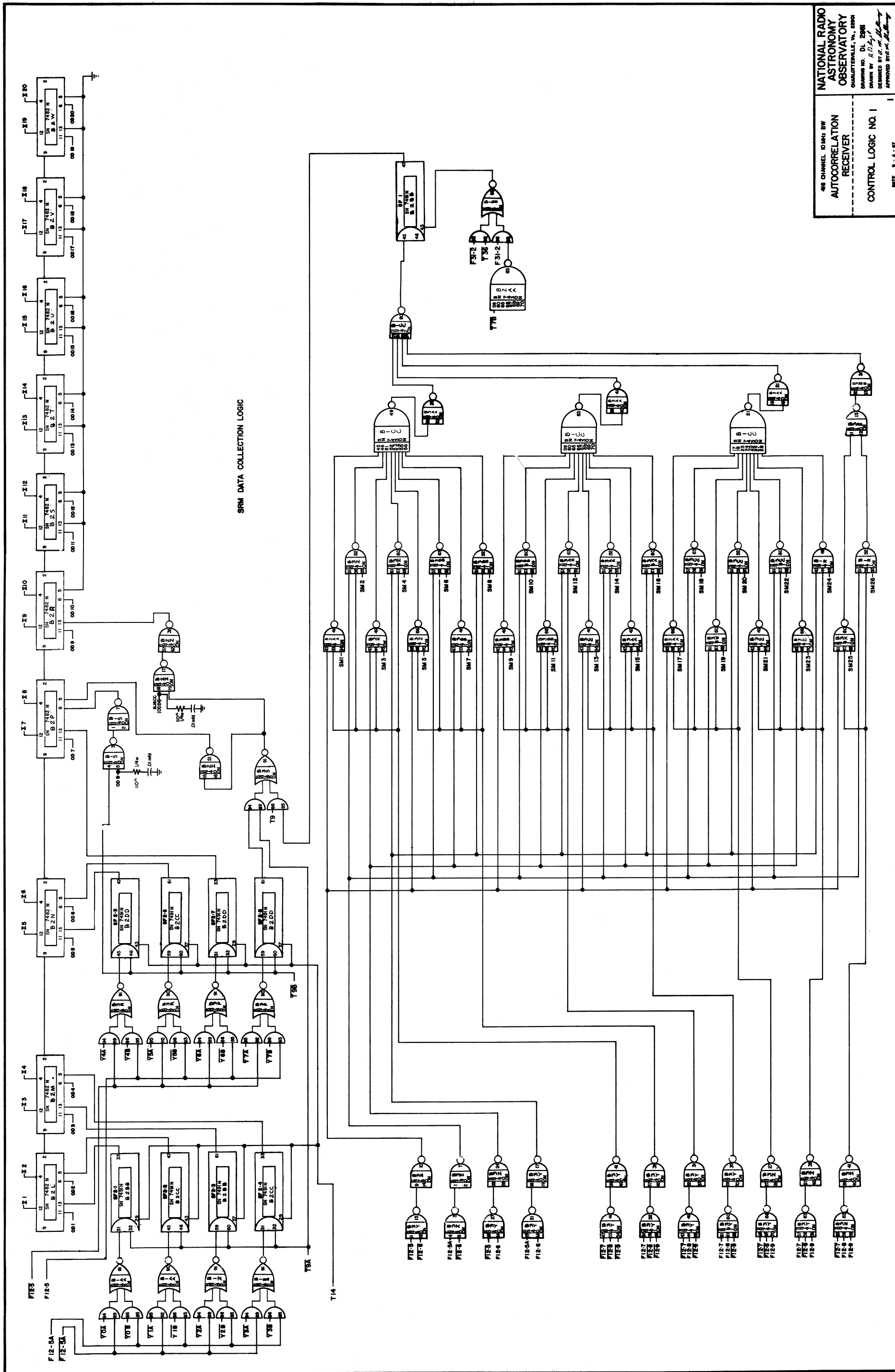
SEE DRAWING NO DP2583 FOR BOARD SIZE



NOTE: DIMENSIONS IN INCHES REFERENCED TO SURFACE A  
TOLERANCE = .005, SOLDER PINS = .020 SQUARE  
ELCO OMNI-COMB UNIT  
TOP VIEW

REV. A DATE 4-30-66 DRAWN BY *H. D. Light* APPROVED BY *E. M. Kelly*  
 NATIONAL RADIO ASTRONOMY OBSERVATORY  
 416 CHANNEL 10 MH BANDWIDTH AUTOCORRELATION RECEIVER  
 CORRELATOR MEMORY MODULE 1  
 DRAWING NO DL2582  
 DATE 11-14-66

Figure 13

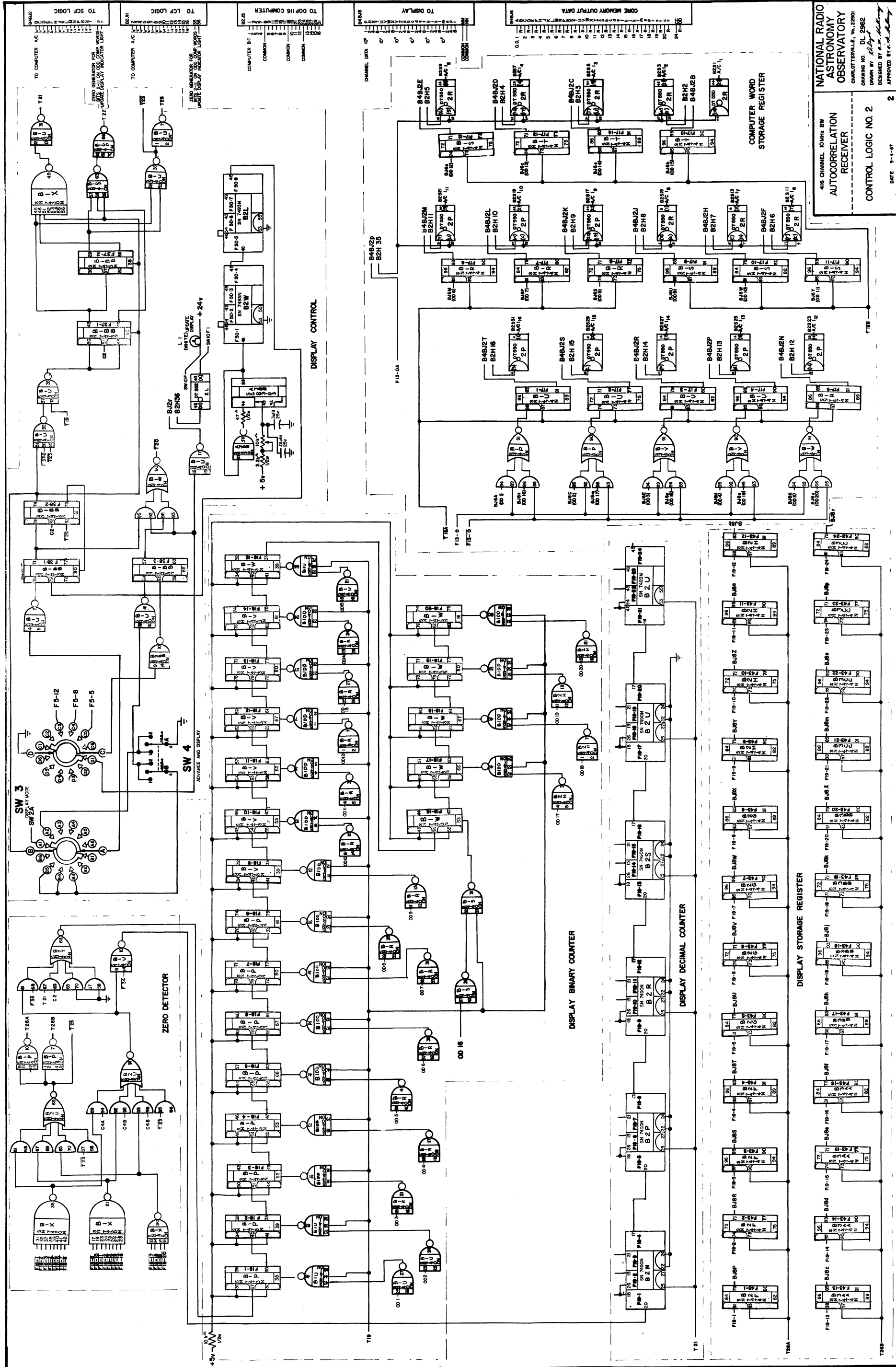


NATIONAL RADIO  
ASTRONOMY  
OBSERVATORY  
AUTOCORRELATION  
RECEIVER  
CONTROL LOGIC NO. 1

DRAWING NO. DI. 2361  
DESIGNED BY H.D. [signature]  
APPROVED BY G.M. [signature]

DATE 3-4-67

Figure 14

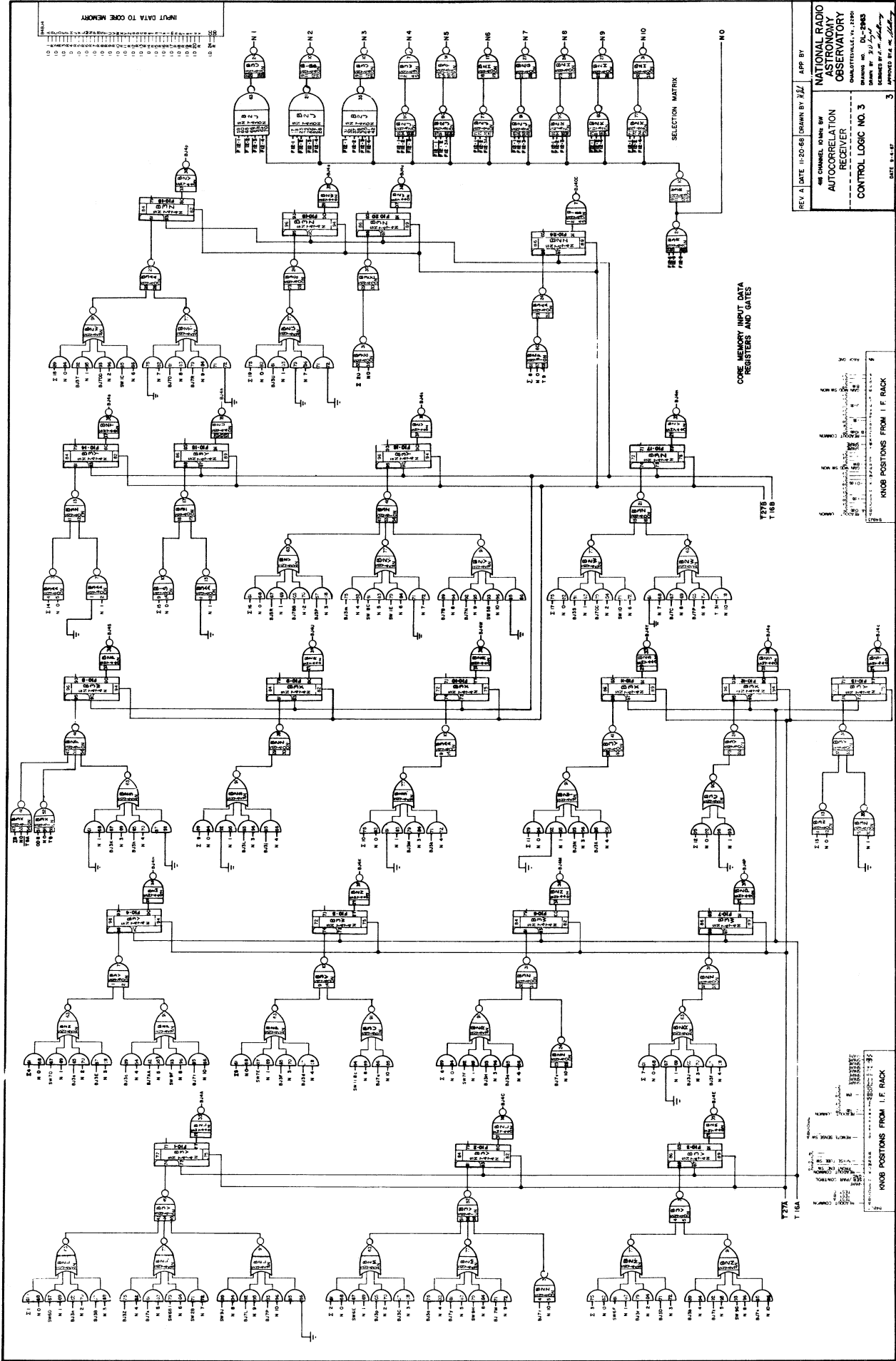


NATIONAL RADIO ASTRONOMY OBSERVATORY  
 CHARLOTTEVILLE, VA. 22901  
 DRAWING NO. DL 2562  
 DESIGNED BY *[Signature]*  
 APPROVED BY *[Signature]*

416 CHANNEL 10MHz BW  
 AUTOCORRELATION RECEIVER  
 CONTROL LOGIC NO. 2

DATE 9-1-67

Figure 15



INPUT DATA TO CORE MEMORY

REV. A DATE 11-20-66 DRAWN BY JLL APP BY  
 NATIONAL RADIO ASTRONOMY OBSERVATORY  
 AUTOCORRELATION RECEIVER  
 CONTROL LOGIC NO. 3  
 DATE 8-4-67

CORE MEMORY INPUT DATA REGISTERS AND GATES

KNOB POSITIONS FROM I.F. RACK

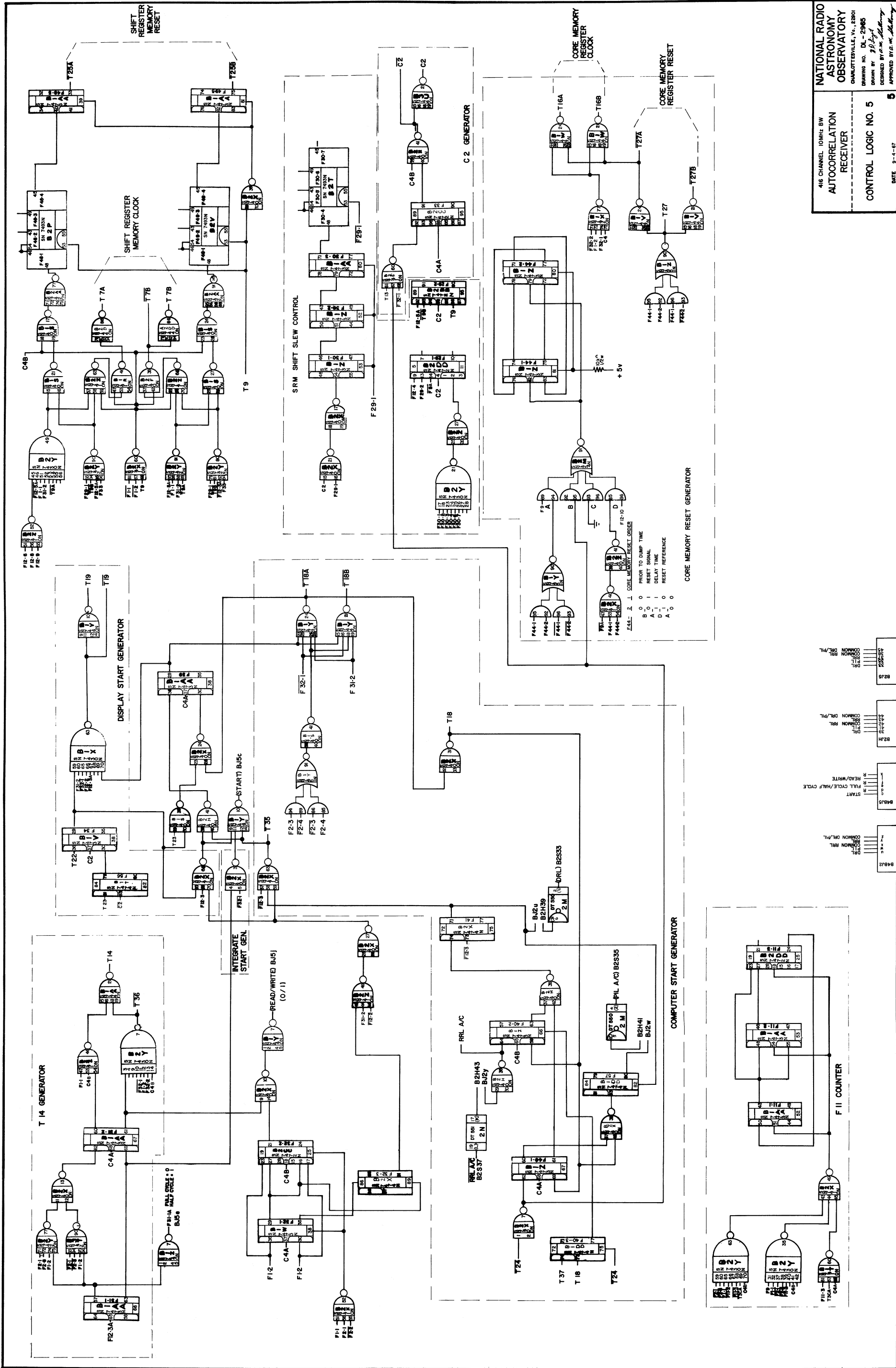
KNOB POSITIONS FROM I.F. RACK

FIG. 16









NATIONAL RADIO ASTRONOMY OBSERVATORY  
 CHARLOTTEVILLE, Va., 22801  
 DRAWING NO. DL-2965  
 DESIGNED BY *[Signature]*  
 APPROVED BY *[Signature]*

416 CHANNEL 10MHz BW  
 AUTOCORRELATION RECEIVER  
 CONTROL LOGIC NO. 5  
 DATE 9-4-67

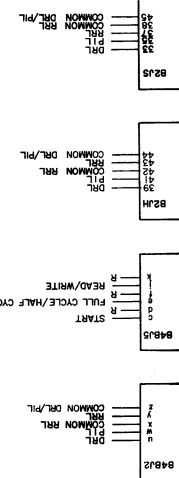
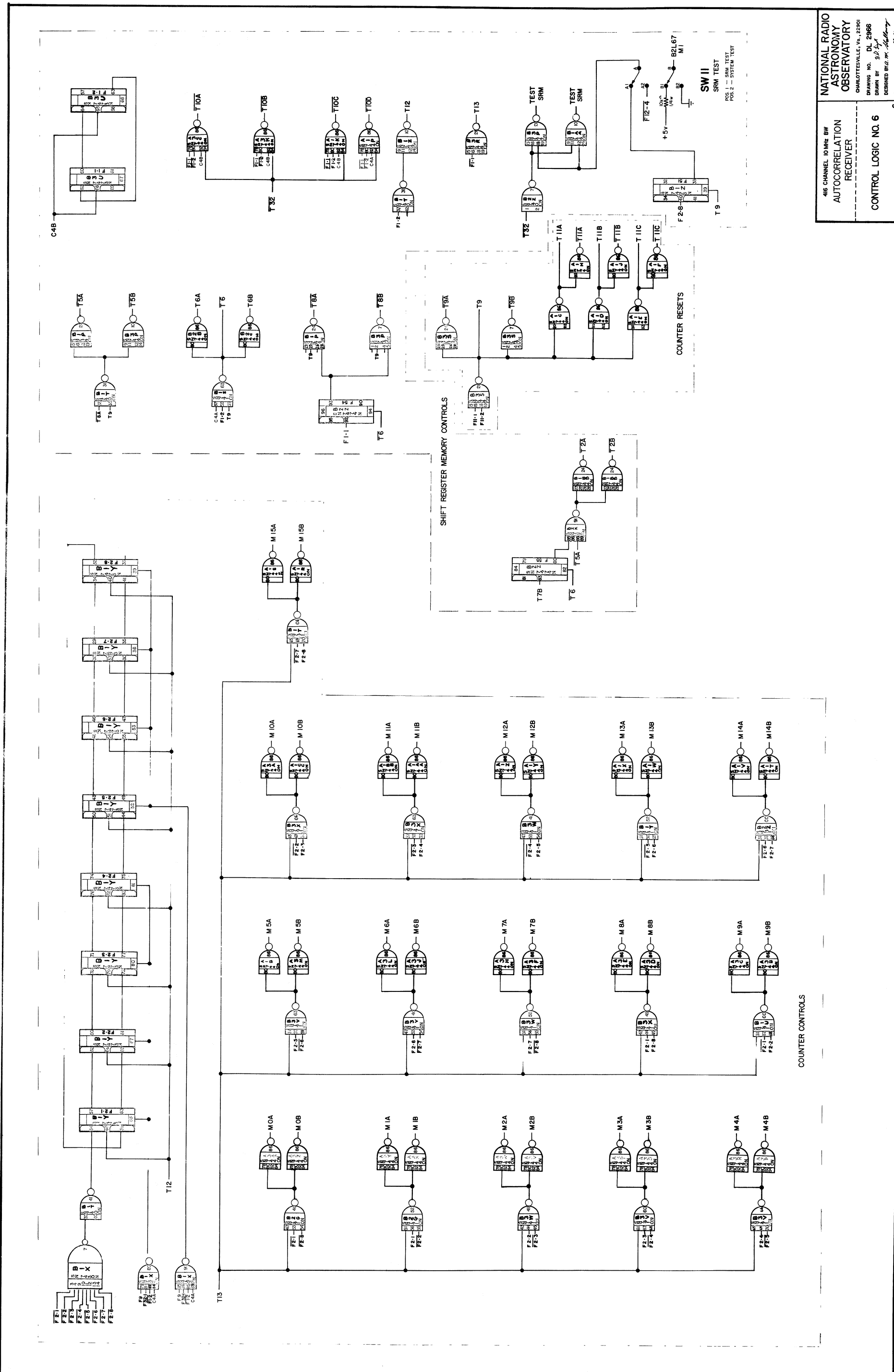


Figure 18



416 CHANNEL 10 MHz BW  
AUTOCORRELATION  
RECEIVER

NATIONAL RADIO  
ASTRONOMY  
OBSERVATORY

CONTROL LOGIC NO. 6

DATE 9-4-67

6

APPROVED BY *G. M. ...*

DESIGNED BY *G. M. ...*

DRAWN BY *J. P. ...*

DL 2966

CHARLOTTEVILLE, VA., 22901

Figure 19

NATIONAL RADIO ASTRONOMY OBSERVATORY  
 CHARLOTTEVILLE, VA, 22004  
 DRAWING NO. DL 2367  
 DESIGNED BY H.D. Taylor  
 APPROVED BY G.W. Stokely

416 CHANNEL 10MHz BW  
 AUTOCORRELATION  
 RECEIVER

CONTROL LOGIC NO. 7

DATE 9-4-67

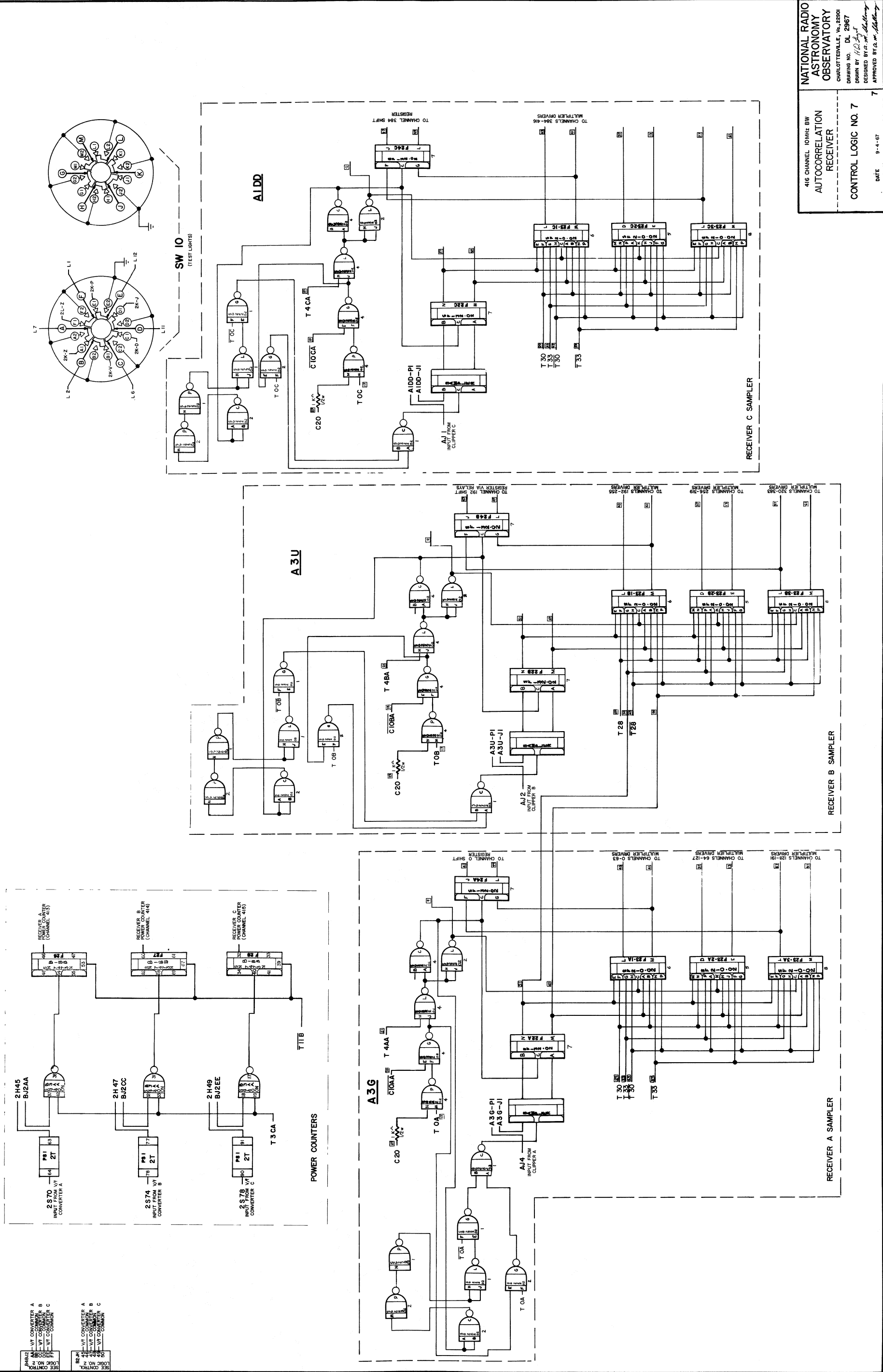


Figure 20







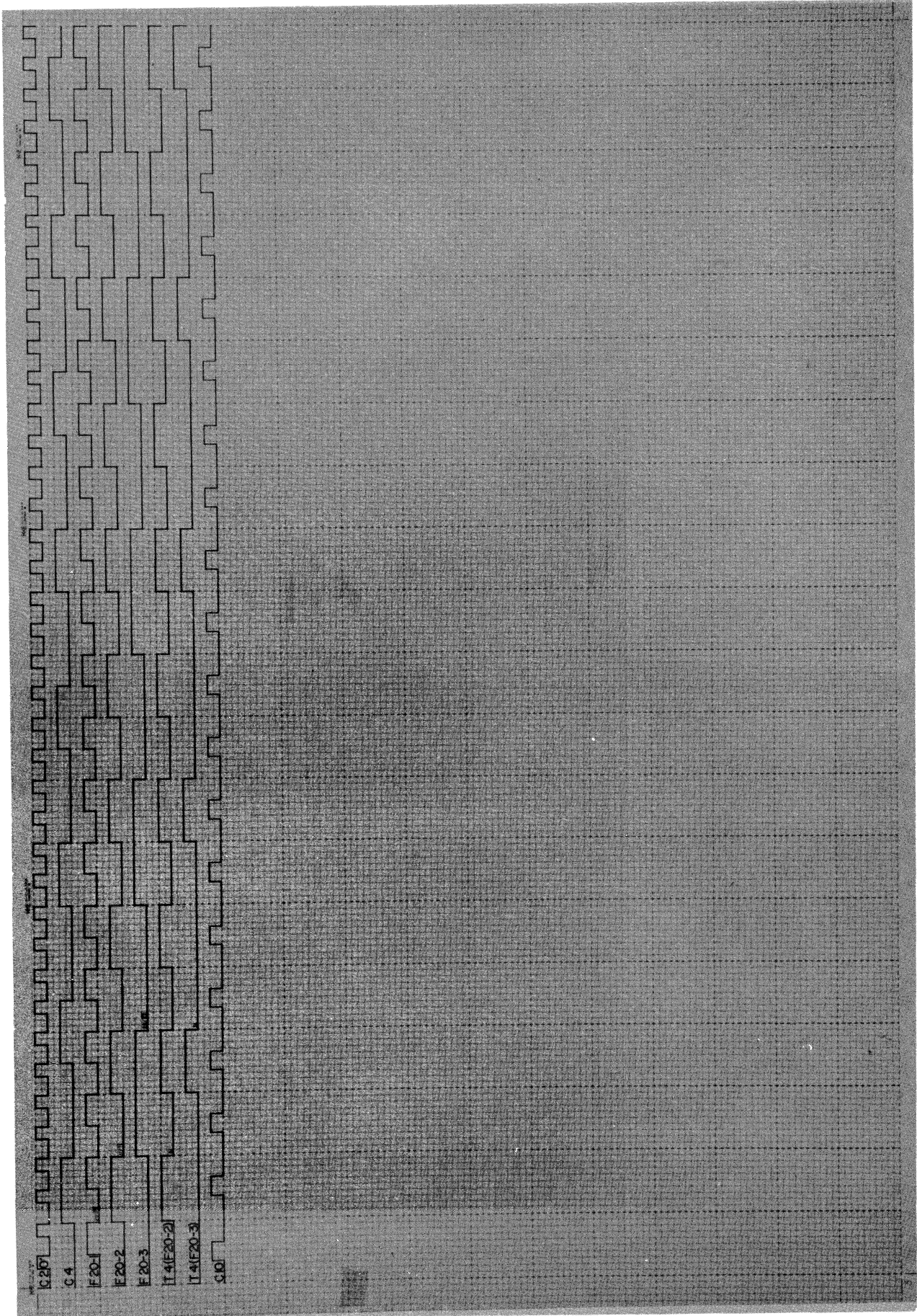


Figure 23. Timing Diagram No. 1 - Sample Rate Generator



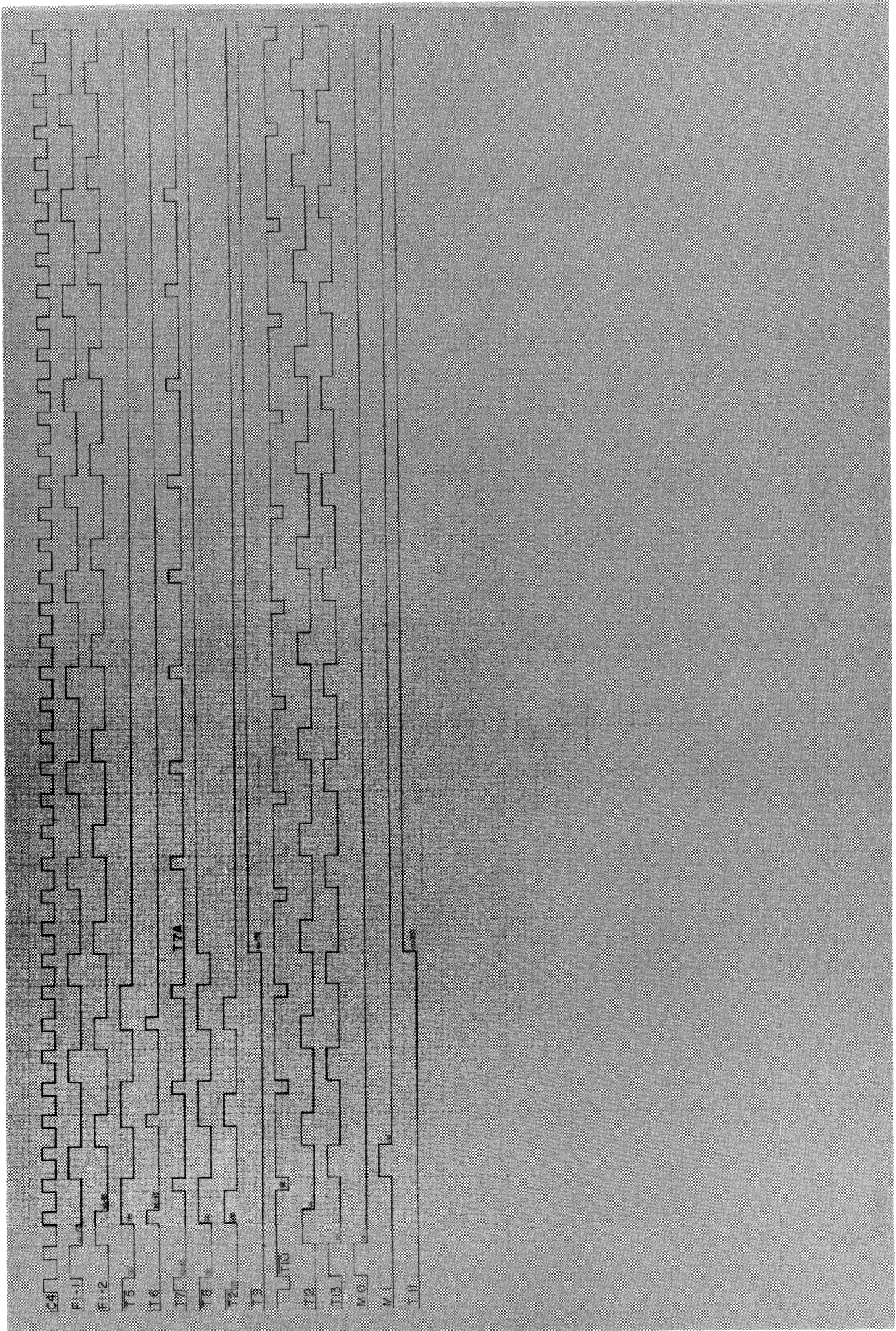


Figure 24. Timing Diagram No. 2 - Shift Register Memory

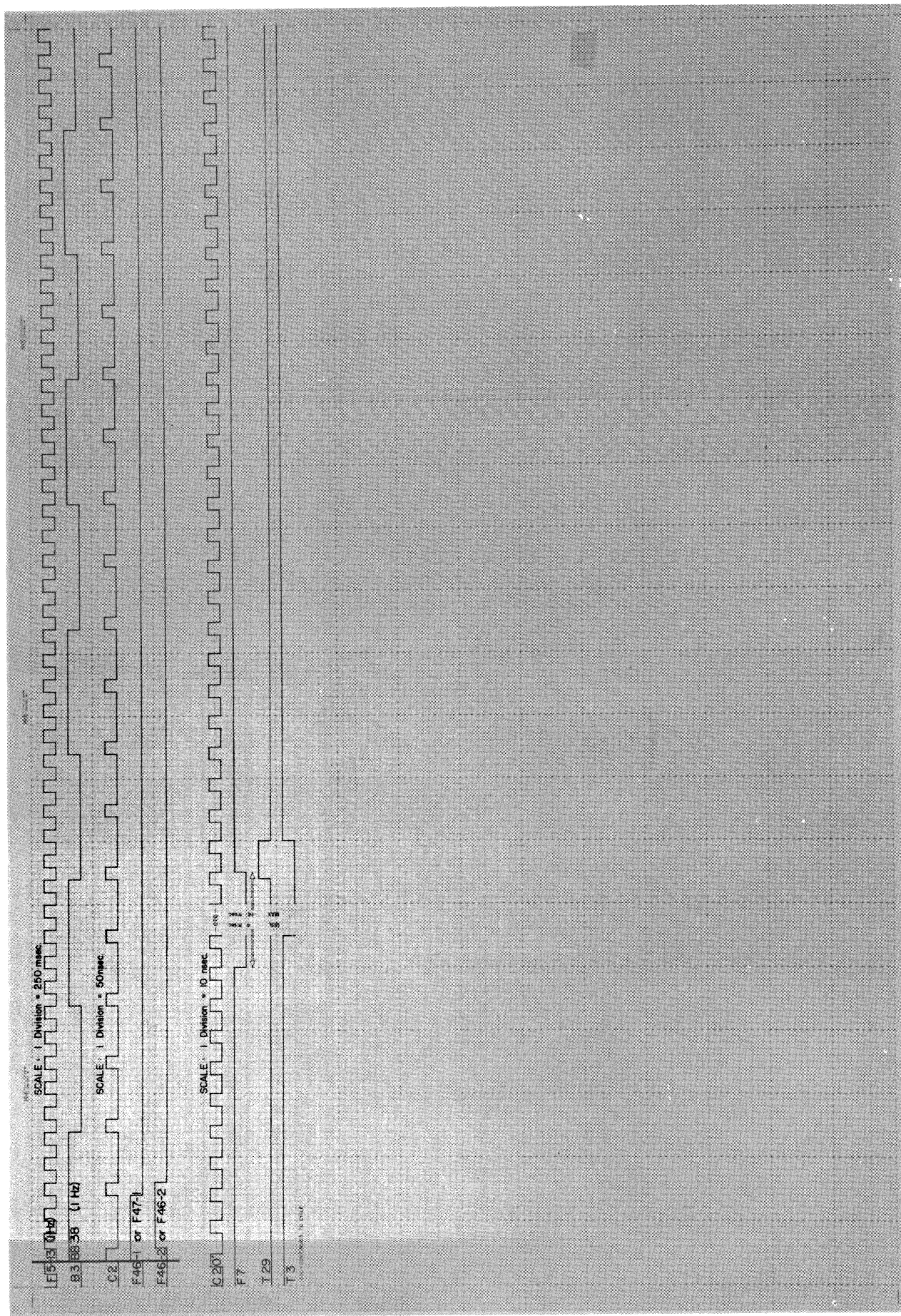


Figure 25. Timing Diagram No. 3 - Switching Signal & Blanking Time Generators

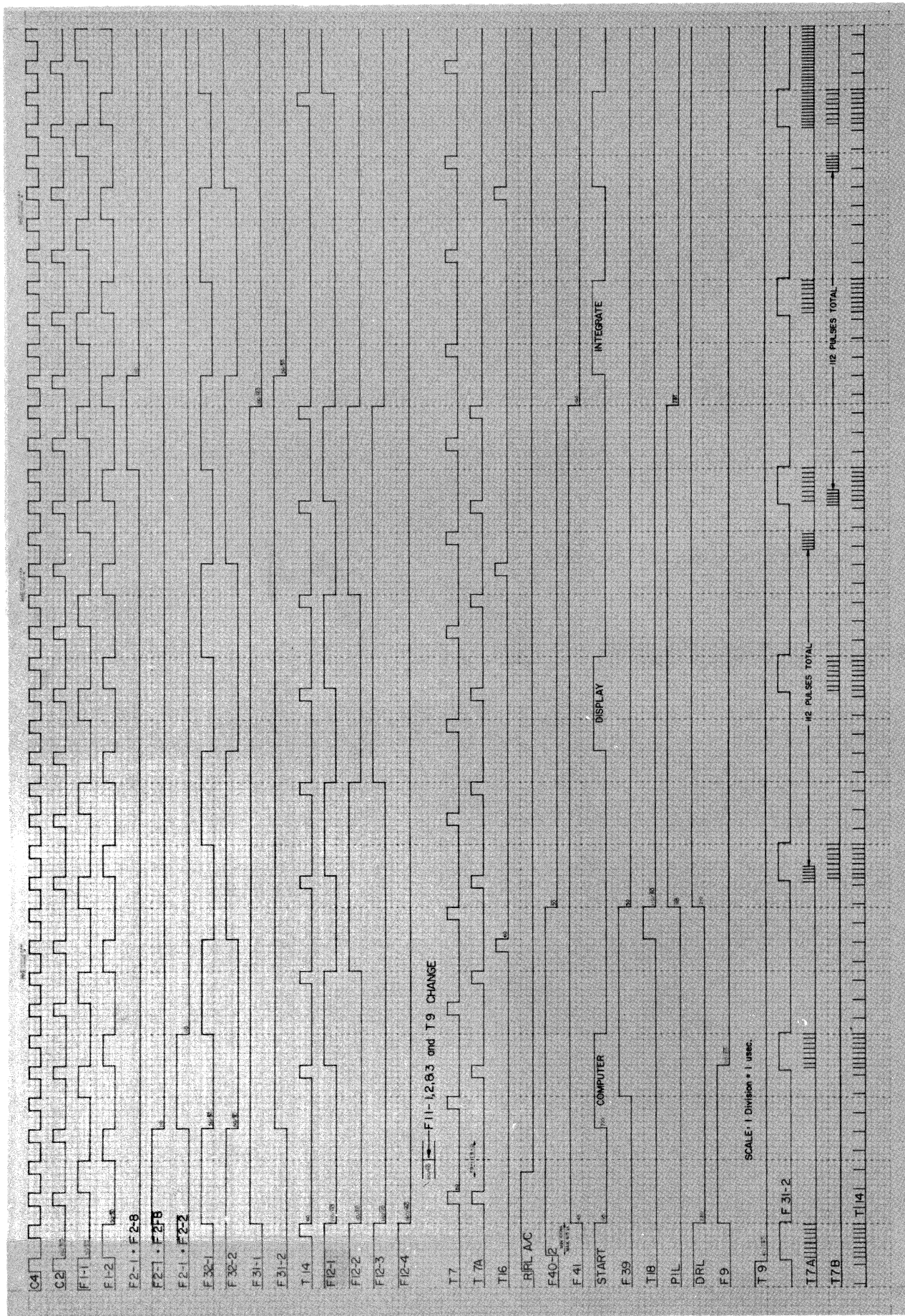


Figure 26. Timing Diagram No. 4 - Miscellaneous

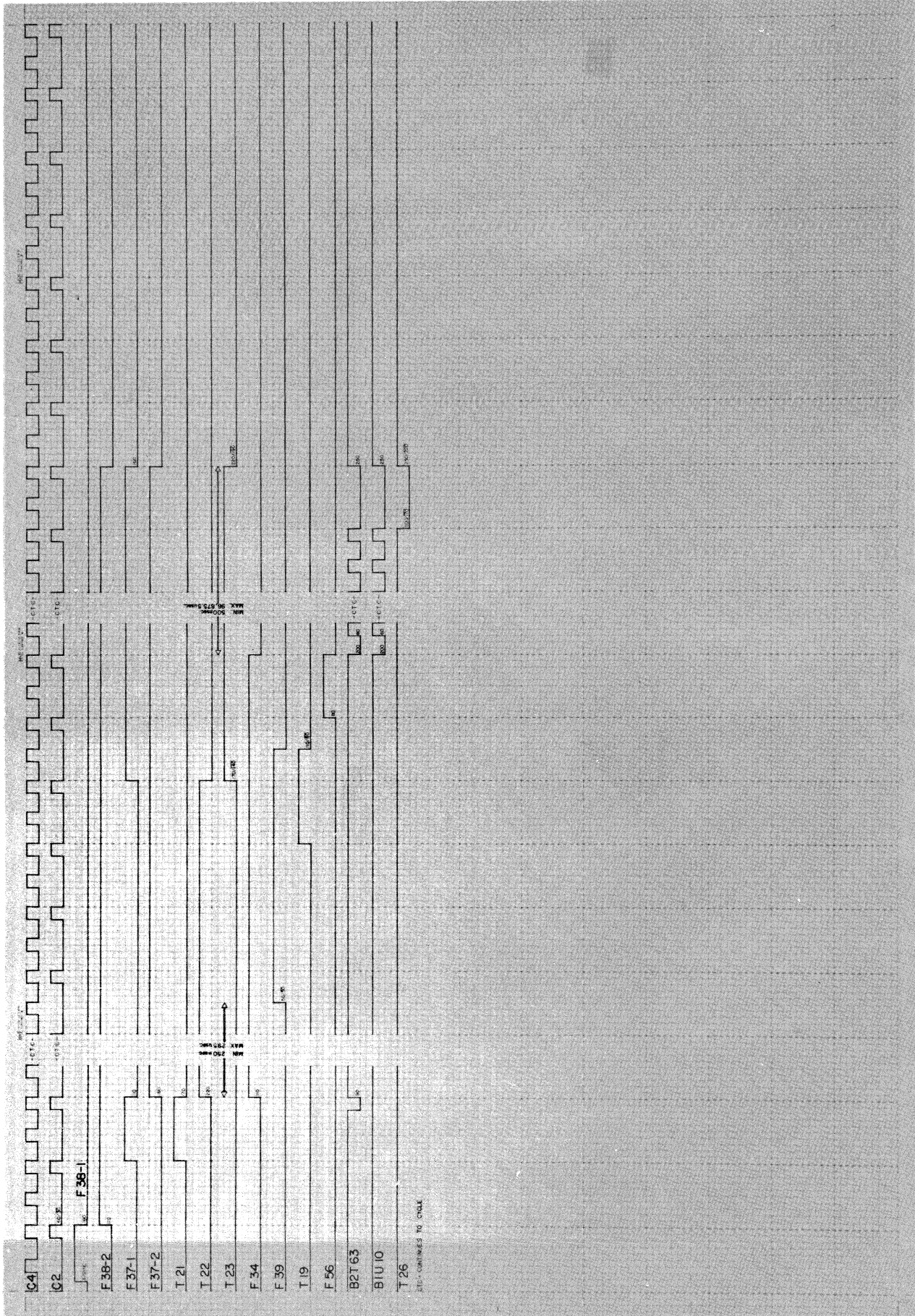
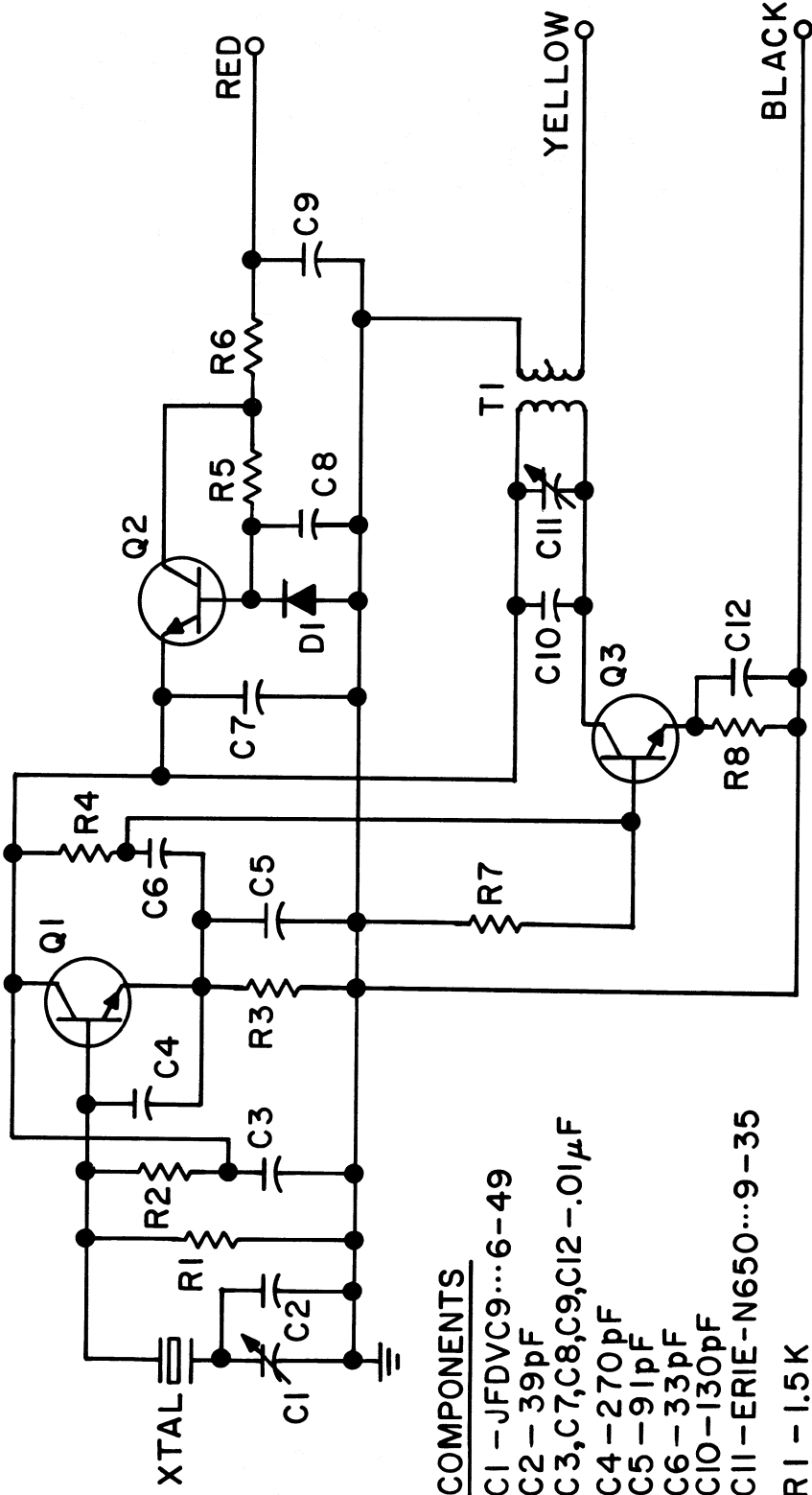


Figure 27. Timing Diagram No. 5 - Display



**COMPONENTS**

- C1 - JFDVC9...6-49
- C2 - 39pF
- C3, C7, C8, C9, C12 - 0.01μF
- C4 - 270pF
- C5 - 91pF
- C6 - 33pF
- C10 - 130pF
- C11 - ERIE-N650...9-35
- R1 - 1.5K
- R2 - 5.6K
- R3 - 2.2K
- R4 - 47K
- R5 - 680Ω
- R6 - 25Ω - 1/4 W
- R7 - 12K
- R8 - 390Ω

Δ All Resistors 1/10 W, Or As Noted.

- Q1, Q3, - 2N3564
- Q2 - 2N697
- T1 - -----
- XTAL - 20 MHz
- D1 - IN721

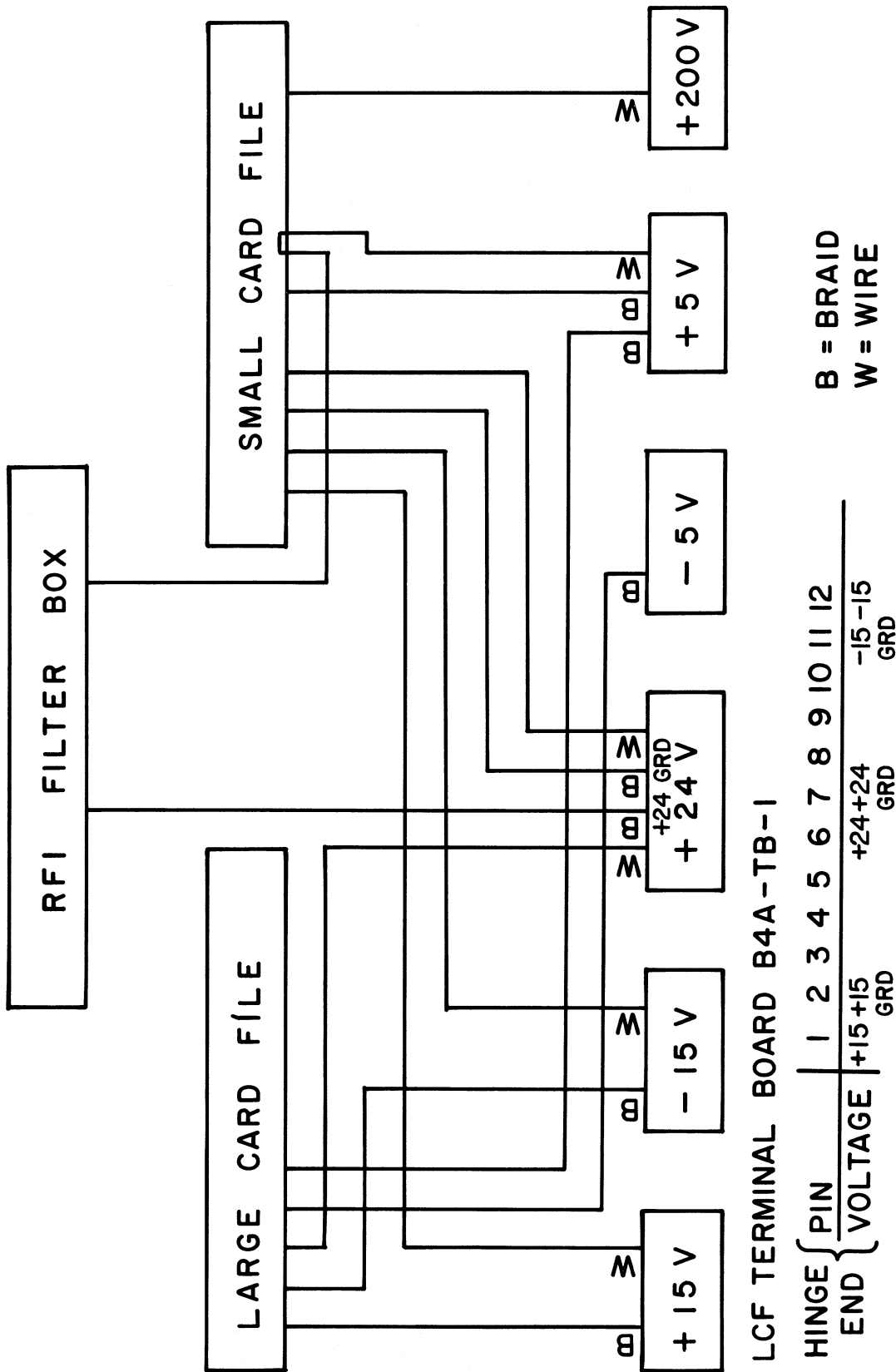
**TERMINAL CONNECTIONS**

- Black 1 - Common
- Yellow 2 - Output > 4 vrms  
Into 5KΩ Load
- 3 - N.C.
- Red 4 - Supply +24 VDC

DWG. # DS2976  
Schematic Diagram  
Crystal Oscillator  
Model DFO-18  
McCoy Electronics Co.  
Freq. 20MHz  
Tol. ± .002 %

20MHZ CLOCK CRYSTAL OSCILLATOR

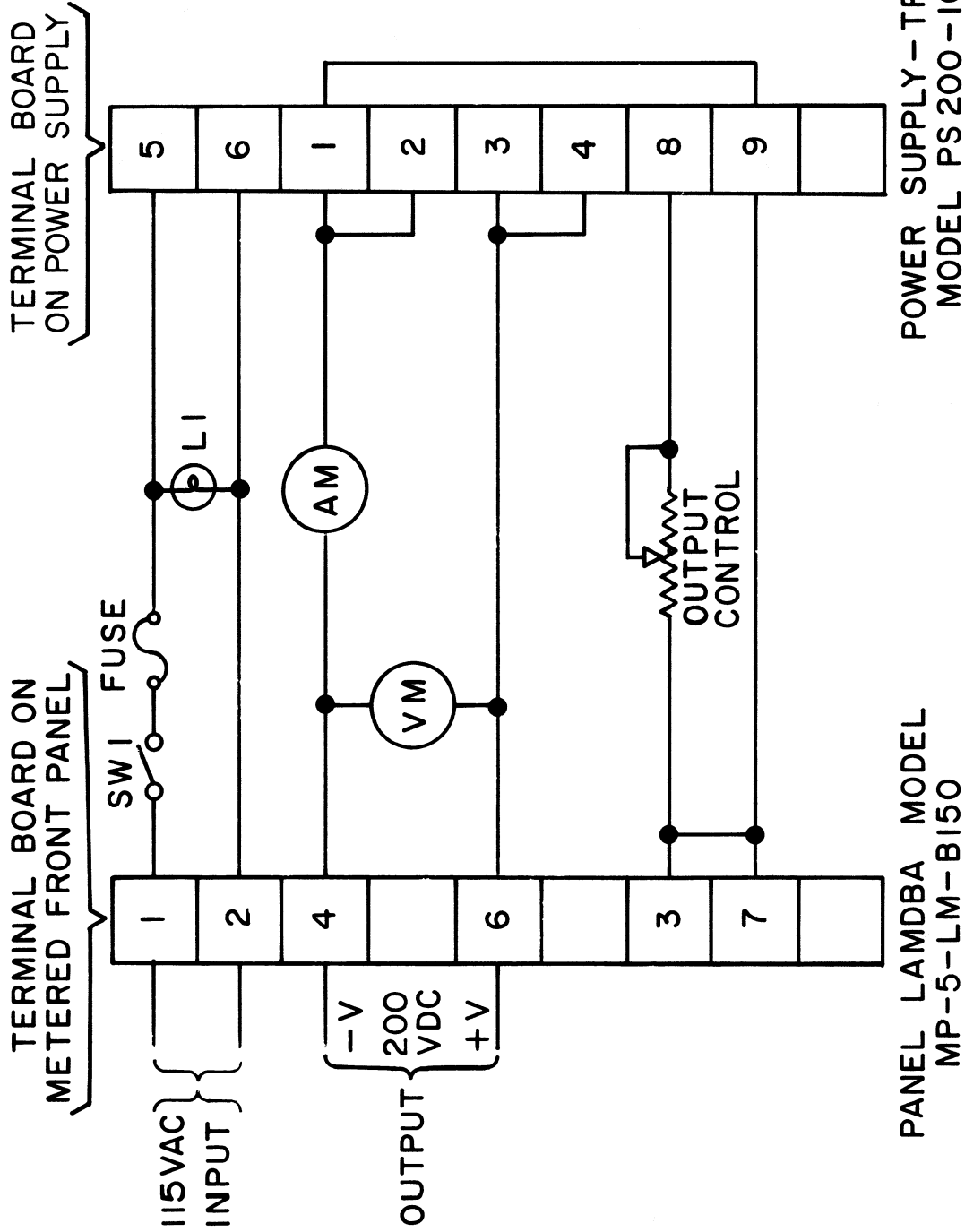
Figure 28



NOTE: ALL LINES REPRESENT THE VOLTAGE AND ITS ASSOCIATED GROUND EXCEPT AS NOTED ON THE +24V SUPPLY.

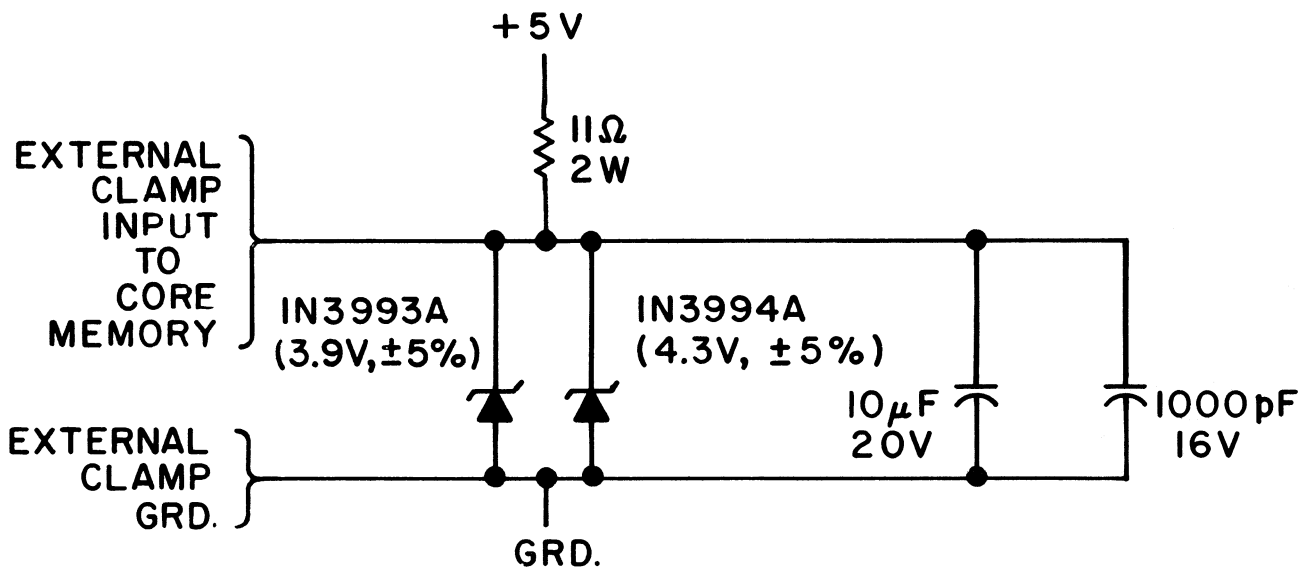
POWER SUPPLY CABLING DIAGRAM

Figure 29



+ 200V NIXIE SUPPLY - EXTERNAL WIRING

Figure 30

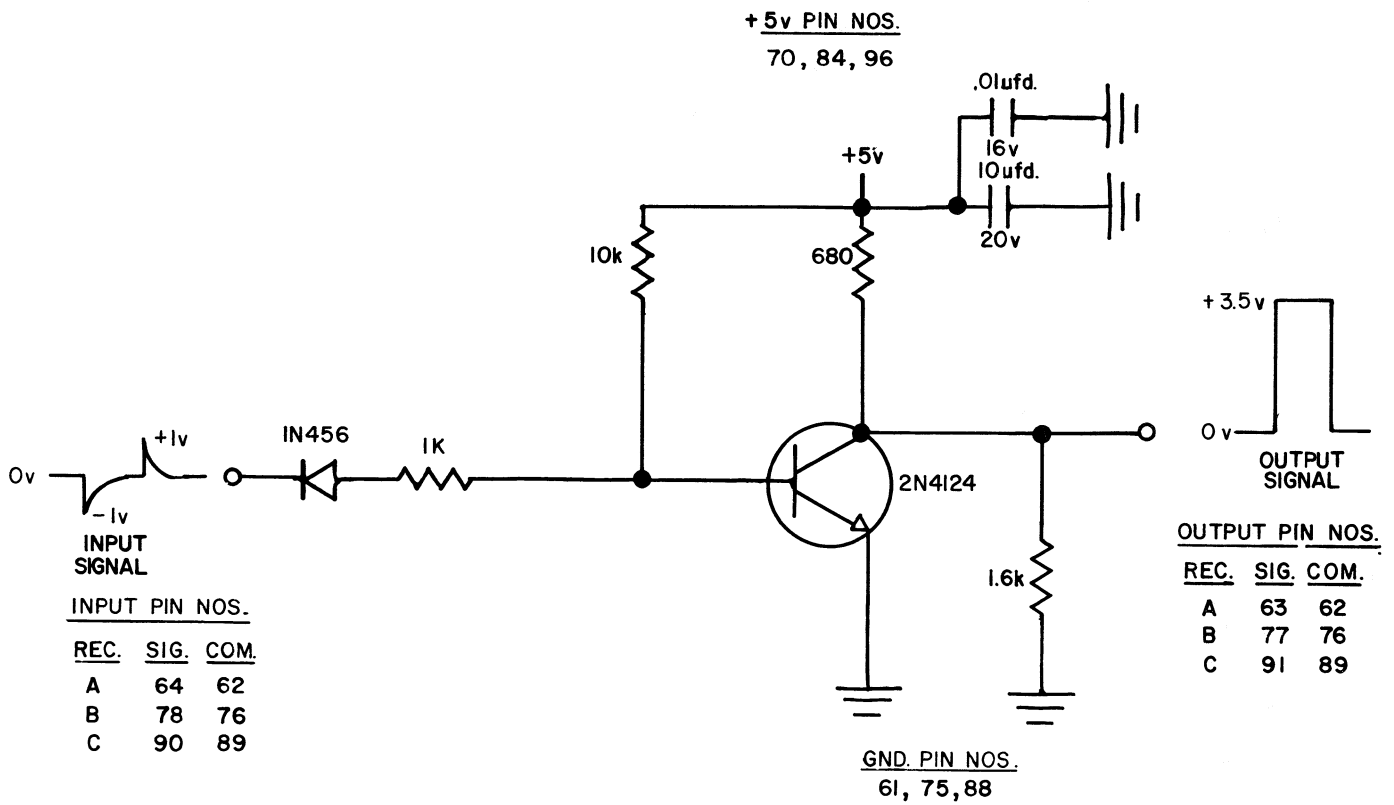


NOTE: THIS CIRCUIT IS LOCATED IN REAR OF B4B CHASIS

### EXTERNAL VOLTAGE CLAMP FOR CORE MEMORY

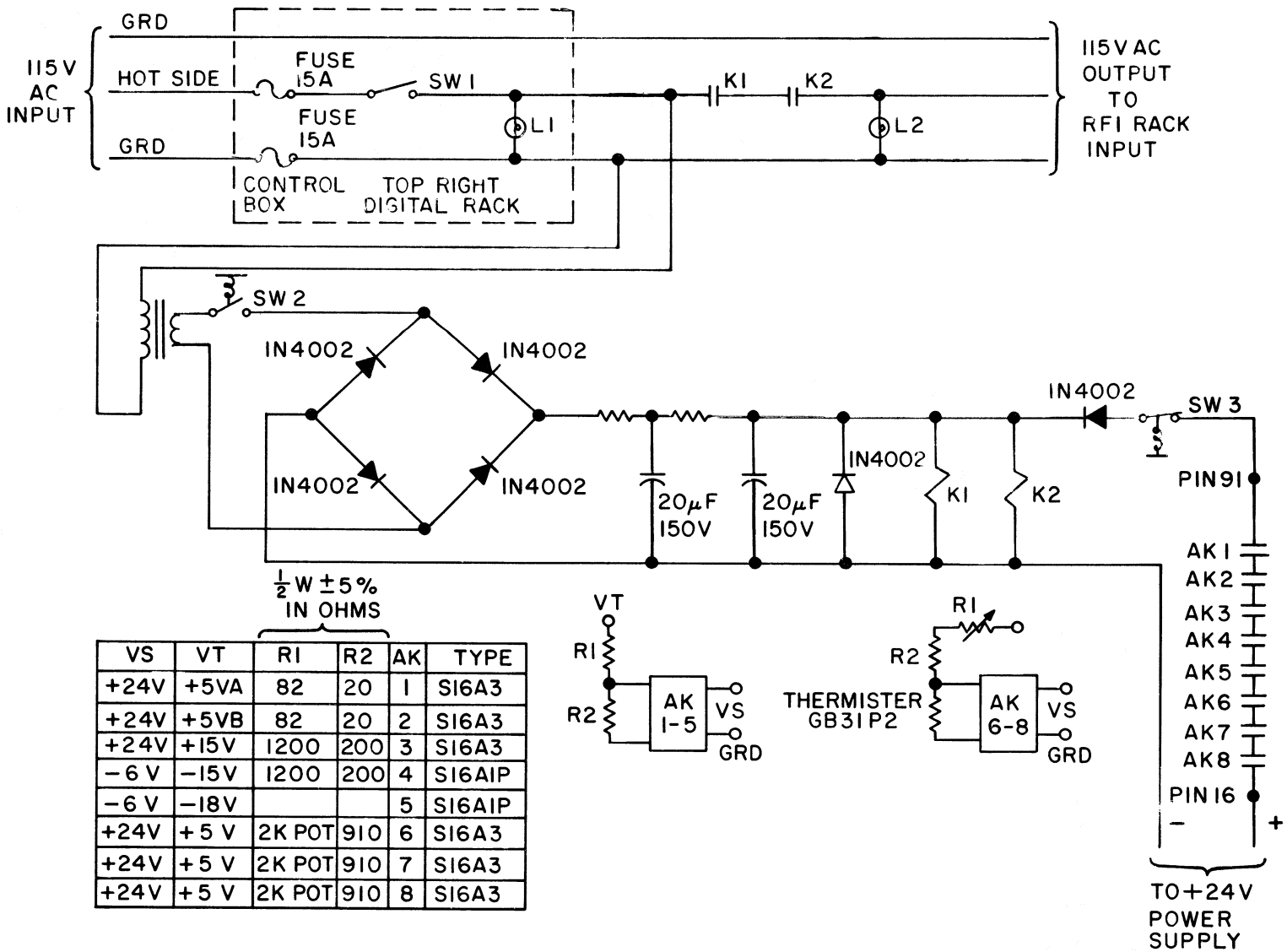
Figure 31





### V/F CONVERTER INTERFACE CIRCUIT

Figure 32



INPUT- OUTPUT	VS GRD	+24V	+5V	+5VA	+5VB	+15V	+VT GRD	-VT GRD	-15V	-18V	-6V	THERMISTERS INPUT		
												A	B	C
PIN NO.	62	77	76	20	34	48	42	8	7	2	21	66	80	90
												65	79	93

NOTE: THERMISTERS LOCATIONS: A(AK6) ON B4A2P; B(AK7) ON B4B2E; C(AK8) ON B2N

POWER CONTROL SCHEMATIC

Figure 33