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SYNCHRONOUS DETECTOR AND READOUT SYSTEM FOR A 50-CHANNEL RECEIVER

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1. General Description

The multichannel detector is used in conjunction with the multichannel filter unit as a line receiver in the absence of a computer. The unit can accommodate up to 52 channels. Each channel has its own synchronous detector and integrator. The control unit determines the modes of operation and selects the output device(s). Figure 1 shows the block diagram of the system when used in conjunction with a Standard Receiver. When in the automatic mode, the unit will integrate for a predetermined period, hold, and provides output of the various channels to a printer and/or paper tape punch. For an input of 20 mV/°K, the output is 1 V/°K or 0.1 V/°K, depending on the gain used.

2. Operation

Two modes of operation are available.

(2.1) Automatic Mode. In this mode, the unit will integrate the incoming signal for a preset duration, at the same time showing the outputs of the different channels on the oscilloscope. After the preset time, the integration is stopped and the output of each channel is held constant. The outputs are then gated to the "printer output" socket one after another; at the same time a contact closure is made to activate the printer/punch. This goes on at the slow sweep rate until all the wanted channels have been gated. The scan rate is then automatically switched to the fast rate for display of the final output voltages on the oscilloscope. The output of the different channels are held constant until the next integration period is required. This cycle is repeated each time the "AUTO-START" button is pushed.

(2.2) Manual Mode. In this mode, the user selects the manner of operation himself. The "Integration Mode" switch controls the integrator, enabling it to integrate, hold, or reset. When on "integrate" the unit will continue to integrate until the "Integration Mode" switch is returned to "Hold" or "Reset". Printout of the channels could be initiated by switching on the "Manual Print" switch.

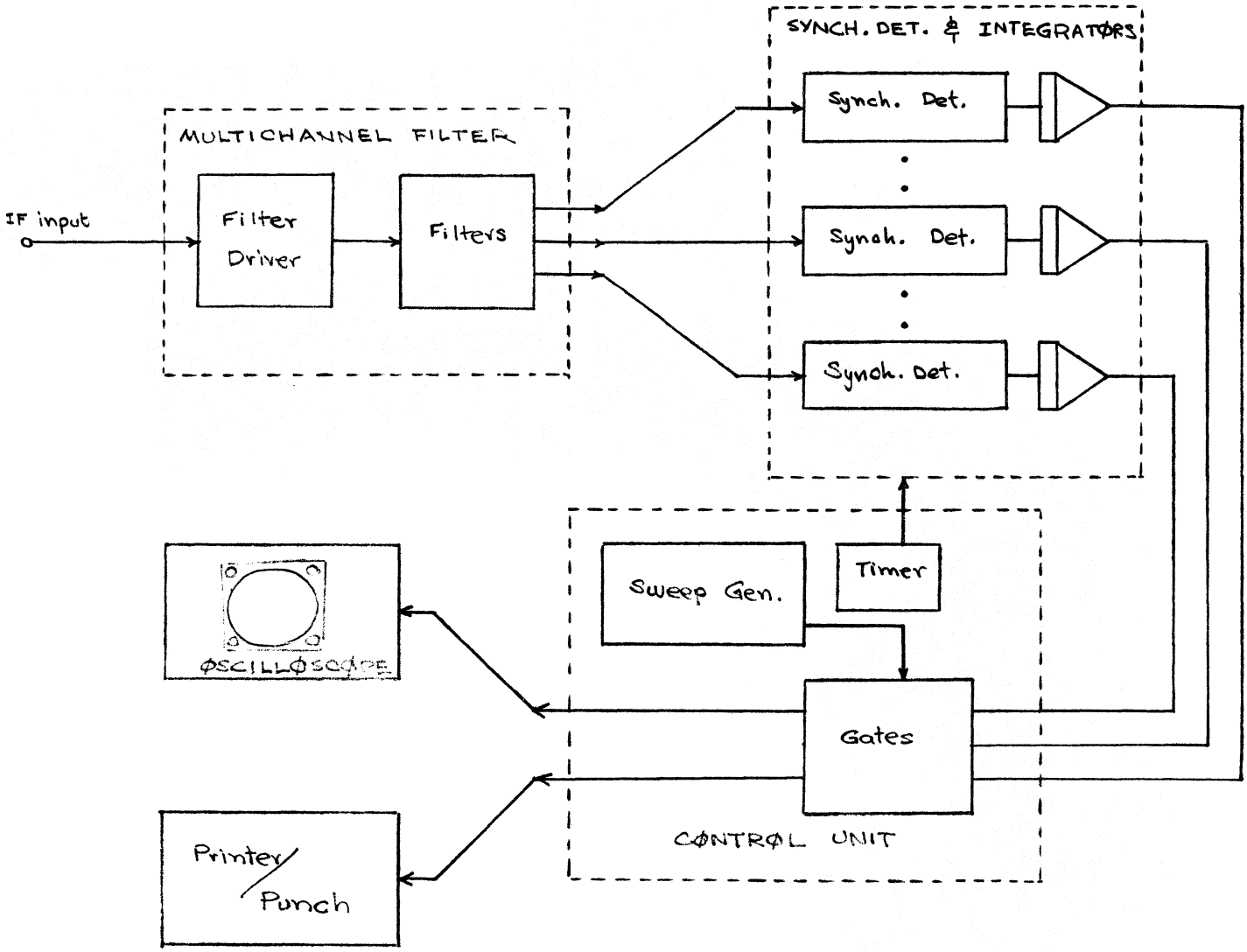


Fig. 1. Multichannel Detector Block Diagram.

(2.3) Switch Positions

(2.3.1) Automatic Mode. For the automatic mode, the following switch settings should be used:

Switch	Set at
Sweep Rate	SCOPE
Manual Print	OFF
Integration Time	Set on duration required (e.g., 5 min).
Integration Mode	AUTO
Integration Rate	AUTO
Scale	10 °K or 100 °K

Push momentarily the "AUTOSTART" button to initiate cycle.

The "SCALE" switch controls the gain of the synchronous detectors. At the 100 °K switch position, the output from the integrator is approximately 1. V/°K. At the 10 °K switch position, the output is approximately 1 V/°K. Additional gain could be realized by setting the "Integration Rate" switch on a different time from the "Integration Time" switch. For example, with the "Integration Time" switch set at 5 minutes (300 sec.) and the "Integration Rate" switch set at 10 sec., then the gain achieved would be,

$$G = \frac{300}{10} = 30$$

(2.3.2) Manual Printing. The different channels' outputs can be manually gated to the printer/punch by doing the following:

(i) Set "Sweep Rate" switch to "Off".

(ii) Push the "Sweep Reset" button momentarily so that all front panel lights go off.

(iii) Put "Manual Print" switch on "ON".

(iv) Set "Sweep Rate" switch to "Printer".

The front panel lights should now come on indicating the channel being gated to the printed. This should start at 1 and go on at the slow rate until the last channel's number. All the lights should go off momentarily after the last channel number, at which time the "Manual Print" switch should be turned "Off". Otherwise, the printing cycle repeats itself.

(2.3.3) Single Channel Readout. Readout of only a single channel can be done by:

(i) Set "Sweep Rate" at "OFF".

(ii) Momentarily push "Sweep Reset" button.

(iii) Pulse "Manual Advance" button enough times until the front panel lights indicate the correct channel number.

3. Detailed Description

The multichannel detector consists of 2 rack units:

(1) Control Unit

(2) Synchronous Detector and Integrator Unit.

(3.0) Control Unit (see Fig. 2). This unit consists of:

(1) An interval timer to set the duration of integration.

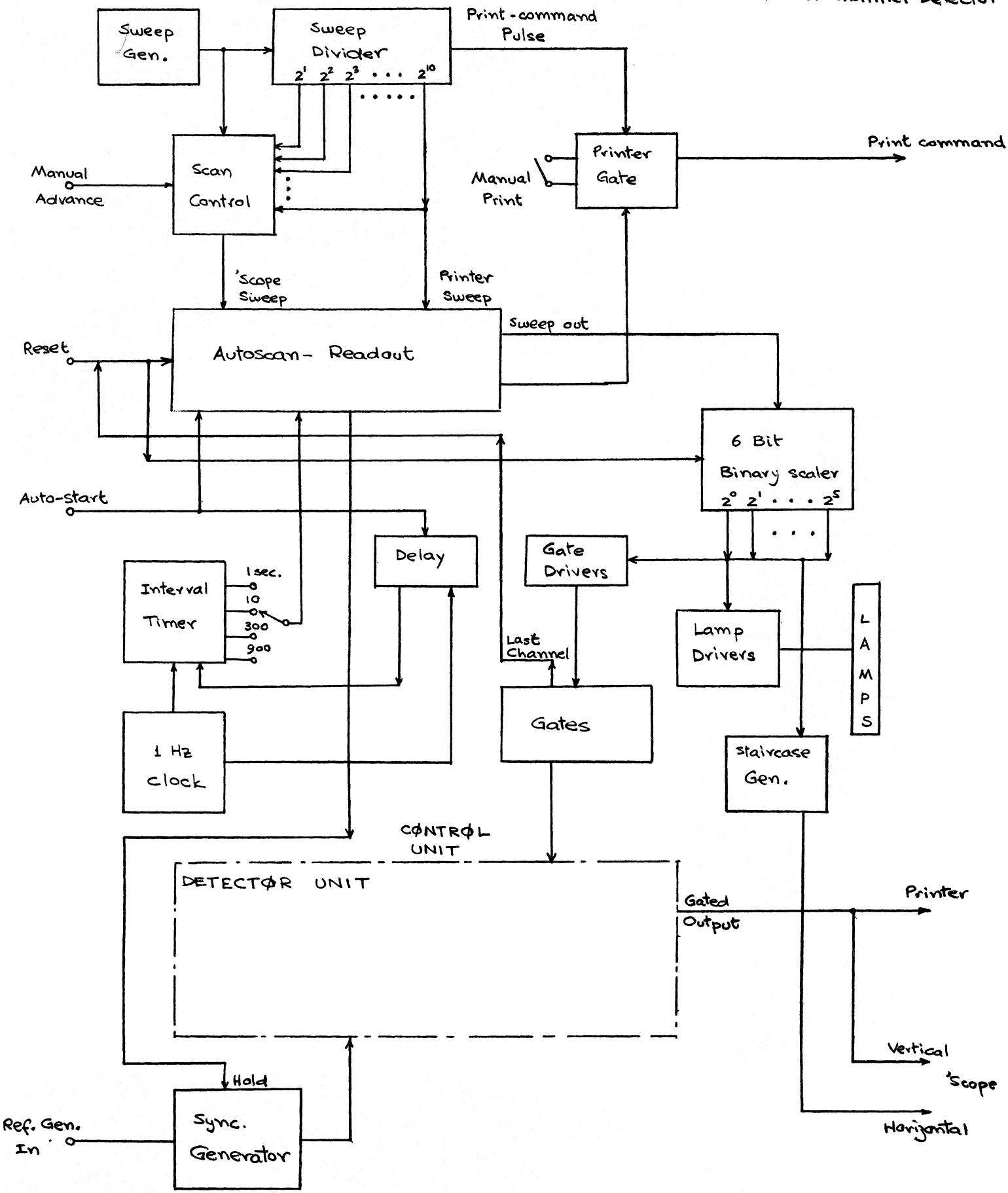
(2) Autoscan circuit to provide the different modes of readout, etc.

(3.1) Interval Timer. This unit consists of the following:

(3.1.1) Clock. This supplies the timing pulses for the interval timer. It is made of a 1 Hz (± 0.005%) clock (Fork Standards, Inc., Model G). The power supply is Zener regulated to provide the +12 V DC required.

(3.1.2) Binary Counter. This is basically a 10-stage binary divider, with AND gates which provide output pulses whenever the count becomes 1 second, 10 seconds, 300 seconds, or 900 seconds. This in turn is used to turn the integrator on and off for a period of integration. The counter is reset, when the "Autostart" button is pushed, and proceeds to count to the preset time (e.g., 5 minutes).

Fig-2 Detailed block Diagram of Multichannel Detector



(3.2) Autoscan Circuit. This unit consists of the following:

(3.2.1) Sync. Generator. This generator provides three outputs when the input consists of a Dicke switch signal from the NRAO Standard Receiver (i.e., a square-wave of 0/-6.0 V) [0 V = signal; -6.0 V = reference source]. The three outputs are:

(a) ±20 V square-wave to switch the synchronous detectors.

(b) ±20 V square-wave (180° out of phase with (a)) — also to switch the synchronous detectors.

(c) ±20 V square-wave test signal (in phase with (a)) with output in the front panel (J4) for test purposes.

Also included in this unit is a "hold" circuitry such that both the outputs, (a) and (b) above, could be held to -20 V DC to switch off the synchronous detectors, hence stop the integration. This is controlled by the "Integration Mode" switch in the front panel of the synchronous detectors, or, when the switch is set on AUTO, then the hold circuitry is controlled by the Internal Timer [Section (3.1)].

(3.2.2) Sweep Generator. This unit provides the pulses for the gating circuits, to control the readout of the different channels of the detector. It consists of two parts:

(a) Astable Multivibrator. This is used in the normal mode of operation. It consists of an astable multivibrator whose period is approximately 1.5 ms and pulse width approximately 0.1 ms. Both period and pulse width could be adjusted by the potentiometers used.

(b) Pulse-shaping Circuit. When the "sweep rate" switch is on "OFF", the astable multivibrator (a) is disengaged and the sweep is manually controlled by the pulse-shaping circuit through a front-panel "Manual Advance" push-button switch. Each pulse on the push-button will advance the readout channel by one.

(3.2.3) Sweep Divider. This is a 10-stage binary divider which divides the output of the Astable Multivibrator by 2^n, where n = 2, 3,... 10. Its output is used to control the sweep rate of the readout. Hence the sweep rates available are:

$$\frac{F_o}{2^n} \qquad \text{where} \quad n = 1, 2, 3 \ldots 10$$

and F_o is frequency of the astable multivibrator ($\approx$ 670 Hz).

The fastest sweep rate is used to display the output of the different channels on the oscilloscope and the slowest sweep rate ($F_o/1024$) is used for printout on a numerical printer and/or paper tape punch. The intermediate rates are not normally used. The sweep rate could be manually set to any of the above rates by the front panel "Sweep Rate" switch, except when the unit is automatically printing, in which case the sweep rate is automatically set at the printer's (slowest) rate.

(3.2.4) Binary Scaler. This essentially is a 6-stage binary divider which generates a 6-bit binary code from the output of the sweep generator. It is used to drive the staircase generator, gates and the lamp drivers. The outputs (complements are also available) operate in the normal binary fashion, i.e., 000001 for channel 1, 000010 for channel 2, etc. The scaler is reset, to 000000 (channel 0), whenever the "Sweep Reset" push-button switch on the front panel is pushed, or when a pulse, indicating that the last desired channel to be read has been reached, is received.

(3.2.5) Staircase Generator. This is used to provide the horizontal sweep on the oscilloscope. The input is taken from the Binary Scaler (3.2.4), fed through a digital-analog converter, and the resulting analog voltage is amplified. The digital-analog conversion is of the current sensing type utilizing an operational amplifier for the summation of input currents. A potentiometer is used to control the gain of the second operational amplifier, used as a voltage amplifier. This is to adjust for full scale horizontal deflection on the oscilloscope when the number of channels desired is changed. (The detector would work with any number of channels up to 52.)

(3.2.6) Lamp Drivers. This is used to drive the front-panel lamps to show (in binary form) the present channel being read out.

(3.2.7) Gate Drivers. This provides the required voltages (and complements) to switch the diode transmission gates. Ones are represented by +20 V and zeros by -20 V. (The other way around for the complement outputs.) The input is taken from the binary scaler (3.2.4).

(3.2.8) Gates. These are diode transmission gates wired such that an output appears when the channel number of the gates coincides with the binary number from the gate drivers, i.e., channel 3 output appears when 000011 appears at the gate drivers. The output levels are approximately +20 volts for "ON" (coincidence) and -19.4 volts for "OFF".

(3.2.9) Readout Control. This controls the mode of operation when the unit is set on automatic. The following happens when the AUTOSTART button is momentarily pushed:

(i) Integrator is reset, internal timer is reset, sweep rate is set at the rate shown on the "Sweep Rate" switch-

(ii) Integration is performed for τ seconds, determined by the setting on the "Integration Time" switch.

(iii) After the preset duration τ, the hold circuit is activated and is held until the next time the AUTOSTART button is pushed.

(iv) Print command signal is gated to the printer; sweep rate is reduced to the slowest rate.

(v) Sweep is initiated at the slow rate beginning at channel 1.

(vi) Gating signal to the print command generator switched off when the last channel has been reached; the sweep rate is switched to the original preset rate.

(vii) This is maintained until the AUTOSTART button is pushed again.

(3.2.10) Print Command Generator. Provides contact closure to activate printer. The pulses from the sweep divider is gated by the readout control (3.2.9) and used to activate a relay. The contact closure makes momentary closures whenever a new channel's output appears at the output to the printer/punch. The gating signal can also be manually inserted by a front panel "Manual Print" toggle switch.

(3.3) Synchronous Detector and Integrator Unit. This unit consists of up to 52 independent synchronous detectors and integrators, one for each channel used.

(3.4) Synchronous Detectors. Figure 3 shows the block diagram of the synchronous detectors used.

Amplifier A1 has a gain of -50 (10 °K) or -5 (100 °K), depending on the switch setting of the toggle "SCALE" switch on the front panel. Amplifier A2 has a gain of -1. The switch S_1 (physically, consists of 2 FET switches) is switched at the same rate as the front end (and gain modulator) between "a" and "c". When the switch is at "b", the detector is on "hold", i.e., the output voltage is zero.

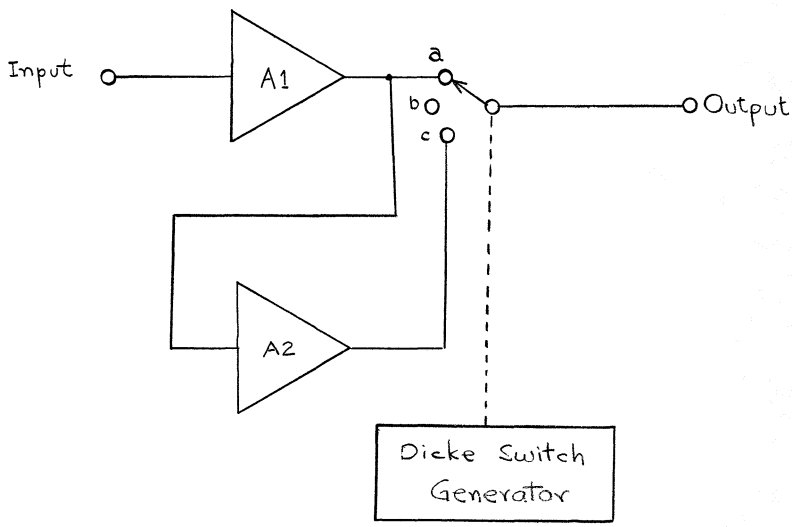


Figure 3 — Synchronous Detector

(3.5) Integrator. The integrator is set so that for all integration durations, the gain is 2, i.e., if,

$$v_{o_{final}} = \frac{1}{RC} \int_0^{\tau} v_{in}\, dt$$

then,

$$RC = \frac{1}{2}\tau$$

Four integration rates are available, i.e., for τ = 1 sec, 10 sec, 300 sec, and 900 sec. The integrator is reset by discharging the integrating capacitor (time constant of discharge $\doteq$ 10 ms). Two outputs are available, a direct output and a gated output. The gated output is zero when the gating signal is at -20 V DC and is the integrator's output when the gating signal is +20 V DC.

(3.6) FET Switches. All switching (synchronous detector, integration rate, reset of integrator, gating of output of integrator) is done by FET switches (Fig. 4).

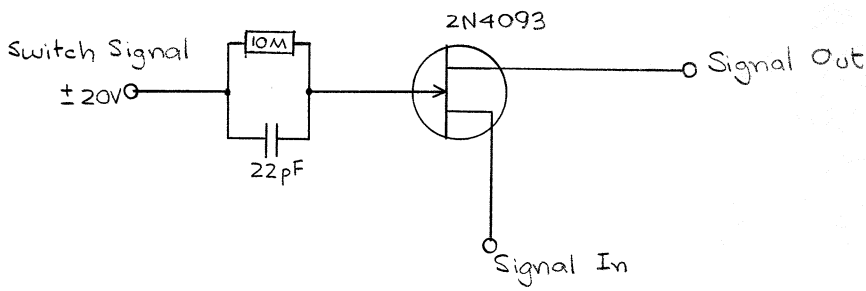


Figure 4 — FET Switch

The switch is "open" for a -20 V DC switch signal and "closed" for +20 V DC switch signal. Figure 7 shows a family of transfer characteristics for the FET switch used. Notice that linearity is conserved for a large enough switch signal.

4. Errors Produced by the Synchronous Detector/Integrator

Shown below is an analysis of the error in the output due to the offsets in the operational amplifiers and other known data. Figure 5 shows the block diagram of the synchronous detector/integrator.

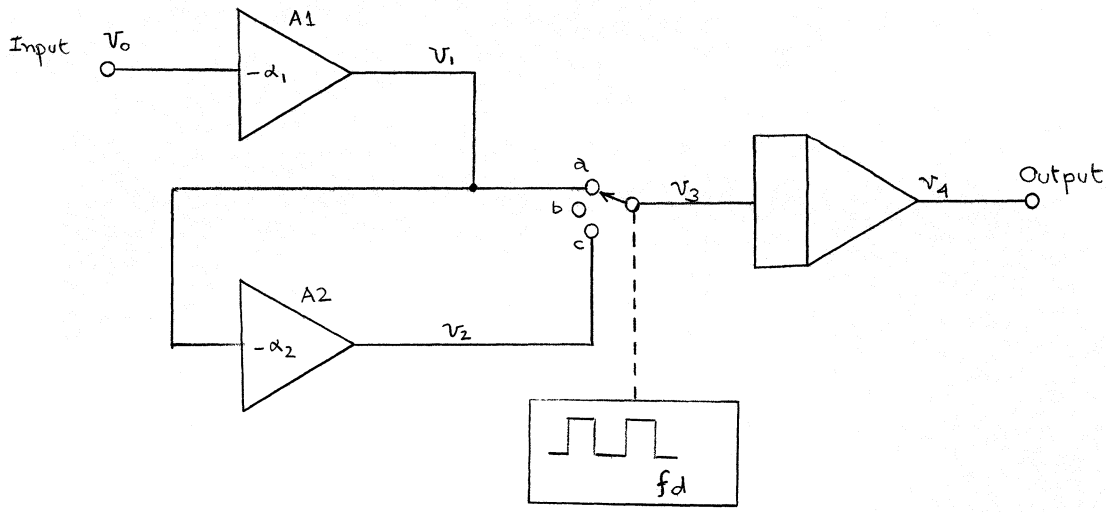


Figure 5 — Synchronous Detector and Integrator

Let v^1_{os} be the output voltage offset tue to the input voltage and input current offset of amplifier A1

v^2_{os} be the output voltage offset of amplifier A2

and α_1 and α_2 are the gains of A1 and A2.

To simplify matters, let the input, v_0, be zero. Hence,

$$v_1 = v^1_{os}$$

and

$$v_2 = (v^1_{os})\,\alpha_2 + v^2_{os}$$

$$v_3 = \frac{v_1 + v_2}{2} \qquad \text{(time average of } v_1 \text{ and } v_2\text{)}$$

$$v_4 = \frac{2}{\tau} \int_0^{\tau} v_3 \, dt$$

but, since v_3 is a constant, the integral becomes,

$$v_4 = \frac{2}{\tau} (v_3 \tau) = 2v_3$$

$$\text{for } \tau >> \frac{1}{fd}$$

For the input, v_0, at zero voltage, v_4 should ideally be zero. But, due to the offsets and error in the gain of A2, we have

$$v_4 = 2v_3 = (v_1 + v_2) = [(1 - \alpha_2) v^1_{os} + v^2_{os}]$$

which is generally a non-zero term.

For A1 and A2, the offset voltages, v^1_{os} and v^2_{os} are approximated by,

$$v^k_{os} \simeq \alpha_k v^k_{is} \simeq \frac{Rf}{Ri} v^k_{is}$$

where v^k_{is} is the input voltage offset. (See Fig. 6.)

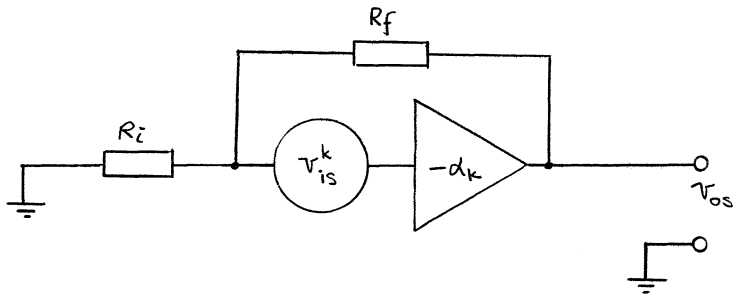


Figure 6 — Voltage Offset in Operational Amplifier

The input current offset is small enough to be neglected. α_2 should be 1 but due to error in resistors Rf and Ri (1% resistors) α_2 can be off by $\simeq$ 2%. Hence $(1 - \alpha_2)$ in the worst case $\simeq$ 0.02.

We therefore obtain for the worst case

$$v_4 \simeq (0.02)\, v^1_{os} + \alpha_2 v^2_{os}$$

$$\simeq 0.02\, v^1_{os} + v_{is}$$

$$\simeq [(0.02)\, \alpha_1 + 1]\, v_{is}$$

v_{is} for the operational amplifiers is given as 10 mV (max.)

α_1 is equal to 5 or 50 depending on the SCALE switch setting, therefore

$v_4 \doteq$ 10 mV [1 + 0.1] for 100 °K scale

$v_4 \doteq$ 10 mV [1 + 1] for 10 °K scale

Hence, the errors in v_4 are

11 mV for 100 °K scale
20 mV for 10 °K scale

These correspond to

0.11 °K for 100 °K scale
0.02 °K for 10 °K scale.

The above shows the values off error voltages if the integrator were perfect. However, the integrator has a current offset of 100 pA maximum. changes the integrator's capacitor (10 μF) by,

$$\frac{1}{C}\int_0^{\tau} i_0\, dt \simeq \frac{1}{C}\, i_0\, \tau$$

$$\simeq 10^{-5}\, \tau$$

$$\simeq 10\ \mu V/sec.$$

Hence, for an integration duration of 5 minutes (300 sec), an additional error of 3 mV occurs. This also occurs when the integrator is on "Hold" (i.e., during printing). Therefore, for an integration duration of 5 minutes, and a total of 1 minute for printing all the channels, the error mounts up to an additional 3.6 mV (.004 °K on 10 °K scale; .04 °K on 100 °K scale).

Combining the two errors, we obtain,

$$\Delta v = v_4 = 0.11\ ^\circ K + 10^{-10}\,\tau\ ^\circ K \quad \text{on} \quad 100\ ^\circ K \text{ scale}$$

$$\Delta v = v_4 = 0.02\ ^\circ K + 10^{-11}\,\tau\ ^\circ K \quad \text{on} \quad 10\ ^\circ K \text{ scale}$$

where τ is the integration duration plus "hold" time.

5. Modifications

This unit could be modified to accept any number of channels up to 52. The modification involves the rewiring of two gating paths.

(i) Last channel gate. This path is between the required last channel on the gate boards (boards 7-14) and the reset terminal of the Autoscan-Readout circuit (board 16, terminal T).

(ii) Counter Reset. This path is between the required last channel plus one (N + 1) on the gate boards to the "Gated Reset" terminal of the Binary Scaler board (board 3, terminal V).

The unit has been modified such that, when on the automatic mode, the integration and readout could be made recycling, i.e., it will integrate, readout, and integrate again without having to push the "Autostart" button. A toggle switch determines whether this option is required. This toggle switch could be reached by opening the panel of the control unit and it is situated at the lower right-hand corner. When in the off position (downwards), the unit operates as described in the section on "Operations". The circuit diagram of the recycling unit follows.

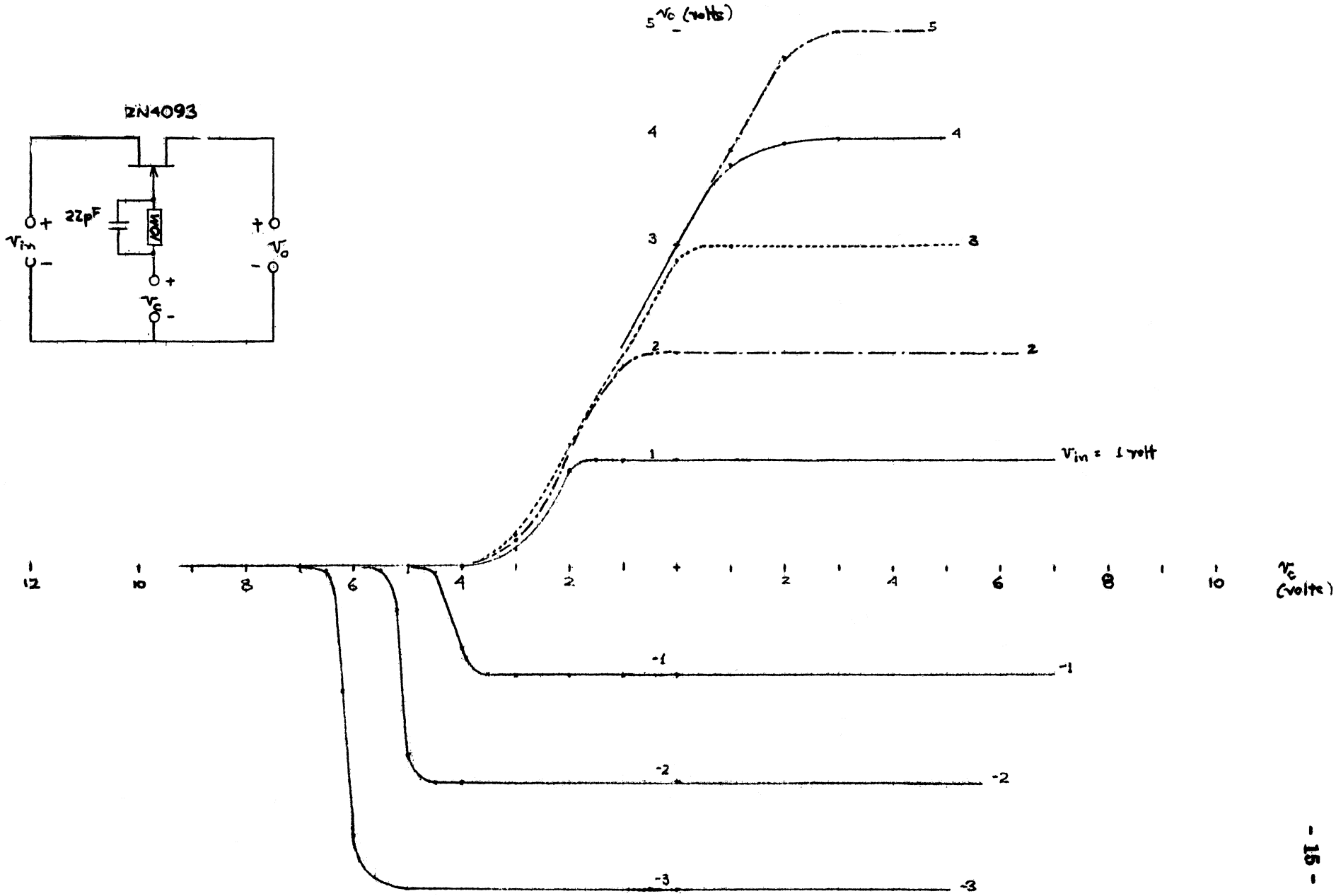
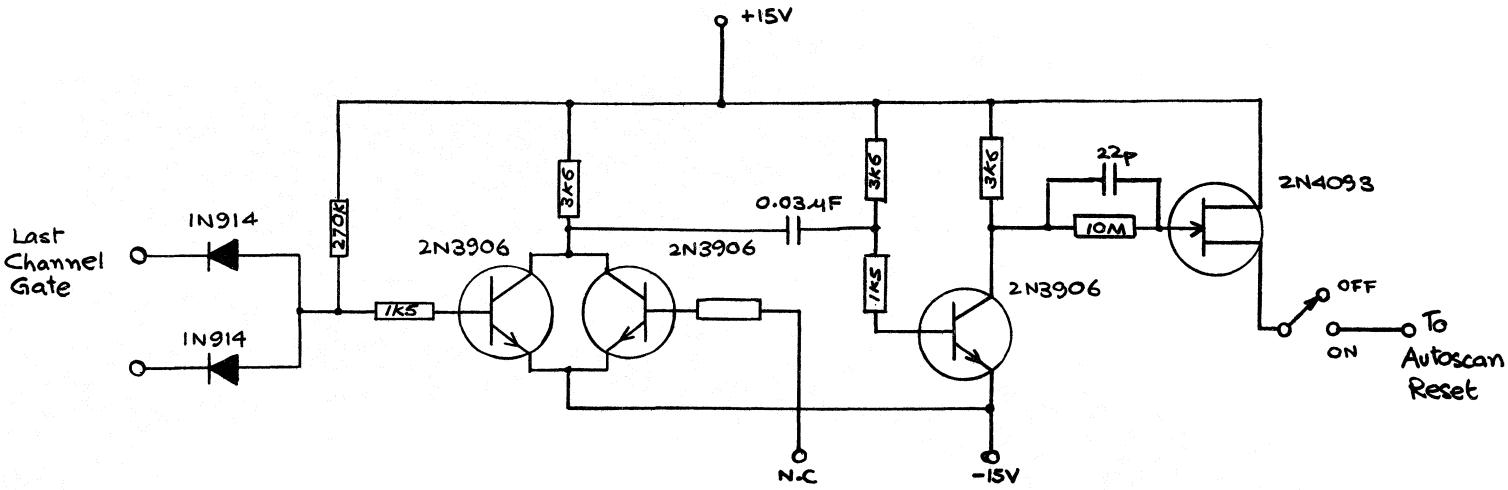
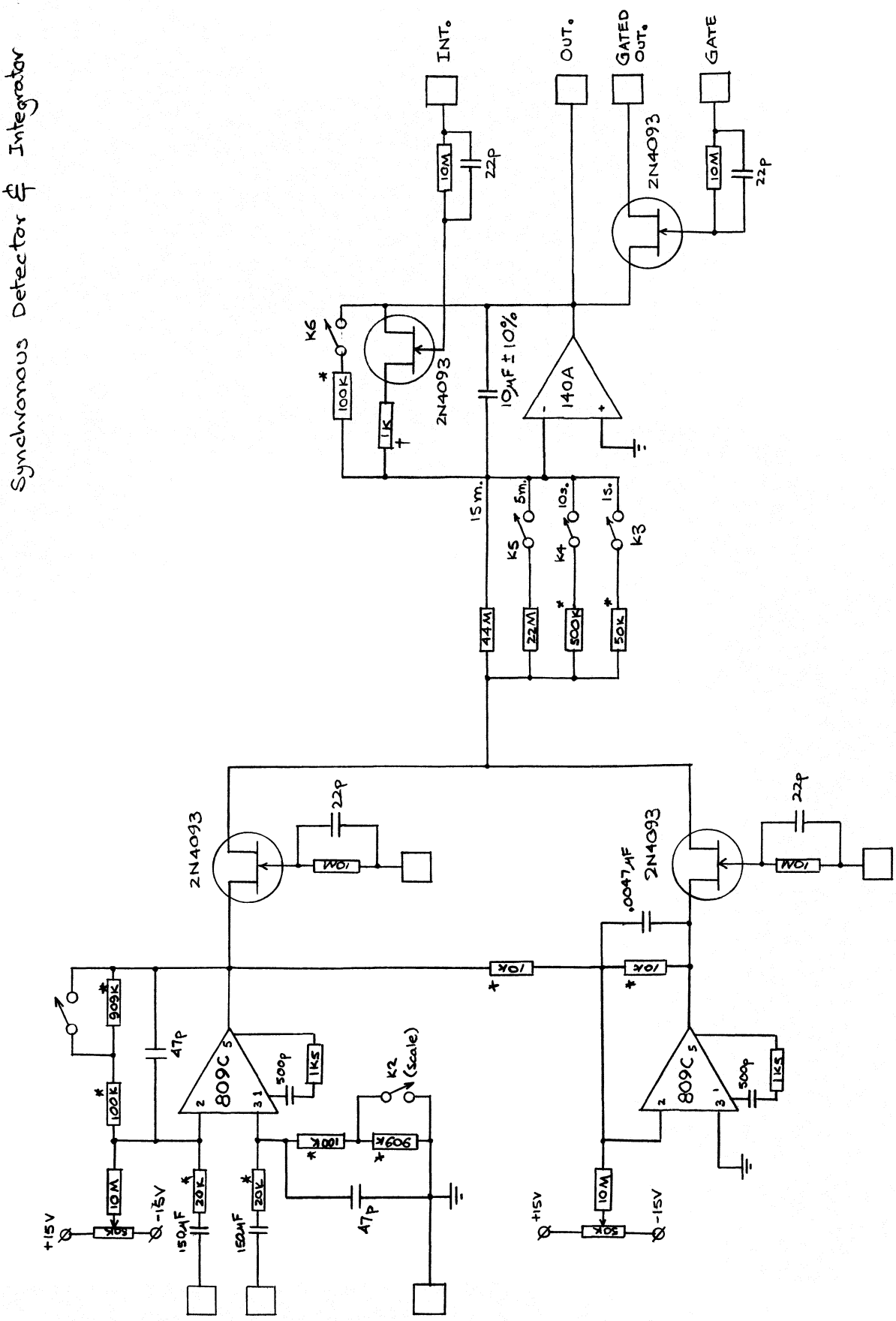


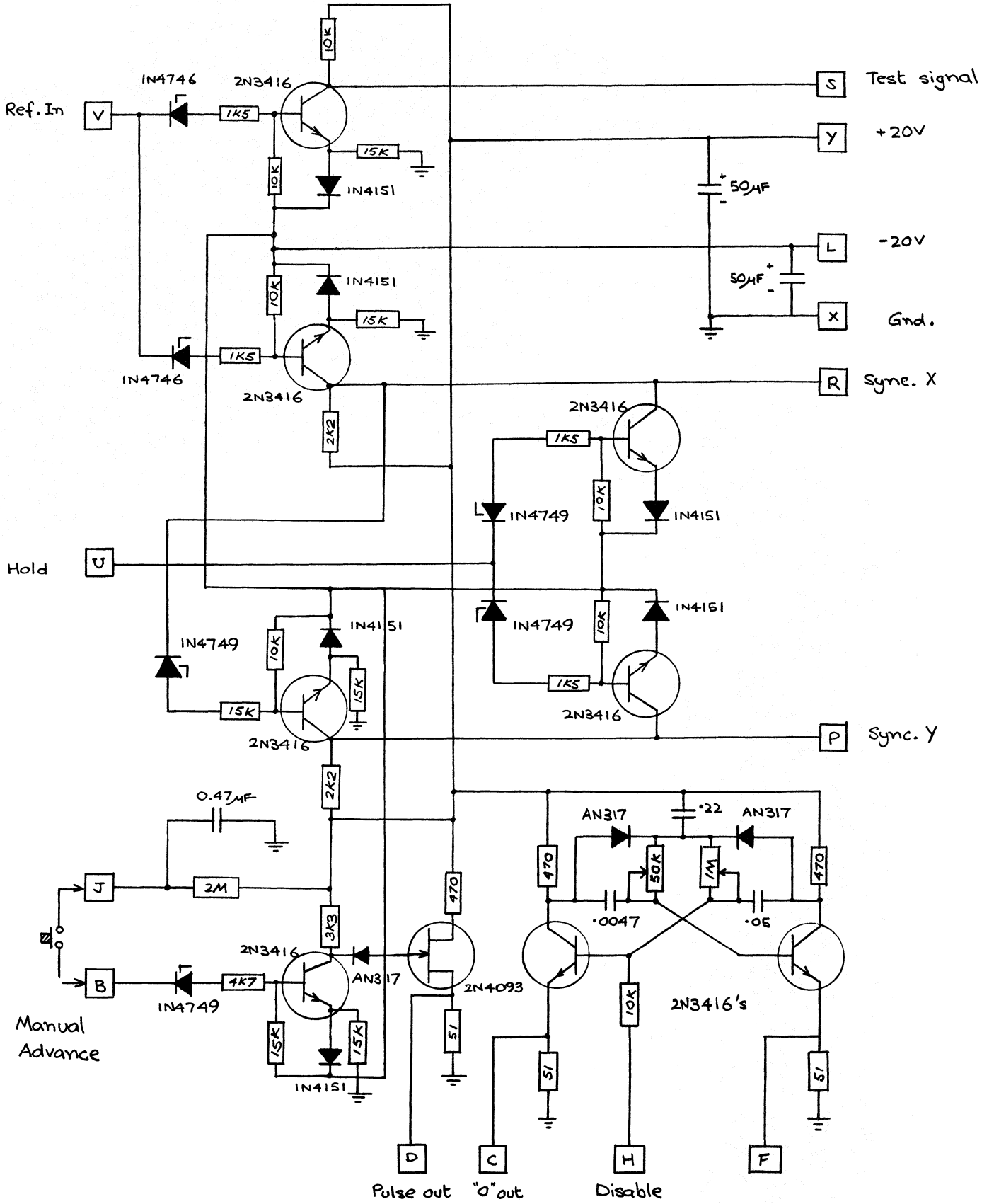
Fig. 7 Transfer Characteristics of FET switch.



Recycling circuit

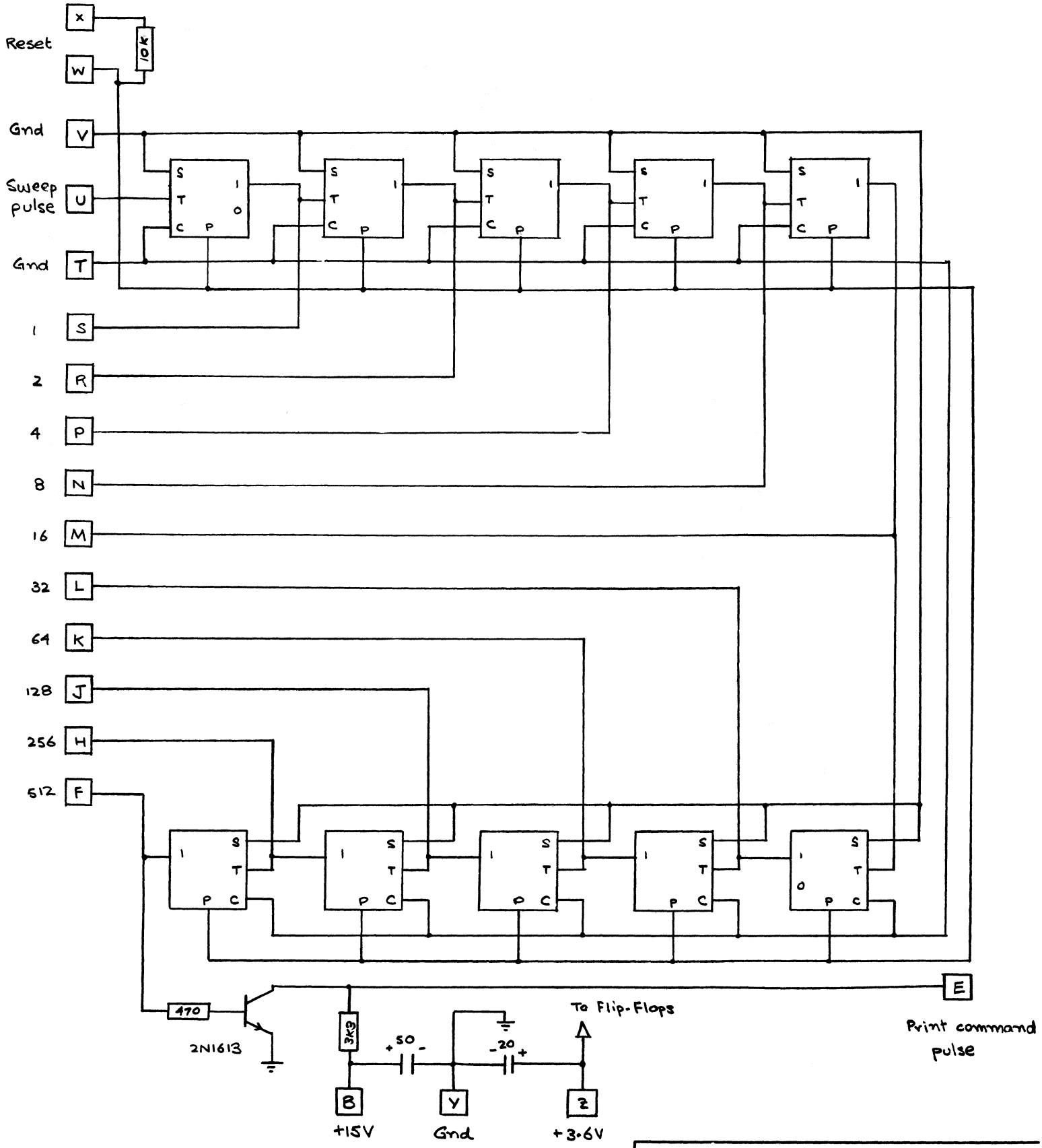
6. Circuit Diagrams


Synchronous Detector & Integrator
All resistors 5% 1/4 watt except
* 1%
† 1 watt
INT.
OUT.
GATED OUT.
GATE
2N4093
140A
809C
10M
22P
100K
1K
10μF ±10%
15m.
5m.
10s.
1s.
K1
K2 (scale)
K3
K4
K5
K6
44M
22M
500K
50K
10K
909K
100K
47P
500P
1K
20K
150μF
.0047μF
+15V
-15V



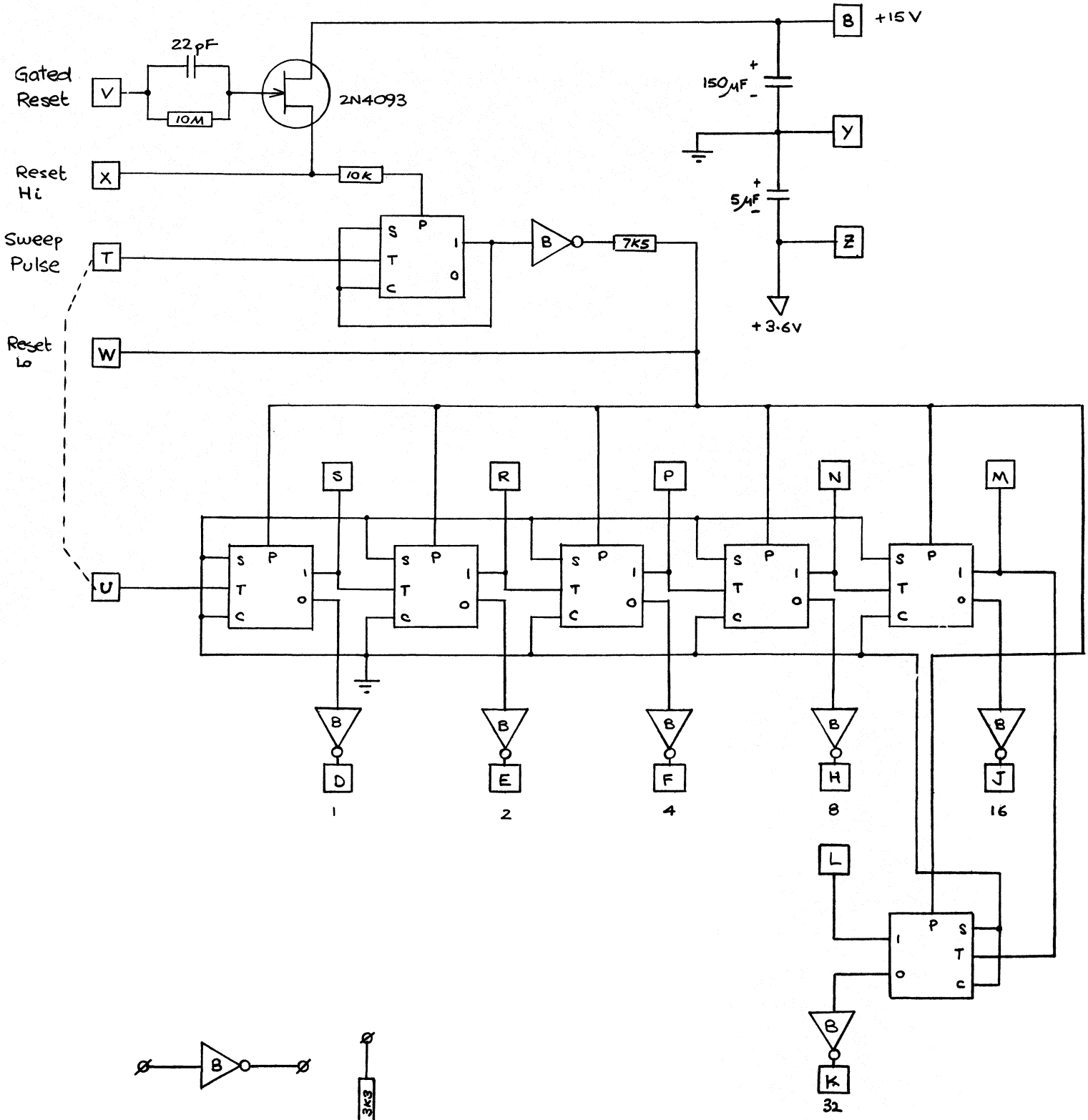
Board # 1

Sync. Generator / Sweep Generator



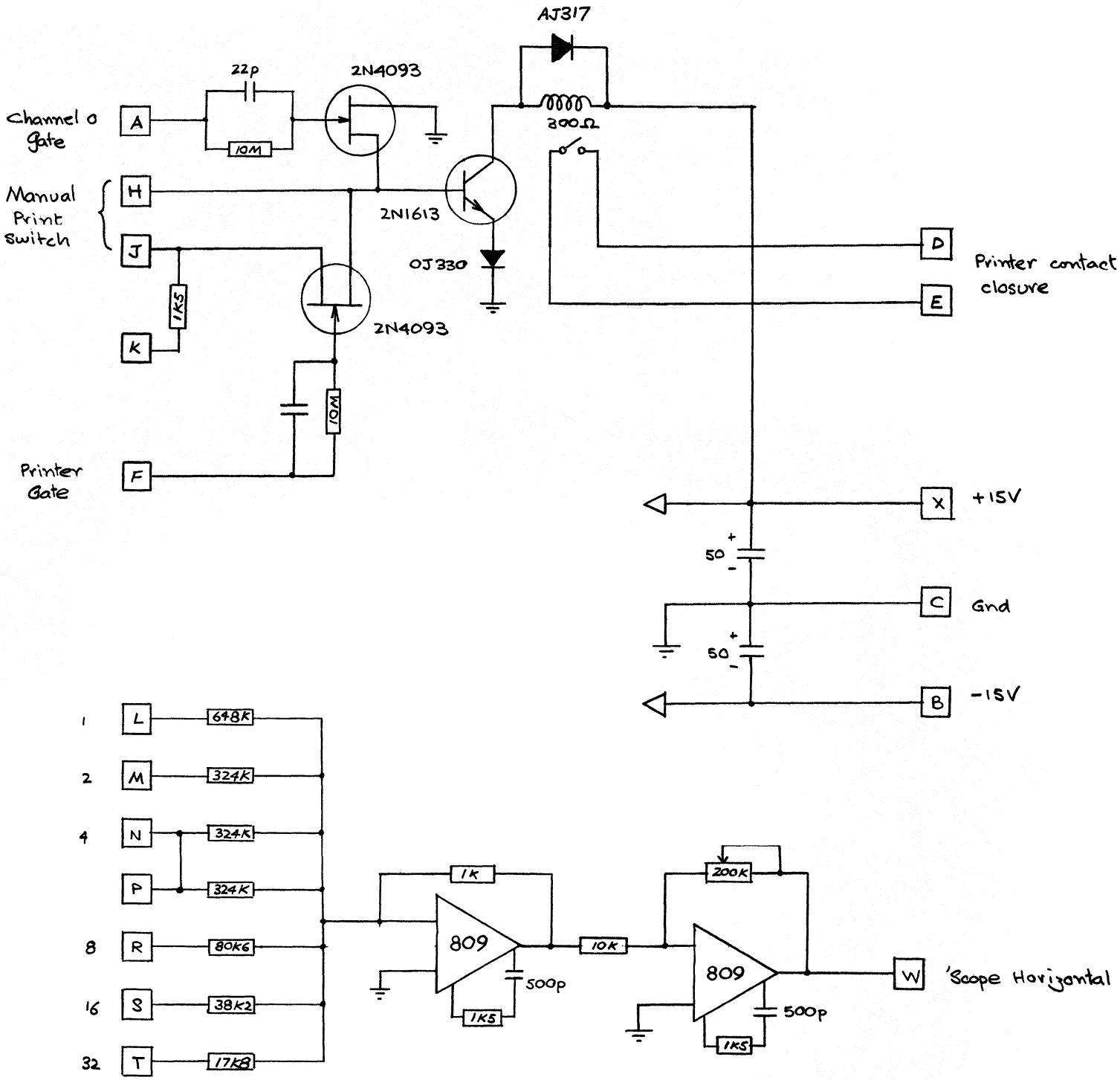
Board #2

Scale of 10 sweep divider



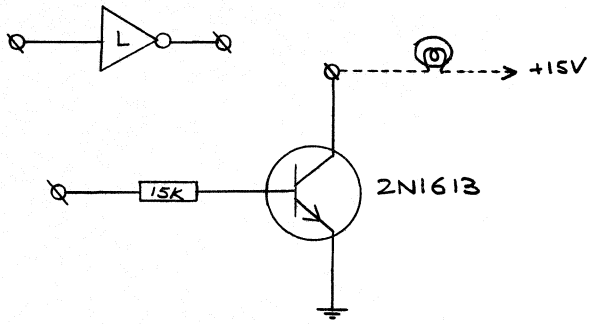
Board #3

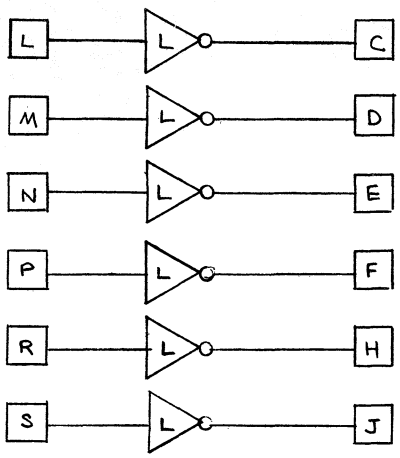
6 Bit Binary Scaler

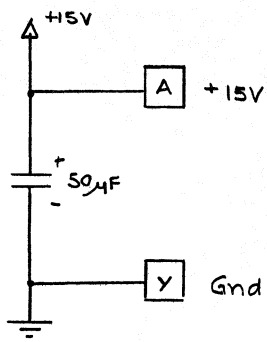


Board #4

Step Generator & Print-command generator

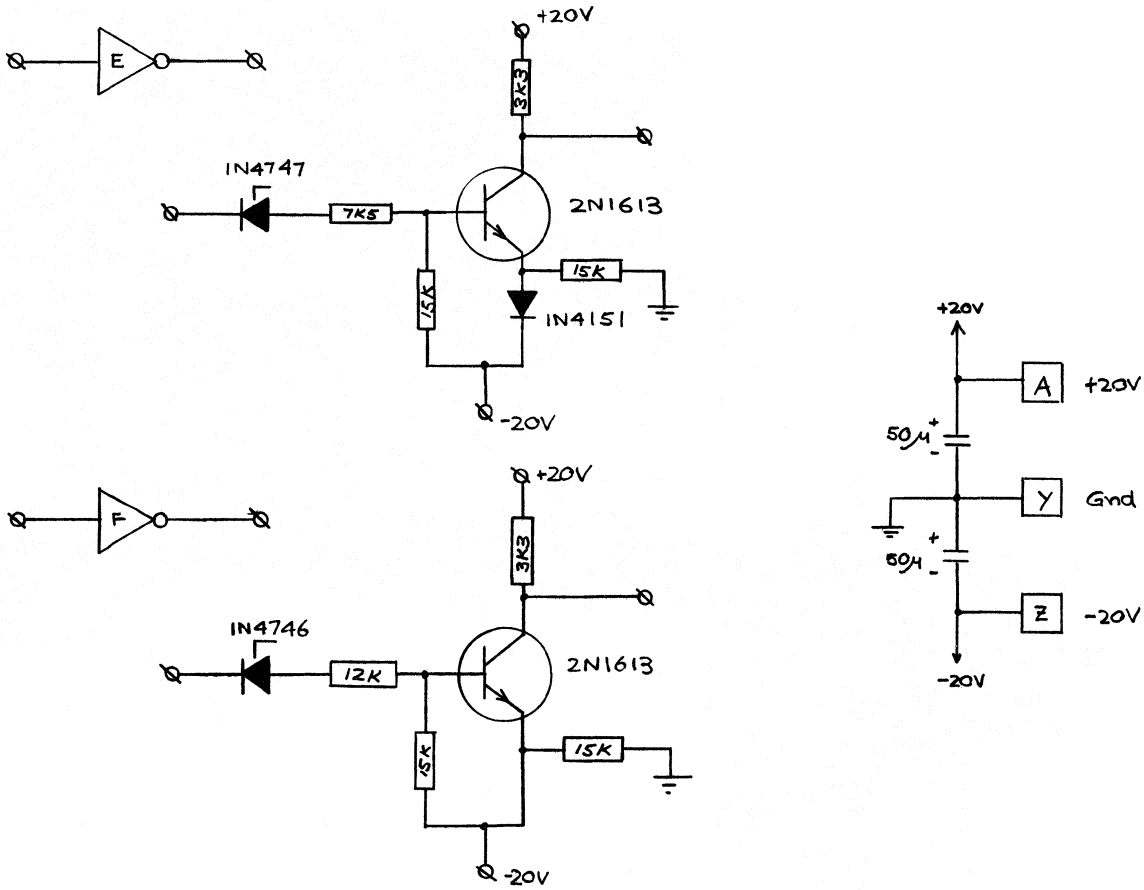


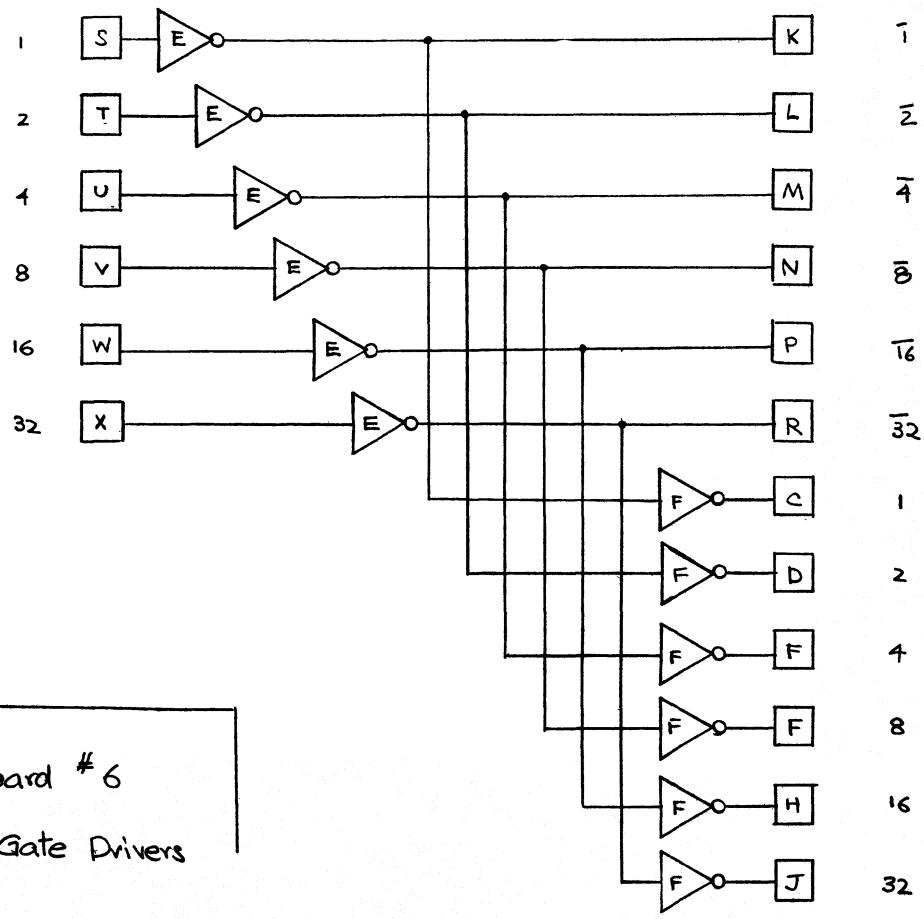




Board #5

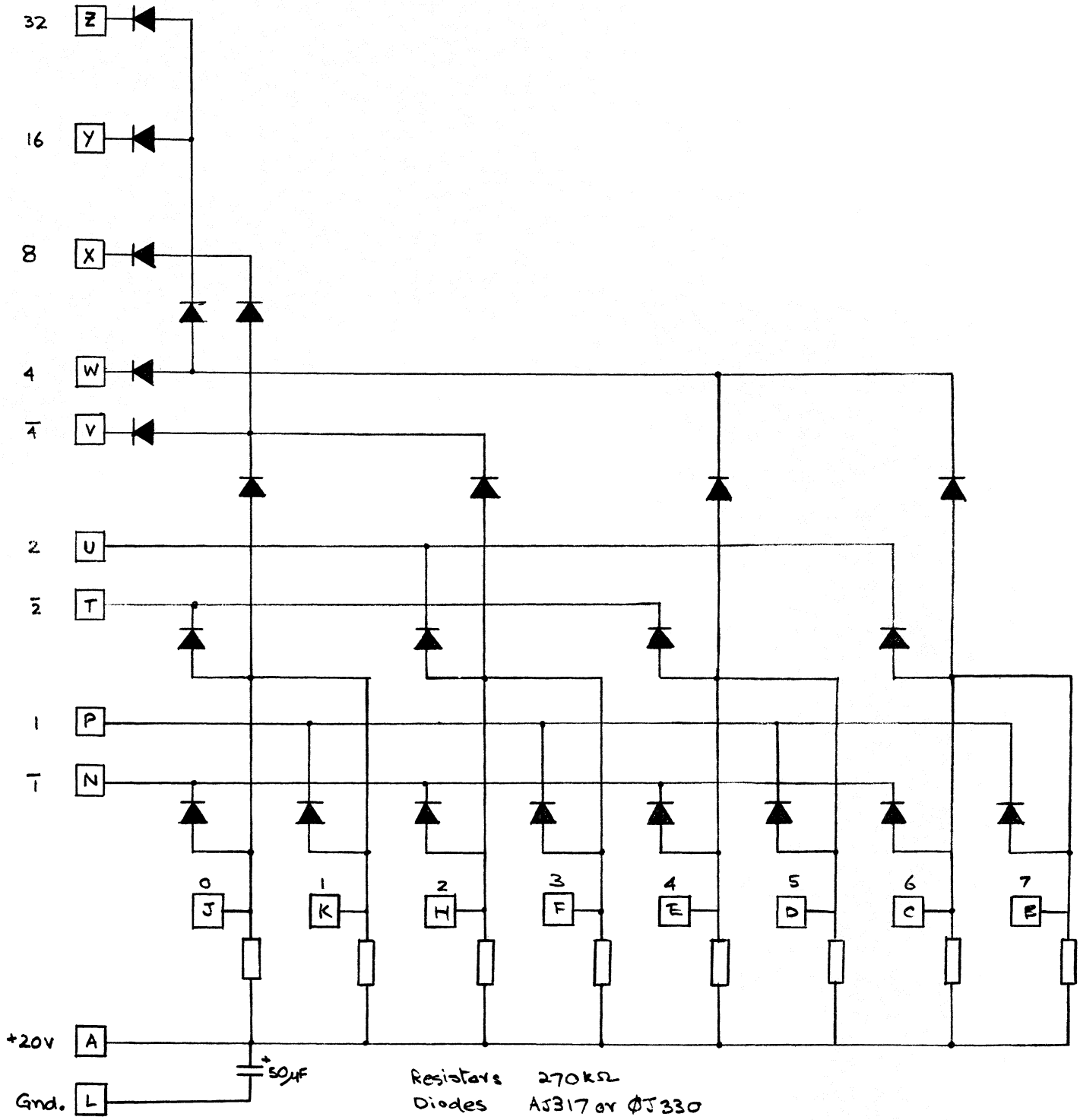
Lamp Drivers





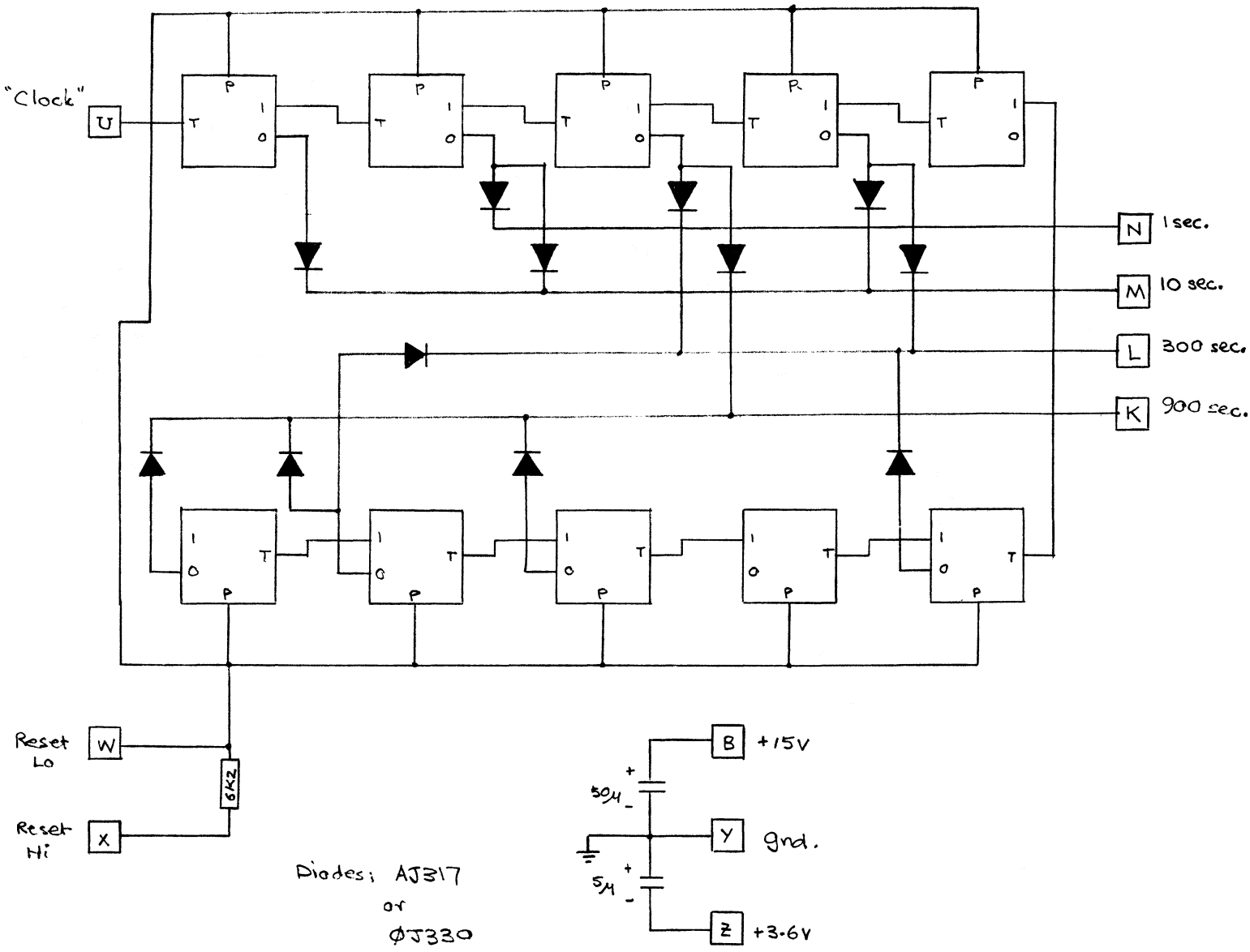
Board # 6

Gate Drivers



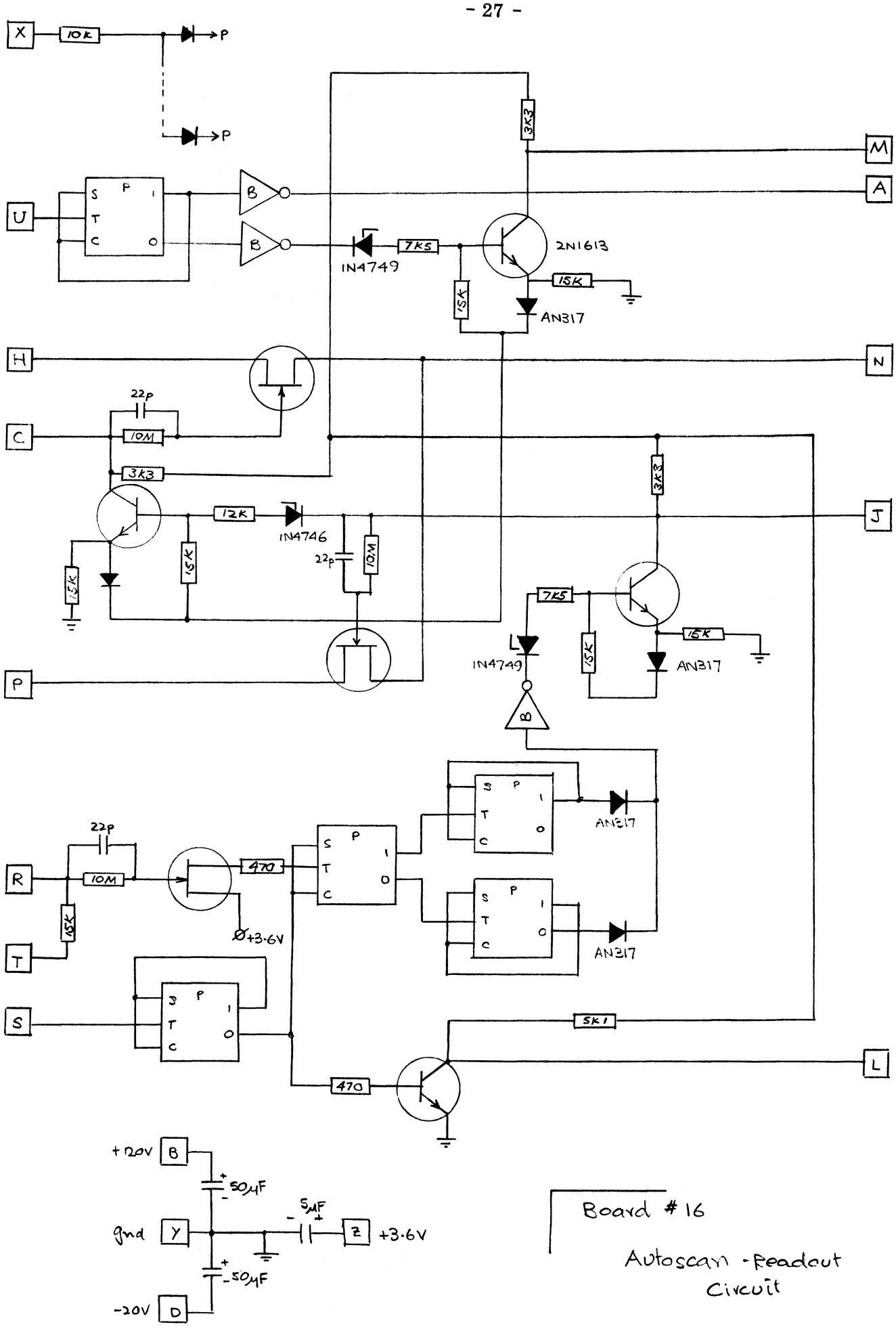
8-Channel Gate

Board #7 (8, 9, 10, 11, 12, 13, 14)



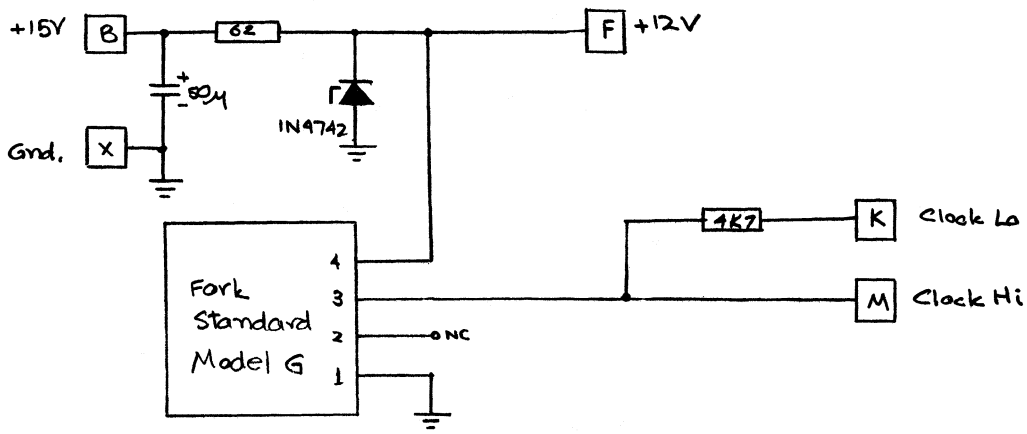
Board # 15

Interval timer



Board #16

Autoscan - Readout Circuit



Board # 17

Clock