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AUTOCORRELATION RECEIVER MODEL II: OPERATIONAL DESCRIPTION

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TABLE OF CONTENTS

LIST OF FIGURES

AUTOCORRELATION RECEIVER MODEL II: OPERATIONAL DESCRIPTION

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I. Introduction

The NRAO Autocorrelation Receiver Model II is a specialized receiver system for observation of spectral lines. It is the equivalent of a multi-channel spectrum analyzer. A block diagram of a complete system using the correlation receiver is shown in Figure 1.

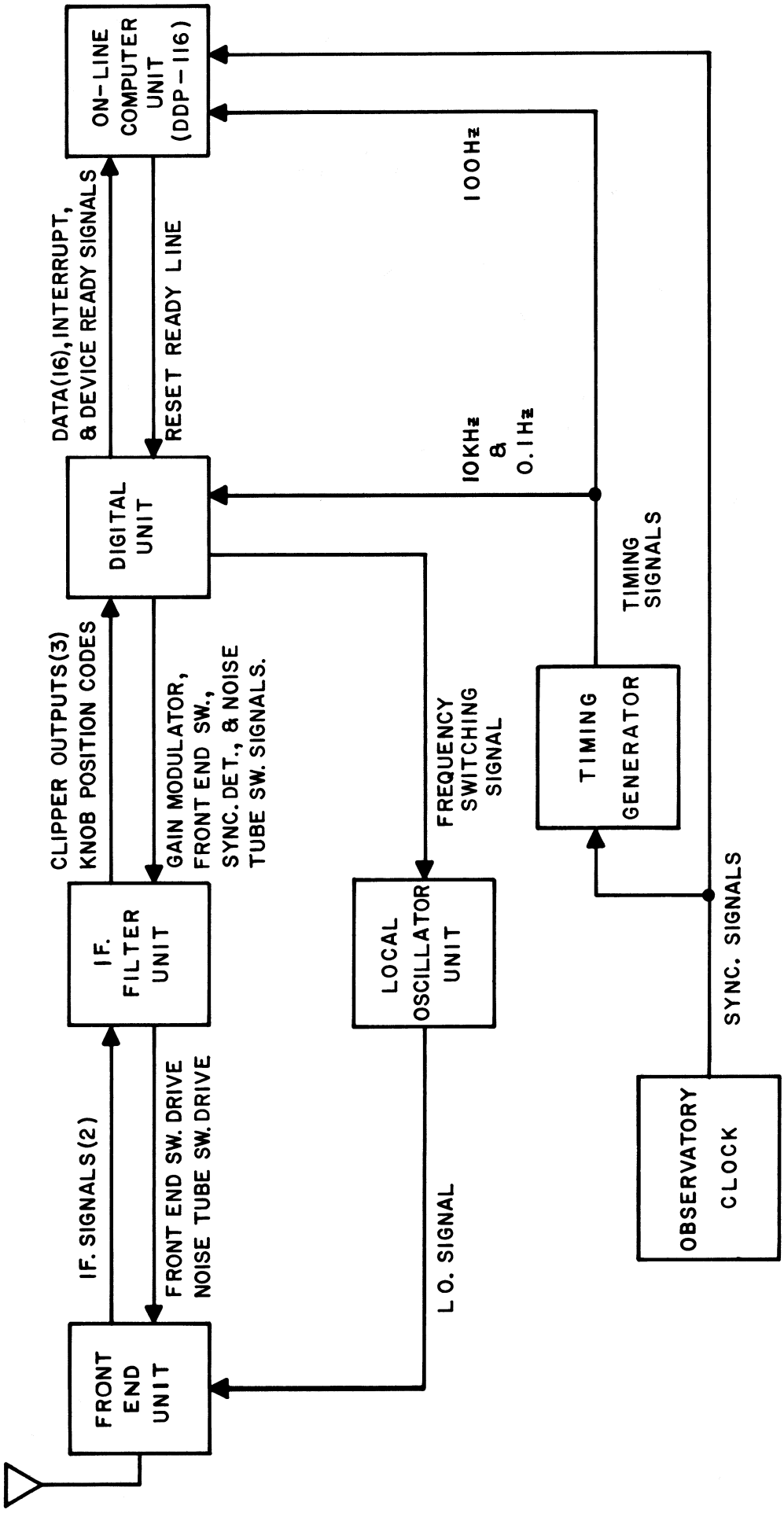
The process consists of filtering out a selected bandpass centered at a desired spectral-line frequency and heterodyning it down to the video-frequency range with one side of the bandpass being at zero frequency. This signal is clipped to provide a rectangular waveshape of fixed amplitude. The only correspondence between the clipped and unclipped signal is that they both cross zero at the same time. The clipped signal is sampled at a frequency equal to twice the bandwidth and the sampled data is used to generate an autocorrelation function with 192 or 384 points.

The integrated autocorrelation function is processed by an on-line computer. The computer performs a Fourier Transform to generate a power spectrum. The computer data is available as an on-line graph on a storage oscilloscope, as a printed-tabular output, and as an output on magnetic tape which can be further processed by an off-line computer.

The autocorrelation receiver can be used with any front-end having a 30 MHz or 150 MHz IF output. The front-end may be either load-switched or frequency-switched and must contain a noise calibration signal that can be modulated.

The next section of this report contains a description of the bandwidth, resolution, and sensitivity parameters of the system. Sections 3 and 4 contain brief descriptions of the IF and digital portions of the system. The on-line computer processing is described in Section 5. Appendix I contains a detailed description of the data available at the correlator output and transferred to the computer. Finally, Appendix II contains photographs of the receiver bandpass functions for all bandwidth settings. (These are useful for checking for proper operation of the equipment.)

A complete description of the one-bit autocorrelation function method of spectral-line measurements is presented in the following report:



SYSTEM BLOCK DIAGRAM

Figure 1

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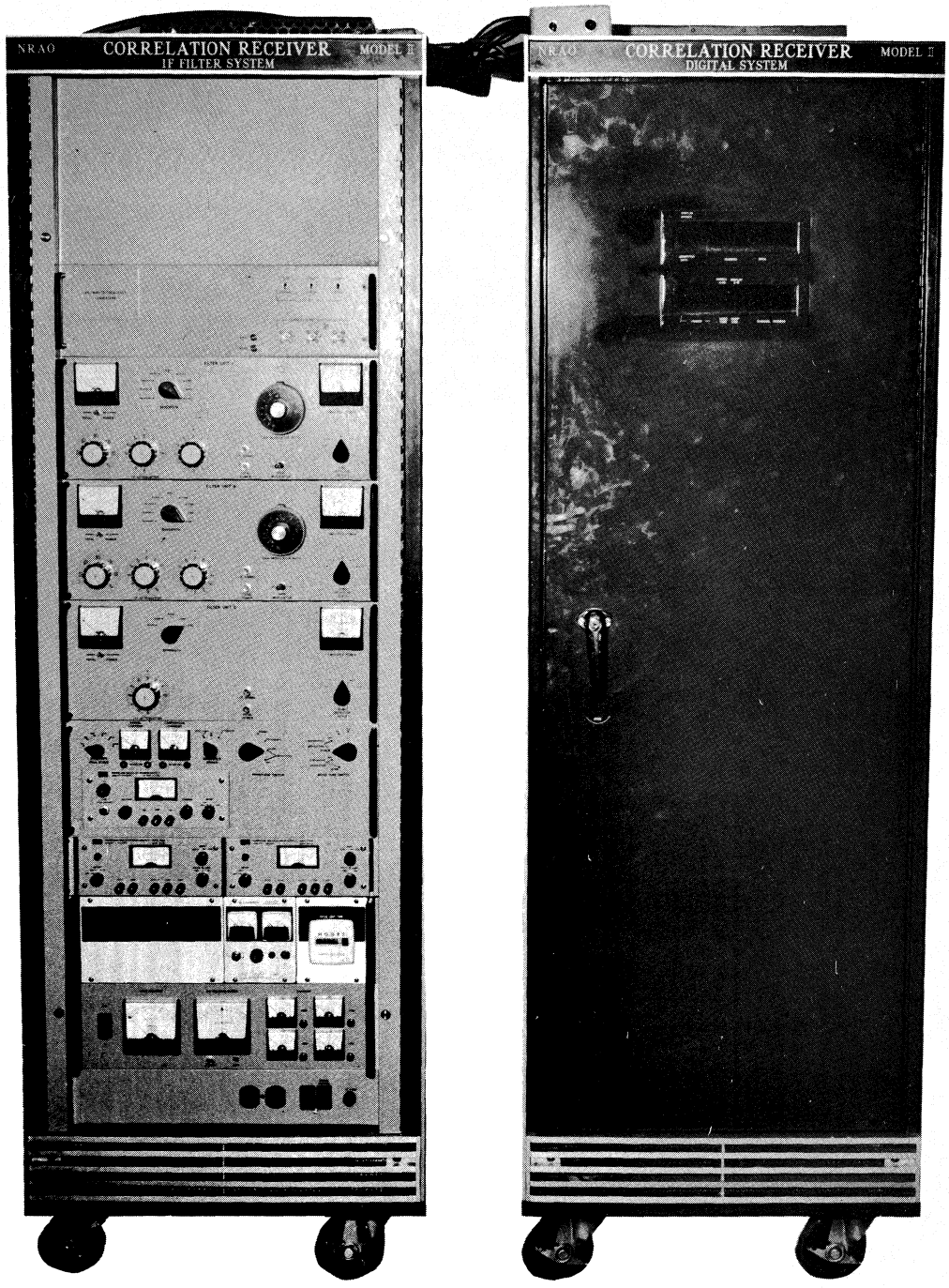


Figure 2 — The Correlation Receiver IF Filter System (left) and Digital System (right) are shown. The IF cabinet contains, from top to bottom, clipper and V/F Converter chassis, IF channels A, B, and C, switch drivers, and power supplies. The display on the digital rack has various indicator lights and a decimal display of the contents of a selected correlator channel.

S. Weinreb, "A Digital Spectral Analysis Technique and Its Application to Radio Astronomy"; Technical Report 412, M.I.T. Research Laboratory of Electronics, Cambridge, Massachusetts, August 30, 1963 — Available as AD-418-413 from U.S. Clearinghouse for Federal Scientific and Technical Information, Springfield, Virginia 22151, $3.00.

II. Bandwidth, Resolution, and Sensitivity

The receiver can be used in two configurations, Serial and Parallel, as selected by a front-panel switch. In the Serial mode a 384 channel receiver (A) and a 29-channel receiver (C) operating on the same input signal are provided. These receivers can be used with different bandwidths and the 29-channel receiver is usually used to set a wide-bandwidth baseline for the 384 channel receiver.

In the Parallel mode two independent 192 channel receivers (A and B) are provided. These receivers can operate on the same or different input signals (arising from different polarizations, antenna beams, or RF center frequencies) and can have different bandwidths. The 29-channel receiver (C) must operate on the same input signal as either one of the 192 channel receivers but may have a different bandwidth.

The output spectrum produced by the on-line computer consists of computed points spaced δf apart over a total bandwidth, B. Each point represents the power within a filter having approximately a sin x/x shape with a half-power width, $\Delta f = 1.21\,\delta f$, and a spacing between nulls of $2\delta f$. The bandwidth, B, can be selected by front-panel switches. The relation between bandwidth, resolution, spacing, and receiver rms fluctuation, ΔT, is as follows:

$$\delta f = \frac{B}{N} \qquad \Delta f = \frac{1.21\,B}{N} \qquad \Delta T = \frac{3.06\,T}{\sqrt{\tau\,\Delta f}}$$

where N is the number of channels (i.e., 384, 192, or 29), T is the system noise temperature and τ is the integration time.

The selectable values of B and the resulting values of Δf, δf, and ΔT are tabulated in Table 1. The values of ΔT in the table are for a system noise temperature of 100° and an integration time of 10 seconds. For an actual noise temperature, T, and integration time, τ, the ΔT value should be multiplied by T/100 and divided by $\sqrt{\tau}/10$.

TABLE 1

BANDWIDTH, RESOLUTION, AND SENSITIVITY

Bandwidth B	Resolution Δf kHz	Channel Spacing δf kHz	RMS Fluctuation for T = 100° and τ = 10 sec ΔT	Usable Channels
384 Channel Receiver A*				
10 MHz	31.5	26.0417	0.55°	11-374
5 MHz	15.8	13.0208	0.77°	15-377
2.5 MHz	7.9	6.5104	1.10°	17-369
1.25 MHz	3.94	3.2552	1.54°	13-376
625 kHz	1.97	1.6276	2.2°	11-371
312 kHz	0.98	0.8138	3.1°	18-375
156 kHz	0.49	0.4069	4.4°	18-371
78 kHz	0.24	0.2034	6.2°	10-372
39 kHz	0.12	0.1017	8.8°	15-371
192 Channel Receiver A or B**				
10 MHz	63.0	52.0834	0.39°	A 6-187 B 9-177
5 MHz	31.5	26.0417	0.55°	A 8-188 B 7-189
2.5 MHz	15.8	13.0208	0.77°	A 9-182 B 7-185
1.25 MHz	7.9	6.5104	1.10°	A 7-188 B 6-188
625 kHz	3.94	3.2552	1.54°	A 6-185 B 6-186
312 kHz	1.97	1.6276	2.2°	A 9-187 B 9-180
156 kHz	0.98	0.8138	3.1°	A 10-185 B 8-186
78 kHz	0.49	0.4069	4.4°	A 5-185 B 5-185
39 kHz	0.24	0.2034	6.2°	A 7-185 B 7-184
29 Channel Receiver C***				
10 MHz	416	344.828	0.15°	1-27
5 MHz	208	172.414	0.21°	1-27
2.5 MHz	104	86.207	0.30°	1-27
1.25 MHz	52	43.103	0.42°	1-27
.625 MHz	26	21.552	0.60°	1-27

* 0 thru 383

** 0 thru 191 and 192 thru 383

*** 384 thru 412 (0 thru 28)

When examining a spectrum, 5.6% of the points should fall outside of a $4\Delta T$ interval, 1.2% outside of a $5\Delta T$ interval, and 0.26% outside of a $6\Delta T$ range.

At the edges of a measured spectrum the RMS fluctuation increases due to the attenuation at the edges of the band restriction filter in the autocorrelator IF section. At the 6 dB attenuation point the RMS fluctuation doubles and data points beyond the 6 dB level should be ignored. The spectrum channel numbers within the 6 dB points of the receiver bandpass are given in Table 1.

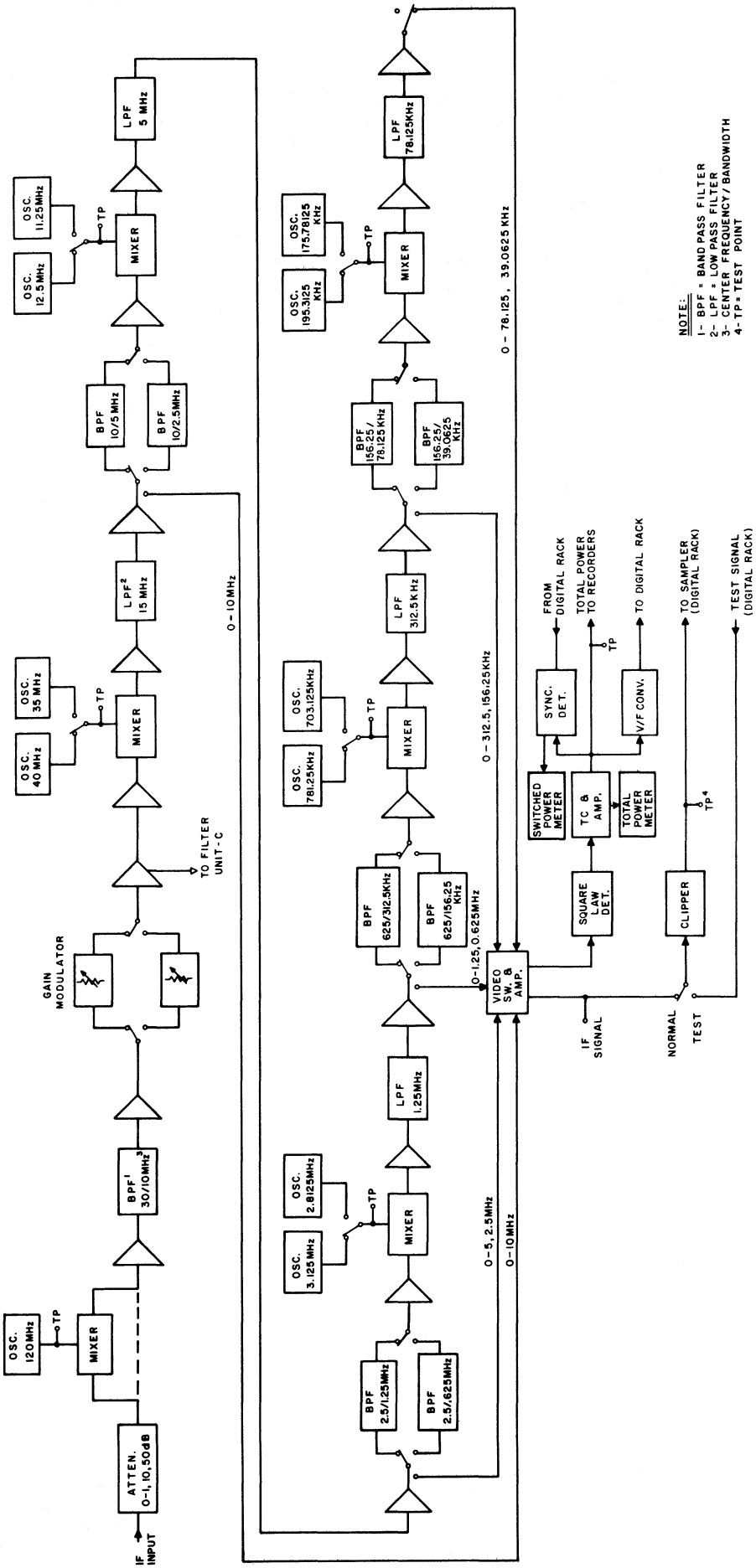
III. IF Filter System

General Description

The IF Filter System receives one or two IF signals from the front-end box, provides filtering of these signals to establish the desired bandwidth, converts them to a lower frequency and clips the signals in preparation for digital processing. The system also includes associated equipment such as gain modulators, total power detectors, synchronous detectors, voltage-to-frequency converters and switch drivers for front-end and noise tube switching.

There are three channels of IF processing equipment in the system. These are housed in separate slide-out drawers and are designated as IF Filter Units, A, B, and C. In the parallel mode of operation, Units A and B each feed 192 correlation channels in the digital rack and Unit C feeds 29 channels. In the series mode of operation, Unit A feeds 384 channels and Unit C feeds 29 channels, as in the parallel mode.

A block diagram of IF Filter Unit A or B is shown in Figure 3; a photograph of the front-panel controls is shown in Figure 4. Units A and B contain a full set of filters permitting independent selection of any one of nine bandwidths from 39.0625 kHz to 10 MHz. Unit C has a bandwidth range from 625 kHz to 10 MHz and receives its input signal from Unit A or B. The input selection is made by a cabling change on the back of the drawer C. Cable B connected to "IF Input" means C is fed from B; cable A connected to "IF Input" means C is fed from A. The input signal for Unit C is taken from a point in one of the other drawers after the attenuators and gain modulator so that these adjustments affect both drawers. Units A, B and C contain square law detectors and synchronous detectors for obtaining total power and switched power readings. These signals are available for recording at the top of the rack.



CORRELATION RECEIVER MODEL II
IF FILTER SYSTEM

Figure 3

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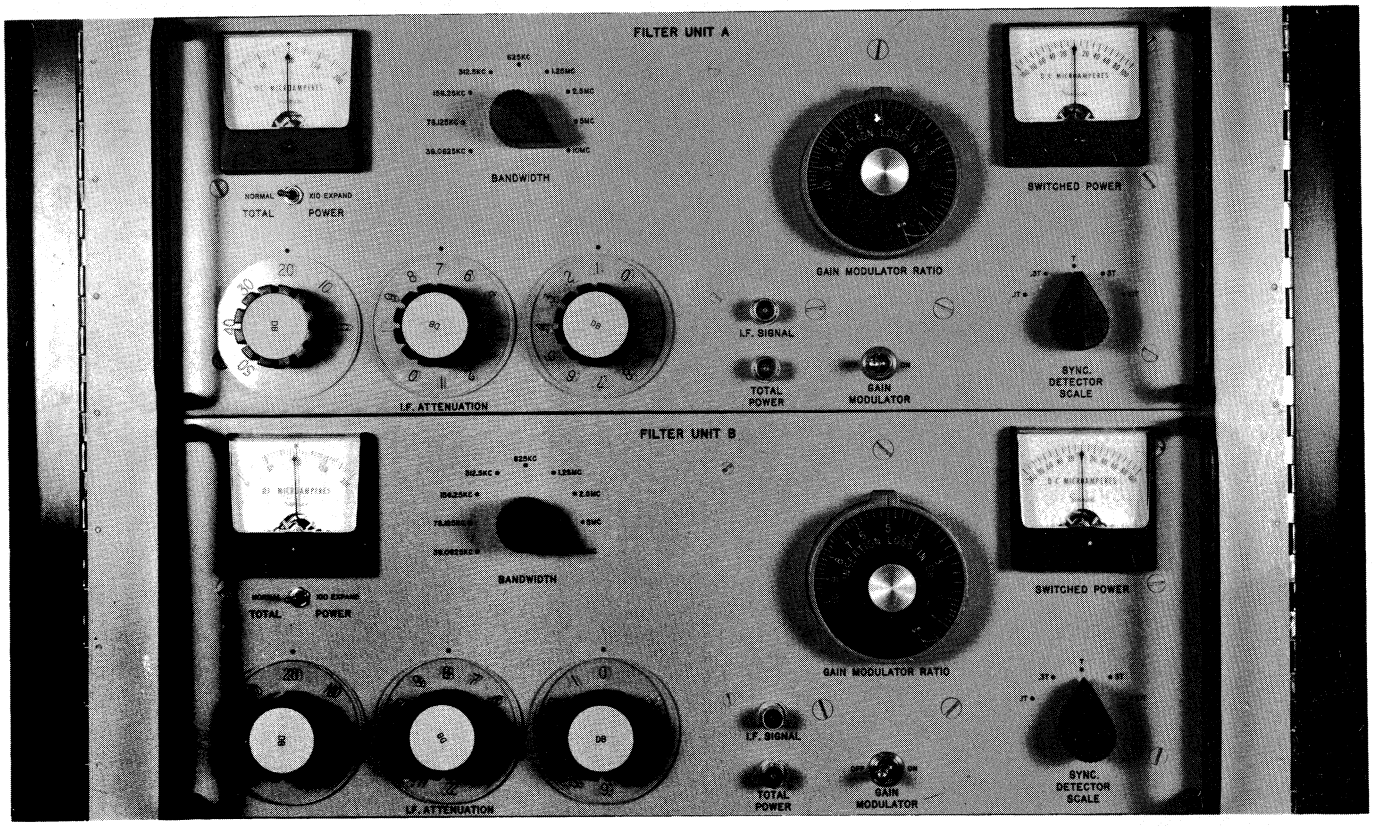


Figure 4 — Front-panel controls of IF Filter Units A and B. In normal operation the IF Attenuation controls are used to center the left-hand (Total Power) meter while the Gain Modulator Ratio control is used to center the right-hand meter (Switched Power). Neither control setting is critical to proper operation.

The main signal output of the three filter units is a spectrum located between zero and a frequency equal to the bandwidth selected. These signals are fed to clippers in a fourth drawer and then to the digital rack for sampling and processing. A parallel signal path through square law detectors and voltage-to-frequency converters provides an output frequency proportional to total power for counting and recording on magnetic tape.

The digital rack furnishes switching signals to the filter rack to operate the gain modulators, synchronous detectors and for developing the drive signals for the front-end and noise tube switches. These drivers are similar to those used in the NRAO Standard Receiver. The noise tube driver is for a diode switch and the front-end drivers are for diode and/or ferrite switches.

Operational Description

The level of the IF inputs must be greater than -50 dBm for 10 MHz bandwidth. This level is for the most sensitive arrangement in the input circuits of the filter units and provides an input signal-to-internal noise ratio of about 26 dB. The signal levels are controlled by step attenuators at the input. Adjustments are made to set the total power meter reading to approximately 100 (mid-scale) giving one volt output for recording. This setting places the level at optimum for the square law detector though offsets up to ± 2 dB should give negligible error.

The input center frequency is normally 30 MHz. A mixer can be added following the attenuators to permit operation at 150 MHz. The oscillator for this mixer is at 120 MHz so that the spectrum is not reversed as a result of changing IF frequency. The gain modulator consists of two variable attenuators of the same type. The one exposed on the front panel is in the circuit when the front-end switch is in the reference position. A synchronous detector has been provided primarily for use in adjusting the gain modulators. Outputs are provided at the top of the rack for recorders.

The chain of filters and mixers shown in Figure 3 provide the bandwidth selection and convert the spectrum to a frequency range between zero and the bandwidth selected. Low gain amplifiers are used between mixers and filters to correct for insertion losses, power loss due to bandwidth reduction and to provide an accurate source and load impedance for the filters. The mixer oscillators are oven controlled with a stability better

than one part in 10^7 per day for frequencies of 2.8 MHz and above, one part in 10^6 for the 781 and 703 kHz, and 5 parts in 10^6 for the 195 and 175 kHz oscillators. The frequency offsets due to drifts in all of these oscillators will usually be less than 100 cps and the drift will be less than 15 cps per day. For observations requiring very high frequency accuracy, the frequencies can be monitored through rear-panel jacks.

The oscillator frequencies have been chosen so that a signal appearing at exactly 30 MHz or 150 MHz at the IF input will appear in the center of the spectrum produced by the computer. This "center" occurs in spectral point 192 in the 384 channel mode, point 96 in the 192 channel mode, and midway between points 14 and 15 in the 29 channel receiver. (It is assumed that the spectral points are numbered from 0 thru 383, 0 thru 191, and 0 thru 28.) The frequency spacing, δf, between spectral points, is given in Table 1.

The spectrum is inverted by each mixer in the IF Unit so that bandwidths of 10, 1.25, 0.625, 0.078, and 0.039 MHz have inverted spectra when correlated. However, the DDP-116 computer corrects the inversion so that all spectra are recorded with increasing IF frequency corresponding to increasing point number or left-to-right on the CRT display. The correspondence to RF frequency will depend on whether the first LO is above or below the line frequency.

The square law detector output is amplified to a one volt nominal level and provided on the front panel and at the top of the rack for monitoring or recording total power. A ten times output with offset is also available for recording. Synchronous detector outputs of ± 10 V full scale are provided. The IF signal jacks on the front panels may be useful when strong interference is suspected. The spectrum at this jack is located at "video" frequency.

Switch drivers for the front-end and noise tube switches are located below the filter drawers. A mode control switch for each driver permits locking the switches in either position or choosing the modulation signals to be used. The inverted positions give a phase reversal of the switching signals. The noise tube switch has both continuous and interrupted modulation. Continuous modulation is similar to the front-end switching signal. Interrupted modulation provides noise tube switching during one dump period and noise tube off during the next period. The switching rates of one, five, or ten cycles per second and dump times of one or ten seconds are determined by switches in the digital rack. Reference should be made to the section on the digital system for further discussion of these and other switches affecting system operation.

Clipper test switches permit feeding test frequencies through the clippers to the digital rack for troubleshooting. The frequency selection of the test signal is made in the digital rack. The position of these and all other pertinent switches and attenuators in both racks is monitored and automatically recorded on magnetic tape. One exception is the gain modulator attenuator settings which cannot be easily monitored.

Input and Output Connections

IF Inputs A and B

Feed Filter Units A and B
Center frequency - 30 or 150 MHz (internal changes required when changing center frequency).
Level — Minus 50 dBm or greater per 10 MHz bandwidth.

Sw. Monitor

Pins A thru F provide for monitoring up to six remotely located switches.

NT Signal

Noise tube logic signal — Zero volts for noise tube off and -6 V for noise tube on.

Total Power X1 A, B and C

Level — 1 V open circuit.
Source impedance — 2000 ohms.
Operating range — 0.5 to 2 V for square law detector error less than 3%.

Total Power X 10 A, B and C

Level — Zero volts nominal for a total power X1 level of one volt.
Source impedance — 2000 ohms.
Operating range — Plus and minus 10 V maximum for +2 and 0 V, respectively, on total power X1.

Synchronous Detector A, B and C

Level — Zero volts nominal for a balanced receiver.
Source impedance — 2000 ohms.
Operating range — ± 10 V maximum.

X-Tal A

Front-end diode switch driver output signal.
Voltage range — 0 to ± 20 V.
Current range — 0 to 0.5 A.
Source impedance — Less than 30 ohms.
Connections — Pin A positive for signal, pin B negative for comparison, alternately; pin C common return; pin D, rack ground.

X-Tal B

Noise tube diode switch driver output signal.
Characteristics same as X-Tal A driver.

Ferrite

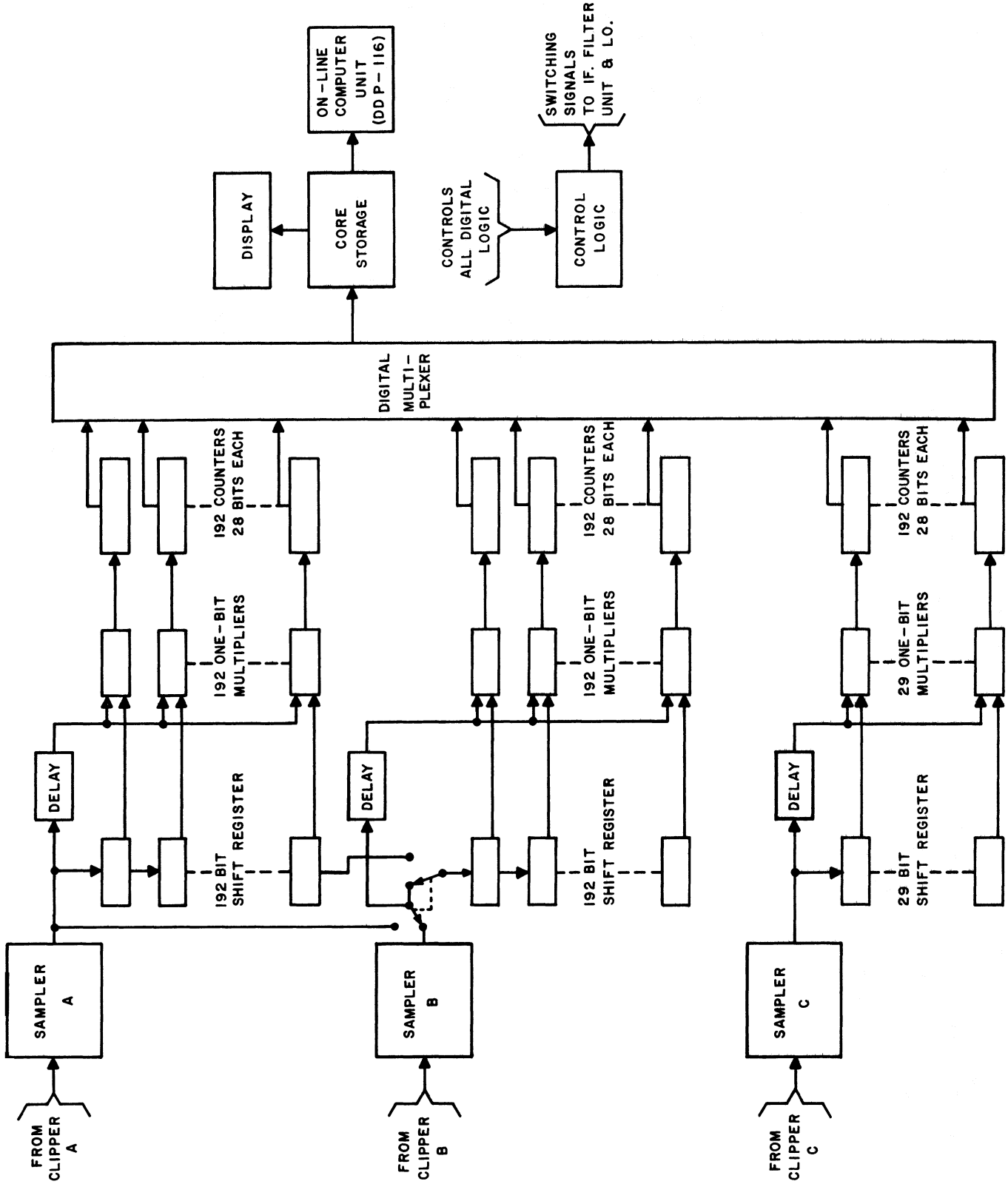
Front-end ferrite switch driver output signal.
Voltage range — 0 to 100 V.
Current range — 0 to 0.9 A.
Source impedance — Adjustable 50 to 800 ohms.
Connections — Pin A, comparison side; pin B, signal side; pin C, return for center tapped coils; pin D, rack ground.

IV. Digital Unit

Reference should be made to the block diagram of Figure 5. The clipper output, which has been previously described as a rectangular waveshape containing the frequency information of the original received signal, is sampled at a rate equal to twice the filter bandwidth. The sampler provides a compatible digital output which is synchronized to the digital system clock.

The sampled data is continuously stored in a 192 bit shift register which is updated at every clock (sample) pulse. Each shift register stage feeds a one bit multiplier. The other input to the multiplier is the "present" (latest) data out of the sampler. This provides a correlation comparison between the present sample and the previous 191 samples, each spaced τ seconds behind the adjacent sample; where τ is the sampling period.

If the two samples sent to a multiplier correlate, the multiplier provides a 1 to the associated counter; if not a 0 is provided. After the appropriate integration time the counters represent 192 points on the autocorrelation curve of the integrated signal.



BLOCK DIAGRAM
DIGITAL UNIT

Figure 5

The first channel always correlates, as it multiplies the present sample times itself. This provides a record of the number of sample pulses used during one integration period. In terms of the NRAO Autocorrelation Receiver Model I, this is what was referred to as $2V_o$.

The digital unit keeps the signal and reference data in separate memory locations of its core memory until dump time (every second or every 10 seconds), at which time the signal and reference data for all channels are sent to the on-line computer. Also sent to the computer are the signal and reference total power measurements for the three receivers. All knob positions are then sent to the computer. The knob positions sent to the computer are determined in the last half switching cycle prior to dump time.

There are 28 bits in each autocorrelation counter. The eight least significant bits are discarded prior to transmittal of the data to the computer. These eight bits are equal to or less than the RMS variations, and thus nothing is lost. There are 20 bits in the total power counters and they are all transmitted to the computer. A detailed description of data transferred to the computer is given in Appendix I.

The digital rack is an RFI shielded rack to prevent transmission of the many signals generated by the digital logic. Therefore, except to change knob positions or to service the instrument, the front and rear doors should always be closed securely.

The digital unit contains approximately 3000 integrated circuits and utilizes very compact construction techniques to allow operation at a clock frequency of 20 MHz. A photograph of a typical circuit card is shown in Figure 6.

The interior controls in the digital unit are shown in Figure 7. Most of these control settings cannot be changed without changing the DDP-116 program and thus should not be changed during normal operation. A brief explanation of the internal controls and the digital display is as follows:

Dump Period

The Dump Period is the integration time in the correlator before dumping data into the computer. Values of 1 second or 10 seconds are allowed; the usual setting is 10 seconds.

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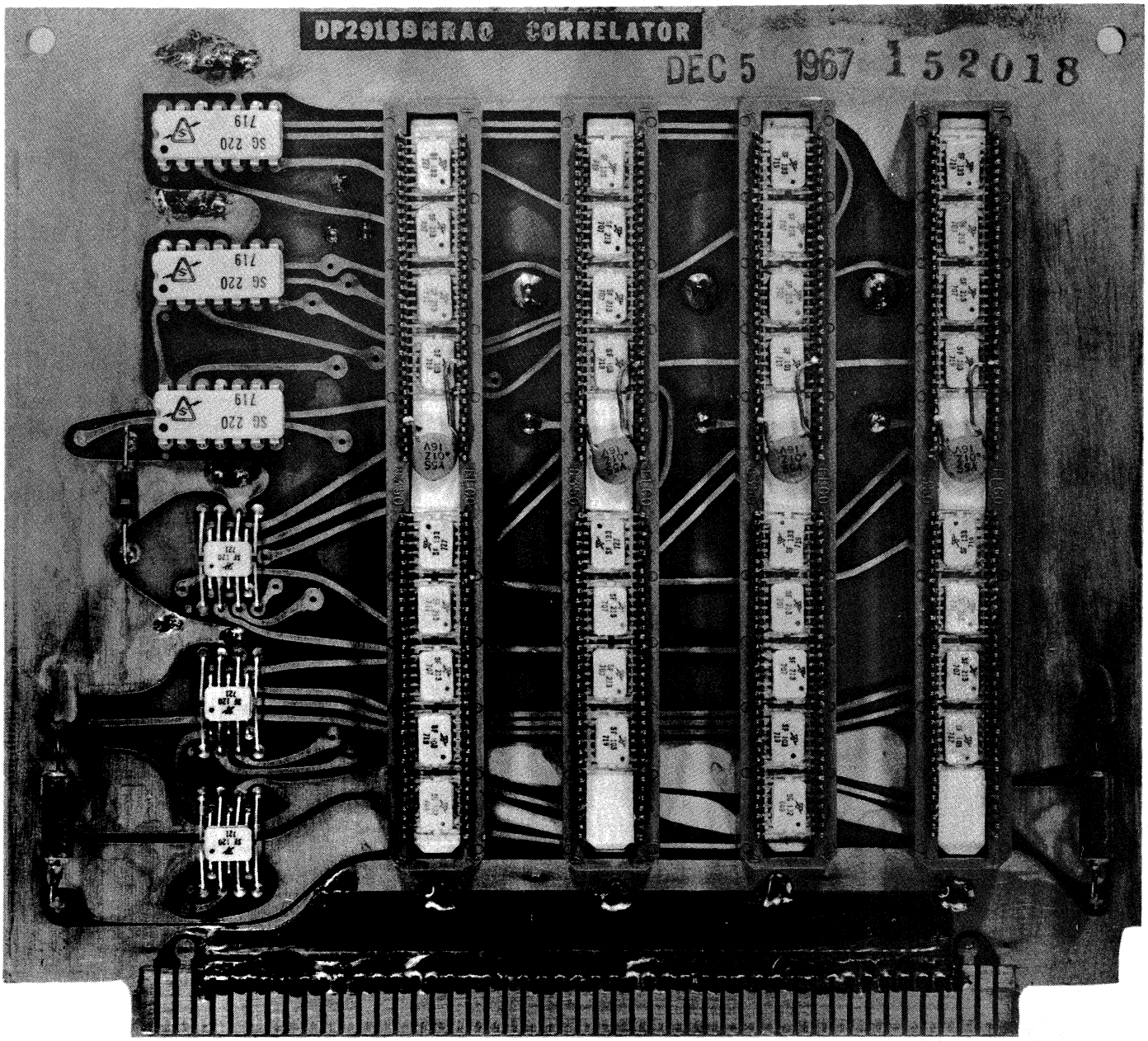

Figure 6 — Typical circuit card in the correlator. Integrated circuit DTL logic is used at clock rates of up to 20 MHz. The 4 stripes on the card are a type of multilayer wiring which allows a high density of circuits on a single card.

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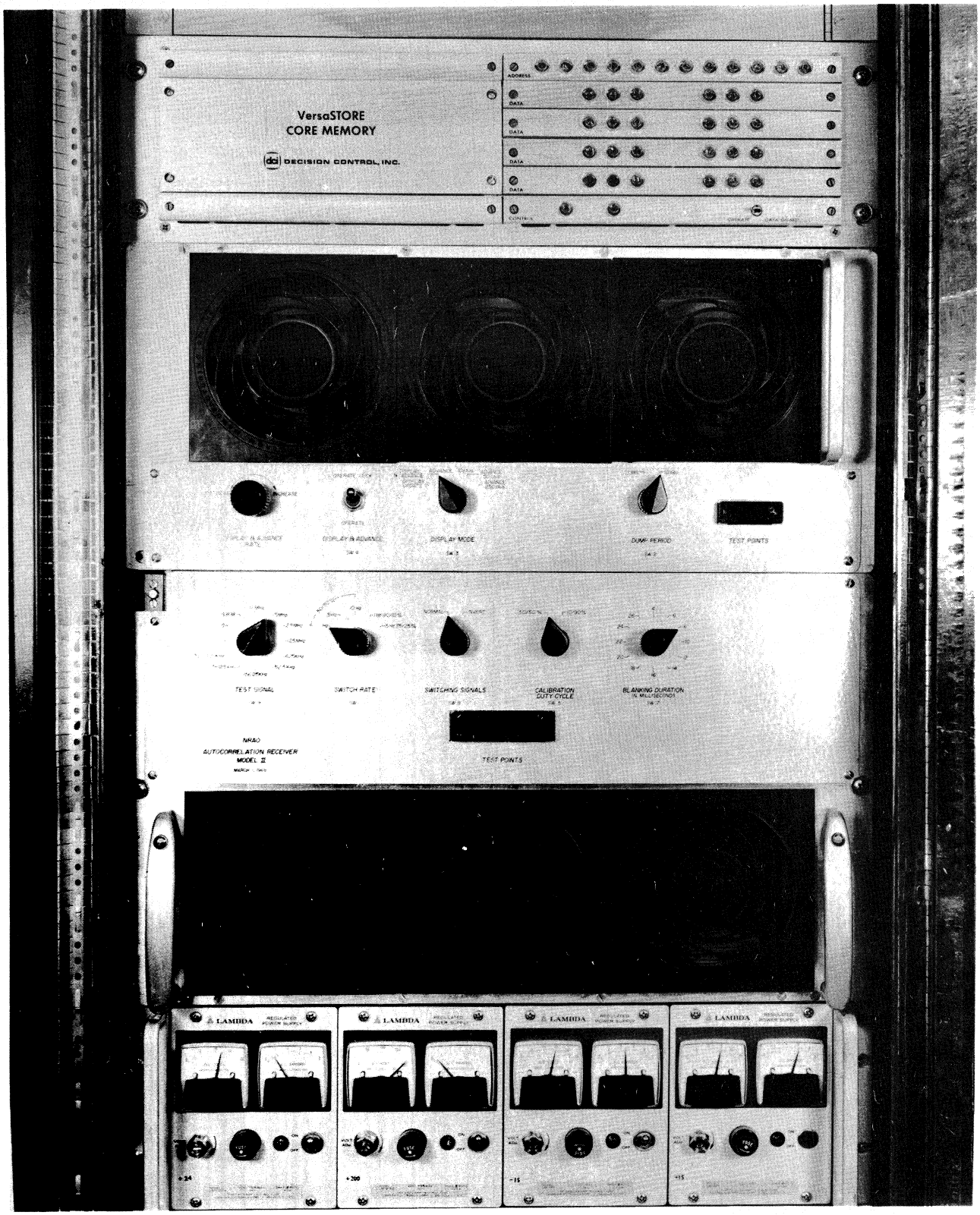


Figure 7 — Interior of digital cabinet. The controls in this cabinet are not adjusted in normal use.

Switching Rates

Switching rates between 1 Hz and 10 Hz can be selected. The signal/reference duty cycle can also be changed. The allowed combinations of switch rate and duty cycle are:

1 Hz — 50%/50%
5 Hz — 50%/50%
10 Hz — 50%/50%
1 Hz — 90%/10%
5 Hz — 75%/25%

As an example, "1 Hz — 90%/10%" means that 0.9 second is spent on signal and 0.1 sec is spent on reference. This mode will improve sensitivity by approximately a factor of 2 if the reference data is integrated in the computer 100 times longer than the signal data. The usual setting is "1 Hz — 50%/50%".

Noise Tube Duty Cycle

In normal operation the noise calibration signal is automatically turned on for every other dump period (50%/50%) or for every tenth dump period (10%/90%). When the noise calibration signal is on, it is not on continuously — it is modulated so that it is on during the signal period and off during the comparison period. The usual setting is 50%/50%.

Blanking Time

Blanking time is a "dead" time at the beginning of each signal or reference period. A small amount of blanking time is needed to clear various registers in the correlator. A longer blanking time can be switch selected to allow front-end or LO switching transient to die out of both analog and digital portions of the system. The allowed blanking time is 4 to 26 ms in steps of 2 ms.

The greater the blanking time, the less the integration time. At 1 Hz switching rate this is an insignificant factor, but at 10 Hz switching rate it becomes important, for the maximum blanking time — 26 ms — can cut the integration time to 24 ms. In this case the integration time becomes less than half the total time available.

To determine the minimum blanking time required use the equation:

$$\text{Minimum blanking time} = X + (Y)\ \frac{1}{(BW)}$$

X = switching time of slowest switch in system which affects the received signal. This is usually the gain modulator switch which is 6 ms.

Y = 100 when in parallel operation and 200 when in series operation.

BW = bandwidth.

The next even value above the one obtained by the formula should then be used as a minimum.

Display

A description of the displays and associated knobs follows:

Channel Data: Indicates data obtained for a particular channel during the previous dump period.

Channel Number: Indicates number of channel whose data is being displayed.

LAMP-DU: Data/Update — Whenever this lamp is on, the channel data information is updated every dump time.

LAMP-CD: Computer Data — This lamp goes on as soon as the data is available for the computer at the beginning of each dump period. As soon as the computer has removed the data, the light goes out. A continuously burning light indicates that the computer is not taking data. If the cable between the Digital Unit and the Computer Unit is disconnected, the light will act as though the computer is removing data.

LAMP —+24 V: +24 volt power supply on-off indicator. +24 volts used on clock crystal oscillator circuit, lamps, and relays.

LAMP — +5 VB: +5 volt power supply on-off indicator. +5 volt B is used on the lower half of the correlator chassis.

LAMP — +5 VA: +5 volt power supply on-off indicator. +5 volt A is used on the upper half of the correlator chassis.

LAMP S-R/I: Signal-Reference Integration. Light on indicates signal is being integrated. Off indicates reference being integrated. This assumes first half of each switching cycle is signal.

LAMP S-R/D: Signal-Reference Display. Light on indicates the channel being displayed is signal data. Light off implies reference. This assumes first half of each switching cycle is signal.

LAMP — -15 V: -15 volt power supply on-off indicator. -15 volts is used on clock amplifiers and sampler circuits.

LAMP — +15 V: +15 volt power supply on-off indicator. +15 volts is used on clock amplifiers and sampler circuits.

LAMP — -18 V: -18 volt and -6 volt power supplies on-off indicator. -18 and -6 volts are used on the input and output level converters.

LAMP — NT: Noise Tube. Light on indicates noise tube on.

LAMP — DT: Dump Time. Light goes off at beginning of dump period. Light goes on when dump period is half over.

KNOB — Light Test: Clockwise rotation turns all lamps except power supply indicators on.

KNOB — Display and Advance Rate: When the Display and Advance (Sw. 4) knob is in the Display and Advance position, this knob controls the rate of advancing from one channel to the next. The rate varies from approximately 0.8 Hz to 3.5 Hz.

KNOB — Display Mode (Sw. 3):

Display Update — Channel number remains constant. Data display is updated at every dump time.

Display & Advance — Channel is advanced at rate determined by Display & Advance Rate knob. As each new channel number appears the data display changes to show the data in that channel.

Advance 10 Ch/s, 50 Ch/s, and 250 Ch/s — Advances the channel display at the rate indicated. The Channel Data Display is inoperative.

TOGGLE SWITCH — Display and Advance (Sw. 4): Up is a locked position. Down is a spring return position. If the toggle is up or down, the Display Mode Knob (Sw. 3) is activated for all positions except Display Update. Display Update does not require the use of this toggle switch.

Testing

Square waves can be sent into the clippers by positioning the desired test toggle switch on the IF filter rack and choosing the desired frequency on the Test Signal Switch (Sw. 9) on the digital rack.

The crystal oscillator clock frequency can be checked by disconnecting the test signal cable between the digital rack and the IF-filter rack — top of the rack. Put the test signal switch on 10 MHz and feed the test output from the digital rack to a stable counter. Multiply the reading by 2. An error of Δf in this oscillator causes an expansion of the frequency scale so that a point at one end of the spectrum is shifted by $\Delta f \cdot B/20$ where B is the spectrum bandwidth in MHz.

V. Computer Processing

The autocorrelation receiver is designed to interface with the Honeywell DDP-116 computers at the NRAO 140-foot and 300-foot telescopes. The computer can also be used for antenna pointing simultaneously with the autocorrelation processing; an executive program exists in the computer for this time sharing operation.

Several different autocorrelation processing programs are anticipated. The contents of this section is general information which should apply to all of these programs.

Computer-Correlator Conversation

The transfer of data from the correlator to the computer is initiated by an interrupt (a break in the normal computer program sequence). The computer responds to the interrupt by transferring the data for the previous correlator dump period into the computer memory. A special multiplexer address is maintained for transfer of data from the correlator. This allows the computer to respond to other input devices and return to the same point. The input transfer requires between 60 and 200 ms, depending on the number of other tasks to which the computer responds.

Since the correlator employs two banks of memory — one for the current dump period and one for the previous dump period — the computer need not respond immediately to an interrupt. Operating with a 10 sec dump time, the computer may take as long as 10 sec to complete the input of data after the interrupt. This provides

for a convenient information buffer in case of special extraordinary conditions — a long queueing line of tasks to be performed by the computer or a tape re-write condition.

The interrupt marks the end of a correlator integration period and is synchronized with the timing generator. The timing generator is in turn synchronized with the Observatory clock. Thus, accurate timing information is available to fix the time associated with a given computer output.

Various tests are performed in the computer to insure the validity of information received from the correlator. Two major tests are made. The high order bit of the words to be transferred is alternately made one and zero by the correlator. The computer checks for this alternation of the high order bit. This procedure checks the validity of the transfers and prevents possible phasing errors. The time required for correlator input is checked. If it is excessive, an error condition is marked. Other tests are made to insure that data input does not overlap an interrupt, that no interrupt is missed and that all data is received. Receiver control indicators are also read by the computer and are compared against expected values.

Integration in the Computer

Some computer programs allow for integration in the computer of the counter data from the autocorrelator. In this case the computer memory serves as an extension of the counters. When this is done the broadband power counters are treated in a special way. Alternate readouts from the correlator are expected to include modulation of the noise tube during signal cycles (interrupted modulation). Thus a complete cycle of the system is not completed until two correlator dump times have passed. The signal counters in this case are integrated into alternate memory locations.

Data Processing

The autocorrelation data is broken into groups according to the receiver configuration. Signal and reference data within a given receiver are handled separately. In all cases four complete sets of calculations are carried out for: Receiver A Signal, Receiver A Reference, Receiver C Signal, and Receiver C Reference. If the parallel configuration is in use, a complete set of calculations is also carried out for Receiver B Signal and Receiver B Reference. The following steps are used:

1. Normalization — Each receiver has, as its first counter output, a count of the number of attempts at correlation. A series of calculations are carried out which are equivalent to the following: half the value of the first counter is subtracted from and divided into the counter value for each channel. This expresses the number of correlations for each channel as a fraction of the number of attempts. These numbers can range -1 to +1 although for most spectra they are less than .1 in magnitude.

2. Clipping Correction — The normalized readout, $\tilde{A}_i$, of the i^{th} channel is used to calculate A_i, the autocorrelation function of the i^{th} channel:

$$A_i = \sin\left(\tilde{A}_i \frac{\pi}{2}\right)$$

3. Fourier Transform — Each receiver has N channels for signal and N channels for reference (N = 29, 192, or 384) with normalized, corrected readouts A_i, i = 0, ... , N - 1. N spectral estimates, P_j, j = 0, ... , N - 1 are computed:

$$P_j = A_o + 2\sum_{i=1}^{N-1} A_i \cos\left(\frac{i\,j\,\pi}{N}\right)$$

This form of the Fourier transform gives the center of the band at a value j = N/2. Thus, for the series configuration, the spectral estimate corresponding to the center of the IF passband (30.0 MHz or 150.0 MHz) occurs in channel 192. The parallel case gives channel 96 and Receiver C is centered between channels 14 and 15. If channel numbers start with 1 rather than zero, these numbers should be increased by 1.

Spectra which are inverted in the IF system are re-inverted in the computer. Computer outputs are arranged so that increasing channel numbers correspond to increasing frequency in the IF.

Spectral Output

The signal and reference spectra can be separately observed in the bandpass display mode of the program. (Which one is displayed is either chosen through the typewriter, a sense switch, or by locking the receiver front-end in signal or reference.) This mode is mainly used to check for proper receiver operation.

The normal output display is the "quotient" spectrum which is computed from the signal transform, S_j, and reference transform, R_j, as follows:

$$Q_j = \frac{S_j - R_j}{R_j} \qquad j = 0, 1, \ldots, N - 1$$

The quotient spectrum is the normal switched output of a spectral-line radiometer corrected for gain variation (by division by R_j). It is proportional to the line temperature and may be converted to temperature units by multiplying by the system temperature. The appropriate system temperature is the sum of receiver noise temperature, antenna signal temperature, and 1/2 the calibration noise temperature, all averaged over the receiver bandwidth. This quantity can be computed from the total power (continuum) counters with calibration noise on and off. This computation is not performed in the DDP-116 computer but is carried out in the NRAO IBM-360 programs.

Tape Output

Programs which include the integration capability record both signal and reference spectra in double precision (30 bits) on magnetic tape. This allows off-line programs to make separate use of signal and reference. For example, a polarization switching experiment requires special processing in which the denominator of the quotients does not contain the line. In that case special measurements should be made to obtain the receiver bandpass.

Programs that do not include the integration capability record single precision (15 bits and sign) quotients on tape.

On-Line Output

Several types of on-line output are possible. They include quotients, signal spectra, and reference spectra (bandpass). Each may be displayed on a memory oscilloscope and may also be printed.

APPENDIX I

DETAILED DESCRIPTION OF DATA TRANSFERRED FROM CORRELATOR TO COMPUTER

Computer Words	Description	Format — DDP-116 Word Bits Note: All even numbered words have a "1" in word bit 1. All odd words have a "0" in word bit 1.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0 thru 825 — 413 Channels of Signal Correlation	Each channel is represented by a 20-bit word which is taken into the computer as two words.	1st word	1	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
		2nd word	0	0	0	0	0	0	0	0	0	0	0	2^{19}	2^{18}	2^{17}	2^{16}	2^{15}
826 Receiver A - Signal Power Counter 827 " " " " 828 Receiver B - Signal Power Counter 829 " " " " 830 Receiver C - Signal Power Counter 831 " " " "	Each counter is represented by a 20-bit word which is taken into the computer as two words.	Same as words 0 - 825.																
832 thru 1657 — 413 Channels of Reference Correlation	Each channel is represented by a 20-bit word which is taken into the computer as two words.	Same as words 0 - 825.																
1658 Receiver A - Reference Power Counter 1659 " " " " 1660 Receiver B - Reference Power Counter 1661 " " " " 1662 Receiver C - Reference Power Counter 1663 " " " "	Each counter is represented by a 20-bit word which is taken into the computer as two words.	Same as words 826 - 831.																
1664 Spare Word	For future requirements.		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1665 Receiver A - Bandwidth	4-bit word: 0 = 10 MHz 1 = 5 MHz 2 = 2.5 MHz 3 = 1.25 MHz 4 = 625 kHz 5 = 312.5 kHz 6 = 156.25 kHz 7 = 78.125 kHz 8 = 39.0625 kHz		0	0	0	0	0	0	0	0	0	0	0	0	2^{3}	2^{2}	2^{1}	2^{0}
1666 Receiver B - Bandwidth	Same as word 1665.	Same as word 1665.																
1667 Receiver C - Bandwidth	3-bit word: 0 = 10 MHz 1 = 5 MHz 2 = 2.5 MHz 3 = 1.25 MHz 4 = 625 kHz		0	0	0	0	0	0	0	0	0	0	0	0	0	2^{2}	2^{1}	2^{0}

Appendix I (continued) --

Computer Words		Description	Format — DDP-116 Word Bits															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1668	Receiver A - Attenuator	2 ea. 4-bit words, 1 ea. 3-bit words: 1 ea. 4-bit BCD word 0 = 0 dB 1 = 0.1 dB 2 = 0.2 dB 3 = 0.3 dB 4 = 0.4 dB 5 = 0.5 dB 6 = 0.6 dB 7 = 0.7 dB 8 = 0.8 dB 9 = 0.9 dB — Word A 1 ea. 4-bit BCD word 0 = 0 dB 1 = 1 dB 2 = 2 dB 3 = 3 dB 4 = 4 dB 5 = 5 dB 6 = 6 dB 7 = 7 dB 8 = 8 dB 9 = 9 dB — Word B 1 ea. 3-bit BCD word 0 = 0 dB 1 = 10 dB 2 = 20 dB 3 = 30 dB 4 = 40 dB 5 = 50 dB — Word C	1	0	0	0	0	2^3	2^2	2^1	2^0 (A)	2^3	2^2	2^1	2^0 (B)	2^2	2^1	2^0 (C)
1669	Receiver A - Gain Modulator	1-bit word: 0 = on 1 = off	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0
1670	Receiver B - Attenuator	Same as word 1668.	Same as word 1668.															
1671	Receiver B - Gain Modulator	Same as word 1669.	Same as word 1669.															
1672	Receiver C - Attenuator	4-bit word - same as section B of word 1668.	1	0	0	0	0	0	0	0	0	0	0	0	2^3	2^2	2^1	2^0

Computer Words	Description	Format — DDP-116 Word Bits															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1673 Gain Modulator and Synchronous Detector Phase	1-bit word: 0 = normal 1 = inverted	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0
1674 Series-Parallel Operation	1-bit word: 0 = series 1 = parallel	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0
1675 Switch Rate and Duty Cycle	3-bit word: 0 = 1 Hz, 1 = 5 Hz, 2 = 10 Hz } 50%-50% Duty Cycle 3 = 1 Hz — 90%-10% (Sig. Ref.) Duty Cycle 4 = 1 Hz — 75%-25% (Sig. Ref.) Duty Cycle	0	0	0	0	0	0	0	0	0	0	0	0	0	2^2	2^1	2^0
1676 Dump Time	1-bit word: 0 = 1 sec. 1 = 10 sec.	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0
1677 Blanking Time	4-bit word: 0 = 4 ms, 6 = 16 ms 1 = 6 ms, 7 = 18 ms 2 = 8 ms, 8 = 20 ms 3 = 10 ms, 9 = 22 ms 4 = 12 ms, 10 = 24 ms 5 = 14 ms, 11 = 26 ms	0	0	0	0	0	0	0	0	0	0	0	0	2^3	2^2	2^1	2^0
1678 Digital Test Signals	These words apply only when word 1679 is not all zeros. 1 ea. 4-bit word, 1 ea. 1-bit word: Word A - 4 bits: 0 = 10 MHz, 1 = 5 MHz, 2 = 2.5 MHz, 3 = 1.25 MHz, 4 = 625 kHz, 5 = 312.5 kHz, 6 = 156.25 kHz, 7 = 78.125 kHz, 8 = 39.0625 kHz } To Clipper (continued) --	1	0	0	0	0	0	0	0	0	0	0	2^0 (B)	2^3	2^2	2^1	2^0 (A)

Appendix I (continued) --

Computer Words		Description	Format — DDP-116 Word Bits																
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1678	Digital Test Signals (continued) --	9 = Logic - 0 - to Sampler Output Flip Flop 10 = Logic - 1 - to Sampler Output Flip Flop 11 = Shift Register Memory Test Signal Word B - 1 bit: Applies only when Word A is 11. 0 = Special Test Signal into Shift Register Memory for servicing purposes only. 1 = Standard Test Signal into Shift Register Memory																	
1679	Clipper Test Signal	3 ea. 1-bit words: Word A: 0 = normal 1 = test } Receiver A - Clipper Word B: 0 = normal 1 = test } Receiver B - Clipper Word C: 0 = normal 1 = test } Receiver C - Clipper	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0 C	2^0 B	2^0 A
1680	Front-End Switch	2-bit word: 0 = Modulated-Inverted 1 = Signal 2 = Reference 3 = Modulated-Normal	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2^1	2^0
1681	Noise Tube Mode	3-bit word: 1 = Continuous Modulation-Normal 2 = Continuous Modulation-Inverted 3 = Interrupted Modulation-Normal 4 = Interrupted Modulation-Inverted 5 = On 6 = Off	0	0	0	0	0	0	0	0	0	0	0	0	0	2^2	2^1	2^0
1682	External Sense Switches	6 ea. 1-bit words: Each bit can be a one or zero to indicate the condition of a switch external to the correlator. For example, a noise tube level switch indicating 10^0 or 100^0.	1	0	0	0	0	0	0	0	0	0	2 F	2^0 E	2^0 D	2^0 Word C	2^0 B	2^0 A

Appendix I (continued) --

Computer Words		Description	Format — DDP-116 Word Bits															
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1683	Noise Tube Duty Cycle and On-Off Indicator	2 ea. 1-bit words: 0 = 50%-50% 1 = 90%-10% (Sig. Ref.) } Word A 0 = Noise Tube Off 1 = Noise Tube On } Word B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2^0 B	2^0 A

APPENDIX II

SPECTRAL OUTPUT WITH IF NOISE GENERATOR INPUT

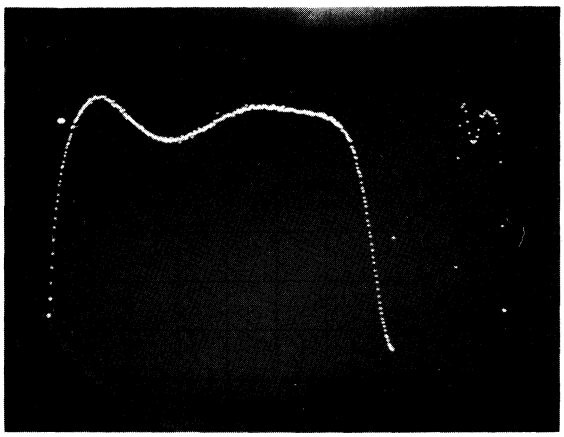
The photographs on the following pages show the bandpass and quotient spectra measured with the internal IF noise generator connected to the inputs of receivers A, B, and C. The same results should be obtained if an unswitched front-end with flat bandpass is connected to the receiver inputs. The noise on the quotient spectra agrees with theoretical predictions.

Bandpass Spectra

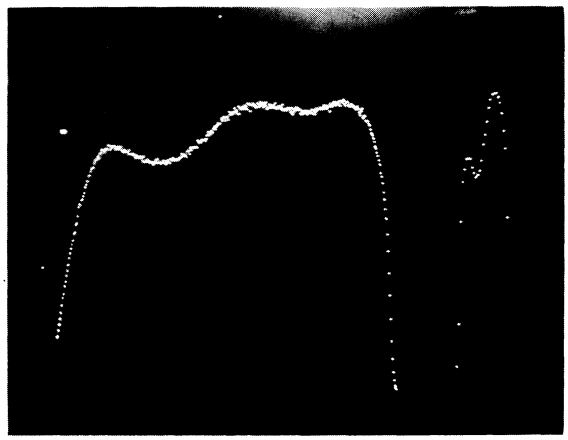
Vertical Scale 0.2 (x System Temperature) per cm

Integration Time - 10 Seconds

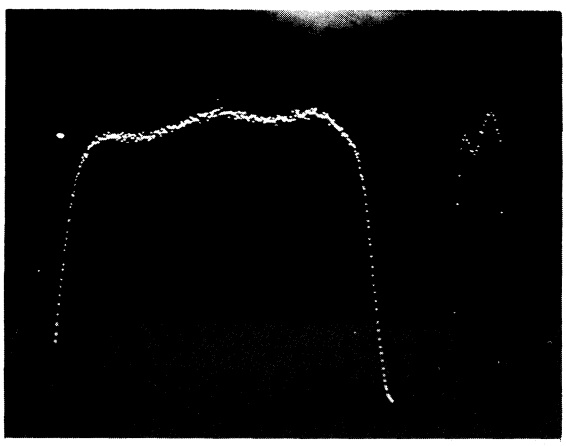
Serial Mode



A - 10 MHz C - 10 MHz

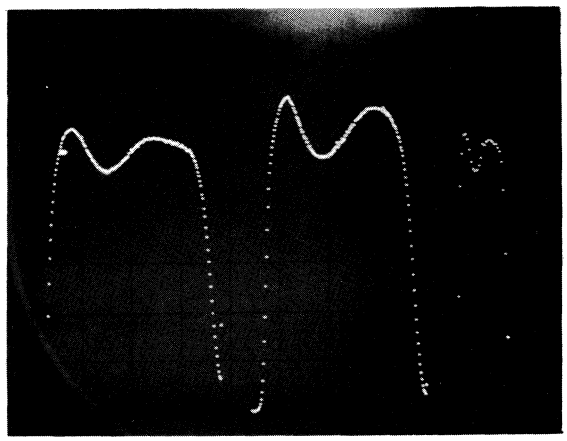


A - 5 MHz C - 5 MHz

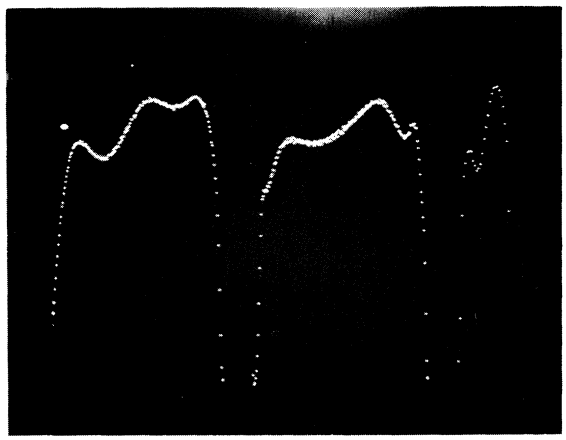


A - 2.5 MHz C - 2.5 MHz

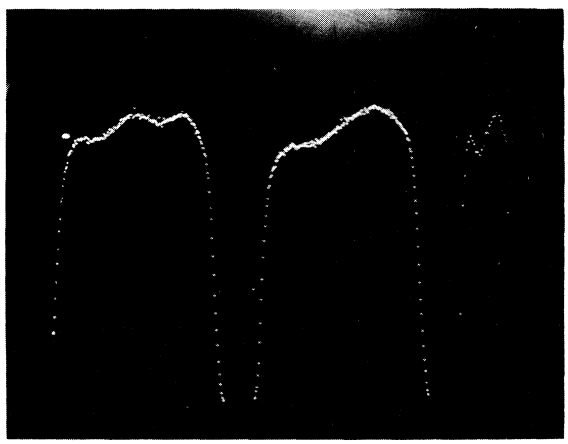
Parallel Mode



A - 10 MHz B - 10 MHz C - 10 MHz



A - 5 MHz B - 5 MHz C - 5 MHz



A - 2.5 MHz B - 2.5 MHz C - 2.5 MHz

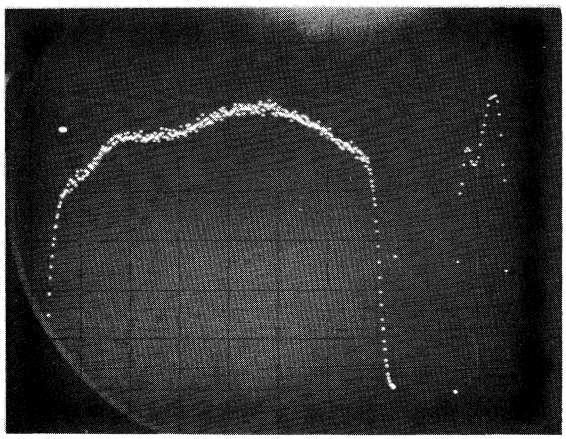
Bandpass Spectra

Vertical Scale 0.2 (x System Temperature) per cm

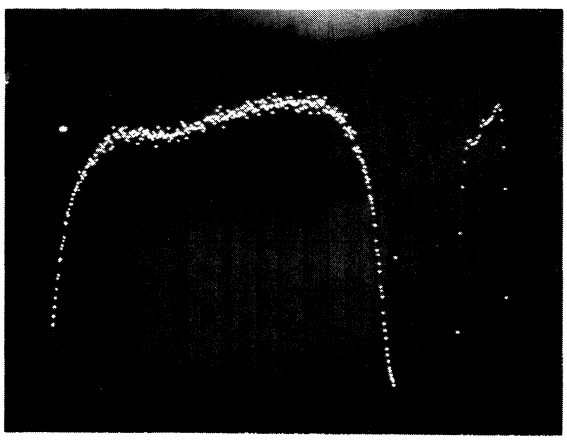
Integration Time - 10 Seconds

Serial Mode

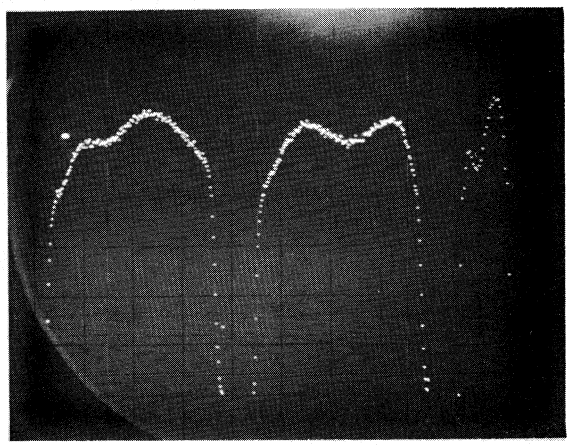
Parallel Mode



A - 1.25 MHz



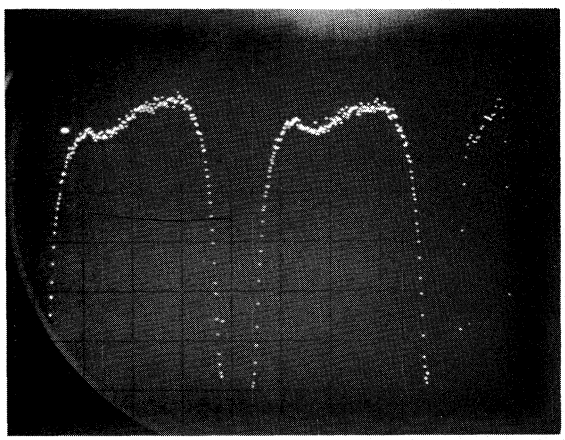
C - 1.25 MHz



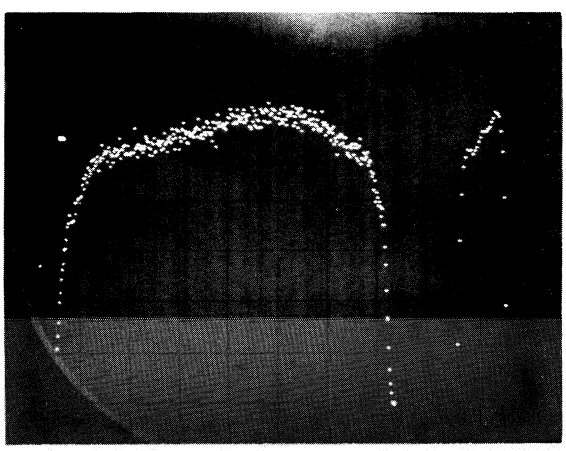
A - 1.25 MHz B - 1.25 MHz C - 1.25 MHz

A - 625 kHz

C - 625 kHz

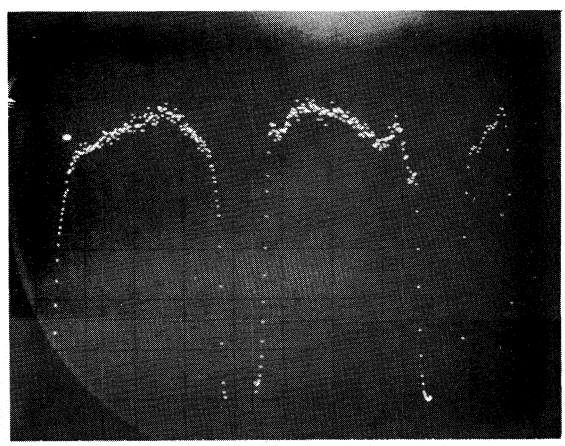


A - 625 kHz B - 625 kHz C - 625 kHz



A - 312 kHz

C - 625 kHz



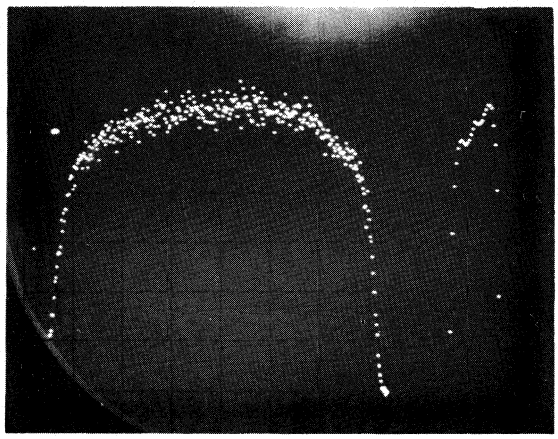
A - 312 kHz B - 312 kHz C - 625 kHz

Bandpass Spectra

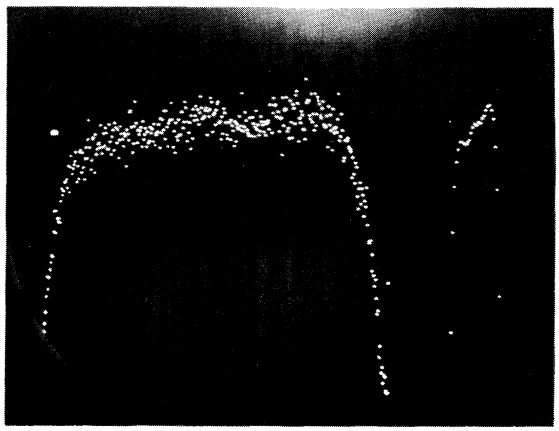
Vertical Scale 0.2 (x System Temperature) per cm

Integration Time - 10 Seconds

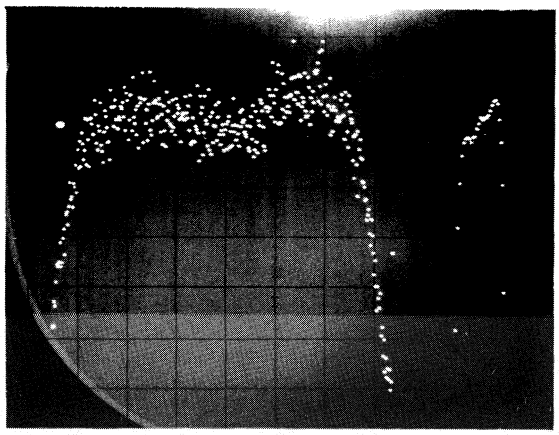
Serial Mode



A - 156 kHz C - 625 kHz

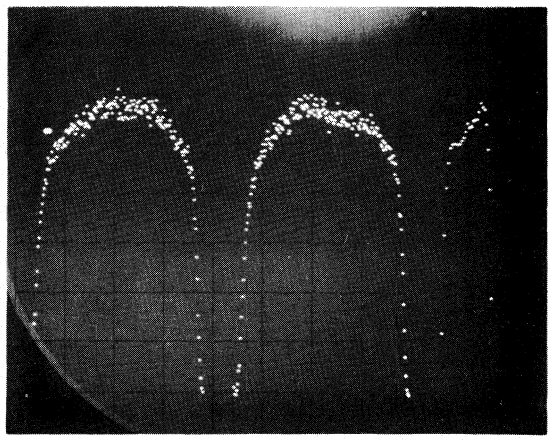


A - 78 kHz C - 625 kHz

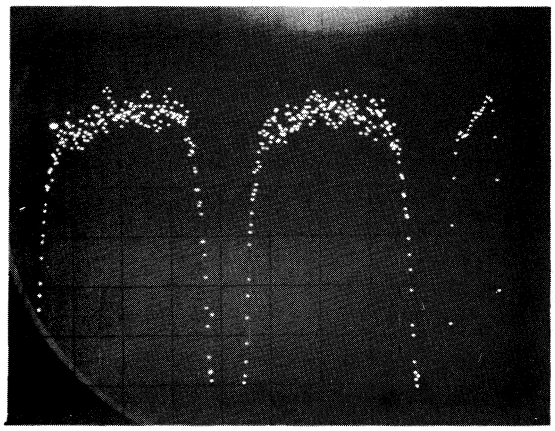


A - 39 kHz C - 625 kHz

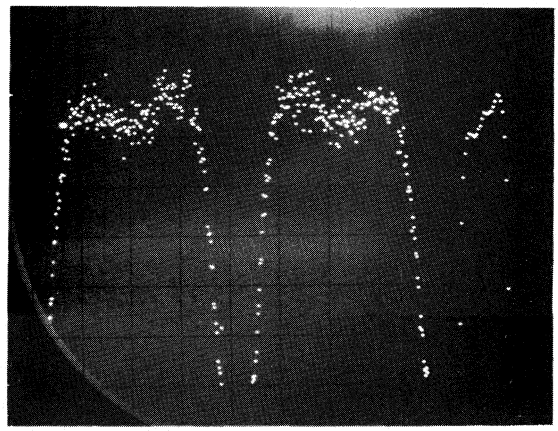
Parallel Mode



A - 156 kHz B - 156 kHz C - 625 kHz



A - 78 kHz B - 78 kHz C - 625 kHz



A - 39 kHz B - 39 kHz C - 625 kHz

Quotient Spectra

Integration Time = 40 Seconds

(Scale expressed as fraction of system temperature per cm)

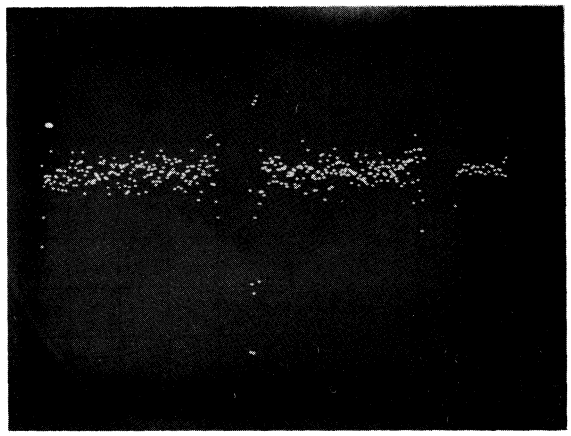
Serial

A - 10 MHz

C - 10 MHz

Scale 0.01/cm

Parallel

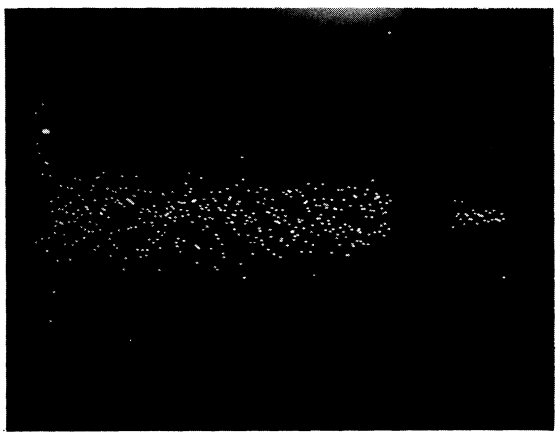


A - 10 MHz

B - 10 MHz

C - 10 MHz

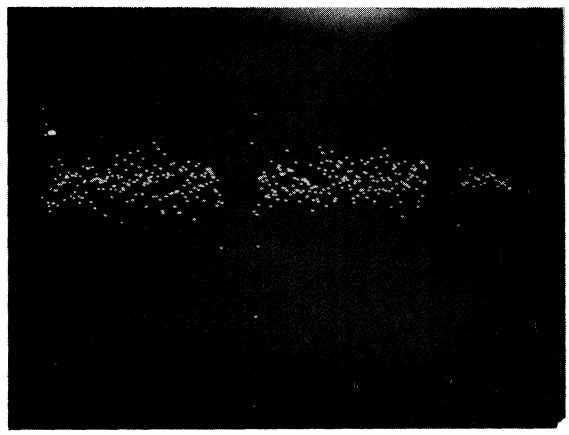
Scale 0.01/cm



A - 5 MHz

C - 5 MHz

Scale 0.01/cm

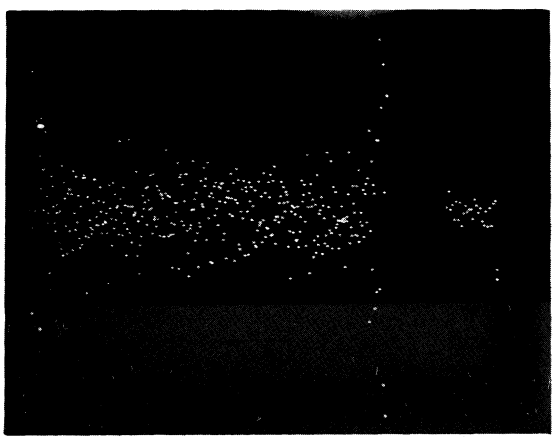


A - 5 MHz

B - 5 MHz

C - 5 MHz

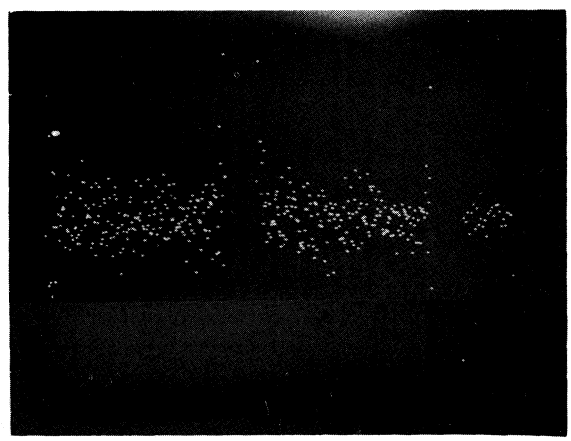
Scale 0.01/cm



A - 2.5 MHz

B - 2.5 MHz

Scale 0.01/cm



A - 2.5 MHz

B - 2.5 MHz

C - 2.5 MHz

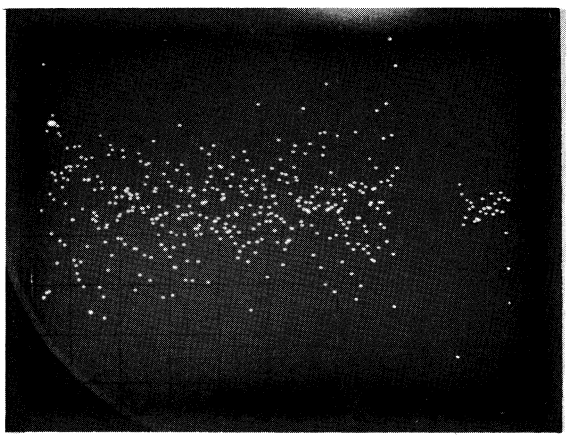
Scale 0.01/cm

Quotient Spectra

Integration Time = 40 Seconds

(Scale expressed as fraction of system temperature per cm)

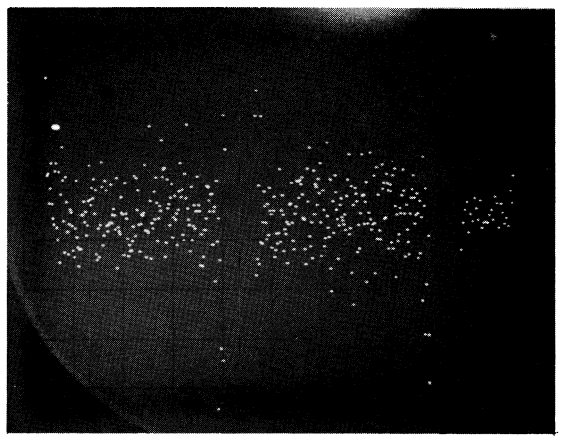
Serial



A - 1.25 MHz C - 1.25 MHz

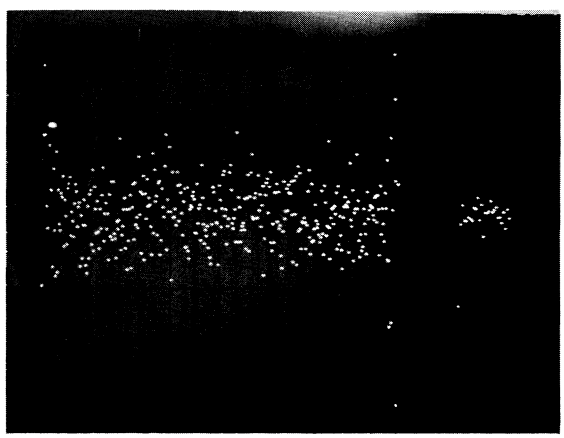
Scale 0.01/cm

Parallel



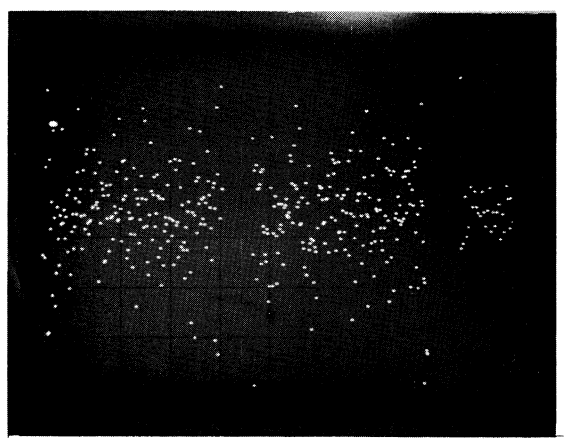
A - 1.25 MHz B - 1.25 MHz C - 1.25 MHz

Scale 0.01/cm



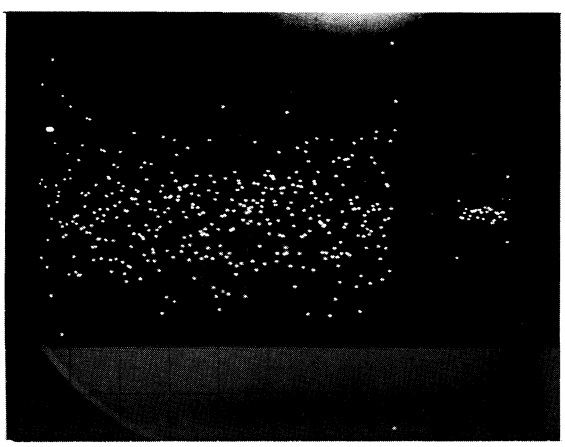
A - 625 kHz C - 625 kHz

Scale 0.02/cm



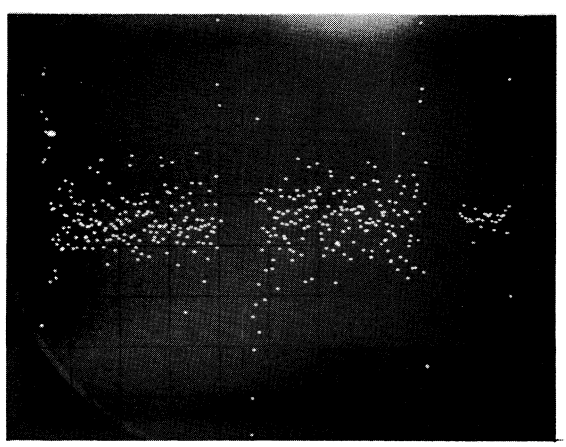
A - 625 kHz B - 625 kHz C - 625 kHz

Scale 0.01/cm



A - 312 kHz C - 625 kHz

Scale 0.02/cm



A - 312 kHz B - 312 kHz C - 625 kHz

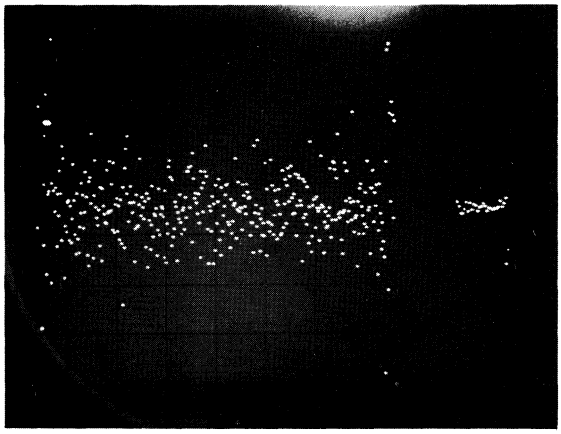
Scale 0.02/cm

Quotient Spectra

Integration Time = 40 Seconds

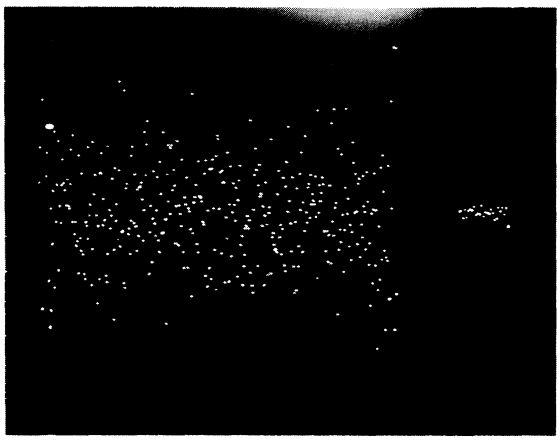
(Scale expressed as fraction of system temperature per cm)

Serial



A - 156 kHz C - 625 kHz

Scale 0.04/cm



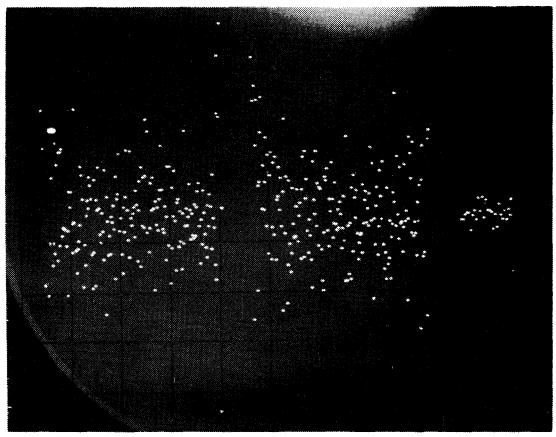
A - 78 kHz C - 625 kHz

Scale 0.04/cm

A - 39 kHz C - 625 kHz

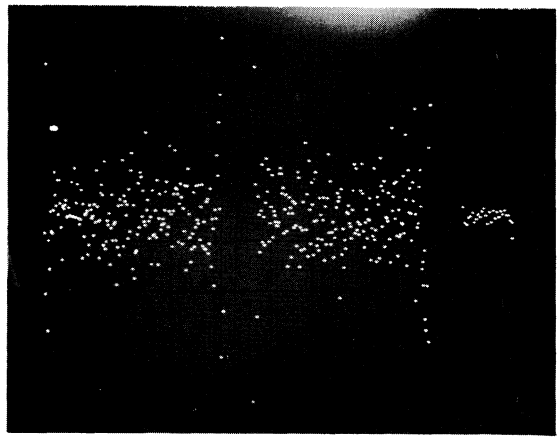
Scale 0.04/cm

Parallel



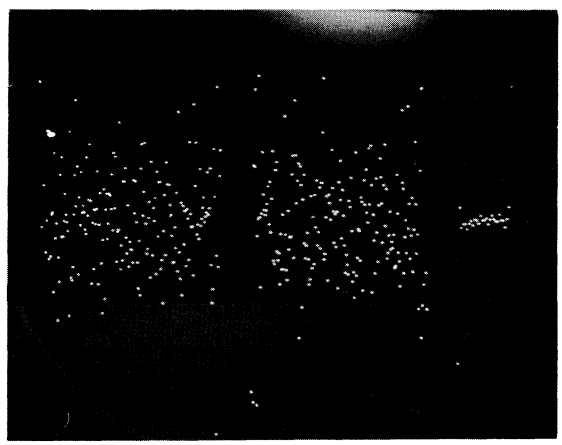
A - 156 kHz B - 156 kHz C - 625 kHz

Scale 0.02/cm



A - 78 kHz B - 78 kHz C - 625 kHz

Scale 0.04/cm



A - 39 kHz B - 39 kHz C - 625 kHz

Scale 0.04/cm