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# Extremely Low-Noise Amplification with Cryogenic FET's and HFET's: 1970-2004

Marian W. Pospieszalski

National Radio Astronomy Observatory Charlottesville, VA 22903

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#### Abstract

Improvements in the noise temperature of field-effect transistors (FET's) and, later, heterostructure field-effect transistors (HFET's) over the last several decades have been quite dramatic. In 1970, a noise temperature of 120 K was reported at 1 GHz and physical temperature of 77 K; in 2003, noise temperatures of 2, 8 and at 35 K were reported at 4, 30 and 100 GHz, respectively, for physical temperatures of 14 to 20 K. The paper reviews developments in this field and attempts to identify important milestones within the broader context of technological developments. Examples of experimental results obtained with different generations of FET's (HFET's) are compared with the model predications. Some gaps in our current understanding of experimental results are emphasized, and some comments on possible future developments are offered.

#### I. INTRODUCTION

The quest for ultra-low-noise reception is as long as the history of radio communication. A list of devices which at one time provided the lowest reported noise temperature in some frequency band is very long: vacuum tubes, crystal mixers, tunnel diode amplifiers, parametric amplifiers, solid-state masers, Schottky diode mixers, superconductor-insulator-superconductor (SIS) mixers, GaAs field-effect transistors (FET's) and heterostructure field-effect transistors (HFET's), hot electron bolometers (HEB's), *etc.* Okwit gives a very interesting historical review of the pre-1970's evolution of low-noise concepts and techniques [1]. Relevant information concerning developments in the 1960's and 1970's can also be found in two special issues of the *IEEE MTT Transactions:* one on *Noise* (September 1968) and the other on *Low Noise Technology* (April 1977).

Three of the low-noise devices mentioned in the previous paragraph, namely solid-state masers, SIS mixers, and HEB's, will operate only at cryogenic temperatures. Most other devices (with the exception of vacuum tubes!) have also been cooled to cryogenic temperatures for two main reasons: improvement in the device performance, usually due to the improvement of the electron transport properties, and reduction of the influence of thermal noise generated by parasitic elements [2], [4], [6].

Cryogenic cooling of receivers to reduce their noise temperature is especially important in satellite and space communication, and in radio astronomy. This is because the antenna noise is determined by celestial sources and the atmosphere. In the absence of strong celestial sources (Sun, Moon, planets, Cassiopeia, Cygnus, Taurus, Virgo, Orion, galactic plane) in an antenna beam, an antenna "looks" at a very cold sky: 2.725 K of the cosmic microwave background radiation modified by the presence of atmosphere [3]. The antenna temperature is typically one order of magnitude or more less than in terrestrial applications (300 K). Consequently, a receiver noise temperature typically would constitute a large part of a system noise temperature, and its reduction by cryogenic cooling offers a very effective way of improving receiver sensitivity.

In the early 1970's, the ultra-low-noise receiving systems for deep space and radio astronomy employed mainly solid-state masers, cryogenically-cooled parametric amplifiers (or converters) and Schottky diode mixers. At the end of that decade, advances in GaAs FET technology made the noise performance of GaAs FET amplifiers competitive with the performance of parametric amplifiers [5]. Also, a new mixing element, the SIS tunnel junction capable of almost quantum-limited detection, was developed [7]-[10]. In the 1980's and 1990's, FET amplifiers were gradually replaced by HFET amplifiers of different generations. The first generation was using AlGaAs/GaAs HFET's, the second generation AlGaAs/InGaAs/GaAs HFET's and the third AlInAs/InGaAs/InP

HEFT's [2], [4]. These amplifiers have become the low-noise technology of choice for frequencies up to W-band (3mm), although ruby masers are still sometimes used in Deep Space Network antennas at X- and K<sub>a</sub>-band frequencies [11]. At W-band frequencies, HFET receivers now compete in performance with SIS/HFET mixerpreamplifiers. At frequencies above 120 GHz up to about 1 THz, SIS mixers demonstrate the best noise performance. Above 1 THz, cooled Schottky diode mixers and HEB mixers provide the lowest noise temperatures [12].

Section II of this paper reviews noise models of FET's and HFET's and their experimental verification from the point of view of their application at cryogenic temperatures. Progress in the noise performance of cryogenic FET's and HEMT's from the first attempts at cryogenic cooling in 1970 until 1993 is addressed in Section III. This section covers the milestones demonstrated with FET's and two generations of HFET's, conventional and pseudomorphic, all based on GaAs substrates. Certain rather old results are interpreted from the point of view of theoretical understanding developed much later. Also, the issue of what makes a good cryogenic device is addressed, and certain gaps in our understanding of HFET properties at cryogenic temperatures are pointed out. Finally, Section IV covers developments from 1993 to the present. This period coincides with the introduction of InP HFET's into cryogenic receiver technology. Some thoughts on possible future developments are offered in Section V.

#### II. NOISE MODELS OF FET'S AND HFET'S AND THEIR EXPRIMENTAL VERIFICATION

The noise performance of field-effect transistors (FET's) was first modeled by A. van der Ziel [13] and has since been a subject of intensive study. Published studies of noise the properties of FET's (HFET's) may be divided into two distinctive groups. The first group, as a starting point of analysis, considers the fundamental equation of transport in semiconductors [13]-[22], [23]. Most papers in this category published over the years may be viewed as progressively more sophisticated treatments of the problem originally tackled by Van der Ziel [13], [14], [22]. Although the HFET's wafer structure is different than that of a MESFET, the methods employed in noise studies were basically the same [19], [21], [24] as those applied to MESFET's [17], [20], [24]. To the best of the author's knowledge, none of these models have been used to explain the performance of FET's at cryogenic temperatures.

The second group of published studies [25]-[35], [40]-[44] addresses the issue of what needs to be known about the device, in addition to its equivalent circuit, to predict noise performance. Until the 1990's, the most often used method was the semi-empirical approach originated by Fukui [25]-[27] in which relations between the minimum noise figure at a given frequency and the values of transconductance  $g_m$ , gate-to-source capacitance  $C_{gs}$ , and source and gate resistances  $r_s$  and  $r_g$ , are established (Fig. 1). A quantitative agreement may be obtained only after the proper choice of fitting factor [25], [26], [28] or fitting factors [29]. The extension of this approach to other noise parameters [26] results quite often in non-physical two-port [27]. The Fukui approach, although very widely used by device technologists, does not provide any insight into the nature of the noise-generating mechanism in a FET as the fitting factors do not possess physical meaning. Nevertheless, device technologists pursuing the goal of lowest-noise FET relied on the semi-empirical expression of Fukui [25], [26] relating the minimum noise temperature with the elements of an equivalent circuit of a FET:

$$T_{\min} \approx T_o K_f \frac{f}{f_T} \sqrt{g_m(r_g + r_s)}$$
(1)

where f is the frequency,  $T_o$  is the standard temperature 290 K,  $f_T$  is the intrinsic cut-off frequency,  $g_m$  is the transconductance,  $r_g$  and  $r_s$  are gate and drain parasitic resistance and  $K_f$  is the fitting factor, assuming values between 1.2 and 2.5 [24].

Over the years, the most referenced treatment of signal and noise properties of a MESFET is that published by Pucel *et al.* [17]. It quite often serves as a bridge between different approaches to noise treatment as many other results are compared to it or adopt similar computational techniques [19]-[21], [24], [26]. The method of Pucel *et al.* [17] calls for three frequency-independent noise coefficients P, R and C to be known in addition to small signal parameters of an intrinsic FET in order to determine four noise parameters at any given frequency. The model proposed by the author [33], [34] has been shown to describe very well the noise properties of FET's versus frequency, temperature and transistor bias [33]-[47]. The principle of this model is illustrated in Fig. 1 which shows the equivalent circuit of a FET chip with its noise sources.



Fig. 1. Equivalent circuit of a FET (HFET) chip. The parasitic elements are shown disconnected from the intrinsic chip. Noise properties of the intrinsic chip are represented by equivalent temperatures,  $T_g$  of  $r_{gs}$  and  $T_d$  of  $g_{ds}$ . Noise contribution of ohmic resistances  $r_s$ ,  $r_g$  and  $r_d$  are determined by physical temperature  $T_a$  of a chip.

Parasitic resistances contribute only thermal noise and, with knowledge of the ambient temperature  $T_a$ , their influence can easily be taken into account. The noise properties of an intrinsic chip are then treated by assigning equivalent temperatures  $T_g$  and  $T_d$  to the remaining resistive (frequency-independent) elements of the equivalent circuit  $r_{gs}$  and  $g_{ds}$ , respectively. No correlation is assumed between noise sources represented by the equivalent temperatures  $T_g$  and  $T_d$ . Consequently, in addition to elements of an equivalent circuit  $T_g$ ,  $T_d$  and  $T_a$  need to be known to predict all four noise parameters at any frequency, temperature, and bias in the frequency range in which 1/f noise and noise caused by the gate leakage current are negligible. For the detailed treatment, the reader is referred to the original papers. However, for the purpose of the discussion in this paper, it is useful to recall the approximate expressions for four noise parameters of an intrinsic chip:

$$R_{opt} \cong \frac{f_t}{f} \sqrt{\frac{r_{gs} T_g}{g_{ds} T_d}}$$
(2)

$$X_{\text{opt}} = \frac{1}{\omega C_{\text{gs}}}$$
(3)

$$g_n = \left(\frac{f}{f_t}\right)^2 \frac{g_{ds} T_d}{T_o}$$
(4)

$$T_{\min} \cong 2 \frac{f}{f_t} \sqrt{g_{ds} T_d r_{gs} T_g}$$
(5)

$$T_{\min} \approx \frac{f}{f_{\max}} \sqrt{T_g T_d}$$
 (6)

or

which are valid if

$$\frac{f}{f_t} \ll \sqrt{\frac{T_g}{T_d}} \frac{1}{r_{gs} g_{ds}}$$
(7)

where

$$f_{T} = \frac{g_{m}}{2\pi C_{gs}}$$
(8)  
$$f_{max} = f_{T} \sqrt{\frac{1}{4 g_{ds} r_{gs}}}$$
(9)

and  $R_{opt}$  and  $X_{opt}$  are the real and imaginary parts of the optimum source impedance,  $T_{min}$  is the minimum effective noise temperature of a chip,  $g_n$  is the noise conductance,  $f_T$  is the transistor cut-off frequency, and  $f_{max}$  is the maximum frequency of oscillations. Since the model's introduction in 1988, its validity has been verified by a number of researchers in the field, among those are works by researchers from the Fraunhofer Institut [41], [42] Ferdinand-Braun-Institut [43], [44], and the Chalmers University of Technology [45]-[47]. An example of a typical fit between measured and modeled noise parameters based on the authors own work [35] is shown in Fig. 2. A direct confirmation of the model's validity at cryogenic temperatures has been given in only two studies [33], [34], [47], although there have been a number of published paper demonstrating an excellent agreement between measured and modeled results for the amplifiers designed under the assumption of model validity [36]-[39], [47]-[54].



Fig. 2. Example of measured and model–predicted noise parameters of a sample MESFET. Points marked by "\*", "x", "o" and "+" are for T<sub>min</sub>, X<sub>opt</sub>, R<sub>opt</sub> and g<sub>n</sub>, respectively. Lines are for model prediction.

There are several important observations concerning the model's behavior. These are illustrated in Table I [34] and Fig. 3 [35], Fig. 4 [35] and Fig. 5 [48]. First, the equivalent drain temperature is linearly dependent on the drain current and, within measurement errors, a single value may be used for all devices having the same gate length, the same semiconductor structure and the same current density per unit gate width. Second, the equivalent drain temperature is usually not a strong function of the device ambient temperature, except for very

low drain current densities per unit gate width. Third, the equivalent gate temperature is lightly dependent on drain current and, within measurement errors, is equal to the ambient temperature of a device. This observation is clearly illustrated by the data of Table I (obtained for an AlGaAs/GaAs HFET) and Figs. 3 and 4 (obtained for a GaAs MESFET) and was recently corroborated by data published by Angelov *et al.* (obtained for a PM HFET) [47]. Another example of the dependence of minimum noise temperature, transconductance and equivalent drain temperature on the drain current for a modern InP device at cryogenic temperatures [48], [49] is shown in Fig. 5. The values of transconductance were d.c. measured, and the values of the minimum noise temperature were measured at 40 GHz. In this case, it was assumed, in computing the values of equivalent drain temperature, that the only element of the HFET equivalent circuit varying with bias and temperature was transconductance  $g_m$ . This approach, necessarily oversimplified in the absence of sufficiently accurate cryogenic S-parameter measurements, nevertheless demonstrates a very similar dependence of  $T_d$  vs. drain current as observed in much more accurate room temperature experiments. This data was used to develop a series of cryogenic amplifiers [49]-[53], and an excellent agreement between measured and modeled results (see Section IV) over a broad temperature range indirectly confirms this approach.

Table I. Comparisons of Noise Parameters of FHR01 Intrinsic Chip							
(f = 8.5  GHz)							
Ta	Comments	T <sub>min</sub>	R <sub>opt</sub>	X <sub>opt</sub>	g <sub>n</sub>	Tg	T <sub>d</sub>
Κ		K	Ω	Ω	mS	K	K
297	Measured	65.6	26.3	59.5	3.0	-	-
	Model Best Fit for $r_{gs} = 2.5 \Omega$	58.7	28.4	66.9	3.27	304	5514
	Model Best Fit for $r_{gs} = 3.5 \Omega$	59.6	28.2	66.9	3.24	210	5468
12.5	Measured	8.2	11.4	65.2	.80	-	-
	Model Best Fit for $r_{gs} = 2.5 \Omega$	7.4	12.3	66.9	.87	14.5	1406
	Model Best Fit for $r_{gs} = 3.5 \Omega$	7.7	12.0	66.9	.85	9.3	1379



Fig. 3. Equivalent gate and drain temperatures versus drain current for the sample MESFET in Fig. 2. Data are shown given for three different devices denoted by different symbols [35].



Fig. 4. Minimum noise temperature  $T_{min}$  (at 10 GHz), equivalent gate temperature  $T_d$ , and intrinsic cut-off frequency  $f_T$  as a function of drain current for the sample MESFET in Figs. 2 and 3 [35].



Fig. 5. The minimum noise temperature  $T_{min}$  (at 40 GHz), dc measured transconductance and equivalent drain temperature vs. drain current at the ambient temperature  $T_a = 18$  K of .1 x 50µm InP HEMT [49].

As was mentioned earlier, the model of Pucel *et al.* requires knowledge of three frequency-independent parameters, R, P and C [17], in addition to knowledge of a FET equivalent circuit to predict noise parameters at any frequency. The model developed by the author requires two frequency-independent parameters  $T_g$  and  $T_d$ . Although the starting points in developing both models are entirely different, both can be made equivalent if one of the parameters in Pucel's model is determined by the other two as given by equation:

$$C = \sqrt{\frac{R}{P}}$$
(10)

The experimental evidence confirming that relationship since it was first noted in 1989 [33], [34] has been quite overwhelming, and papers by P. Heynmann *et al.* [43], I. Angelov *et al.* [47] and P. Tasker *et al.* [42] are especially noteworthy. Furthermore, experimental evidence that one of the parameters, the equivalent gate temperature, follows within the accuracy of experiments the ambient temperature of a FET device leads to a noise model with only one parameter  $T_d$ . In fact, this is the only approach successfully used in the design of amplifiers at cryogenic temperatures [36]-[39], [45], [48]-[53].

It is interesting to note that device technologists, in their efforts to improve the noise performance of FET's in the 80's and early 90's, relied mostly on the guidance given by the Fukui equation (1). Their progress was achieved by addressing two issues in FET (HFET) design:

- 1) maximization of intrinsic cut-off frequency  $f_T = \frac{g_m}{2\pi C_{os}}$ , and
- 2) minimization of parasitic resistances of gate and source, rg and rs, respectively

The first issue was addressed by progress in the technology of artificially structured semiconductors on which FET structures are built, and progress in the definition and fabrication of submicrometer length gates (see, for instance, [55]). The epitaxial GaAs material used exclusively for low-noise FET fabrication in the 1970's was replaced by progressively more complex heterostructures: AlGaAs/GaAs, AlGaAs/InGaAs/GaAs and AlInAs/GaInAs/InP. The gate length of low-noise GaAs FET's in the 1970's was about 1  $\mu$ m [18] and < .1  $\mu$ m in the 1990's [55] as a result of the development of electron beam lithography.

The second issue was addressed by improvements in FET layout, fabrication of "mushroom" or T-shaped gates, reduction in drain-to-source separation ("self-aligned" ohmic contacts) and progress in the technology of ohmic contacts [55].

A corresponding approximate expression for the minimum noise temperature of a FET chip, which is based on equation (5) can be written as:

$$\Gamma_{\min} \approx 2 \frac{f}{f_{\rm T}} \sqrt{r_{\rm t} T_{\rm g} g_{\rm ds} T_{\rm d}}$$
(11)

where  $r_t = r_s + r_g + r_{gs}$ . Thus, both expressions (1) and (11) can explain the improvement in noise temperature resulting from technological improvements. Expression (11), however, allows for a deeper insight into how the FET bias affects the minimum noise temperature and how its value is minimized. Only  $T_d$  and  $f_T$  are strong functions of transistor bias. Consequently, the bias optimal from the point of view of minimum noise temperature at any frequency is that minimizing the value of

$$f(V_{ds}, I_{ds}) = \frac{\sqrt{T_d g_{ds}}}{f_T}$$
(12)

or alternatively

$$f(V_{ds}, I_{ds}) \cong \frac{\sqrt{I_{ds}}}{g_m}$$
(13)

as  $C_{gs}$  is not a strong function of gate bias (and drain currennt  $I_{ds}$ ) and  $T_d$  is to a first approximation proportional to  $I_{ds}$ . This observation is clearly illustrated in both Figs. 4 and 5. Consequently, an excellent low-noise FET, in addition to having parasitic resistances as small as possible, should have as large as possible cut-off frequency  $f_T$  at as small as possible current  $I_{ds}$ . This property has long been observed, especially at cryogenic temperatures, and is sometimes referred to as "quality of pinch-off." It even served as a criterion for a selection of good cryogenic devices even before the nature of this relationship was understood [57]-[59].

#### III. CRYOGENIC FET'S AND HFET'S: 1970-1993

The first attempt at investigating the noise properties of GaAs FET's at cryogenic temperatures was described in [60] in 1970 by Loriou *et al.* The experiment was done at the frequency of 1 GHz. The change in noise temperature  $T_n$  from 360 K at room temperature to 120 K at the temperature of 77 K was observed. Two years later somewhat similar results of  $T_n = 93$  K at 77 K ambient temperature at 1.5 GHz were reported [61]. The next important results were published in 1976 when Liechti and Larrick [62] reported  $T_n = 60$  K at  $T_a = 90$  K at 12 GHz for a device and  $T_n = 130$  K for a three-stage, 31 dB gain amplifier at  $T_a = 60$  K.

A more systematic study of the cryogenic noise behavior of FET's was undertaken by Weinreb and collaborators [63], [64] who investigated the noise properties of GaAs FET's at the very important radio astronomy frequencies in L- and C-bands. In 1980, noise temperature  $T_n = 20$  K was reported at 5 GHz and 20 K ambient temperature; in 1982,  $T_n = 7$ K was reported at 1.4 GHz and 20 K ambient temperature.

In 1984, the author undertook the study of noise parameters of different commercial FET's at X-band [65]. A noise temperature of 20 K was repeatedly demonstrated for packaged commercial FET's (Fujitsu FSC10FA) at the frequency of 8.4 GHz and ambient temperature of 14 K, although noise temperatures as small as 15 K were observed for individual devices under the same conditions [65].

The first experimental HFET using AlGaAs/GaAs heterostructure was demonstrated by several laboratories in 1980 [55]. The first cryogenic testing of a .25  $\mu$ m gate length HFET, developed by Cornell University, was performed at NRAO in 1985 [66] and a record low-noise performance of  $T_n = 10$  K at 8.4 GHz was reported [66]. Shortly thereafter, a consortium of the NRAO Central Development Laboratory (CDL), GE's Military Electronics Division and the Jet Propulsion Laboratory started a program to develop very low-noise cryogenic HFET's for the purpose of equipping the NRAO Very Large Array (VLA) with low-noise receivers to provide reception for the Voyager spacecraft during its encounter with Neptune in August 1989. This very successful program produced devices with  $T_n = 6$  K at 8.4 GHz [57]-[59].

A group of studies published by the author between late 1984 and early 1988 [57]-[59], [65]-[68] identified a number of effects observed at cryogenic temperatures for which only some, later on, had satisfactory explanations.

It was observed that room-temperature performance is not always a good indicator of cryogenic performance. It certainly can be understood in terms of the model presented in Section II and especially equation (11). Relatively large parasitic resistances could mask otherwise excellent noise behavior of an intrinsic chip at room temperature. Excellent noise properties of an intrinsic chip could only be revealed at cryogenic temperatures as the thermal sources are reduced by as much as a factor of 25.

It was observed that vastly different performance at cryogenic temperatures for devices with similar roomtemperature performance can usually be traced to poor pinch-off characteristics at cryogenic temperatures. It is interesting to recall the data on the GE HFET's shown in Fig. 6 and published in 1986 [57]. Devices with very similar room-temperature performance differed greatly in their transconductance vs. drain current characteristics at cryogenic temperatures and small currents. This observation proved to be extremely useful in diagnosing amplifier performance, even in the case where the amplifiers were built with devices from the same wafer. As an example, a set of g<sub>m</sub> vs. I<sub>ds</sub> characteristics for several devices from the same wafer, taken at room and cryogenic temperatures, with corresponding values of measured minimum noise temperature, are shown in Fig. 7 [59]. If the performance of an amplifier was subpar from the point of view of noise temperature, the dc characteristics of a first-stage device were measured. That simple dc measurement allowed for a screening of bad cryogenic performers, irrespectively of any other problem possibly arising with amplifier construction. Obviously, this behavior can now be easily interpreted in terms of the noise model and its dependence on bias as discussed in Section II. As follows from equation (13), a larger drain current for a given transconductance indicates higher minimum noise temperature.



Fig. 6. Minimum noise temperature  $T_{min}$  at 8.4 GHz and dc measured transconductance  $g_m$  at 297 K and 12.5 K for two different General Electric AlGaAs/GaAs HFET's with and without spacer layer. The devices have similar room temperature performance but vastly different cryogenic performance [57].



Fig. 7. Comparison of  $g_m(I_d)$  characteristics for three HFET's from a single wafer having very similar room temperature performance and very different cryogenic performance [59].

A typical performance of Voyager/Neptune amplifiers is shown in Fig. 8, while a photograph of the amplifier itself is shown in Fig. 9. It is interesting to note that the VLA 8.4-GHz system, which even today is considered to be the most sensitive radio astronomy instrument in the world, is still operating using amplifiers designed almost 20 years ago.



Fig. 8. Noise temperature and gain of typical Voyager/Neptune amplifier at 14 K. The resulting noise temperature of the whole receiver is also plotted for comparison [58].



Fig. 9. Photograph of 8.4 GHz Voyager/Neptune amplifier with cover removed [58].

It has been observed that the dc, RF, and noise performances of AlGaAs/GaAs HFET's at cryogenic temperatures are sensitive to light [57-59], [65]-[68]. Almost all devices, if kept under dark conditions, exhibited memory at cryogenic temperatures. That is to say, their performance depended not only on current bias conditions but also on the device history, for example, previous bias conditions and temperature. Quite often, a device, if kept dark at cryogenic temperatures, would exhibit an increase in noise temperature on time scales of hours and days, showing degradation in noise of 50 percent and more with no significant change in RF characteristics [57], [58], [65], [66]. Furthermore, the characteristic of minimum noise temperature vs. ambient temperature would show an anomalous behavior in the temperature range of 150 to 175 K. This effect, sometimes referred to as a "camel-hump" effect, is

illustrated in Fig. 10. It was present in all AlGaAs/GaAs HFET's, although not observed in GaAs FET's. None of these effects were satisfactorily explained. These effects are thought to be related to a charge-trapping mechanism which has been reported to be the cause of the collapse of I-V characteristics at cryogenic temperatures. Trapping, however, was never considered as a possible influence on noise performance at frequencies as high as X-band, and a convincing explanation of these effects still remains a mystery. An explanation of the phenomena at that time did not seem to be of particular priority as these were present only outside of normal operating conditions and illumination with red light made the devices "well-behaved" at cryogenic temperatures [57]-[59], [65]-[68].



Fig. 10. Example of noise temperature of AlGaAs/GaAs GE HFET at 8.4 GHz amplifier vs. ambient temperature for two different bias currents illustrating unexpected behavior around 175 K.

Conventional HFET's with about .2  $\mu$ m gate length, which became available in the 1980's, allowed for construction of cryogenic amplifiers with sufficient gain and noise temperature to be competitive with other low-noise technologies up to K<sub>a</sub>-band frequencies [36], [58], [59]. By the end of that decade, two great technological advances had been made. First, the concept of a pseudomorphic HFET, introduced in 1985, was reduced to practice. Second, the manufacture of gates as short as .1  $\mu$ m became possible [55]. Pseudomorphic devices using .1- $\mu$ m gate length made low-noise amplification possible up to 95 GHz, although for cryogenic applications the noise performance at W-band frequencies was not yet competitive with well-established SIS mixer technology [38]. Pseudomorphic HFET's with .1- $\mu$ m gate lengths made possible the development of cryogenic receivers covering 40-45 GHz for the Very Large Baseline Array (VLBA) [38], [69]. Typical characteristics of a NRAO-designed amplifier developed in 1991, its gain and noise performance, and a comparison between measured and modeled results are shown in Figs. 11 and 12. A photograph of a completed amplifier having WR22 waveguide input and output is shown in Fig. 13.



Fig. 11. Comparison of model-predicted and measured performance of 40-45 GHz amplifier at 297 K. The amplifiers were built in 1991 for the Very Large Baseline Array Q-band receivers with .1-µm gate length pseudomorphic HFET's.



Fig. 12. Comparison of model-predicted and measured performance of 40-45 GHz amplifier at 18 K. The amplifiers were built in 1991 for the Very Large Baseline Array Q-band receivers with .1-µm gate length pseudomorphic HFET's.



Fig. 13. Photograph of 40-45 GHz VLBA amplifier with cover removed.

Since 1991, the pseudomorphic AlGaAs/InGaAs/GaAs HFET's have replaced conventional AlGaAs/GaAs HFET's in all commercial low-noise applications. However, these devices also suffer from a similar lack of repeatability of performance at cryogenic temperatures, as was the case with conventional HFET's. For example, the best noise performance at that time, measured at 40 GHz using .1  $\mu$ m PM-HFET's, was about 20 K [38], but it was not uncommon to measure twice this number for devices with very similar room-temperature performance (T<sub>n</sub>  $\cong$  200 K) from other manufacturers.

## IV. InP HFET'S AT CRYOGENIC TEMPERATURES

A promise of excellent microwave performance from an AlInAs/InGaAs/InP HFET, usually referred to as InP HFET, was demonstrated in 1987 [70]. Two years later, Mishra and colleagues at the Hughes Research Laboratories, incorporating the technology of .1-µm-long mushroom T-gates and AlInAs/InGaAs/InP wafer structure, shattered records for low-noise performance at room temperature [71]. They demonstrated a noise figure of .9 dB (67 K noise temperature) at 63 GHz. Several laboratories in 1990 and 1991 demonstrated similar results and as little as 1.2 db noise figure (93 K noise temperature) at 94 GHz [72]-[74]. In 1991, the author predicted the behavior of noise performance of these InP HFET's vs. temperature [38]. It was possible by combining the knowledge of an equivalent circuit of a state-of-the-art InP HFET with the knowledge of equivalent gate and drain temperatures vs. temperature and current gained from evaluation of PM HFET's with .1-µm gate length (which was at that time routinely used at NRAO). The results were published in [38] in the form of graphs of minimum noise measure vs. frequency expected of InP HFET's at different cryogenic temperatures. The minimum noise measure of a device determines the minimum possible noise temperature that can be exhibited by an amplifier with sufficiently large gain using this device. The results of this calculation, done in 1991, are shown in Fig. 14. The prediction of attainable noise temperatures at cryogenic temperatures for InP HFET amplifiers has held up remarkably well over the last decade. Some recent experimental results were included in this figure to illustrate this point.



Fig. 14. A minimum noise measure of .1-µm gate length AlInAs/GaInAs/InP HFET [38]. The best experimental results from different laboratories are also shown [72]-[74].

Generally, InP HFET's at cryogenic temperatures are much less sensitive to illumination than conventional HFET's. These devices do not seem to exhibit any memory at cryogenic temperatures if not illuminated. The unrepeatable noise performance at cryogenic temperatures can usually be traced to the behavior at pinch-off, in the similar way as it was discussed for conventional devices, and/or to the presence of gate leakage. For InP HFET's, the gate leakage at room temperature is of the order of several  $\mu$ A, and for good devices decreases at cryogenic temperatures by at least an order of magnitude. However, if the gate current of the order of several  $\mu$ A is still present at cryogenic temperatures, it can greatly influence the cryogenic noise performance to the point that it may completely erase any advantage that an InP HFET may have over a conventional or PM device. An illustration of this observation is shown in Fig. 15 which shows a comparison of the minimum noise measure of 80-µm-wide devices [69] computed with and without the presence of gate leakage current. For the model, it was assumed that the noise influence of the gate leakage could be represented by an ideal shot noise current source.



Fig. 15. An illustration of the influence of the gate-to-drain leakage current generating pure shot noise on the minimum noise measure of an InP HFET with .1  $\mu$ m x 80  $\mu$ m gate dimensions [69] at T<sub>a</sub>=18 K.

Current knowledge about noise and signal models of "well-behaved" InP HFET's at cryogenic temperatures is sufficiently accurate to allow for computer-aided design of cryogenic amplifiers with optimal, according to some criterion, noise bandwidth performance. Usually an amplifier has to satisfy other requirements, such as input return loss, unconditional stability, and minimum gain and gain flatness, *etc.* All of these parameters can now be reliably investigated using CAD tools.

An example of noise and gain characteristics and a comparison with model prediction for a room-temperature InP HFET, six-stage, W-band amplifier are shown in Fig. 16. The devices have gate dimensions .1 x 50  $\mu$ m and are biased at V<sub>ds</sub> = 1.0 V and I<sub>ds</sub> = 5 mA. For the purpose of modeling, the equivalent circuit given in [49] is used. The noise model of [33], [34] is assumed for noise computation with T<sub>g</sub> = 297 K and T<sub>d</sub> = 1500 K (compare Fig. 5). An example of noise and gain characteristics and comparisons with the model prediction for a cryogenic amplifier are shown in Fig. 17. The transistors were biased at V<sub>ds</sub> = .9 V and I<sub>ds</sub> = 3 mA in the first two stages and I<sub>ds</sub> = 5mA in the last three stages. For the model data, the only changes from room temperature were: T<sub>g</sub> = T<sub>a</sub> = 20 K and T<sub>d</sub> = 500 K and about a 20 percent increase in transconductance g<sub>m</sub>. A photograph of the amplifier is shown in Fig. 18.



Fig. 16. A comparison of measured gain and noise characteristics of a W-band amplifier with model prediction at room temperature. Measured noise temperature includes the contribution of pyramidal horn and receiver ( $T_r = 2000$  K).



Fig. 17. A comparison of measured gain and noise characteristics of a W-band amplifier with model prediction at cryogenic temperature  $T_a = 20$  K. Measured noise temperature includes the contribution of dewar window, pyramidal horn at  $T_a = 20$  K, and room temperature receiver ( $T_r = 2000$  K).



Fig. 18. Photograph of W-band MAP amplifier with cover removed.

Examples of the comparisons between measured and modeled data for K-band amplifiers, under exactly the same assumptions, are shown in Figs. 19 and 20. A photograph of the amplifier is shown in Fig. 21 [51].



Fig. 19. A comparison of measured gain and noise characteristics of a K-band amplifier with model prediction at room temperature. Measured noise temperature includes the contribution of pyramidal horn and receiver ( $T_r = 2000$  K).



Fig. 20. A comparison of measured gain and noise characteristics of a K-band amplifier with model prediction at cryogenic temperature  $T_a = 20$  K. Measured noise temperature includes the contribution of dewar window, pyramidal horn at  $T_a = 20$  K, and room temperature receiver ( $T_r = 2000$  K).



Fig. 21. Photograph of K-band MAP amplifier with cover removed.

There have only been several wafers of InP devices which exhibited an excellent cryogenic performance since their introduction in 1993. The most recent best results are usually demonstrated with devices produced at TRW Space Technology Division (now Northrop Grunman Space Technology) in collaboration with JPL [56]. A summary of what is currently believed to be the best results at cryogenic temperatures is shown in Fig. 22, together with the author's 1992 prediction. The experimental results are those published by NGST, JPL and Chalmers University [45], [54], [56], [75-76] and some measured at X-, K-, K<sub>a</sub>- and Q-bands at NRAO.



Fig. 22. Comparison between the predication for the minimum noise measure of a .1- $\mu$ m gate length cryogenic InP HFET (1992) and the best results reported to date for cryogenic amplifiers employing NGST/JPL devices. Below 50 GHz, the noise temperatures for the Chalmers 4-8 GHz [45] and NRAO X-, K-, K<sub>a</sub>- and Q-band amplifier designs are shown. For higher frequencies, the noise temperatures reported for the NGST/JPL MMIC designs are shown [54], [56], [76].

### V. CONCLUDING REMARKS

The noise performance of cryogenic FET's and HFET's has made tremendous progress over the last several decades. The most rapid advances seem to have occurred between 1980 and 1995. Three different generations of HFET's were proposed and reduced to practice during that period. Since 1995, no significant new ground has been broken in device technology. However, InP HFET technology has matured and allowed construction of extremely low-noise amplifiers. These amplifiers were used in the construction of several instruments for investigation of the physics of the early Universe. Among those one should mention the Wilkinson Microwave Anisotropy Probe (WMAP) launched in June 2001, the Cosmic Background Explorer (CBI), the Degree Angular Scale Interferometer (DASI), and the Very Small Array (VSA). Also, the performance of receivers installed on existing radio astronomy telescopes has been greatly improved by the availability of broadband InP HFET cryogenically-coolable amplifiers, especially in the K<sub>u</sub>-, K-, K<sub>a</sub>- and Q-bands, on NRAO's Very Large Array and the Green Bank Telescope. This technology made possible the installation of 3-mm wavelength receivers on the Very Large Baseline Array and the MPI Effelsberg Radio Telescope.

It is difficult to predict at this moment whether further dramatic improvements are possible. Each new generation of HFET's has required huge investments in the establishment of repeatable device technology, driven mostly by commercial and military applications. Radio astronomy has been able to derive great benefits from these advances. Still, even today, InP HFET technology has not been able to consistently reproduce noise performance at cryogenic temperatures, although performance at room temperature has been sufficiently reproducible. Furthermore, performance at room temperature in commercial and military applications below 50 GHz has been sufficiently good for any terrestrial system as the system noise temperature tends to be dominated by the antenna temperature (about 300 K). Consequently, a very costly investment in device technology would return very little in performance for terrestrial systems. Therefore, not unexpectedly, research into new structures from the point of view of noise performance has lost momentum. In the author's opinion, only InAs/AlSb HFET's offer a possibility of further improvements in the noise temperature at cryogenic temperatures. So far, only devices with .25-µm gate length have been demonstrated [78]. It remains to be seen whether the potential for very low-noise amplification using this technology will ever materialize.

Most of the low-noise receivers below W-band are now taking advantage of the extremely low noise performance of cryogenic InP HFET's. At W-band frequencies, HFET's compete with SIS mixers, and the choice between these two technologies is less likely to be determined by noise performance alone but rather by other system requirements. Above W-band frequencies, the noise performance of SIS mixers is considerably better than that of InP amplifiers. For example, the best-ever HFET amplifier at 185 GHz exhibited noise performance of about 150 K [75], [76] which is very much in line with expectations published in 1992 [38], while SIS mixer receivers with 60 SSB noise temperatures are now routinely built for 210-270 GHz (for example, [77]). The difference in performance is so large that, for terrestrial systems in which cooling requirements for an SIS mixer can be easily met, it is very unlikely that, even with advances in HFET technology, they will ever displace SIS mixers as a preferred technology for frequencies above 150 GHz.

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