NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 279

A NEW APPROACH TO MODELING OF NOISE PARAMETERS OF FET'S AND MODFET'S AND THEIR FREQUENCY AND TEMPERATURE DEPENDENCE

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JULY 1988

NUMBER OF COPIES: 200

TABLE OF CONTENTS

I. Introduction 1
II. Noise Parameters of FET Chip 3
A. Circuit Theory Concepts 3
B. Noise Parameters of a FET Chip 6
C. Approximations and Discussion 10
III. Experimental Verification 12
IV. Discussion of Results 24
V. Comparison with Other Methods 25
VI. Conclusions 30
VII. Acknowledgement 30

TABLES

Table I. Noise Parameters of FHR01FH at Different Stages of Deembedding, f = 8.5 GHz, V_{ds} = 2 V 16

Table II. Comparisons of Noise Parameters of FHR01 Intrinsic Chip, f = 8.5 GHz 18

FIGURES

Fig. 1: Noise Representation in Linear Two-Ports 3

Fig. 2: Equivalent Circuit of a FET (HEMT, MODFET) Chip 7

Fig. 3: Noise Equivalent Circuit of an Intrinsic Chip 7

Fig. 4: Equivalent Circuit of FHR01FH HEMT at T_a = 297 K, V_{ds} = 2 V, I_{ds} = 10 mA 14

Fig. 5: Comparison Between S-Parameters of FHR01FH Measured by Fujitsu [38] and Those Predicted from Model of Figure 4 . . . 15

Fig. 6: Noise Parameters and Associated Gain of FHR01FH HEMT at T_a = 297 K and V_{ds} = 2 V, I_{ds} = 10 mA 19

Fig. 7: Noise Parameters of FHR01X (Chip) HEMT at T_a = 297 K 20

Fig. 8: Noise Parameters and Associated Gain of FHR01FH HEMT at T_a = 12.5 K and V_{ds} = 2 V, I_{ds} = 5 mA 21

Fig. 9: Noise Parameters of FHR01X (Chip) HEMT at T_a = 12.5 K 22

Fig. 10: Comparison Between Model Prediction and Measured Performance of Three-Stage FHR01FH Amplifier at 297 K and 12.5 K 23

Fig. 11: Comparison Between Model and Experimental Data for NE045 Chip 28

References 31

A NEW APPROACH TO MODELING OF NOISE PARAMETERS OF FET'S AND MODFET'S AND THEIR FREQUENCY AND TEMPERATURE DEPENDENCE

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Abstract

A simple noise model of microwave MESFET (MODFET, HEMT, etc.) is described and verified at room and cryogenic temperatures. Closed form expressions for T_{min} - minimum noise temperature, Z_{gopt} - optimum generator impedance, g_n - noise conductance, and Z^M_{gopt} - generator impedance minimizing noise measure, are given in terms of frequency, the elements of FET equivalent circuits, and equivalent temperatures of intrinsic gate resistance and drain conductance to be determined from noise measurement. These equivalent temperatures are demonstrated in the example of Fujitsu FHR01FH MODFET to be independent of frequency in the frequency range in which 1/f noise is negligible. Thus, the model allows prediction of noise parameters for a broad frequency range from a single frequency noise measurement. The model predicts the noise behavior in general agreement with previous studies, but it is much simpler and all its parameters possess physical meanings. It also reconciles the existing discrepancies between different approaches to the modeling of noise properties of FET's.

I. Introduction

The noise performance of field-effect transistors (FET's) has been a subject of study for more than a quarter of a century [1]-[20]. It remains to be a subject of active research [18]-[20], as MODFET's (HEMT's) continue to set records of noise performance both at room and cryogenic temperatures (for example, [22]-[26]). In spite of considerable effort in this field, a noise model which could be helpful in understanding the noise sources within a FET (MODFET, HEMT) and at the same time be useful in circuit design has not really emerged.

The published studies of noise properties of FET's (MODFET's) may be divided into two distinctive groups. The first group, as a starting point of analysis, considers fundamental equation of transport in semiconductors [1]-[11]. Most papers in this category published over the years may be viewed as progressively more sophisticated treatments of the problem originally tackled by Van der Ziel [1], [2]. Ultimately, a full Monte Carlo particle study of noise figure of FET's has been proposed [11]. Although the MODFET wafer structure is different than that of a FET, the methods employed in noise studies are basically the same [8], [10], [20] as those applied to FET's [5], [9], [20].

The second group of published studies [12]-[19] addresses the issue of what needs to be known about the device in addition to its equivalent circuit to predict noise performance. Most often used is the semi-empirical approach originated by Fukui [12]-[16] in which relations between the minimum noise figure at a given frequency and the values of transconductance g_m, gate to source capacitance C_{gs}, and source and gate resistances r_s and r_g, are established. A quantitative agreement may be obtained only after proper choice of fitting factor [12], [13], [15] or fitting factors [16]. The extension of this approach to other noise parameters [12] results quite often in non-physical two-port [14]. The Fukui approach, although very widely used by device technologists, does not provide any insight into the nature of noise generating mechanism in FET as the fitting factors do not possess physical meaning.

The most comprehensive treatment of signal and noise properties of a MESFET is that published by Pucel *et al.* [5]. It quite often serves as a bridge between different approaches to noise treatment as many other results are compared to it or adopt similar computational technique [7]-[10], [13], [20]. The method of Pucel *et al.* [5] calls for three frequency independent noise coefficient P, R and C to be known in addition to small signal parameters of an intrinsic FET in order to determine four noise parameters at any given frequency. Recent work by Gupta *et al.* [18], [19], however, claims good agreement over wide frequency range between measured noise parameters and those predicted from knowledge of an equivalent circuit and a single frequency-independent constant.

The method presented in this paper reconciles this discrepancy. It uses simple circuit theory agreements to show that for an intrinsic device two frequency independent constants (equivalent temperatures of intrinsic gate resistance and drain conductance) in addition to elements of an equivalent circuit need to be known to predict all four noise parameters at any frequency. These constants in the experimental example of a Fujitsu FHR01FH HEMT are frequency independent in the frequency range in which 1/f noise is negligible. Surprisingly, it is also demonstrated that both at room and cryogenic temperatures the effective gate temperature is within measurement errors equal to the ambient temperature of the device, thus partially corroborating the room temperature results of Gupta *et al.* [18], [19].

The second section of this paper presents the derivation of expressions for the noise parameters of an intrinsic FET (MODFET, HEMT). The proposed model is then applied to the analysis of noise performance of FHR01FH HEMT both at room and cryogenic temperatures in Section III and the results are discussed in Section IV. Finally, comparisons with other models are offered in Section V.

II. Noise Parameters of FET Chip

A. Circuit Theory Concepts

Circuit theory concepts which have been found to be most useful in describing noise properties of FET's (MODFET's) are summarized here. Two representations of noise in linear two-port are shown in Figure 1 [28]. The representation in Figure 1.A is natural for admittance representation of signal properties of a two-port and the corresponding noise parameters are [28] (refer to Figure 1):

$$G_1 = \frac{\overline{|i_1|^2}}{4k\,T_o\,\Delta F}, \qquad G_2 = \frac{\overline{|i_2|^2}}{4k\,T_o\,\Delta F}, \qquad \rho_c = \frac{\overline{i_1^* i_2}}{\sqrt{\overline{|i_1|^2}\;\overline{|i_2|^2}}} \tag{1}$$

where k is Boltzmann's constant, T_o = standard temperature of 290 K, Δf = incremental bandwidth. The representation in Figure 1.B is natural for ABCD matrix representation and the corresponding noise parameters are [28]:

$$R_n = \frac{\overline{|e_n|^2}}{4k\,T_o\,\Delta F}, \qquad g_n = \frac{\overline{|i_n|^2}}{4k\,T_o\,\Delta F}, \qquad \rho = \frac{\overline{e_n^* i_n}}{\sqrt{\overline{|e_n|^2}\;\overline{|i_n|^2}}} \tag{2}$$

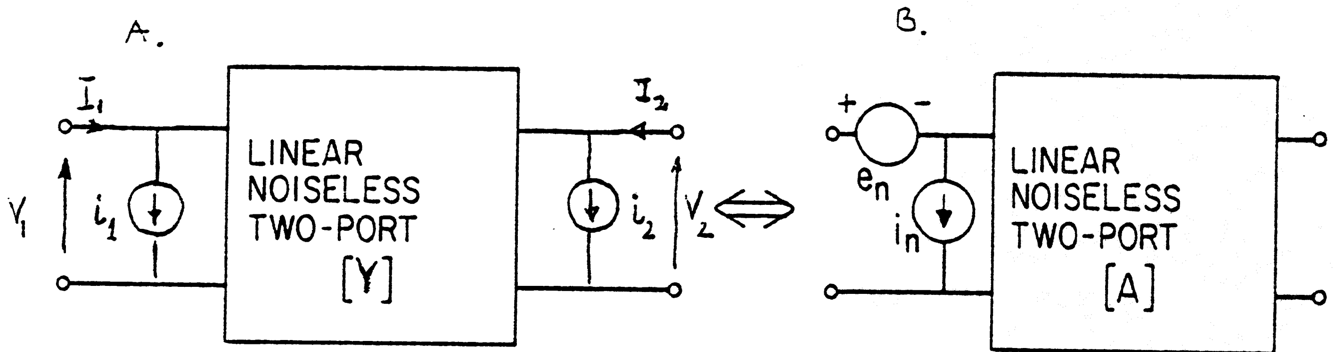


Fig. 1: Noise representation in linear two-ports: (A) involving current noise sources at the input and output and (B) involving current and voltage noise source at the input.

It should be noted that lower case notation for noise conductance has been chosen, which follows that of Rothe and Dahlke [28]. A noise conductance, G_n, is used there to denote the portion of g_n which represents the part of noise source $\overline{|i_n|^2}$ which is uncorrelated with noise source $\overline{|e_n|^2}$. This notation follows that prevailing in English literature (for example, [5], [20], [29]) although examples can be found to the contrary (for example, [27], [30]).

Transition from the set (1) of noise parameters to the set (2) of noise parameters is given by (for example, [31])

$$R_n = \frac{G_2}{|y_{21}|^2} \quad , \quad g_n = \frac{1}{|y_{21}|^2} \left(|y_{21}|^2 G_1 + |y_{11}|^2 G_2 - 2\mathrm{Re}\{y_{11}^* \; y_{21} \; cor_c^*\} \right)$$

$$cor = \frac{1}{|y_{21}|^2} \left(y_{11} G_2 - y_{21} \; cor_c^* \right) \tag{3}$$

where $cor = \rho \sqrt{R_n \, g_n} \quad , \quad cor_c = \rho_c \sqrt{G_1 \, G_2}$

and y_{mn} denote the elements of admittance matrix [y] of a two-port.

Although the noise representations (1) and (2) are very convenient in derivation of noise parameters of a FET (MODFET), a representation involving minimum noise temperature and optimal generator impedance Z_{opt} (optimal reflection coefficient Γ_{opt}) is usually employed by a circuit designer. It is subsequently demonstrated that the representation consisting of minimum noise temperature T_{min}, optimal source impedance $Z_{opt} = R_{opt} + j X_{opt}$ and noise conductance g_n or parameter $N = R_{opt} \, g_n$ (as defined by Lange [32]) results in simple, easily-interpretable expressions. From this point of view, the two expressions for noise temperature T_n of a two-port driven by generator impedance Z_g most convenient to use are:

$$T_n = T_{min} + T_o \frac{g_n}{R_g} |Z_g - Z_{gopt}|^2 = T_{min} + NT_o \frac{|Z_g - Z_{gopt}|^2}{R_g \, R_{opt}} \tag{4}$$

$$T_n = T_{min} + 4NT_o \frac{|\Gamma_g - \Gamma_{opt}|^2}{(1 - |\Gamma_{opt}|^2)(1 - |\Gamma_g|^2)} \tag{5}$$

where $\Gamma_{opt} = \frac{Z_{opt} - Z_o}{Z_{opt} + Z_o}$

and Z_o is a reference impedance. The usefulness of these expressions is further corroborated by the property of T_{min} and N to remain invariant if a lossless reciprocal two-port is connected to the input (and/or output) of a noisy two-port [32]. Also, for T_{min} and N to represent a physical two-port, a following inequality has to be satisfied [33], [14], [27]:

$$T_{min} \leq 4NT_o \tag{6}$$

The significance of the inequality (6) lies not only in establishing bounds on noise parameters in a presence of measurement errors [27]. In case of small measurement errors, the value of ratio $4NT_o/T_{min}$ may help determine the nature of noise generating mechanism in a FET (HEMT), as it is demonstrated in the following section.

Transition from the set of noise parameters defined by (2) to those used in expressions (4)-(6) is given by [30], [31]:

$$X_{opt} = \frac{Im\{cor\}}{g_n} \quad , \quad R_{opt} = \sqrt{\frac{R_n}{g_n} - X_{opt}^2}$$

$$T_{min} = 2T_o\left(g_n R_{opt} + Re\{cor\}\right) \; . \tag{7}$$

Noise parameter g_n is the same as in the representation given by (2).

Finally, the noise measure of a linear two-port is defined by [36]:

$$M = \frac{T_n}{T_o} \frac{1}{1 - \frac{1}{G_a}} \tag{8}$$

where G_a is available gain. The minimum value of noise measure M_{min} which occurs for certain generator impedance $Z^M_{opt} \neq Z_{opt}$ is invariant upon arbitrary linear lossless embedding [36], [37].

B. Noise Parameters of a FET Chip

An equivalent circuit of FET chip is shown in Figure 2. Parasitic resistances contribute only thermal noise and with knowledge of the ambient temperature T_a their influence can be easily taken into account. In fact, an arbitrary lossy reciprocal two-port at input and/or output and/or in a feedback path can be easily deembedded using formulas of [34] and [35]. The noise properties of an intrinsic chip are then treated by assigning equivalent temperature T_g and T_d to the remaining resistive (frequency independent) elements of the equivalent circuit r_{gs} and g_{ds}, respectively. No correlation is assumed between noise sources represented by the equivalent temperatures T_g and T_d. This yields a noise equivalent network for an intrinsic chip shown in Figure 3.

Straightforward comparison of equivalent networks of Figure 1.A and Figure 3 and use of definitions given by (1) gives:

$$G_1 = \frac{T_g}{T_o} \frac{r_{gs} (\omega C_{gs})^2}{1 + \omega^2 C_{gs}^2 r_{gs}^2} \tag{9}$$

$$G_2 = \frac{T_g}{T_o} \frac{g_m^2 r_{gs}}{1 + \omega^2 C_{gs}^2 r_{gs}^2} + \frac{T_d}{T_o} g_{ds} \tag{10}$$

$$cor_c = \rho_c \sqrt{G_1 G_2} = \frac{-j\omega g_m C_{gs} r_{gs}}{1 + \omega^2 C_{gs}^2 r_{gs}} \frac{T_g}{T_o} \tag{11}$$

It should be stressed that the noise representation of Figure 1.A is used as an intermediate step in all previous analyses, which lead to the determination of four noise parameters [5], [8], [9], [10]. Comparison with Pucel *et al.* [5] shows $\rho_c = -jC$. Assuming $T_d = 0$ in (10) gives $\rho_c = -j1$. That is the noise voltage source $\overline{e_{gs}^2}$ (Figure 3) models a noise process which produces perfectly correlated noise currents in drain and gate with purely imaginary correlation coefficient. Consequently, the current noise source $\overline{i_{ds}^2}$ models a noise process which produces noise current only in a drain circuit.

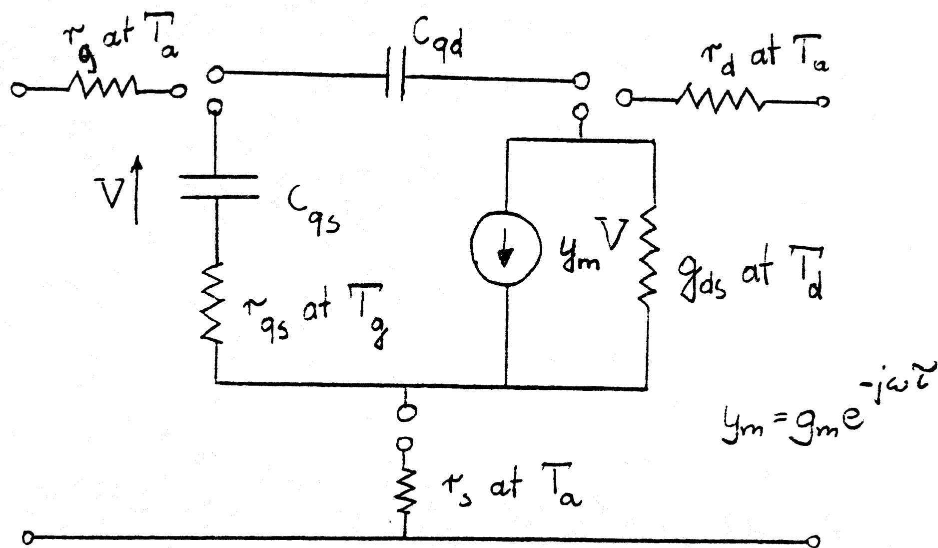


Fig. 2. Equivalent circuit of a FET (HEMT, MODFET) chip. Noise properties of an intrinsic chip are represented by equivalent temperatures: T_g of r_{gs}, and T_d of g_{ds}. Noise contribution of ohmic resistances r_s, r_g and r_d are determined by physical temperature T_a of a chip.

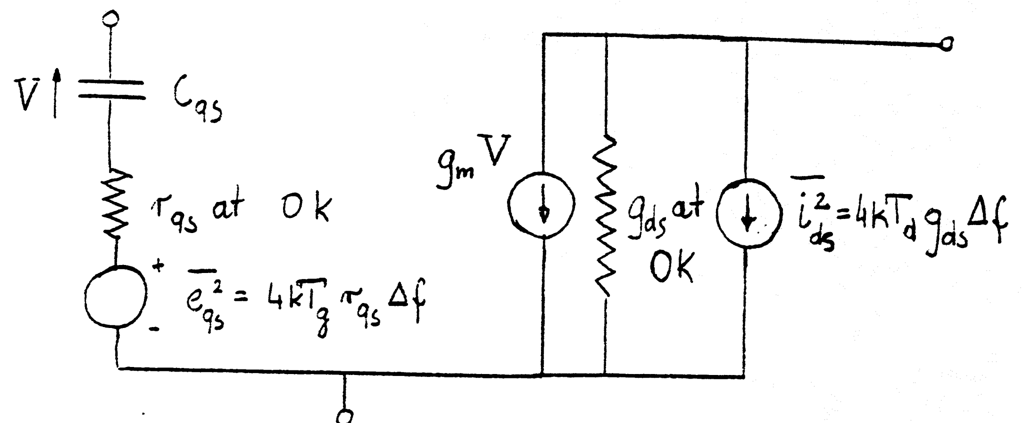


Fig. 3. Noise equivalent circuit of an intrinsic chip.

Straightforward substitution of equation (9)-(11) into the set of noise parameters defined by (2) (noise equivalent circuit of Figure 1.B) with the use of

$$y_{11} = \frac{j\omega\, C_{gs}}{1 + j\, r_{gs}\, \omega\, C_{gs}} \quad , \quad y_{21} = \frac{g_m}{1 + j\, \omega\, C_{gs}\, r_{gs}} \tag{12}$$

yields

$$R_n = \frac{T_g}{T_o}\, r_{gs} + \frac{T_d}{T_o}\, \frac{g_{ds}}{g_m^2} \left(1 + \omega^2\, C_{gs}^2\, r_{gs}^2\right) \tag{13}$$

$$g_n = \frac{T_d}{T_o}\, \frac{g_{ds}}{g_m^2}\, \omega^2\, C_{gs}^2 \tag{14}$$

$$cor = \rho \sqrt{R_n\, g_n} = \frac{T_d}{T_o}\, \frac{g_{ds}}{g_m^2} \left(\omega^2\, C_{gs}^2\, r_{gs} + j\omega\, C_{gs}\right) \tag{15}$$

Substitution of (13)-(15) into relations (7) gives

$$X_{opt} = \frac{1}{\omega\, C_{gs}} \tag{16}$$

$$R_{opt} = \sqrt{\left(\frac{f_t}{f}\right)^2 \frac{r_{gs}}{g_{ds}}\, \frac{T_g}{T_d} + r_{gs}^2} \tag{17}$$

$$T_{min} = 2T_o\, g_n \left(R_{opt} + r_{gs}\right) =$$

$$= 2\, \frac{f}{f_t} \sqrt{g_{ds}\, r_{gs}\, T_g\, T_d + \left(\frac{f}{f_t}\right)^2 r_{gs}^2\, g_{ds}^2\, T_d^2} +$$

$$+ 2\left(\frac{f}{f_t}\right)^2 r_{gs}\, g_{ds}\, T_d \tag{18}$$

$$g_n = \left(\frac{f}{f_t}\right)^2 \frac{g_{ds} T_d}{T_o} \quad (19)$$

and

$$\frac{4NT_o}{T_{min}} = \frac{2}{1 + \frac{r_{gs}}{R_{opt}}} \quad (20)$$

where

$$f_t = \frac{g_m}{2\pi C_{gs}} \quad (21)$$

The expression for available gain may be written in the form dual to that introduced in [37]:

$$\frac{1}{G_a} = \frac{1}{G_{amax}} + \frac{g_g}{R_g} \left| Z_g - Z^G_{opt} \right|^2 \quad (22)$$

where Z^G_{opt} stands for the generator impedance realizing maximum available gain. For an equivalent circuit of an intrinsic chip (Figure 3) G_{amax}, g_g and Z^G_{opt} are given by

$$G_{amax} = \left(\frac{f_T}{f}\right)^2 \frac{1}{4 g_{ds} r_{gs}} \quad (23)$$

$$g_g = \left(\frac{f}{f_T}\right)^2 g_{ds} \quad (24)$$

$$Z^G_{opt} = r_{gs} + j \frac{1}{\omega C_{gs}} \quad (25)$$

Finally, using the definition of noise measure (8) and expressions (14), (16)-(19), (22), (23)-(25) one may search for generator impedance Z^M_{opt} which minimizes the value of noise measure. The result is

$$X^M_{opt} = X^G_{opt} = X_{opt} = j \frac{1}{\omega C_{gs}} \tag{26}$$

$$R^M_{opt} = r_{gs} \left\{ \sqrt{\left(\frac{T_g}{T_d} - 1\right)^2 + \frac{R^2_{opt}}{r^2_{gs}} - 1} - \frac{T_g}{T_d} \right\} \tag{27}$$

$$= r_{gs} \left\{ \sqrt{\left(\frac{T_g}{T_d} - 1\right)^2 + 4G_{amax} \frac{T_g}{T_d}} - \frac{T_g}{T_d} \right\}$$

where R_{opt} and G_{amax} are given by (17) and (23), respectively. Minimum value of noise measure may be obtained by substituting appropriate relations into (8).

C. Approximations and Discussion

The expressions derived in previous section are simple and easily interpretable. They assume even simpler form if certain conditions are satisfied. Specifically, if (compare equation (17))

$$\frac{f}{f_T} \ll \sqrt{\frac{T_g}{T_d} \frac{1}{r_{gs}\, g_{ds}}} \tag{28}$$

then

$$R_{opt} \gg r_{gs}$$

and the expression for R_{opt} and T_{min} may be approximated by

$$R_{opt} \simeq \frac{f_T}{f} \sqrt{\frac{r_{gs}\, T_g}{g_{ds}\, T_d}} \tag{29}$$

$$T_{min} \simeq 2 \frac{f}{f_T} \sqrt{g_{ds}\ T_d\ r_{gs}\ T_g} \tag{30}$$

Consequently,

$$\frac{4NT_o}{T_{min}} \simeq 2 \tag{31}$$

The frequency dependence of noise parameters given by (16), (19), (29) and (30) is the same as assumed in [23] for the purpose of design of amplifiers at frequencies other than the frequency of measurement of noise parameters. Under this approximation, the noise parameters R_{opt}, T_{min}, and g_n are functions only of $\frac{f}{f_T}$ and products $g_{ds}\ T_d$ and $r_{gs}\ T_g$, which could be considered as noise constants if values of intrinsic gate resistance and drain conductance are not precisely known.

Another interesting limiting case is for $T_g \rightarrow 0$. Then only a current noise source in the drain uncorrelated with the gate current noise source exists and

$$R_{opt} \simeq R^M_{opt} \simeq R^G_{opt} = r_{gs} \tag{32}$$

$$T_{min} \simeq 4\left(\frac{f}{f_T}\right)^2 r_{gs}\ g_{ds}\ T_d \tag{33}$$

and

$$\frac{4NT_o}{T_{min}} \simeq 1 \tag{34}$$

It is rather surprising to discover that the noise representation of Figure 1.A with only $\overline{i_2^2}$ noise source present ($G_1 = 0$ or $T_g = 0$) is equivalent to the representation of Figure 1.B with $\overline{e_n^2}$ and $\overline{i_n^2}$ noise sources being perfectly correlated. That is, $\rho = y_{11}/|y_{11}|$ and consequently $4NT_o = T_{min}$.

If the noise parameters of a FET (MODFET) can be described by the model, then the measured ratio of $\frac{4NT_o}{T_{min}}$ must satisfy

$$1 \le \frac{4NT_o}{T_{min}} \le 2 \tag{35}$$

at all frequencies. The left hand side inequality is quite fundamental (compare equation (6)), while the right hand side is a limitation of the model only. The parameter N is rather sensitive to measurement errors [27] and, therefore, not always the value of $4NT_o/T_{min}$ by itself may provide useful information. If, however, it is accurately known, it provides a fast and easy check of the validity of the model and provides insight into the nature of noise sources within the transistor, without any knowledge of the transistor equivalent circuit or intervening lossless two-port (N and T_{min} are both invariant under lossless transformation at the input and/or output).

The inclusion of other elements of the equivalent circuit of a chip in this theory is straightforward, but results in rather complicated expressions. It may be viewed as parallel and/or series and/or cascade connection of a noisy two-port of an intrinsic chip with linear passive two-ports with thermal noise source only. This can be done quite generally in a computer routine (for example, [31], [42]) using relations published in [34] and [35].

It is interesting to observe two invariance properties of the model upon inclusion of source delay τ and drain to gate capacitance C_{dg}.

First, it is easy to show that the inclusion of delay τ alone will not change the final expression for noise parameters T_{min}, Z_{opt}, and g_n. Second, the expression for minimum noise measure M_{min} for a chip with τ and C_{dg} included will be the same as for an intrinsic chip of Figure 3.

III. Experimental Verification

The derivation of the expression for noise parameters of an intrinsic chip presented in the previous section is simple. The created model by proper choice of constants T_g, T_d may represent the noise processes in the intrinsic chip which at gate-source and drain-source terminals produce partially correlated noise currents (Figure 1.A) with purely imaginary correlation coefficient. The noise constants T_g and T_d need to be determined from measurement but if the equivalent circuit of a chip and its noise parameters are known, the determination is straightforward.

An equivalent circuit of FHR01FH HEMT is shown in Figure 4. The values of elements of the equivalent circuit were found from Fujitsu S-parameter data for both chip and packaged devices at bias V_{ds} = 2V, I_{ds} = 10 mA [38]. The comparisons between the S-parameters predicted from the model and those measured by Fujitsu for the packaged (FHR01FH) device are shown in Figure 5. DC characteristics and noise parameters of the FHR01FH device (lot #C923) for room and cryogenic temperatures were given in a previous paper [23]. Although the S-parameter [38] and noise parameters [23] were measured for different devices, an agreement between measured single-stage X-band test amplifier characteristics and computed with the help of the equivalent circuit of Figure 4 was excellent. As the discrepancies between measured and predicted results were about the same as differences between measured results for different transistors from the same lot (#C923), the equivalent circuit of Figure 4 was assumed to represent properly the transistors from that lot.

It is also interesting to point out a good agreement between the dc measured values of transconductance g_m and source-to-drain resistance $r_{ds} = 1/g_{ds}$ [23] with those determined from S-parameters [38]. For most GaAs FET's the value of r_{ds} determined from microwave measurements is by a factor of about 2 or more smaller than the dc measured value [39]-[41]. This phenomenon has been linked to the existence of traps in GaAs and/or at the interface between active and buffer layers [39], [41]. The absence of this phenomenon in the case of the FHR01FH HEMT points to a very low trap density. An excellent noise performance of FHR01FH and relative insensitivity to an illumination at cryogenic temperatures [23] corroborates this observation.

The knowledge of the equivalent circuit of Figure 5 and the noise parameters of the packaged device and its physical temperature allows the determination of noise parameters of an intrinsic chip. This process known as deembedding may be done with the help of general relations from [34], [35] which lend themselves naturally to computer implementation [31], [42].

The values of noise parameters of a FHR01FH transistor at different stages of deembedding are tabulated in Table I. The data for packaged device in the first row of Table I are the same as published in [23]. The data in subsequent rows were obtained by removing the influence of the package parasitics (second row), the gate, drain and source parasitic resistances (third row) and finally the gate-to-drain capacitance (fourth row). For room temperature the elements of the equivalent circuit of Figure 4 were used. For cryogenic temperature the transconductance g_m and drain-to-source resistance r_{ds} were changed to 50 mS and 500 Ω, respectively. These values were obtained by multiplying the respective values of g_m and r_{ds} from Figure 5 by the ratios determined from measurement of their d.c. counterparts (ref. (23), Fig. 6).

The values of noise parameters from the last row of Table I may now be compared with those resulting from expressions (16)-(19) of Section I for the best fit of equivalent temperatures T_g and T_d. This is done in

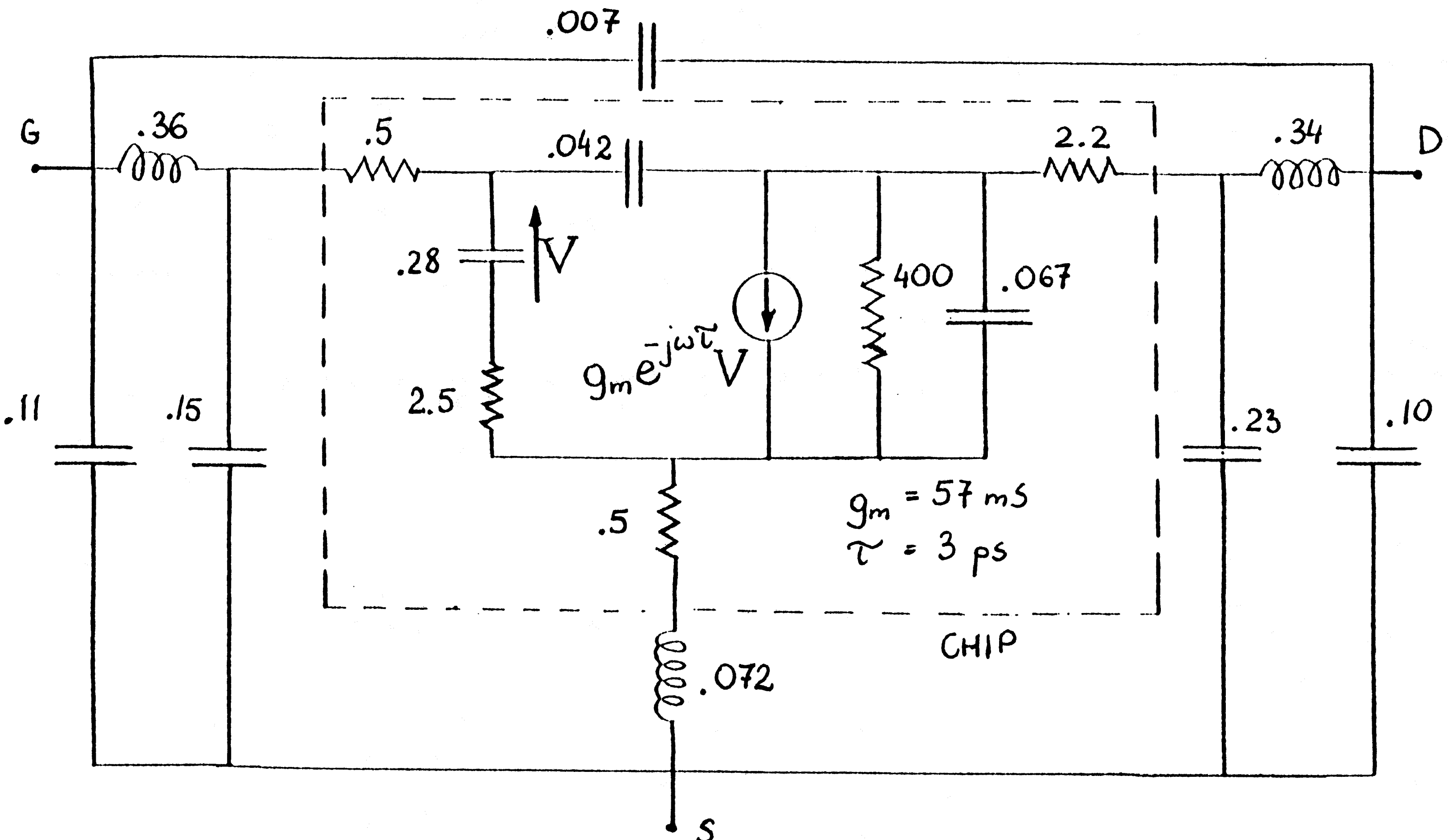
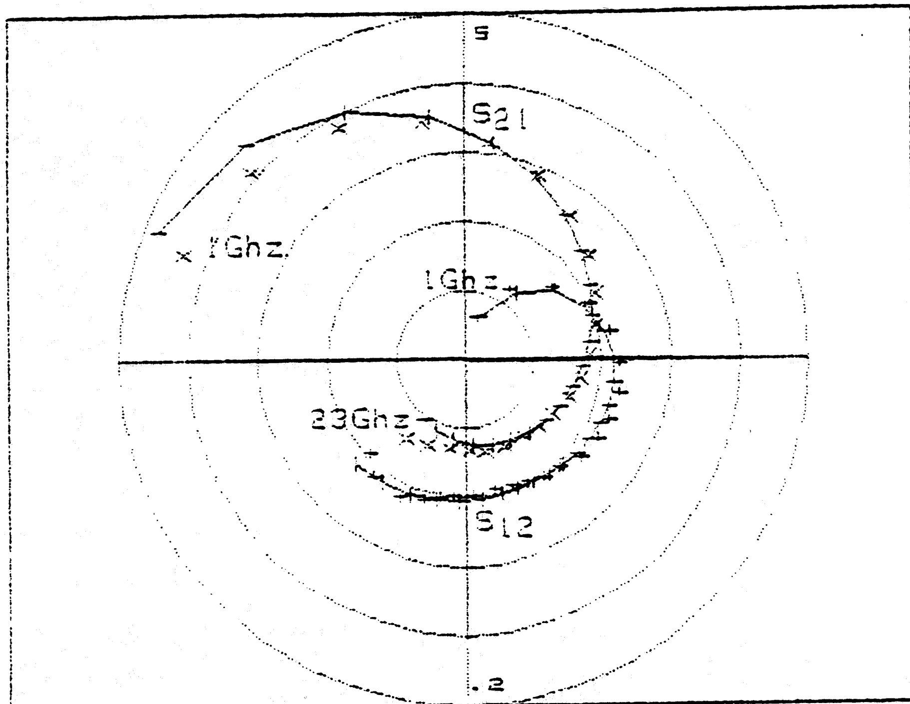


Fig. 4: Equivalent circuit of FHR01FH HEMT at T_a = 297 K, V_{ds} = 2 V, I_{ds} = 10 mA. Values of resistance, capacitance and inductance are given in ohms, picofarads and nanohenries.



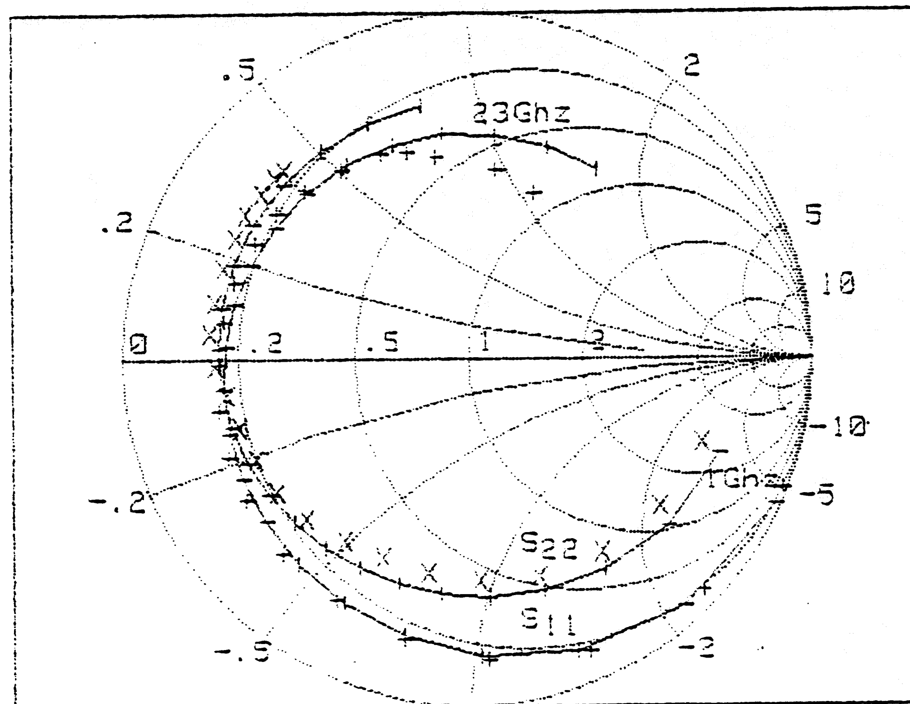


Fig. 5: Comparison between S-parameters of FHR01FH measured by Fujitsu [38] and those predicted from model of Figure 4. Lines with ticks are for computed data while crosses indicate measured points.

TABLE I. Noise Parameters of FHR01FH at Different Stages of Deembedding
$f = 8.5$ GHz, $V_{ds} = 2$ V

	$T_a = 297$ K, $I_{ds} = 10$ mA				$T_a = 12.5$ K, $I_{ds} = 5$ mA			
NOISE PARAMETERS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS
PACKAGED FET	78.0	10.5	17.5	9.4	10.0	4.4	17.0	2.6
FET CHIP	79.1	26.3	53.8	3.8	10.1	11.2	57.2	1.0
INTRINSIC CHIP WITH C_{gd}	64.6	20.7	53.7	3.8	8.1	8.8	57.2	1.0
INTRINSIC CHIP WITHOUT C_{gd}	65.6	26.3	59.5	3.0	8.2	11.4	65.2	.80

Table II. First, the consistency of the model may be verified by comparing the values of optimal source reactance, as both values were arrived at independently: one is derived from measured noise parameters [23] deembedded from the influence of the packaged HEMT parasitics, the other is simply $1/\omega C_{gs}$. The agreement is indeed remarkable, well within the range of estimated accuracy of noise parameter measurements [23]. The remaining three noise parameters, T_{min}, R_{opt}, g_n, of the model were determined by finding T_g and T_d which by the use of equations (17)-(19) provide the best fit in mean square sense to the deembedded measured noise parameters.

For the purpose of discussion to follow in Section III, the process of deembedding and fitting of T_g and T_d was repeated for $r_{gs} = 3.5\ \Omega$ and the results are also included in Table II.

The knowledge of the equivalent temperatures T_d, T_g and the elements of the equivalent circuit at a given ambient temperature T_a allows computation of noise parameters at any frequency. The computed results for FHR01FH device (packaged) and FHR01X device (chip) at 297 K and 12.5 K are shown in Figures 6, 7, 8 and 9, respectively. They are also compared with available experimental results.

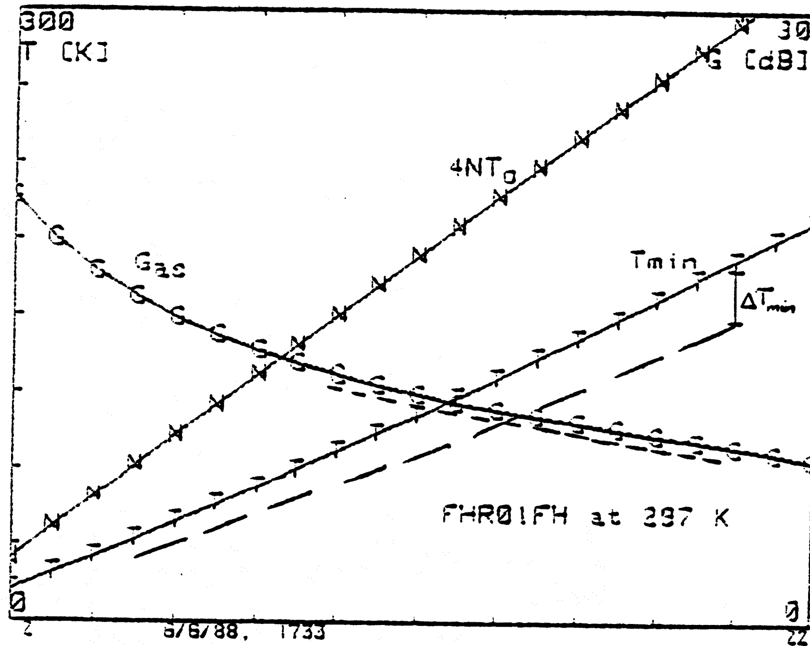
For the packaged device, the experimental results at 8.5 GHz are those of Table I (first row) and previously published in [23]. The cryogenic results at 4.8 GHz and 10.7 GHz are derived from multi-stage amplifier measurements also reported in [23]. The room temperature and cryogenic results at 15 GHz are to be reported in [43]. The room temperature data for T_{min} and G_{as} from FHR01FH (packaged) data sheet [38] are also included. Analysis of noise parameters data of FHR01FH published by Fujitsu [38] for the frequency range 4 to 20 GHz reveals good agreement for T_{min} and G_{as} (shown in Figure 6.A), excellent agreement for X_{opt}, and relatively poor agreement for R_{opt} and g_n. The FHR01FH Fujitsu data should, however, be viewed with caution as the invariant parameter $4NT_o$ computed from this data is not monotonically increasing function of frequency and for the frequencies 18 GHz and 20 GHz falls below the value of T_{min}, thus violating the fundamental inequality (6).

To the contrary, the Fujitsu noise data for FHR01X (chip) [38] from 4 to 20 GHz show good agreement with the prediction of the model, as is demonstrated in Figure 7. The model data are for the chip as outlined by a broken line in Figure 5, while the chip data from Fujitsu include the gate bonding wires. Again the model data are determined from a measurement of a single packaged device at 8.5 GHz, representing well the devices from lot #C923. It is not known if Fujitsu chip data are a representation of measurements of many samples or a single sample measurement data. In any case, an agreement between measured and predicted values of Z_{gopt} is excellent. The divergence in X_{opt} values which increases with frequency is due to the effect of bonding wires for Fujitsu data. The disagreement between measured and predicted values of T_{min}, g_n, and $4NT_o$, although larger than for Z_{opt}, can be easily explained by slightly smaller values of products $r_{gs}\ T_g$ and $g_{ds}\ T_d$ for Fujitsu sample (compare equations (16)-(19)). Also for comparison, a variation in noise temperature values at 20 GHz established for FHR01X's by Fujitsu [38] is given in Figure 7. The only experimental point for cryogenic FHR01X (chip) is derived from amplifier measurement reported in [23].

TABLE II. Comparisons of Noise Parameters of FHR01 Intrinsic Chip

f = 8.5 GHz

T_a K	Comments	T_{min} K	R_{opt} Ω	X_{opt} Ω	g_n mS	T_g K	T_d K
297	From Table I	65.6	26.3	59.5	3.0	-	-
	Model Best Fit for r_{gs} = 2.5 Ω	58.7	28.4	66.9	3.27	304	5514
	Model Best Fit for r_{gs} = 3.5 Ω	59.6	28.2	66.9	3.24	210	5468
12.5	From Table I	8.2	11.4	65.2	.80	-	-
	Model Best Fit for r_{gs} = 2.5 Ω	7.4	12.3	66.9	.87	14.5	1406
	Model Best Fit for r_{gs} = 3.5 Ω	7.7	12.0	66.9	.85	9.3	1379



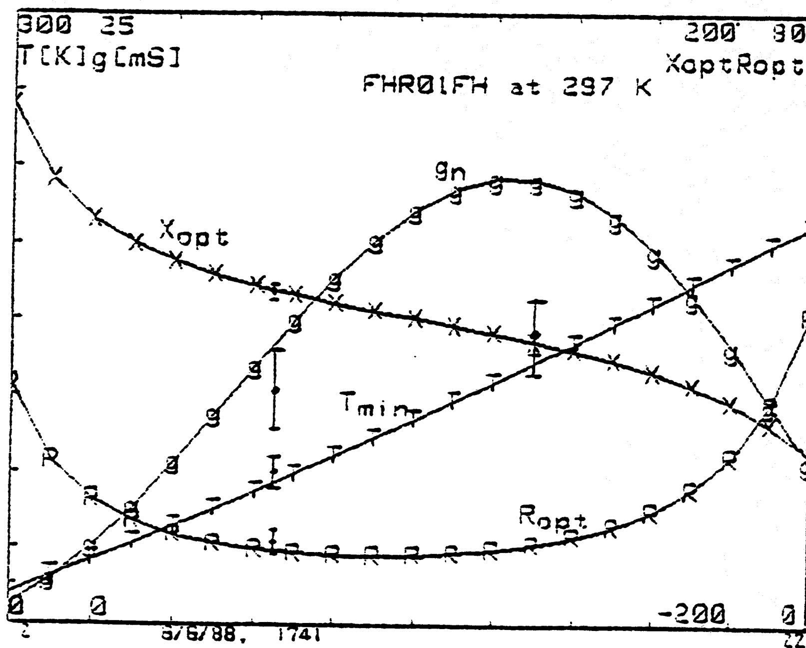
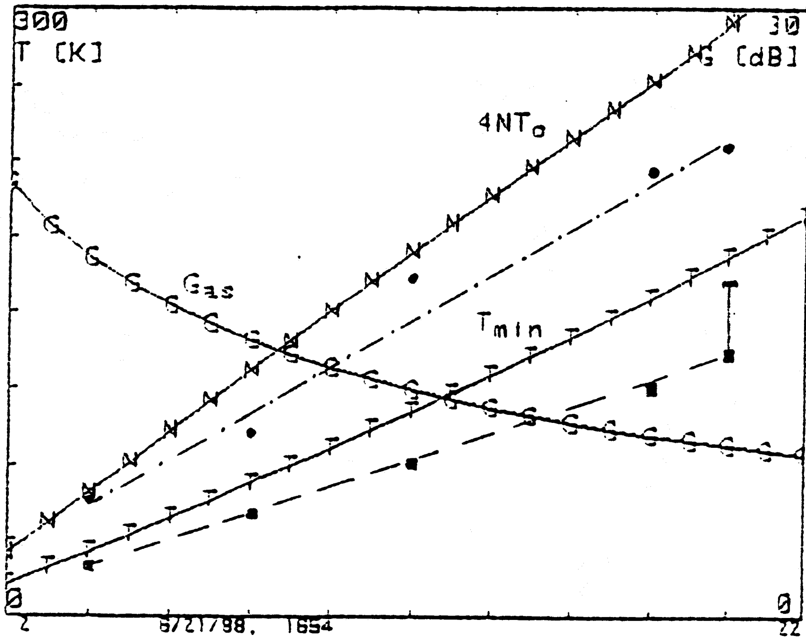


Fig. 6: Noise parameters and associated gain of FHR01FH HEMT at T_a = 297 K and V_{ds} = 2 V, I_{ds} = 10 mA. Solid lines indicate data obtained from the model using the equivalent circuit of Fig. 4, T_g = 304 K and T_d = 5514 K. Broken lines represent data obtained from Fujitsu data sheet [38]. Points indicate data from [23] and [43].



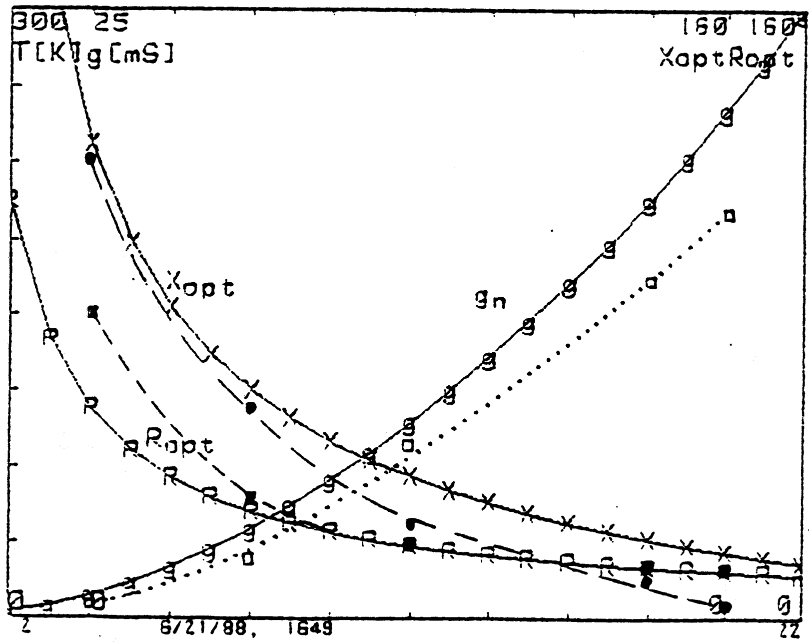
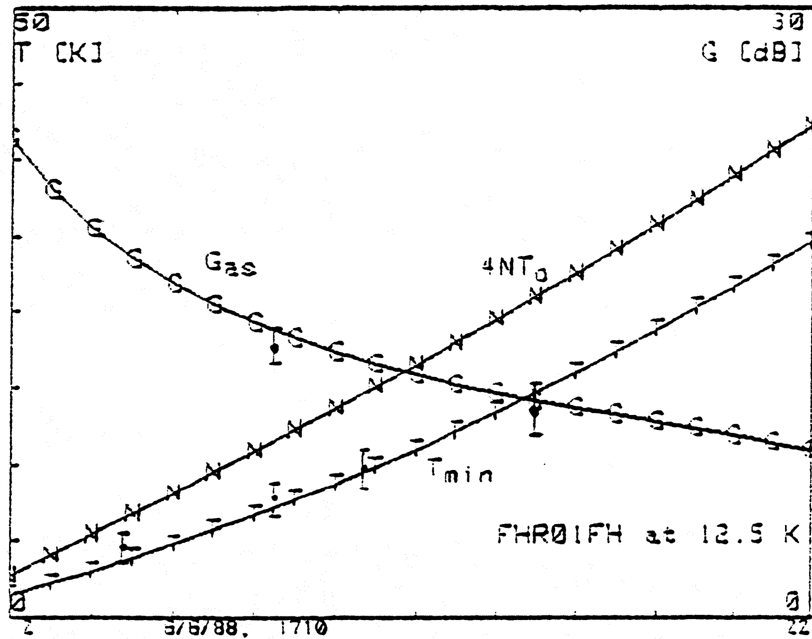


Fig. 7: Noise parameters of FHR01X (chip) HEMT at room temperature computed from the model. A part of the equivalent circuit of Figure 4, denoted by broken lines, was used with $T_g = 304$ K, $T_d = 5514$ K, and $T_a = 297$ K to compute the noise parameters (solid lines). Dotted and broken lines connect the points representing experimental results from Fujitsu data sheet [38]; see text for additional comments.



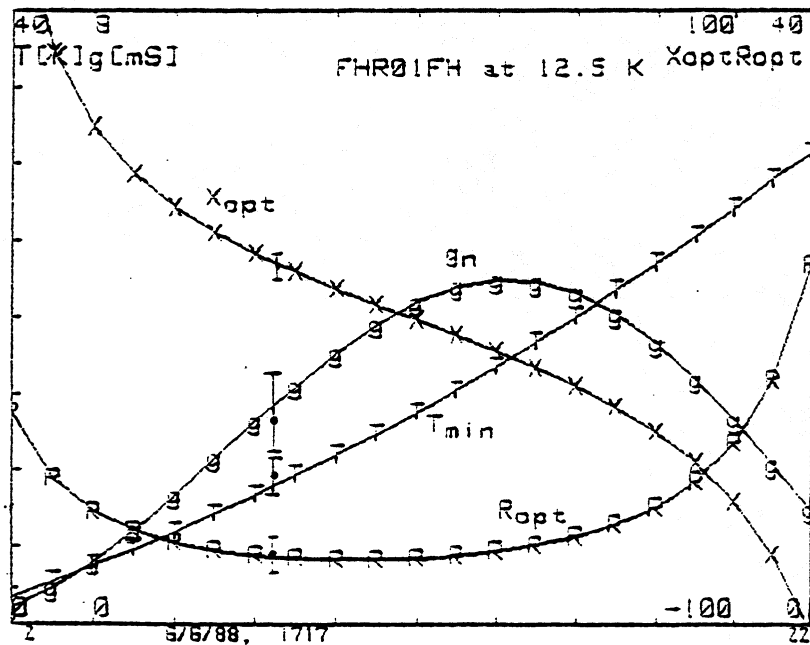


Fig. 8: **Noise parameters and associated gain of FHR01FH HEMT at T_a = 12.5 K and V_{ds} = 2 V, I_{ds} = 5 mA. Solid lines indicate data obtained from the model using equivalent circuit of Figure 4, g_m = 50 mS, r_{ds} = 500 Ω, T_g = 14.5 K and T_d = 1406 K. Points indicate experimental data from [23] and [43].**

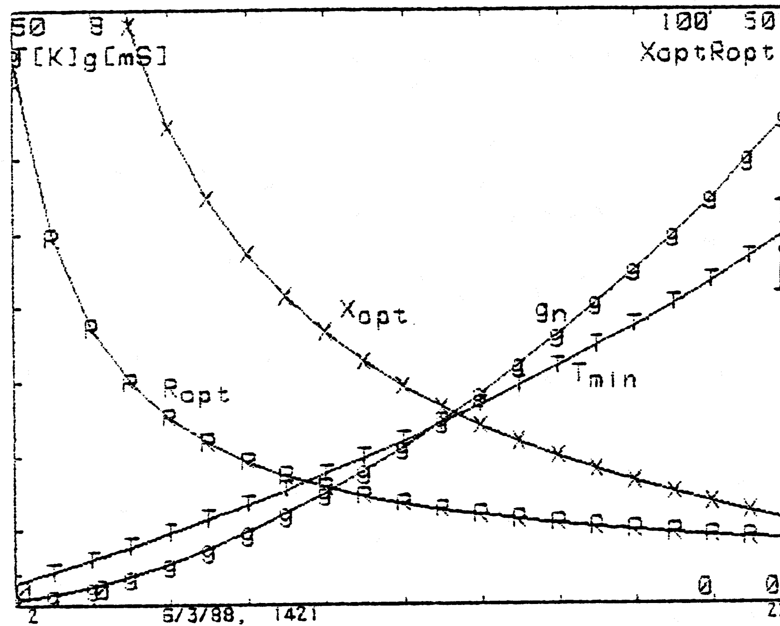
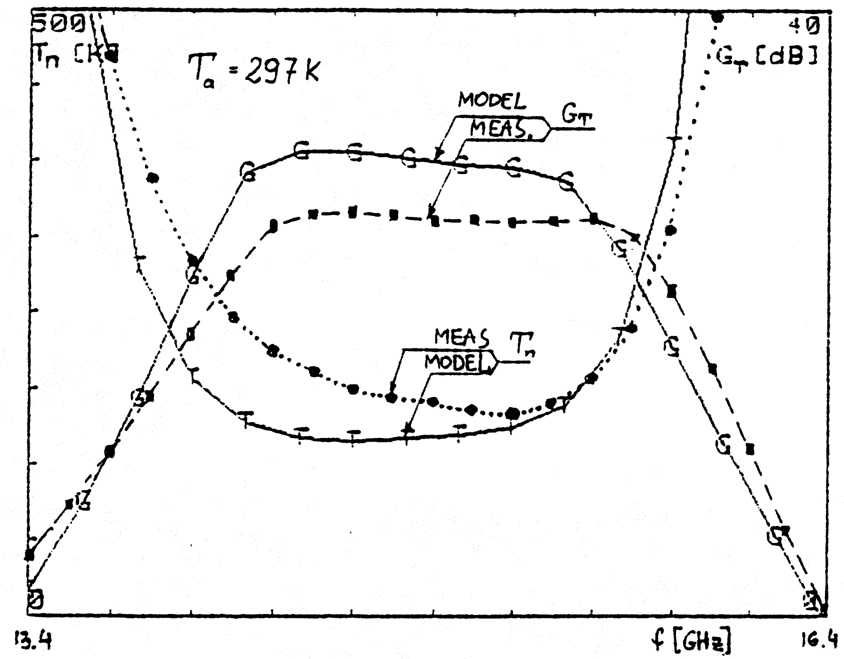


Fig. 9: Noise parameters of FHR01X (chip) HEMT at T_a = 12.5 K. The equivalent circuit of Figure 4 was used with g_m = 50 mS, r_{ds} = 500 Ω, T_g = 14.5 K and T_d = 1406 K. The experimental point at 22 GHz is determined from noise temperature measurement of multi-stage amplifier [23].

No direct measurement of four noise parameters of FHR01FH (lot #C923) at frequency other than 8.5 GHz was performed. The accuracy of the model was, however, indirectly checked by comparison of measured performance of multi-stage 15 GHz amplifier [43] with that predicted by the model. The comparison of measured and computed results at room and cryogenic temperatures is shown in Figure 10 demonstrating a good agreement. Also good agreement between model prediction and experiment could be obtained for a microstrip K-band amplifier as it is demonstrated in [23] (Figure 14.C). Although the method of modeling of frequency dependence of noise parameters used there is equivalent to this one under the condition (28), the results of both methods are within the boundaries established by model, circuit, and measurement uncertainties.

Our experimental data displayed in Figure 6 through Figure 10 were not taken for a single transistor but for many transistors from the same lot #C923. The repeatability of cryogenic noise temperature measurement at X-band for 20 transistors from the same lot was within ± 1.5 K, which is about the same as estimated accuracy of measurement at this frequency. Bearing this in mind, the agreement of measured and model predicted results over 4 to 22 GHz range should be judged excellent. At frequencies below 2 GHz, significant departure from the model may be expected due to the influence of 1/f noise.



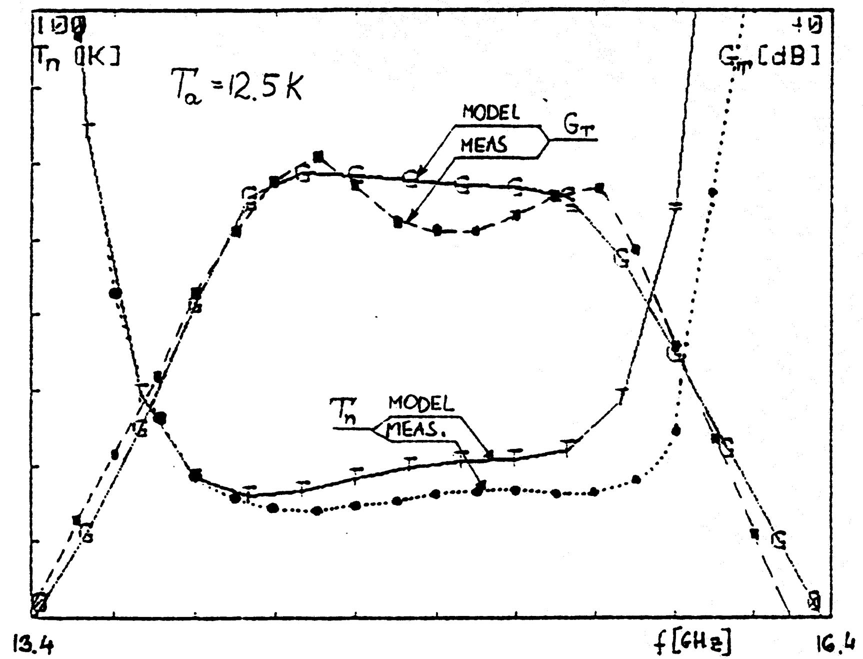


Fig. 10: Comparison between model prediction and measured performance of three-stage FHR01FH amplifier at 297 K and 12.5 K. At room temperature all transistors are biased at V_{ds} = 2 V, I_{ds} = 10 mA. At cryogenic temperature all transistors are biased at V_{ds} = 2 V, I_{ds} = 5 mA.

IV. Discussion of Results

A very interesting question to pose is what physical significance, if any, should be attached to the values of gate and drain equivalent temperatures, T_g and T_d. Clearly, T_d is an equivalent temperature of output impedance of FET if the gate at the chip terminal is open-circuited. The value of about 5000 K at room temperature (compare Table II) is very consistent with recently published results of equivalent noise temperatures of "resistor-like" AlGaAs-GaAs structures [44]. The values in excess of 1000 K were measured for average electric field intensity of about $4x10^3$ V/cm. If the data were extrapolated to the value of field intensity of about 10^4 V/cm (2 V across 2 μm gate-to-drain separation of FHR01 HEMT), the values of equivalent noise temperatures would be in several thousand Kelvins range. This quantitative agreement between different wafer and device structures [44], [45] encourages the interpretation of drain equivalent temperature as a physical parameter and not merely a fitting factor in a model.

An interpretation of gate equivalent temperature as a physical temperature of resistance r_{gs} poses greater difficulty. As it is clear from derivation of noise parameter expressions, an assignment of an equivalent gate temperature to the intrinsic gate resistance can model any noise process within a FET which produces a perfectly correlated short-circuit noise currents at input and output with purely imaginary correlation coefficient. However, any noise generating mechanism postulated by other method of analysis [1]-[11] will produce current noise sources at intrinsic chip terminals which can always be split into a pair of perfectly correlated current noise sources with purely imaginary correlation coefficient at gate and drain terminals and a single uncorrelated current noise source at a drain terminal. Thus, random variations of depletion layer boundary (channel "breathing" [5]), random variation of a quantum well width, random variation of sheet density of 2 DEG, etc. may all be viewed as application of a voltage noise generator in series with depletion layer capacitance. If r_{gs} correctly models the resistance through which the depletion layer capacitance is charged or discharged, then this noise source may be modeled by an assignment of a certain temperature T_g to the resistance r_{gs}.

It is a well known fact that an accurate determination of r_{gs} is very difficult [41]. The value of r_{gs} in any S-fitting algorithm may be easily traded for values of parasitic resistance r_g or parasitic resistance r_s and transconductance g_m. For example, the S-parameter data for FHR01FH of Figure 4 could be fitted well within measurement error by the circuit model of Figure 4 but with $r_{gs} = 3.5\ \Omega$. Repeating process of deembedding and fitting for this modified circuit results in as good a fit of noise parameters, but for very much different values of T_g (compare Table II). In view of discussion from Section II, this is not surprising as the noise parameters are function of products $r_{gs}\ T_g$ and $g_{ds}\ T_d$. Whether T_g may be treated as a fitting factor or a parameter with physical meaning is, therefore, determined by how accurately the value of r_{gs} is known.

The values of T_g in Table II for $r_{gs} = 2.5\ \Omega$ are about equal to the ambient temperature. By changing the value of r_{gs} within the measurement error, the best fit value of T_g can be made either larger or smaller. However, upon cooling the value of T_g decreases in proportion to ambient temperature, while the value of T_d does not (compare Table II). This observation strongly suggests that the source of noise producing perfectly correlated noise currents at gate and drain terminals is inherently thermal in origin. If this observation is correct, an upper bound could be established for r_{gs}. For example, in the case of FHR01FH HEMT, $r_{gs} \leq 2.5\ \Omega$, as the values of $r_{gs} > 2.5\ \Omega$ result in best fit values of T_g which are smaller than ambient temperature T_a (Table II).

More experimental data need to be gathered and analyzed to confirm or deny the assertion of the thermal origin of the noise source producing perfectly correlated noise currents at gate and drain with purely imaginary correlation coefficient. It is recognized, however, that there exists an anisotropy in electron dynamics in a HEMT channel, as the diffusion coefficient D is not only field dependent but also very different in directions perpendicular and parallel to the interface [10]. In analogy the parameters T_g and T_d could be interpreted as electron temperatures averaged over the length of the channel in direction perpendicular and parallel to the channel, respectively. Thus, electron heating by the electric field would be negligible in the direction perpendicular to the channel resulting in T_g values being close to the ambient temperature.

V. Comparison with Other Methods

The most elegant and detailed theory of noise properties of MESFET is that of Pucel, Haus and Statz [5]. It encompasses early work by van der Ziel [1], [2] and Baechtold [3]. Many later papers [7]-[10], [13] draw heavily on ideas presented in [5] as reviewed in a recent paper by Cappy [20]. Therefore, this work will be compared directly to the results of [5] and those reviewed in [20]. This comparison will be limited to the noise properties of an intrinsic chip only, as the inclusion of parasitic elements is computationally straightforward.

Equations (92a) and (92b) of [5], p. 247, correspond to equations (9) and (10) of this paper. Note that under the assumption $(\omega\, C_{gs}\, r_{gs})^2 \ll 1$, simple equivalence relations can be established between frequency independent constants P and R of [5] and T_g and T_d. These are

$$R = g_m\, r_{gs}\, \frac{T_g}{T_o} \tag{36}$$

$$P = \frac{g_{ds}}{g_m}\, \frac{T_d}{T_o} + R \tag{37}$$

As a result, the correlation coefficient ρ_c in equation (11) is given by

$$\rho_c = -j \frac{g_m r_{gs}}{\sqrt{\frac{R}{P}}} \frac{T_g}{T_o} = -j \sqrt{\frac{R}{P}} \tag{38}$$

That is using notation of [5]

$$C = \sqrt{\frac{R}{P}} \tag{39}$$

The examination of (86) in [5], p. 243, reveals that C is not entirely dependent on constants R and P, as called for by (39).

Comparing further the expressions (16), (19), (29) and (30) which give the noise parameter of an intrinsic chip under the small frequency approximation with (95) of [5], p. 248, or (17)-(19) of [20], one finds them identical under equivalence relations (36), (37) and (39). In terms of K_g, K_c, and K_r constants [5], equivalence relations can be rewritten as

$$K_g = \frac{g_{ds}}{g_m} \frac{T_d}{T_o} \tag{40}$$

$$K_r = g_m r_{ds} \frac{T_g}{T_o} \tag{41}$$

$$K_c = 1 \tag{42}$$

It demonstrates that if (39) or (42) are not satisfied as called for in [5], the only difference in the noise parameter expression under small frequency approximations will be in X_{opt} because [5], [20]:

$$X_{opt} = \frac{K_c}{\omega C_{gs}} \tag{43}$$

Experimental data of Section II and other experiments [40] show K_c to be equal to unity within an experimental uncertainty. The example of Monte Carlo simulation presented in [20], Figure 5, gives $K_c = 1.25$. The values of K_c of about 2 or more given in Figures 23 and 24 of [5] should be, therefore, treated with caution. A qualitative explanation of this

discrepancy is quite simple. The correlation coefficient C in [5] is computed assuming that the modulation of charge due to random drain current variations occur only in "active" part of the depletion layer, while gate-to-source capacitance is computed for the whole depletion layer including edge effects (equation (33) in [5], p. 221). However, in any small signal model of a FET, the C_{gs}, across which the voltage controlling a current source is built, should represent only an "active" part of the depletion layer; the remaining capacitance should be a part of an embedding circuit.

While under small signal approximation, the model of Pucel *et al.* [5] and its extensions and improvements [20] are "nearly" equivalent in formal sense to the model of Section II, they reveal a different physical picture of noise phenomena. If the gate noise current of an intrinsic chip was indeed induced by drain current fluctuations, then the rate of decrease of T_d and T_g upon cooling should be about the same. The data of Table II do not confirm this observation as discussed in Section IV. More accurate experimental data should resolve this discrepancy as well as that of the expression for X_{opt}.

Recent work by Gupta *et al.* [18], [19] claims that the noise parameters over wide frequency range may be predicted from a single output noise power measurement at low frequency and knowledge of elements of FET equivalent circuit. In view of the results of Section II, III and IV of this paper, several comments need to be made.

First, it should be noted that in derivation of their expressions, (7)-(9) in [18], (1) in [19], the noise resistance R_n and correlation admittance Y_r do not possess usual meaning [28] as they are for "fictitious" FET in which C_{gs} and R_T (a sum of r_{gs}, r_g and r_s) were incorporated into input circuit and a voltage controlling a current source is built across open-circuit terminals (Figure 2 in [18]). This tends to obscure the unstated assumption of analysis [18] that R_T (which includes r_{gs}) is at temperature T_a = 290 K and, therefore, generates Johnson noise.

In our model the best fit of measured noise parameters of FHR01FH indeed results in the equivalent gate temperature T_g quite close to the ambient temperature T_a. The discussion of Section IV, however, indicates that this *a priori* assumption may lead to a large error if only a small error in estimation of r_{gs} and, therefore, R_T is present (compare data of Table II). As an illustration, the data for NE045 chip (Table I in [19]) were transferred into a set of noise parameters T_{min}, Z_{opt} and g_n. T_d and R_T were then fitted under the assumption T_g = 296 K. The results are presented in Figure 11. The maximum deviation of measured NE045 chip noise temperature and model prediction for $R_T = 4.8\ \Omega$ (see Figure 11) is only 13 K as compared with 26 K (Figure 2 in [19]) for Gupta's model in which $R_T = 7.1\ \Omega$ (Table II in [19]).

In their paper Gupta *et al.* [18] report no change in output noise power over frequency range from 30 MHz to 1.2 GHz. This is surprising since there is ample evidence for the influence of 1/f noise well into 1 GHz range for GaAs FET's (for example, [24], [46], [47]).

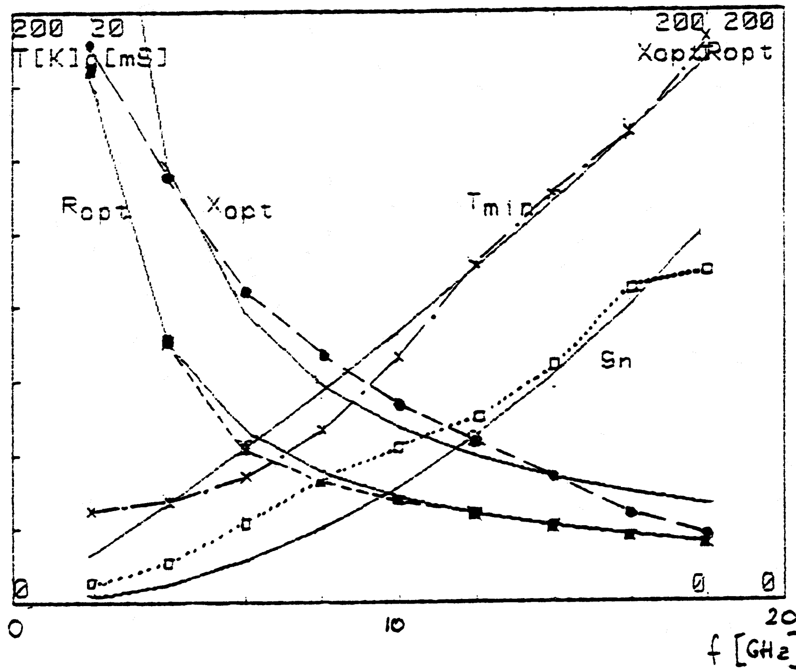


Fig. 11: Comparison between data for NE045 chip given in paper by Gupta and Greiling (Table I in [19]) and the present model. Under the assumption T_g = 296 K, r_{ds} = 450 Ω and g_m = 36.5 mS, the values of R_T nd T_d were best fitted using model expression for T_{min}, R_{opt} and g_n. The values of C_{gs} was best fitted using the expression for X_{opt}. These best fit values are: R_T = 4.8 Ω, C_{gs} = .27 pF and T_d = 2374 K. See text for additional comments.

In conclusion, the method of [18] may give good prediction of noise parameters if:

- the assumption of T_g = 290 K correctly represents gate current noise for a given R_T,
- the measured output noise power is devoid of the influence of 1/f noise,

and the conditions validating other approximations stated in [18] are satisfied.

Gupta and Greiling [19] discuss the case of lossy embedding (package) on the noise parameters of a chip. The chip and the embedding circuit discussed can be represented by a cascade connection of two two-ports (Figure 1 in [19]). In this case the process of deembedding (embedding) can be described by a simple matrix equation [34], [35] as, for example, applied in [27] or implemented into a computer program [31], [42]. While the choice of a particular method of deembedding (embedding) is a matter of preference, it is difficult to see how good agreement could have been obtained between the noise parameters of a NE045 chip and those of packaged devices (Table I in [19]) by any embedding procedure.

If the invariance of T_{min} (F_{min}) is preserved as clearly demonstrated by the data of Table I in [19], then the parameter $4NT_o$ should have remained invariant as well. But the same data reveal that, for example, at 14 GHz the values of ratio $\frac{4NT_o}{T_{min}}$ (compare expression (35) of Section II.C) are 1.9 and 7.1 for a chip and packaged device, respectively. Futhermore, the same ratios at 18 GHz are 1.3 and .25 for a chip and packaged device, respectively. Not only do these values differ by a factor of several, but also the ratio at 18 GHz for the packaged device violates by a factor of four the fundamental inequality (6). Large errors must be involved in measurement of Γ_{opt} and R_n for the packaged device and any conclusions drawn from that data should be treated with caution.

One more comparison of the results of Section III can be made with those of recent paper by Oxley and Holden [16]. They find experimentally that the noise figure and its departure from linear frequency dependence is strongly dependent on gate width for otherwise identical devices. They explain that in terms of distributed model of a FET, finding that the departure from a linear dependence occurs at frequency at which the gate width is about 1/20 of an average wavelength of first two lowest order propagation modes. This frequency in their data could be as low as 20 GHz for 100 μm gate width, .3 μm gate length device (Figure 7 in [16]). To the contrary, a recent theoretical study [48] predicts no significant difference between lumped element model and distributed model for 100 μm, .25 μm device for up to 50 GHz. In our model a significant departure from linear dependence of noise temperature on frequency will occur at about

$$f_c \simeq \frac{g_m}{2\pi C_{gs}} \sqrt{\frac{T_g}{T_d} \frac{1}{r_{gs} g_{ds}}} \tag{44}$$

which follows directly from inequality (28). This is confirmed by experimental data for FHR01FH HEMT (which is 200 μm wide) of Section III indicating absence of distributed type effects for the device up to 22 GHz. The experimental data of [16] can, however, be qualitatively explained by a wafer non-uniformity. Both T_{min} for $f \ll f_c$ (equation (30)) and f_c (equation (44)) will remain invariant upon change in the gate width if the values of the ratio g_m/C_{gs}, the product $r_{gs}\, g_{ds}$, and equivalent temperatures T_g and T_d remain invariant under the condition of a constant current per unit gate width. The presence of non-uniformities at the interface between active and buffer layers and/or variations in epilayer thickness will affect much stronger the values of g_m [7], g_{ds} and T_d than those of C_{gs}, r_{gs} and T_g. In this case for increasing gate width, the ratio $\frac{g_m}{C_{gs}}$ is likely to go down while the product $g_{ds}\, r_{gs}$ and T_d are likely to go up. That is, T_{min} increases (equation (30)) and f_c decreases (equation (44)) providing a qualitative explanation of the experimental data of [16].

VI. Conclusions

This paper presented a new approach to the modeling of noise behavior of FET's and MODFET's over wide frequency range. Simple closed form expression for minimum noise temperature T_{min}, optimal source impedance Z_{opt}, noise conductance g_n, and source impedance Z^M_{gopt} minimizing noise measure were derived. These were found to be functions of the elements of a small signal equivalent circuit of a FET and two frequency independent constants, named equivalent gate and drain temperatures. The equivalent temperatures in the example of FHR01FH MODFET were demonstrated to be independent of frequency in the frequency range in which 1/f noise is negligible. Thus, the model allows prediction of noise parameters for a broad frequency range from a single frequency noise parameter measurement. The same example of FHR01FH MODFET presents a different physical picture of the source of the gate noise in MODFET's than that usually accepted, showing that to be of thermal origin only. More accurate experiments for both FET's and MODFET's should resolve this question. The equivalence relations and/or conditions between this new approach and other relevant studies were established, allowing in turn to reconcile the differences between previously existing models. The model uses only circuit theory concepts and, therefore, it is very easy to implement in any CAD and/or CAM package. Finally, it is hoped that it may be used by device manufacturers as a standard noise description of commercial devices.

VII. Acknowledgement

The author would like to thank Dr. Sander Weinreb of the National Radio Astronomy Observatory for his helpful comments. Also, the excellent experimental and technical assistance of William Lakatosh is greatly appreciated.

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