327 MHz AND 610 MHz, LOW-NOISE, FET AMPLIFIERS

R. HARRIS AND W. LAKATOSH

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I. Introduction

This report describes the construction and testing of a low-noise (approximately 0.4 dB noise figure or 28K noise temperature) GASFET amplifier designed for room temperature operation. The amplifier is easy to construct, operates from a single +8 to +15 volt supply, and provides approximately 33 dB gain.

Simultaneous noise and power match at the input is achieved by utilization of feedback within the FET device. The power match requires that the output tank circuit of the first FET be tuned to a higher frequency than the frequency for best input match; this results in the gain peaking at a higher frequency than input match. A broadband output match is achieved with a built-in attenuator pad.

II. Initial Assembly

After fabricating the circuit board, certain precautions must be taken to reduce the possibility of oscillations due to ground loops on the surface of the board. Short lengths of #22 tinned-copper wire must be inserted through the seven 0.031" diameter holes in the circuit board. Solder both sides of the board and remove excess wire.

It is important throughout construction of this amplifier to use good quality 2% silver-bearing solder along with appropriate flux (see Parts List).

Mount the nine chip capacitors, carefully avoiding the application of excessive heat. The 680 pF chip capacitor for the MGF-1412 source bypass should be mounted with the capacitor's inner surface on a line with the outside etched surface on the board. This is illustrated on NRAO Drawing No. A53201M013, detail C. The 680 pF chip capacitor for source bypass of MGF-1402 should have the outside surface on a line with this etched surface (refer to detail C).

Next, mount all the D.C. bias components including the two R.F. chokes (L₁, L₂) which form a D.C. return on the amplifier input. Do not mount the source resistors, transistors, or inductors (L₃, L₄) at this point.

Place partially completed board into modified chassis (see NRAO Drawing Nos. A53201M001 and A53201M002). Do not mount input and output connectors or feed-thru bypass capacitor. Secure board to chassis rails using eight #2-56 screws. Cut center pin and Teflon on SMA connectors as shown on NRAO Drawing No. A53201M003, detail C.

Prepare inductors L₃ and L₄, referring to NRAO Drawing No. A53201M013. The input inductor L₃ is eight turns, #26 AWG, .150" diameter, approximately .155" long, formed as shown in detail A. It is very important to wind this inductor in
a counter-clockwise direction (CCW). Inductor \( L_4 \) consists of eight turns, #26 wire, .150 diameter, .155" long, formed as shown in detail B. This inductor must be wound in a clockwise direction (CW).

Prepare both transistors by cutting gate length to .050"; do not cut drain lead.

III. Final Assembly

Use one of the previously prepared MGF-1412 GASFET's and center the transistor body between the two 680 pF source bypass capacitors \((C_2, C_3)\). Precut the source leads to allow a 50 to 100% overlap on the source bypass capacitors; then solder leads in place. Place toroid core \((FB_1)\) on drain lead and position drain lead to expose approximately .130" of length. Solder in place. The toroid core may be fixed in place with a drop of GC Electronics Q-Dope, catalog #37-2.

Repeat above procedure using MGF-1402.

Place inductor \( L_1 \) into position assuring the coil is wound in a counter-clockwise direction; then solder in place. At this time source resistor \( R_1 \) may be soldered along with resistor \( R_6 \).

Inductor \( L_4 \) may now be mounted, assuring the coil is wound in a clockwise direction. Mount the inductor on an angle of approximately 45° with a line through the center of the two transistors (refer to NRAO Drawing No. A53201M013, detail C). This completes the amplifier assembly.

IV. Testing

A scalar network analyzer similar to the Wiltron Model 560A will be necessary for the next phase.

The object is to achieve a return loss greater than 15 dB over the band of interest. For NRAO's purposes, the passband was 312 to 342 MHz, and gain at mid-band was approximately 33 dB.

The tuning elements available are the gate inductors \((L_3, L_4)\), the source resistors \((R_1, R_6)\), and the position of the first-stage source bypass capacitors. Changing the center-to-center distance of \( C_2 \) and \( C_3 \) provides some variation in first-stage source inductance. The output attenuator, provided to terminate the second stage over a wide frequency range, can be used to set overall amplifier gain.

The gate inductors should be positioned close to the surface of the board. Coils can be compressed or expanded, and their position relative to the board surface can be varied while observing the return loss on the network analyzer.

If sufficient bandpass is difficult to attain, the source resistor may be adjusted to produce slightly lower gain and slightly more bandwidth. If necessary, the first-stage source inductance may be varied by readjusting the center-to-center distance of the source bypass capacitors.
After the desired return loss and gain characteristics have been achieved, the amplifier should be tested for any sign of high frequency oscillations.

The input should be terminated with approximately 20 cm sliding short. While varying the input source impedance, there should be no sign of instability. The amplifier should be stable at all phase angles, terminated or unterminated. The cover plate should be installed and securely fastened while testing.

The noise characteristics of this amplifier are rather broad. After proper return loss and gain characteristics are obtained, no attempt should be made to minimize noise temperature. The ultimate noise temperature is a function of the particular input transistor chosen.

V. 610 MHz Amplifier

The materials and assembly procedures used for a 610 MHz amplifier are very similar to that used for the 327 MHz, low-noise, FET amplifier described here. The only changes required are to the input inductors $L_3$ and $L_4$ of the first and second stages; these are shown in attached drawings for both 327 MHz and 610 MHz. The gain, noise temperature, and input return loss for both frequencies are shown in Figures 1 and 2.
Fig. 1. Noise Temperature and Gain Characteristics of 327 MHz Amplifier.
Fig. 2. Noise Temperature and Gain Characteristics of 610 MHz Amplifier.
NOTES

1. REWORK OF CHASSIS # PCC170-075-1

2. DEBURR INSIDE EDGES OF CHASSIS.

NATIONAL RADIO ASTRONOMY OBSERVATORY

VLBA

PROJ: 327 MHz FE.  327 MHz CHASSIS

TITLE: NOTE 1

MATERIAL: NONE

ANGLES: 8 DEGREES

DRAWN BY: N. DILL

DRAWN BY: A. H. W.
2 REQ

NATIONAL RADIO ASTRONOMY OBSERVATORY
VLBA

PROJ: 327 MH F.E
TITLE: RAIL
MATERIAL: ALUM
FINISH: ALUMINUM
SHEET NUMBER: 4
DRAWING NUMBER: A53201M002

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES TOLERANCES
ANGLES:
3 PLACE DEC.(MM). ± 0.01
2 PLACE DEC.(IN) ± 0.001
1 PLACE DEC. (G) ± 0.2
ITEM "A" WITH DIELECTRIC AND CENTER CONDUCTOR SHORTENED
**DETAIL B - 2ND STAGE**

MATERIAL: #26 AWG ENAMEL

TOROID CORE TO BE FIXED IN POSITION WITH GC ELECTRONICS Q-DOPE CAT. NO. 37-2.

**DETAIL C - COMPONENT LAYOUT**

*NOT TO SCALE:*

**DETAIL A - 1ST STAGE**

MATERIAL: #26 AWG ENAMEL

8 FULL TURNS

8 FULL TURNS

---

NATIONAL RADIO ASTRONOMY OBSERVATORY

VLBA

PROJ:

327 MHE FET COMPONENT LAYOUT

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

ANGLES

3 PLACE DEC.(mm) ±
2 PLACE DEC.(mm) ±
1 PLACE DEC. (°) ±

MATERIAL: DRAWN BY: BLAKATO

FINISH: DESIGNED BY:

APPROVED BY:

DATE: 10/21/93

DATE:

DATE:

SHEET NUMBER:

DRAWING NUMBER: A53701M0013

REV.

SCALE: NONE
NOTES
1. ALL RESISTORS 1/8W 5%
2. C2, C3, C9, C10 ARE 680pf.
**DETAIL B - 2ND STAGE**

MATERIAL: *26 AWG ENAMEL*

**DETAIL A - 1ST STAGE**

MATERIAL: *26 AWG ENAMEL*
NOTES
1. ALL RESISTORS 1/8W 5%.
2. C2, C3, C9, C10 ARE 680pf.
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<th>ITEM</th>
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<td>L1, L2, L3</td>
<td>R.F. CHOKE, .22 uH</td>
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