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LOW-NOISE, 4.8 GHz, COOLED GaAs FET AMPLIFIER

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Low-Noise, 4.8 GHz, Cooled GaAs FET Amplifier

R. D. Norrod and R. J. Simon

I. Introduction

This report describes the design procedure, construction, and testing of a microwave transistor amplifier that operates at a physical temperature of 15 Kelvin. The amplifier was designed to operate reliably on a closed-cycle refrigerator in various radio astronomy receiving systems. Approximately twenty of these amplifiers have now been constructed and tested at the NRAO - Green Bank laboratories. The frequency range of interest is 4.6 to 5.1 GHz and the amplifiers typically provide 31 to 34 dB of gain with minimum noise temperature of 15 to 18 Kelvin (Figure 1). A photograph of a completed amplifier is shown in Figure 2.

The construction technique used in this amplifier is similar to that used in amplifiers at higher frequencies by the NRAO Central Development Labs [1], [2], [3]. The major characteristics of the design are:

1) The three-stage amplifier uses commercially available, packaged, GaAs field-effect-transistors.

2) An input isolator and a flange mounted output attenuator are incorporated to improve the amplifier match and stability.

3) A coaxial geometry with a round center conductor in a square outer conductor is used. Tuning of the amplifier performance is achieved by adjusting the position of low impedance slugs

on a 50 ohm center conductor and by adjusting the length of small diameter wires used as series inductors. Input and output DC blocks are formed by quarter-wave reentrant transmission lines, and chip capacitors are used for interstage DC blocks.

II. Design Process

The first step in the design of this amplifier was to select a transistor. Based on results at the NRAO CDL, three transistor types were selected for testing and evaluation at cryogenic temperatures: the Nippon Electric NE75083, the Mitsubishi MGF1412, and the Fujitsu FSC10FA. Samples of each of these types were mounted in a single-stage amplifier such that the impedance presented to the transistor gate and drain could easily be adjusted [3]. The minimum noise temperature was then measured for at least five values of the real part of the impedance seen by the FET gate, and at several bias points. From this data, and an accurate circuit model, the transistor noise parameters can be calculated [2]. Figures 3, 4, and 5 show the variation of minimum noise temperature versus generator resistance for one of each of the transistor types, at 13 Kelvin. Figure 6 shows the performance of a Mitsubishi FET at 300 Kelvin. The room temperature and cryogenic performance of the three types of transistors is summarized in Table 1.

In order to do the curve fitting illustrated in Figures 3 through 6, and to calculate the noise parameters given in Table 1, it was necessary to develop an accurate model of the amplifier

matching and bias networks. Figure 7 shows the model used for the input and output networks. In this model, XF1 is the quarter--wavelength tuning slug, XF2 is the variable length 50 ohm line, XF3 is the open-circuited quarter-wavelength DC block, XF4 is the high impedance line used to realize a series inductor, and XF5 is the quarter-wavelength bias choke. C1, C2, C3, and C4 are fringing capacitances, and C5 is a chip bypass capacitor. A closed form approximation formula was used to calculate the values of the fringing capacitances [4]. Analysis of the circuit model was accomplished using the NRAO microwave circuit analysis program, FARANT.

Based on the results in Table 1, it was initially decided to use the NE75083 FET for the first stage of the three stage amplifier. At 13 Kelvin, R_{opt} is higher and G_n is lower than the other two FETs, desirable because the amplifier noise response will be broader in frequency. The NEC FET costs three times as much as the other FETs, so it was decided to use it only in the amplifier first stage. Since the MGF1412 has been used in many NRAO cooled amplifiers, we decided to use it for the second and third stages. The early design work was done and several amplifiers built with this configuration. However, a later batch of NEC FETs purchased had much poorer performance, and later we found that NEC had discontinued manufacturing the NE75083, so we then redesigned the amplifier using the MGF1412 in all three amplifier stages. The design information in this report is for that, three MGF1412, configuration.

A circuit model for the FET was required in order to do the multi-stage amplifier simulations using FARANT. The starting point was a model used at NRAO - CDL (Figure 8) and element values obtained by M. Pospieszalski [2] from manufacturer's data on the FSC10FA FET. Figure 9 shows S_{11} and S_{22} plotted from manufacturer's data for the MGF1412 and calculated from Model 1. As expected, they do not match well, so we then proceeded to reoptimize the element values using the MGF1412 data.

The optimization procedure used was to minimize the difference between the magnitude and angle of the S-parameters calculated from Model 1 and the manufacturer's data. Equation 1 was used as the FARANT error function, summed over the 2 - 6 GHz frequency range at 2 GHz increments.

$$\sum_{\text{freq}} \sum_{i} \sum_{j} \left[\left| |S_{ij}|_{\text{manuf}} - |S_{ij}|_{\text{model}} \right| + \left| \frac{\angle S_{ij_{\text{model}}} - \angle S_{ij_{\text{manuf}}}}{180} \right| \right] \qquad (1)$$

First S_{11} and S_{22} were optimized, starting with the element values given in column (a) of Table 2, and letting elements 2, 4, 7, 18, and 20 vary. The results of this optimization were used as initial values while S_{12} and S_{21} were optimized, letting elements 1, 3, 5, 6, 8, 9, 17, and 19 vary. During the optimizations, it was found to be to some advantage to add resistances in series with the gate-source and gate-drain capacitances, yielding Model 2 (Figure 10). A final optimization of all four S-parameters was then done, letting all model elements vary. The

final element values are shown in column (b) of Table 2 and the resulting calculated S_{11} and S_{22} plotted in Figure 11. Agreement with S_{12} and S_{21} was also quite good. This model was used in all subsequent FARANT simulations.

Figure 12 shows the calculated and experimental performance of a single-stage amplifier. This figure illustrates the strong effect of any source lead inductance. The experimental data doesn't match the calculated data as well as desired, but if the experimental gain were increased uniformly by about 1 dB, then the match to a calculated curve would be fairly good for source inductance somewhere between 0.01 and 0.1 nH. During the multistage simulations, source inductance of 0.05 or 0.1 nH was used. The noise curves in Figure 12 agree fairly well, but the experimental curve is somewhat narrower than the calculated curve. The square-law detector used in the noise measurements tended to saturate at frequencies where the amplifier had both high gain and high noise, and this may account for the rapid increase in noise below 4.5 GHz. Another factor that should be pointed out is the way that the FARANT programs simulate the variation in the noise parameters with frequency. Because of the time involved, we usually measure the noise parameters only near the center of the frequency range of interest and use equations 2 through 5 to estimate the parameter variation with frequency.

$$T_{min}(f) = T_{min}(f_{meas}) \cdot \left(\frac{f}{f_{meas}}\right)^{a} \quad (2)$$

$$R_{opt}(f) = R_{opt}(f_{meas}) \cdot \left(\frac{f_{meas}}{f}\right)^{a} \quad (3)$$

$$X_{opt}(f) = X_{opt}(f_{meas}) \cdot \left(\frac{f_{meas}}{f}\right)^{a} \quad (4)$$

$$g_{n}(f) = g_{n}(f_{meas}) \cdot \left(\frac{f}{f_{meas}}\right)^{2} \quad (5)$$

Most of the work at NRAO-CDL has used a = 1. Based on my measurements here on transistors at 3.2 GHz and 4.8 GHz, a = 0.5 seems to fit better (at 13 Kelvin), and that is what was used in the simulations.

Figure 13 shows the interstage network model used in the FARANT multistage simulations. XF1 and XF6 are the high impedance lines used as tuning inductors, XF2 and XF4 are short lengths of 50 ohm line, and XF3 is the low impedance tuning slug. XF5 and C5 simulate the DC blocking capacitor, and C1 through C4 fringing capacitances.

The FARANT optimization routines were used to design the three-stage amplifier. Starting with the models described above, a two-stage amplifier was optimized. The output matching network

was fixed as that which had been selected experimentally. The following parameters of the input matching network were allowed to vary: the length and impedance of XF1, and the length of XF4. The following parameters of the interstage network were allowed to vary: the length and impedance of XF3, and the lengths of XF1 and XF6. The error function minimized was:

$$\text{ERROR} = \sum_{\text{freq}} \left[\left(\frac{2\ T_N}{\text{GAIN}} \right)^2 + e^{10(1-K)} \right] \tag{6}$$

This function tends to minimize the amplifier noise and maximize the gain while forcing the stability factor to stay greater than one. Once the two-stage performance was satisfactory, work began on optimizing the second interstage of a three-stage amplifier. The error function used was:

$$\text{ERROR} = \sum_{\text{freq}} \left[\left(\frac{T_{MIN}}{10} \right)^2 + e^{10(1-K)} + (V - \text{GAIN})^2 + \frac{34}{V} \right] \tag{7}$$

T_{MIN}, the amplifier noise achievable with an ideal input matching network, was used in the first term rather than T_N, the actual amplifier noise, because the amplifier input matching network dominates T_N and hides the effect of the interstage networks. V was one of the optimization variables. The third term in eq. 7 forces the gain to be constant over the frequency range, and the fourth term attempts to maximize that constant. The numerator of the fourth term was selected to equal the nominal value of V. Once a satisfactory second interstage network was found, an iterative process was started, where each of the matching networks

was re-optimized using the most recent values for the remaining networks. Only a couple of iterations were required, and Figure 14 shows the calculated performance of the optimized three-stage amplifier. At this point, the first three-stage amplifier was constructed, using the optimized networks. The construction process is described in the next section.

III. Amplifier Construction

Drawings and a bill of materials for the amplifier are appended to this report. The 3-stage amplifier body is milled from OFHC copper stock and is plated with 80 μin gold. The following instruments are needed for assembly:

1) 700°F soldering iron with narrow tip.

2) Low power microscope.

3) Temperature variable hot plate.

4) Ersin solder, type SN62, .062 inch diameter.

5) Assorted tweezers.

The construction procedure is as follows:

1) Check all chip capacitors with a capacitance meter.

2) Heat amplifier body (B53205M101) on a hot plate to 375-425°F (190-220°C). Tin all capacitor locations and ground post holes with solder. Place ground posts and chip capacitors in their proper locations and allow the assembly to cool. Clean amplifier body with flux remover. Check mechanical stability of the chip capacitors and re-check values with meter.

3) With the 700°F soldering iron, solder the 50 ohm chip resistors, bias resistors, and protection diodes into place.

4) Heat output endplate (2.605-856-001) on the hot plate to 375-425°F (190-220°C). Solder the DC bias connector into the endplate and allow to cool. Clean with flux remover.

5) Using a small soldering iron, solder #30 AWG enameled copper wire into DC connector. Bolt output endplate to amplifier body and solder bias wires to chip capacitors and the ground wire to the ground pole.

6) Mill .025 inch off tip of two transistor straps (2.605-838-001). Overall length of transistor strap should now be .215 inch. Prepare two pieces of .001 inch thick Kapton by cutting into a .075 inch square.

TABLE 3

(All dimensions in inches.)

Stage	1	2	3
Type	MGF1412-11-08	MGF1412-11-08	MGF1412-11-08
Gate	.050	.010	.010
Drain	.010	.010	.050
Source	.175	.175	.175

7) Cut leads of the transistor for stage one to dimensions given in Table 3.

8) Place Kapton under each source lead and clamp the first stage FET using the modified transistor straps.

9) Prepare the transistors for stages 2 and 3 by trimming to dimensions given in Table 3. Place two .097 inch diameter ferrite beads on the source leads of FET #3. Mount FET's in amplifier by clamping with the standard transistor straps.

10) Using a small soldering iron, solder the .031 inch diameter DC blocking stub to the gate of FET 1 and to the drain of FET 3.

11) Stretch a 1 inch length of #22 thin wall Teflon tubing over a .035 inch diameter drill rod. Use a heat gun and tweezers for this procedure. Place the stretched tubing over the .031 inch diameter DC blocking stubs. The teflon should extend approximately .030 inch over the end of the DC blocking stubs. NOTE: The actual length of the stubs and the tubing are determined during testing.

12) Press one teflon support bead (BOM item 5) into input end plate (2.605-856-002) and one into output end plate (2.605-856-001).

13) Prepare and mount the 50 ohm input and output lines in each endplate. Mount the selected tuning slugs on these lines. Slide the teflon covered DC blocking stubs into the input and output 50 ohm lines. Also mount the 1st and 2nd interstages in the amplifier.

14) Using a small soldering iron, solder a 4.7 pF chip capacitor onto the end of each interstage 50 ohm line.

15) Cut six lengths of 36 AWG enameled wire to .60 inch. Remove .015 to .020 inches of insulation from each end of each wire. Wind four complete turns on a #73 (.024 inch dia.) drill rod. Solder the coil between the 4.7 pF bias capacitor and the gate and drain of each FET.

16) Place a .070 inch diameter ferrite bead on the drain lead of FET 2.

17) Solder 28 AWG wire between the FET's and the interstages with SN62 solder. Lengths are selected during testing.

18) Clean entire amplifier body with flux remover. Using a low power microscope, inspect the entire amplifier to insure there are no poor or cold solder joints. Also, verify correct component placement.

19) To hold ferrite beads in place, apply a small amount of Duco cement or equivalent.

The ferrite beads mounted on the drain of the second FET and the source leads of the third FET serve to surpress high frequency oscillations. The Kapton under the source leads of the first FET is used to increase the source lead inductance of that stage, found to reduce the amplifier gain below 4 GHz and increase the amplifier stability. The .031 inch diameter DC blocking stub is formed from half-hard brass wire, copper and gold plated. The 36 AWG wire forms the bias coils and the 28 AWG wire forms the series tuning inductors.

A mechanical outline drawing and electrical schematic for this amplifier are included in the drawings appended to this report.

IV. Results

When the first amplifier was assembled, we found it necessary to adjust the lengths of the tuning inductors. Evidently a simple transmission line is not an adequate model for them. Some experimentation with the impedances and lengths of the interstage tuning slugs was also done, but the final values are very close to the FARANT optimization results. On most of the subsequent units only the position of the tuning slugs is adjusted, with the rare case where the lengths of the tuning inductors must be trimmed. The amplifiers constructed with three MGF1412 transistors seem to be repeatable, even when the lot number of the transistors change.

The output 1 dB compression point of these amplifiers is typically greater than 0 dBm. Figure 16 shows the typical input and output return loss at 13 Kelvin. Figure 17 shows the measured

amplifier noise temperature versus ambient temperature, and the same with the effect of the input isolator removed.

V. Future Work

Additional work should be done on the computer models. Relying on the manufacturer's data for the transistors is adequate for fairly narrowband amplifiers, but to achieve better modeling results, we should attempt to measure some actual transistor S-parameters. Careful noise measurements on a single FET at several widely spaced frequencies should be done to try to determine the variation in noise parameters with frequency more accurately. We would like to design a more complex input matching network to provide wider bandwidth in the amplifier noise temperature response. Finally, when HEMT devices become available, we hope to incorporate one of these extremely low noise transistors in the amplifier first stage.

VI. Acknowledgements

We would like to express our thanks to R. Bradley for his work on the transistor model and to the Green Bank machine shop personnel for their excellent work. Special thanks go to S. Weinreb for helping duplicate his test stations and for getting us started in this work. R. Harris taught us how to assemble a reliable cryogenic amplifier and M. Pospieszalski has many excellent suggestions.

REFERENCES

[1] "Low Noise, 15 GHz, Cooled, GaAsFET Amplifier," EDIR No. 235, R. D. Norrod and R. Harris, September 1983.

[2] "Low-Noise, 8.0-8.8 GHz, Cooled, GASFET Amplifier," EDIR No. 254, M. Pospieszalski, December 1984.

[3] "Low-Noise, 10.7 GHz, Cooled, GASFET Amplifier," EDIR No. 222, G. Tomassetti, S. Weinreb, and K. Wellington, November 1981.

[4] "The Computation of Coaxial Line Step Capacitance," P. I. Somlo, IEEE Transactions on MTT, V15, 1, January 1967.

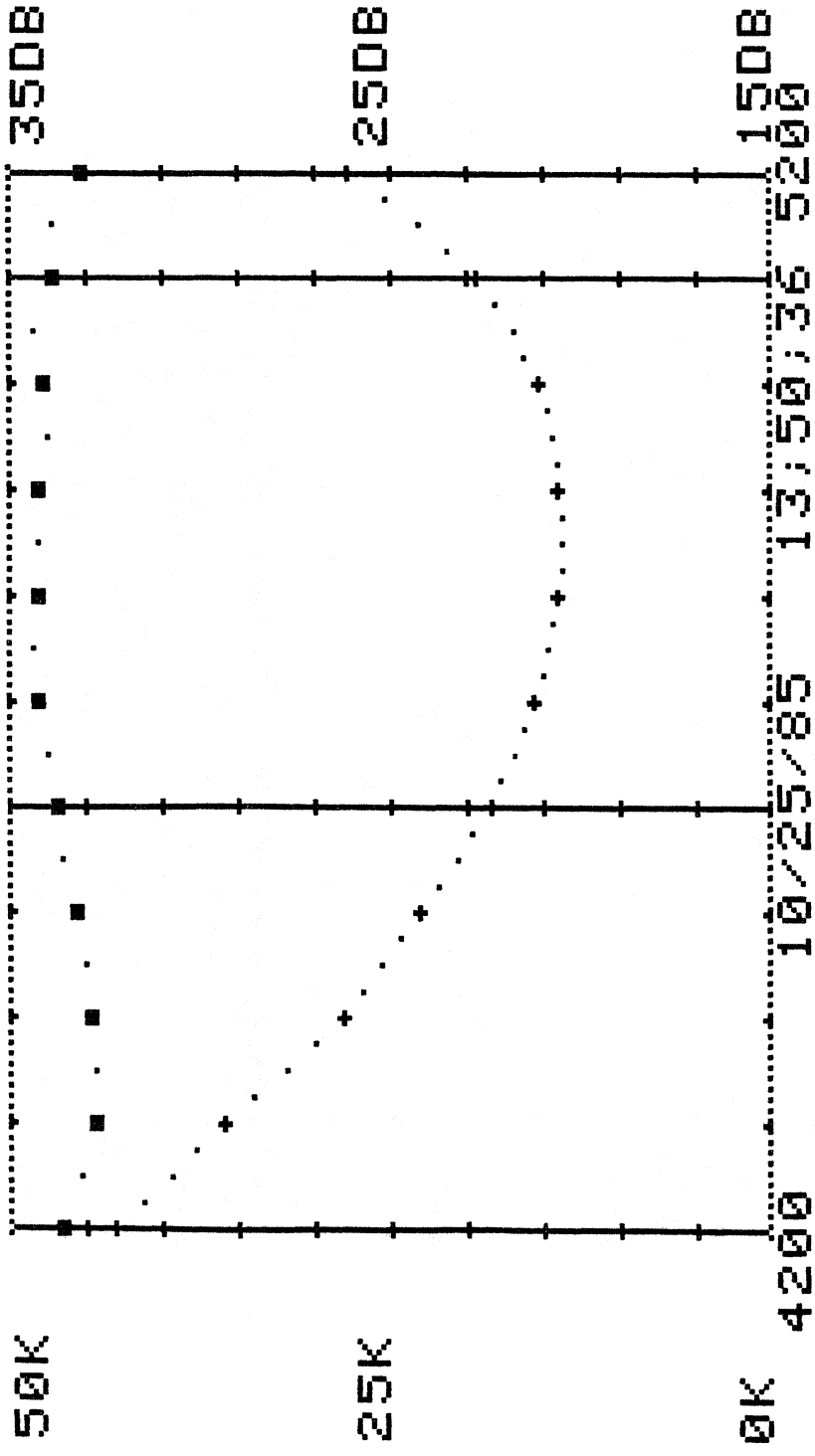

FIGURE 1. Noise temperature and gain of a typical amplifier without the input isolator. The isolator will increase the noise by about 3 Kelvin.

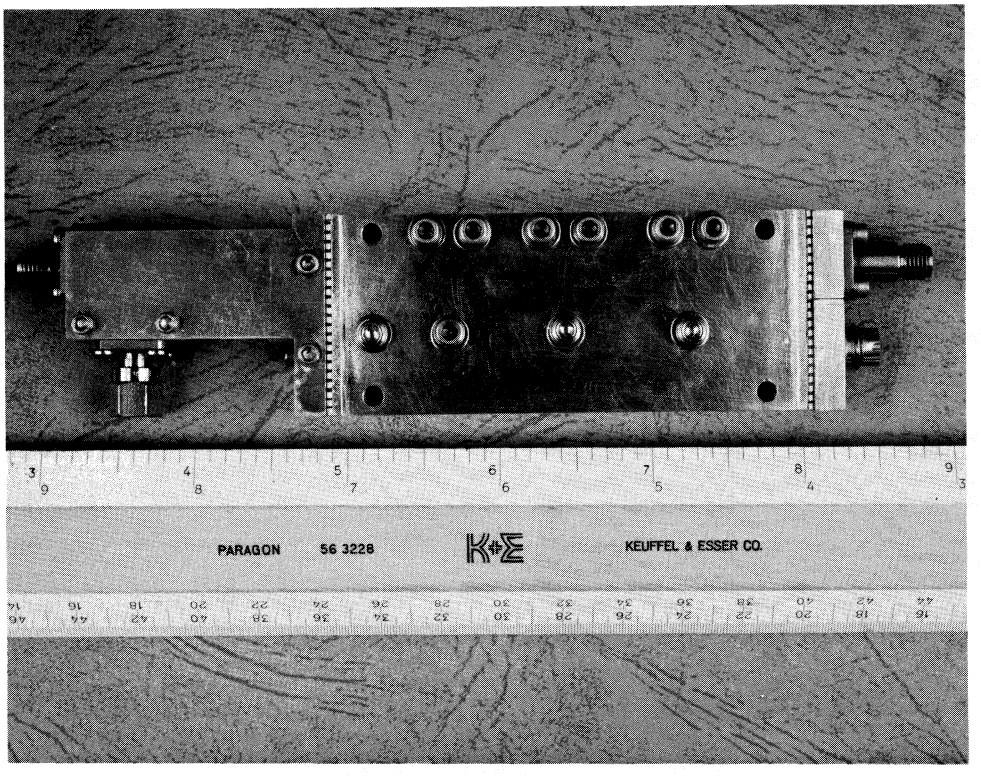

FIGURE 2. A completed amplifier assembly. The input isolator with cold strap is on the left and the output attenuator and DC connector are on the right.

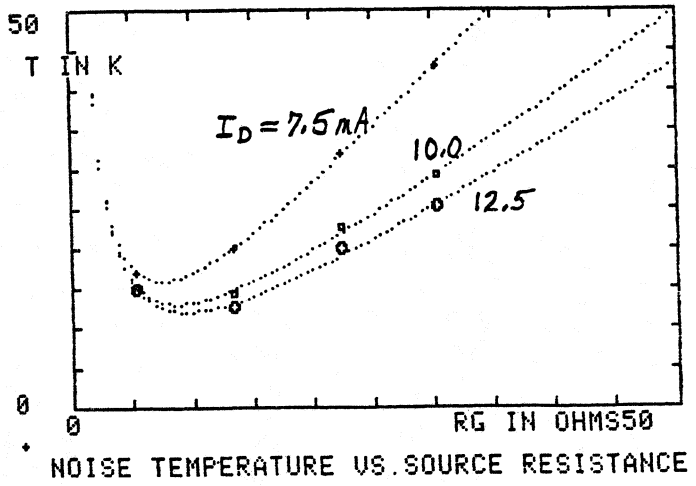

FIGURE 3. Experimentally determined noise parameters of FSC10FA, Lot PT02, at 13 Kelvin.

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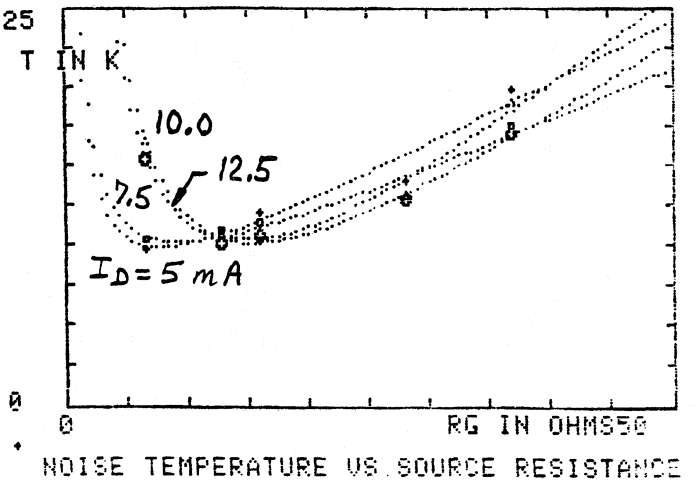

FIGURE 4. Experimentally determined noise parameters of NE75083, Lot 72A, at 13 Kelvin.

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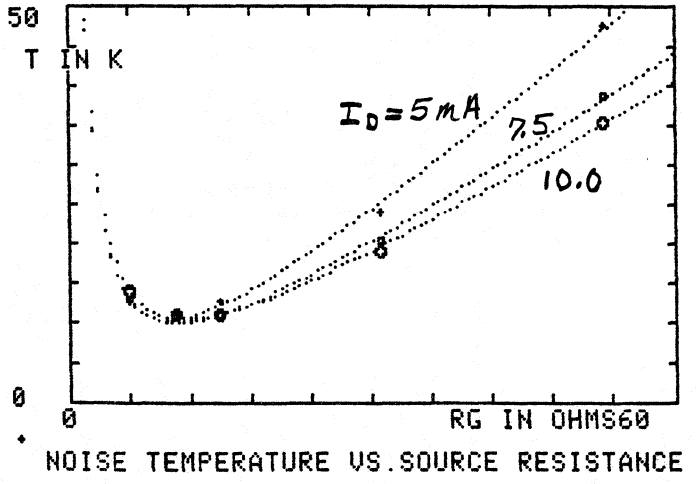

FIGURE 5. Experimentally determined noise parameters of MGF 1412, Lot 3YAJ8, at 13 Kelvin. Drain voltage 3 V.

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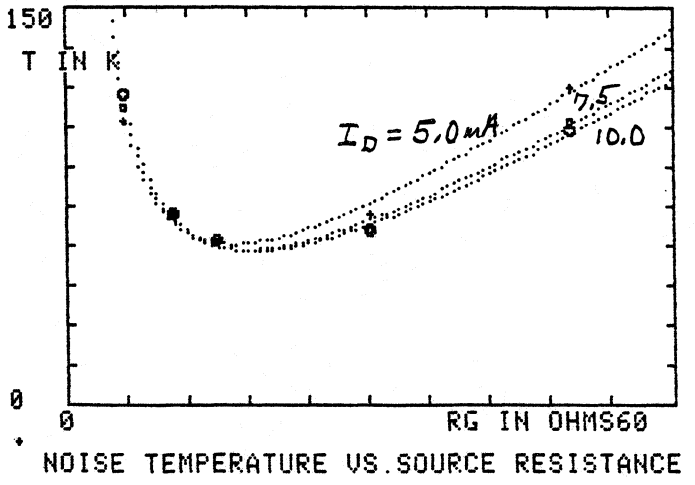

FIGURE 6. Experimentally determined noise parameters of MGF 1412, Lot 3YAJ8, at 300 Kelvin. Drain voltage 3 V.

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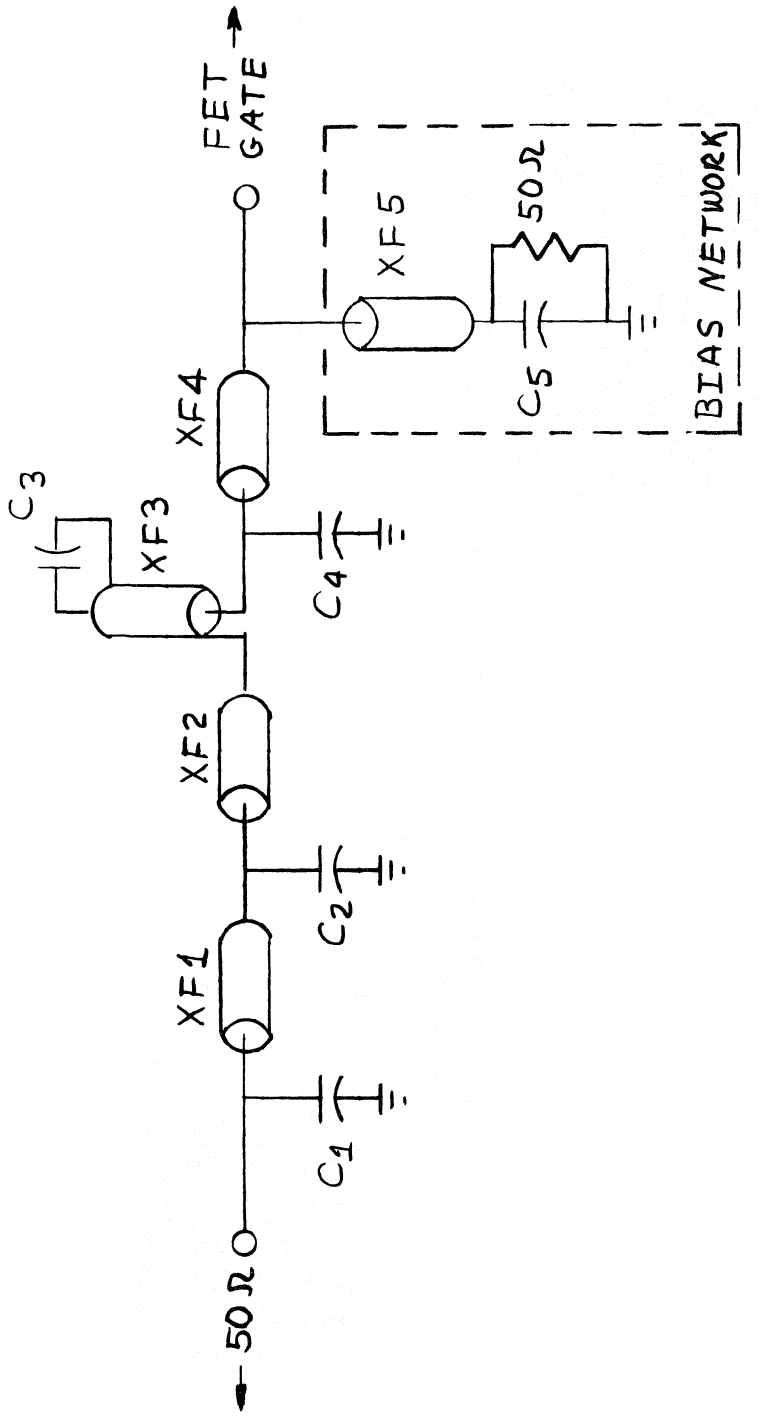


FIGURE 7. Input and output matching network model.

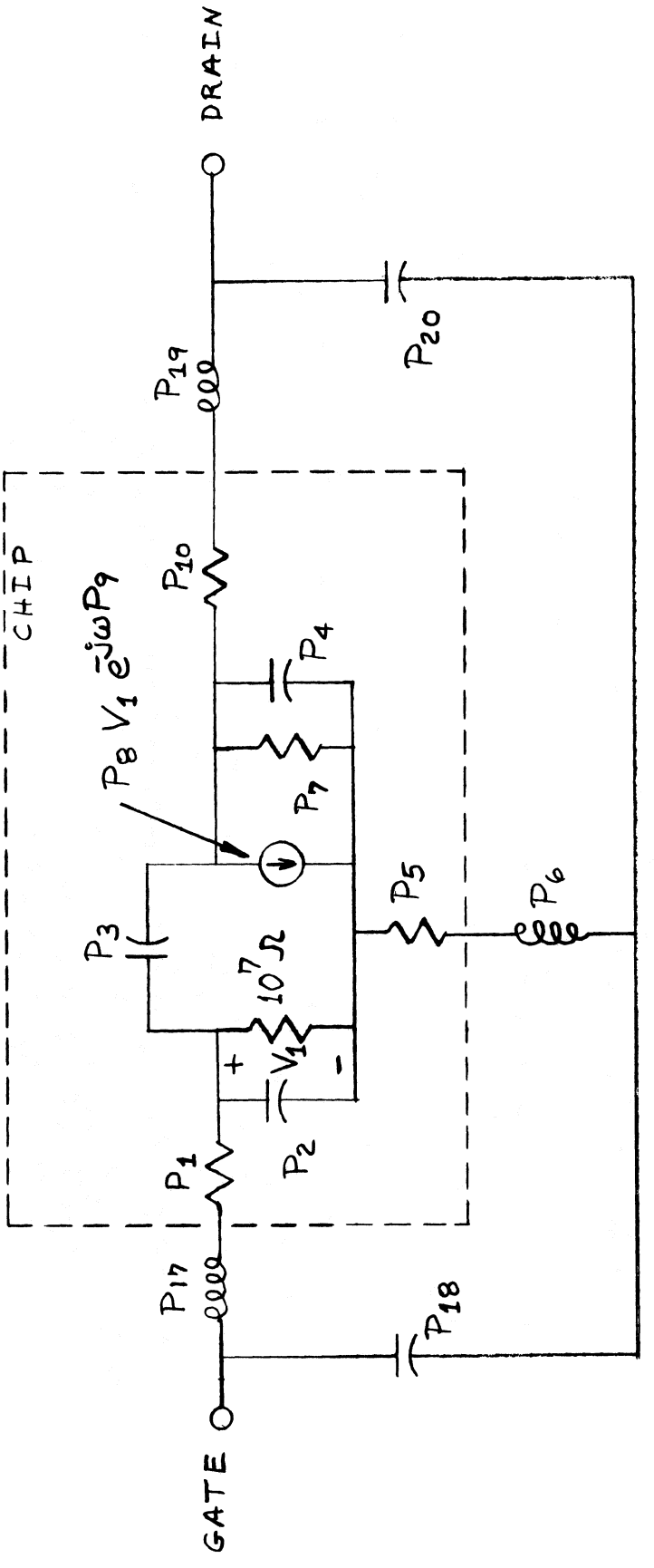


FIGURE 8. GaAs FET Model 1

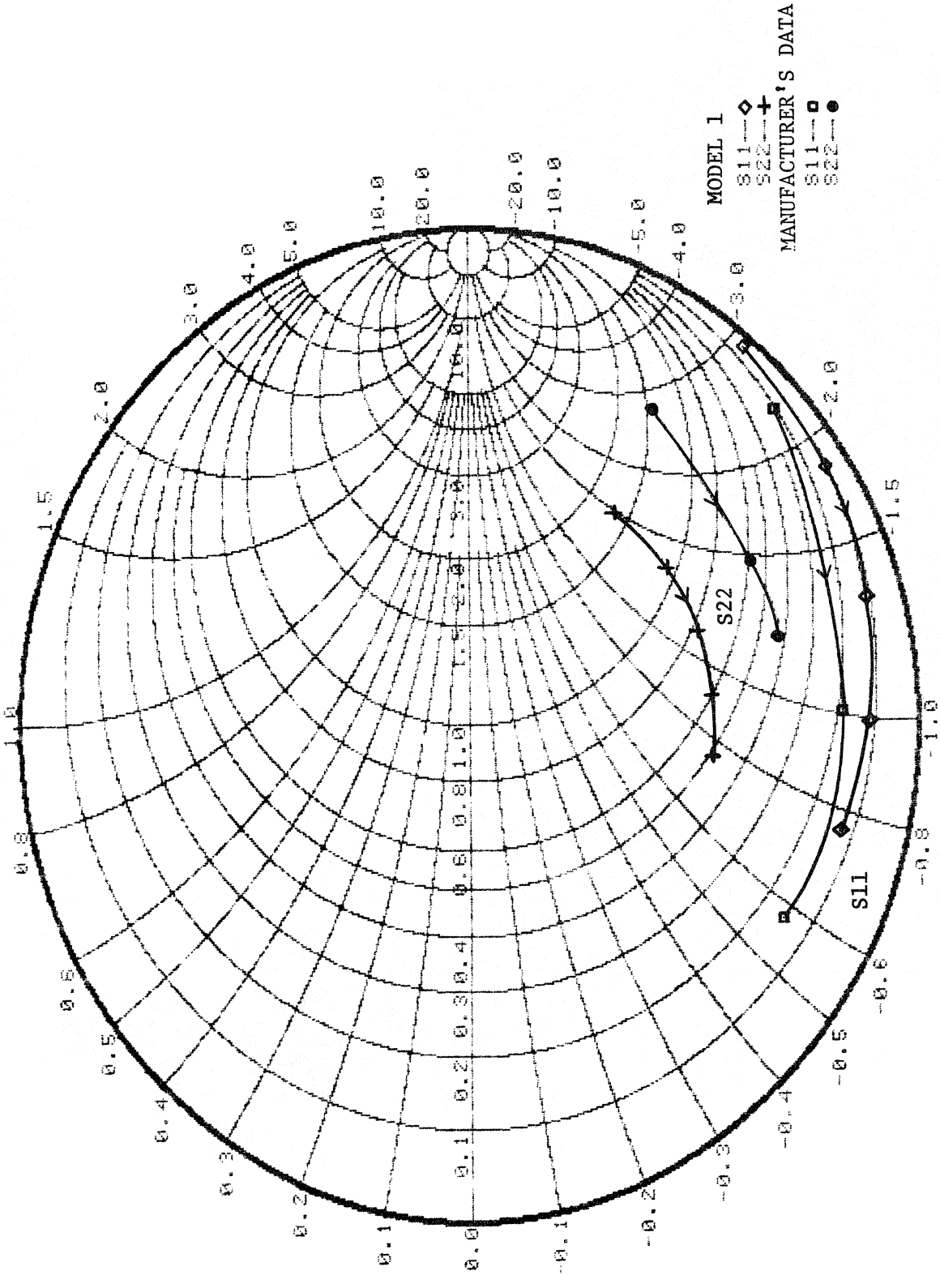


FIGURE 9. S_{11} and S_{22} plotted from manufacturer's data for the MGF 1412 and from Model 1.

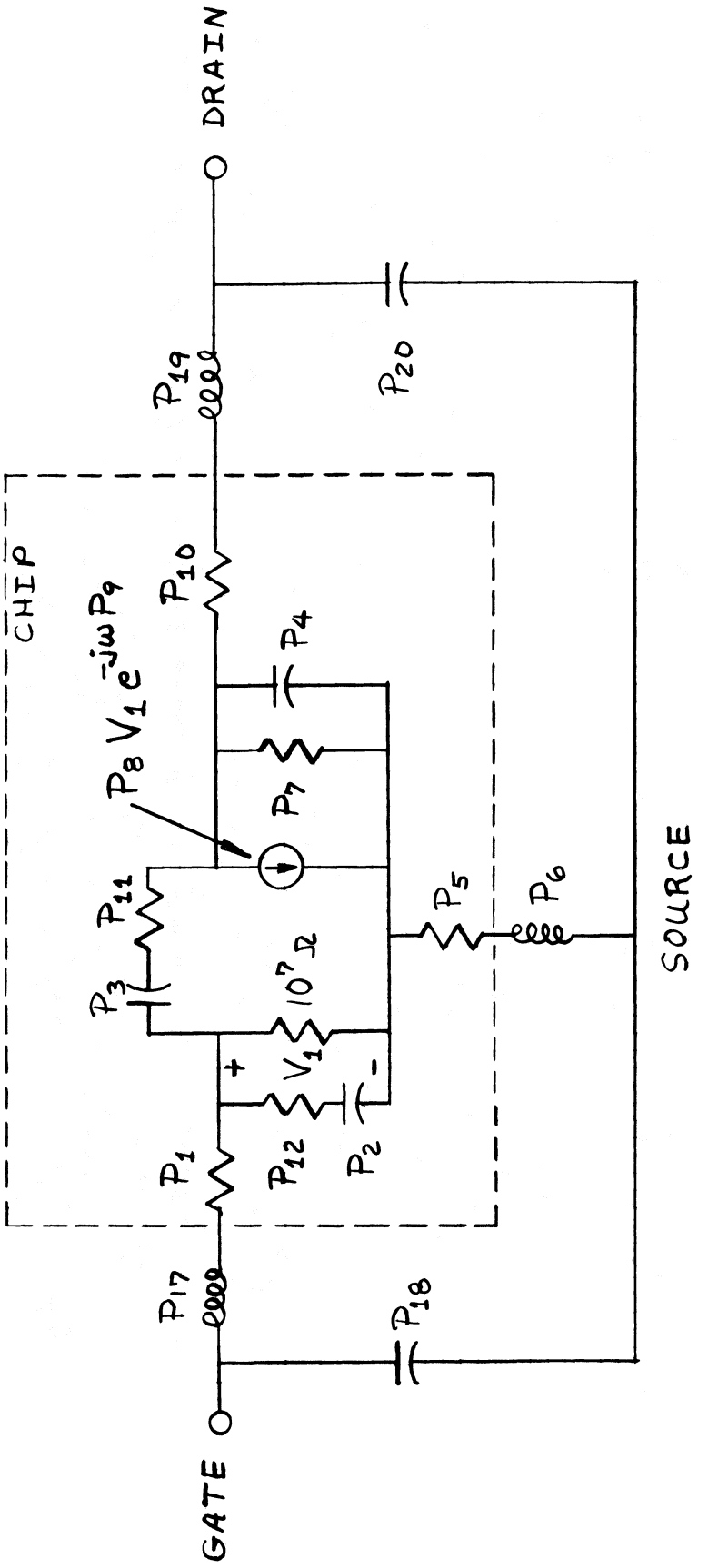


FIGURE 10. GaAs FET Model 2 with resistors added in series with the gate-source and gate-drain capacitors.

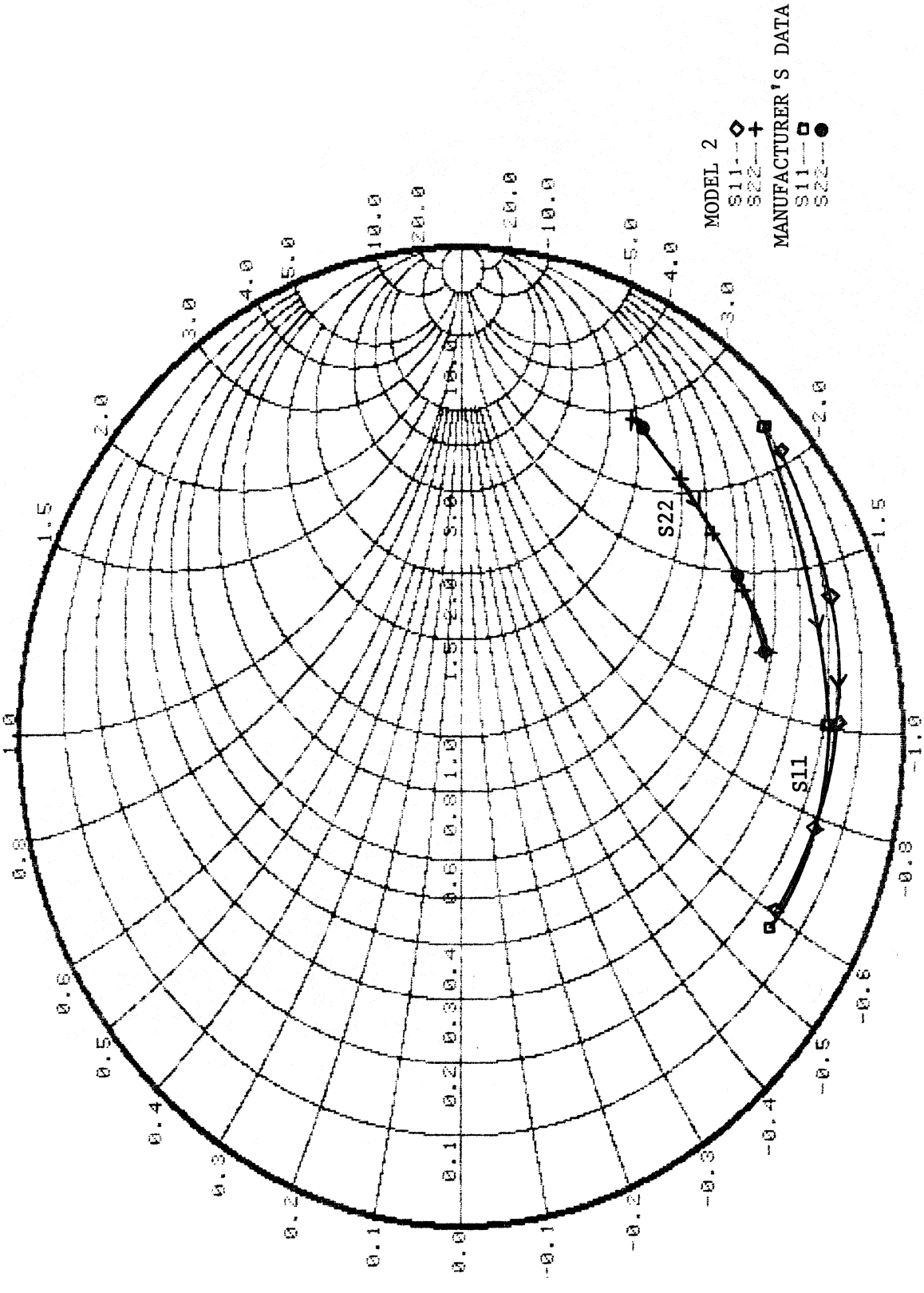


FIGURE 11. S_{11} and S_{22} plotted from manufacturer's data for the MGF 1412 and from Model 2.

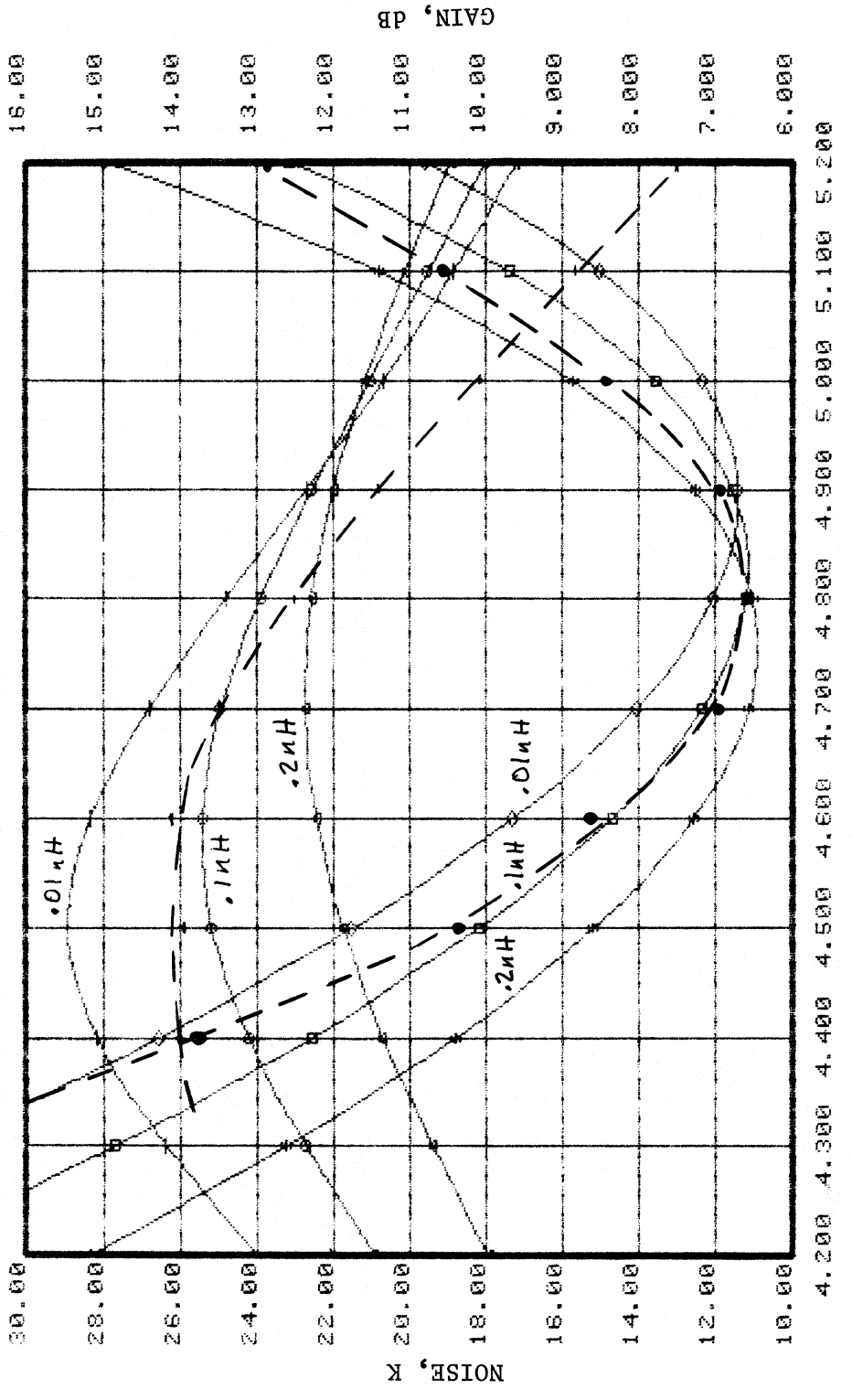


FIGURE 12. Calculated performance of a single-stage amplifier using FET Model 2 and input/output matching networks illustrated in Figure 7, and for three values of source lead inductance. Dashed lines show performance of an amplifier measured in the lab.

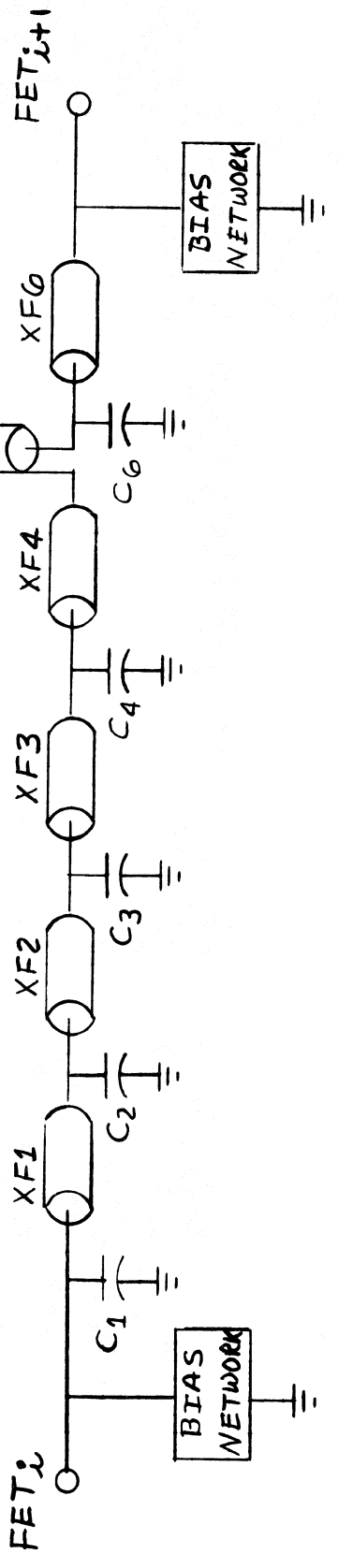
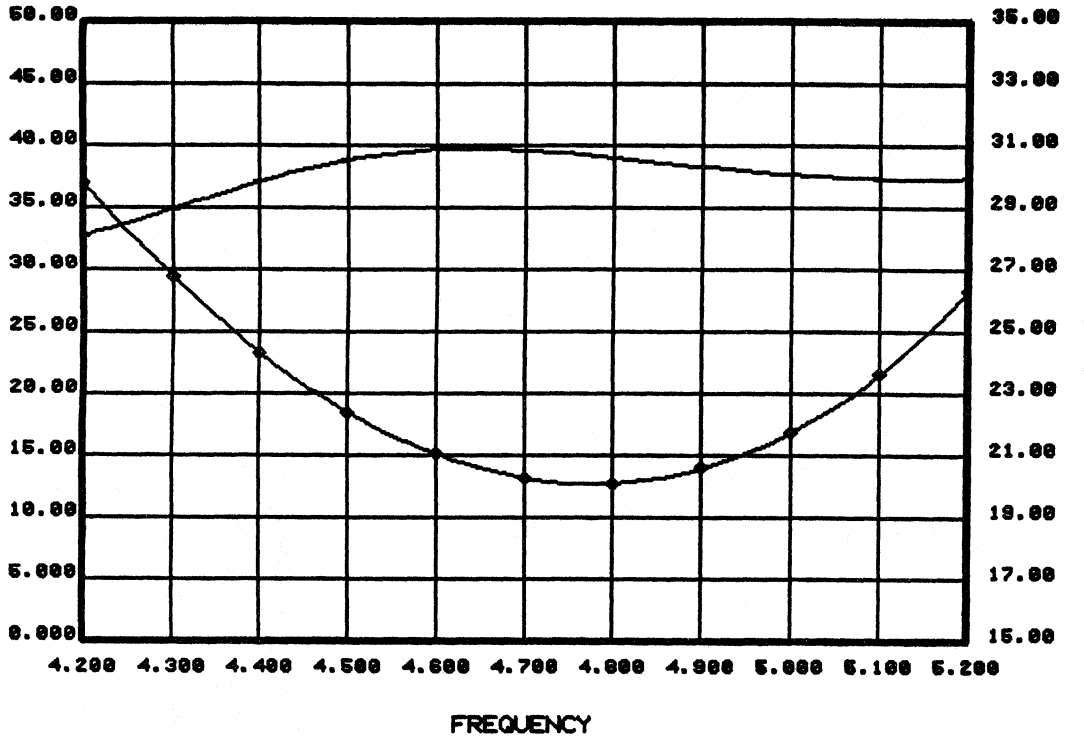


FIGURE 13. Model of the amplifier interstage networks. The bias networks are identical to those in Figure 7.



Input Matching Network

C1 = .003; C2 = .003; C3 = 0.4
C4 = .006; C5 = 4.7 (pF)

	$Z_i(\Omega)$	Len(in)	ε_r
XF1	24.5	.427	2.1
XF2	50.0	.050	1.0
XF3	18.0	.460	2.0
XF4	101.0	.147	1.0
XF5	211.0	.600	1.0

Output Matching Network

C1 = .001; C2 = .001; C3 = 0.4
C4 = .006; C5 = 4.7 (pF)

	$Z_i(\Omega)$	Len(in)	ε_r
XF1	34.5	.427	2.1
XF2	50.0	.050	1.0
XF3	18.0	.460	2.0
XF4	101.0	.147	1.0
XF5	211.0	.600	1.0

Interstage 1

C1 = .001; C2 = .010; C3 = .010
C4 = .010; C5 = 4.7 ; C6 = .010 (pF)

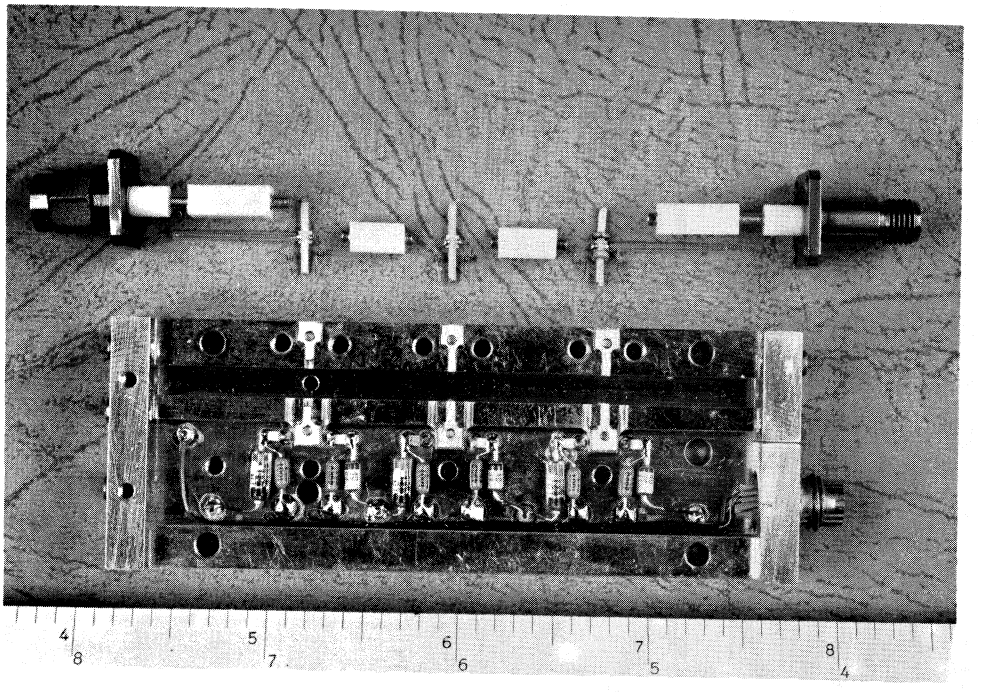
	$Z_i(\Omega)$	Len(in)	ε_r
XF1	154.0	.135	1.0
XF2	50.0	.050	1.0
XF3	15.2	.290	2.1
XF4	50.0	.050	1.0
XF5	50.0	.010	1.0
XF6	154.0	.100	1.0

Interstage 2

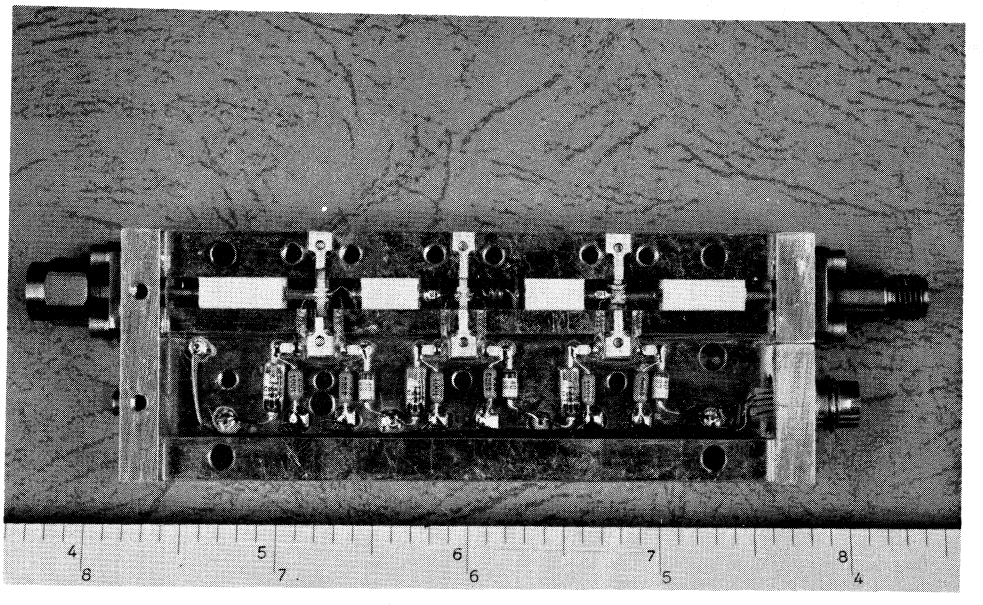
C1 = .001; C2 = .010; C3 = .006
C4 = .006; C5 = 4.7 ; C6 = .010 (pF)

	$Z_i(\Omega)$	Len(in)	ε_r
XF1	154.0	.500	1.0
XF2	50.0	.050	1.0
XF3	19.1	.300	2.1
XF4	50.0	.040	1.0
XF5	50.0	.010	1.0
XF6	154.0	.210	1.0

FIGURE 14. Calculated three stage amplifier performance. See Figures 7 and 13 for circuit model topologies.

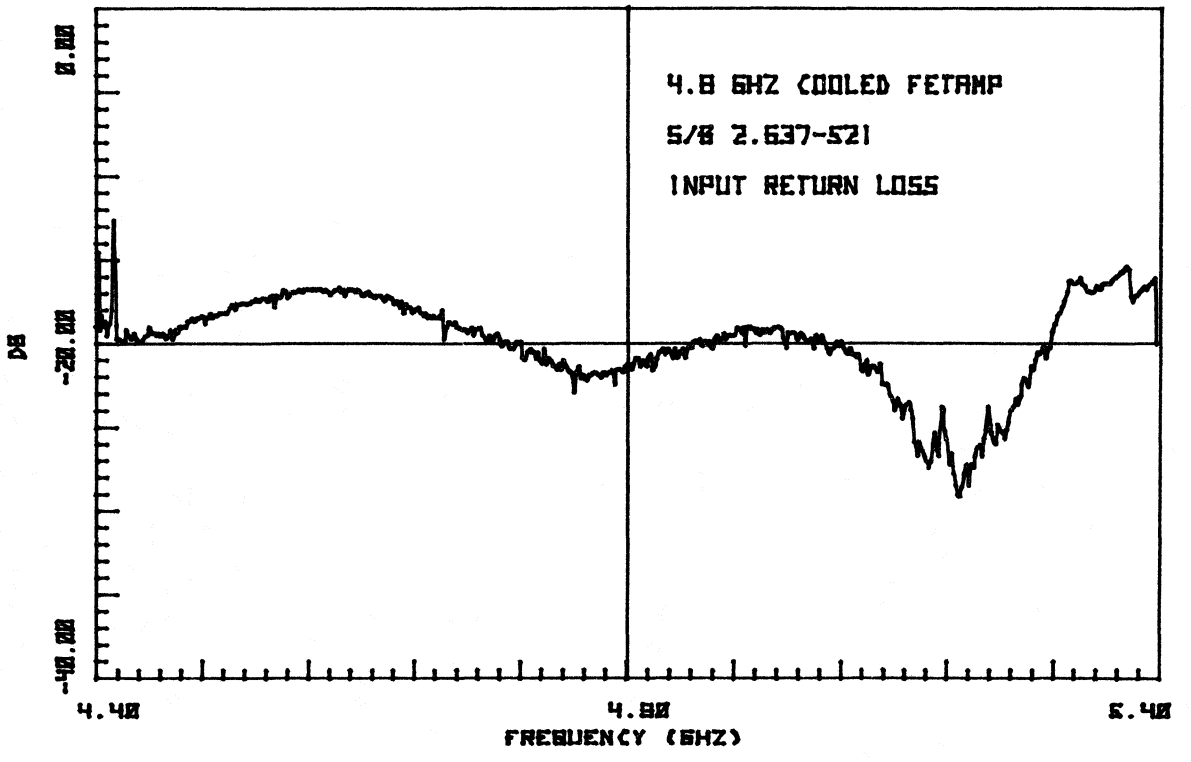


(a)



(b)

FIGURE 15. The amplifier during construction.
(a) With the RF lines ready to be mounted.
(b) A completed amplifier.



(a) ↑ (b) ↓

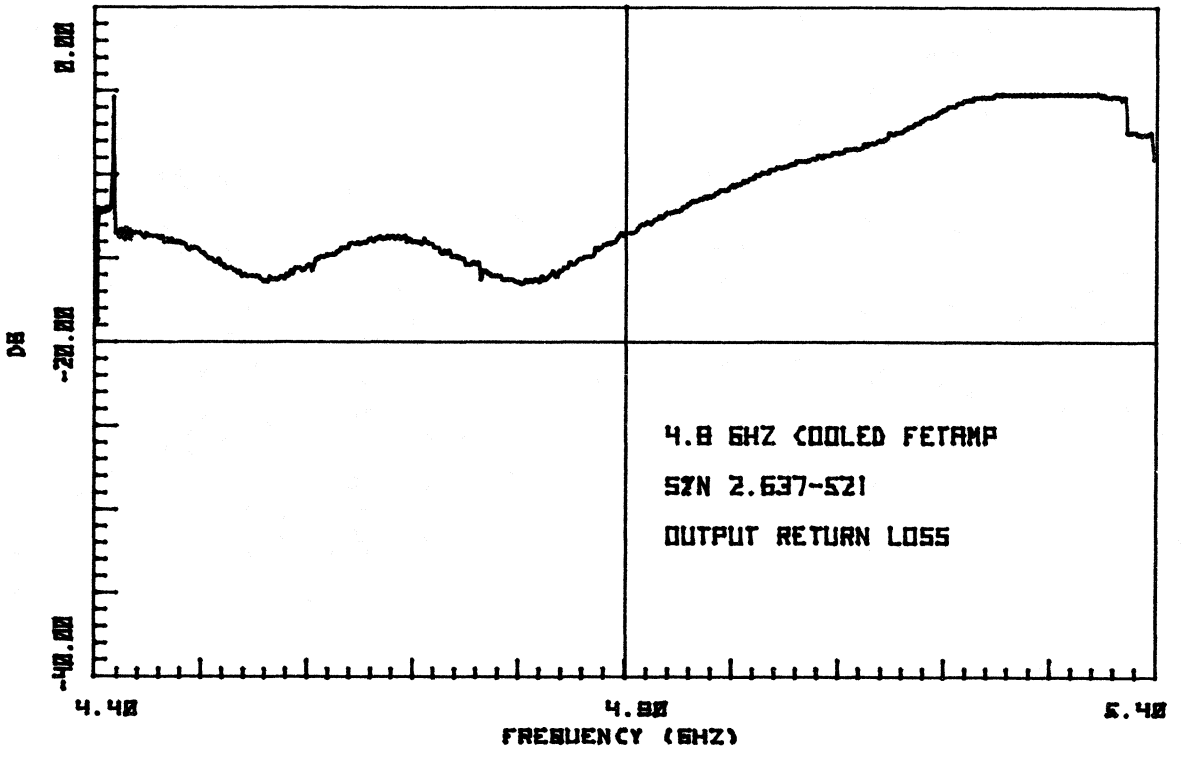


FIGURE 16. Amplifier input (a) and output (b) return loss at 13 Kelvin.

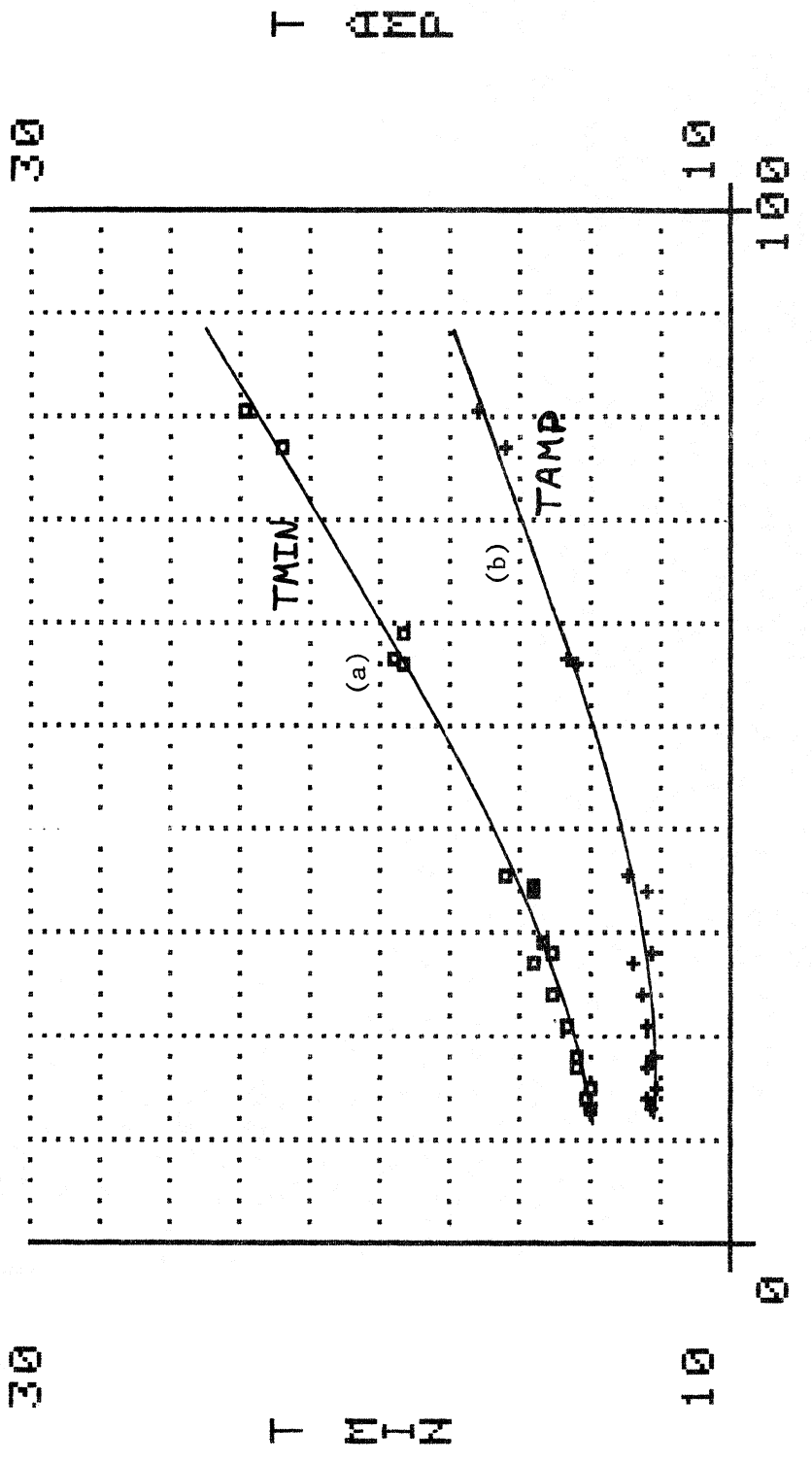


FIGURE 17. Amplifier noise temperature versus ambient temperature.
(a) Measured.
(b) After subtracting the effect of the input isolator.

TABLE 1

Comparison of FET's at 4.8 GHz

Ambient Temperature - 300 K							
FET	V_{DS} (V)	I_{DS} (mA)	R_{opt} (Ω)	X_{opt} (Ω)	g_n (mmho)	T_{min} (K)	Assoc. Gain (dB)
MGF1412-3YAJ8-M015	3.0	7.5	17.8	53	7.9	57.8	10
FSC 10-PT02-F004	3.0	12.5	25.9	47	4.5	75.1	10
NEC 750-72A-N001	3.0	10.0	21.7	65	6.0	51.6	12
Ambient Temperature - 13 K							
FET	V_{DS} (V)	I_{DS} (mA)	R_{opt} (Ω)	X_{opt} (Ω)	g_n (mmho)	T_{min} (K)	Assoc. Gain (dB)
MGF1412-3YAJ8-M015	3.0	7.5	10.7	53	2.9	9.9	12
FSC 10-PT02-F004	3.0	12.5	9.6	47	3.3	11.9	11
NEC 750-72A-N001	3.0	10.0	15.0	65	1.8	10.0	13

TABLE 2

Element Values for GaAs FET Models

(a) Model plotted in Figure 9.
(b) Model plotted in Figure 11.

Parameter	Name	(a) Model 1	(b) Model 2
1	Gate Resistor (Ω)	6.3	0.0548
2	Gate/Source Cap (pF)	0.22	0.5389
3	Gate/Drain Cap (pF)	0.039	0.0467
4	Drain/Source Cap (pF)	0.18	0.2655
5	Source Resistor (pF)	1.2	16.1528
6	Source Inductor (nH)	0.10	0.1433
7	Drain/Source Resistor (Ω)	157.0	199.1638
8	Transconductance	30.0	85.0097
9	Phase Delay (ps)	0.0	0.2118
10	Drain Resistor (Ω)	0.0	0.4579
11	G/D Fringing Resistor (Ω)	-	798.6768
12	Gate and Channel Resistor (Ω)	-	3.2906
.			
.			
.			
17	Package Gate Inductor (nH)	0.83	0.9159
18	Package Gate Capacitor (pF)	0.26	0.3794
19	Package Drain Inductor (nH)	0.69	1.0037
20	Package Drain Capacitor (pF)	0.26	0.2072

BILL OF MATERIAL: **A53205B101**

TITLE: **4.8 GHz Cooled FET Amplifier**

APPROVED BY/DATE: R.D. Hall 29 Jan 86

PREPARED BY/DATE:

REV: DATE:

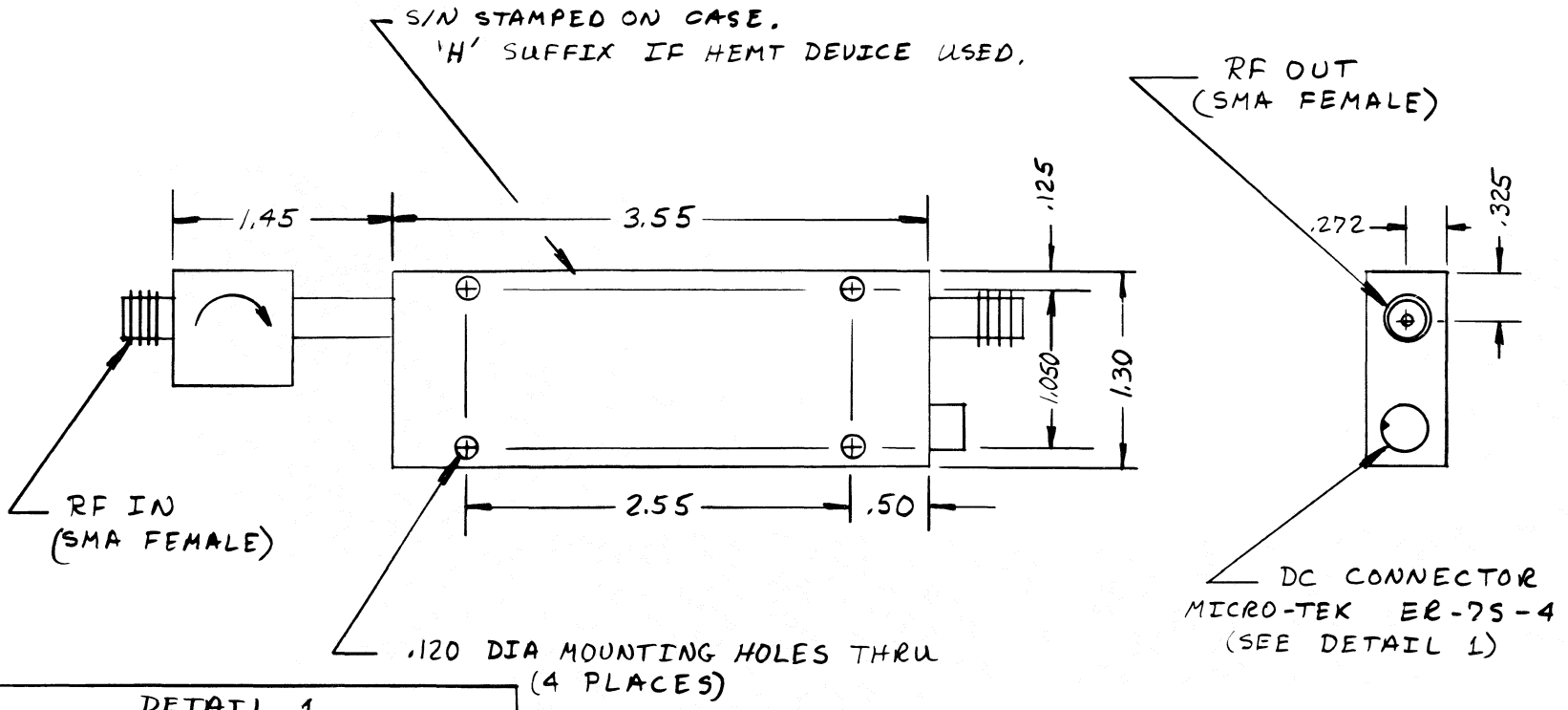
Item	Qty. Req.	Description	Designation	P/N	Suggested Manufacturer
1.	1	Circulator		CTB-1107	Pamtech
2.	1	Termination, SMA Male, 50 ohm		4112P	EMC
3.	1	SMA Connector, Jack		6540	EMC
4.	1	SMA Connector/Attenuator, 6 dB		7406	EMC
5.	2	Teflon Support Bead		6400-00-3	EMC
6.	1	Amplifier Body		B53205M101	NRAO
7.	1	Cover		B53205M102	"
8.	1	Endplates, Input and Output		2.605.856 -xxx	"
9.	1	Tuning Slug, Input		B53205M103 -007	"
10.	1	Tuning Slug, Interstage 1		B53205M103 -009	"
11.	1	Tuning Slug, Interstage 2		B53205M103 -012	"
12.	1	Tuning Slug, Output		B53205M103 -006	"
13.	2	50 Ohm Input/Output Line (Select Length in Test)		B53205M104 -0xx	"
14.	2	50 Ohm Interstage Line		B53205M104 -102	"
15.	6	Transistor Strap II		2.605-838 -001	
16.	1	Circulator Cold Strap		A53205M106	"
17.					
18.	2	Transistor Lead Extensions (Select Length in Test)		2.605-837 -001	"
19.	AR	28 AWG Solid Copper Wire, Tuning Coils		8054	Belden
20.	REF	FET Mounting Detail 2		B53205M105	NRAO

BILL OF MATERIAL: A53205B101 | TITLE: **4.8 GHz Cooled FET Amplifier** | APPROVED BY/DATE: R.D. Mond 29 Jan 86 | PREPARED BY/DATE: | REV: DATE:

Item	Qty. Req.	Description	Designation	P/N	Suggested Manufacturer
21.	1	DC Connector, Solder Mount		ER-7S-4	Micro-Tek
22.	1	DC Connector, Mating		EP-7S-1	Micro-Tek
23.					
24.	3	Gallium Arsenide FET		MGF-1412 -11-08	Mitsubishi
25.	1	Ferrite Bead, .070" Dia.		T7-6	Micrometal
26.	2	Ferrite Bead, .097" Dia.		T10-6	Micrometal
27.					
28.	6	680 pF Chip Capacitor		ATC700B 681KP50	American Technical Ceramics
29.	6	22 pF Chip Capacitor		ATC100A 220JP50X	"
30.	8	4.7 pF Chip Capacitor		ATC100A 4R7DP50X	"
31.					
32.					
33.	6	50 ohm Chip Resistor		WA-13PG -500J-S	Mini-Systems
34.	6	Diode, Zener		1N821	Motorola
35.	6	Diode, Zener		1N4099	Motorola
36.					
37.	3	Resistor, Metal Film, 1 K ohm		RLR05C-1001FS	Dale
38.	3	Resistor, Metal Film, 49.9 ohm		RLR05C-49R9FS	Dale
38.	AR	30 AWG Solid Copper Wire, Bias Input		8055	Belden
40.	AR	#22 Teflon Tubing		TFT 400	Alpha

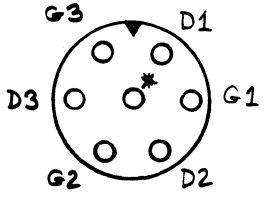
BILL OF MATERIAL:	TITLE:	APPROVED BY/DATE:	PREPARED BY/DATE:	REV: A DATE:
A53205B101	**4.8 GHz Cooled FET Amplifier**	R.D. Hall		18FEB86

Item	Qty. Req.	Description	Designation	P/N	Suggested Manufacturer
41.	AR	36 AWG Solid Enameled Copper Wire		8058	Belden
42.	6	2-56 x 3/8 Socket Head Cap Screws			All-Metal
43.	4	2-56 x 1/4 Socket Head Cap Screws			All-Metal
44.	11	#2 Flat Washers			All-Metal
45.	13	#2 Lock Washers			All-Metal
46.	2	2-56 x 3/16 Socket Head Cap Screws			All-Metal
47.	2	2-56 x 5/8 Flat Head Screws			All-Metal
48.	6	4-40 x 3/8 Socket Head Cap Screws			All-Metal
50.	10	#4 Flat Washers			All-Metal
51.	10	#4 Lock Washers			All-Metal
52.	5	Ground Poles		1528/2	Keystone
53.					
54.	6	0-80 x 3/16 Socket Head Cap Screws			All-Metal
55.	6	#0 Flat Washers			All-Metal
56.	AR	Ersin SN62 Rosin Core Solder			Ersin Multicore
57.	AR	Kaptan Film, 1 mil thick			
58.	REF	Interface Drawing		A53205M107	
59.	REF	Schematic		A53205S001	
60.					



DETAIL 1

(VIEW FROM OUTSIDE AMP CASE)



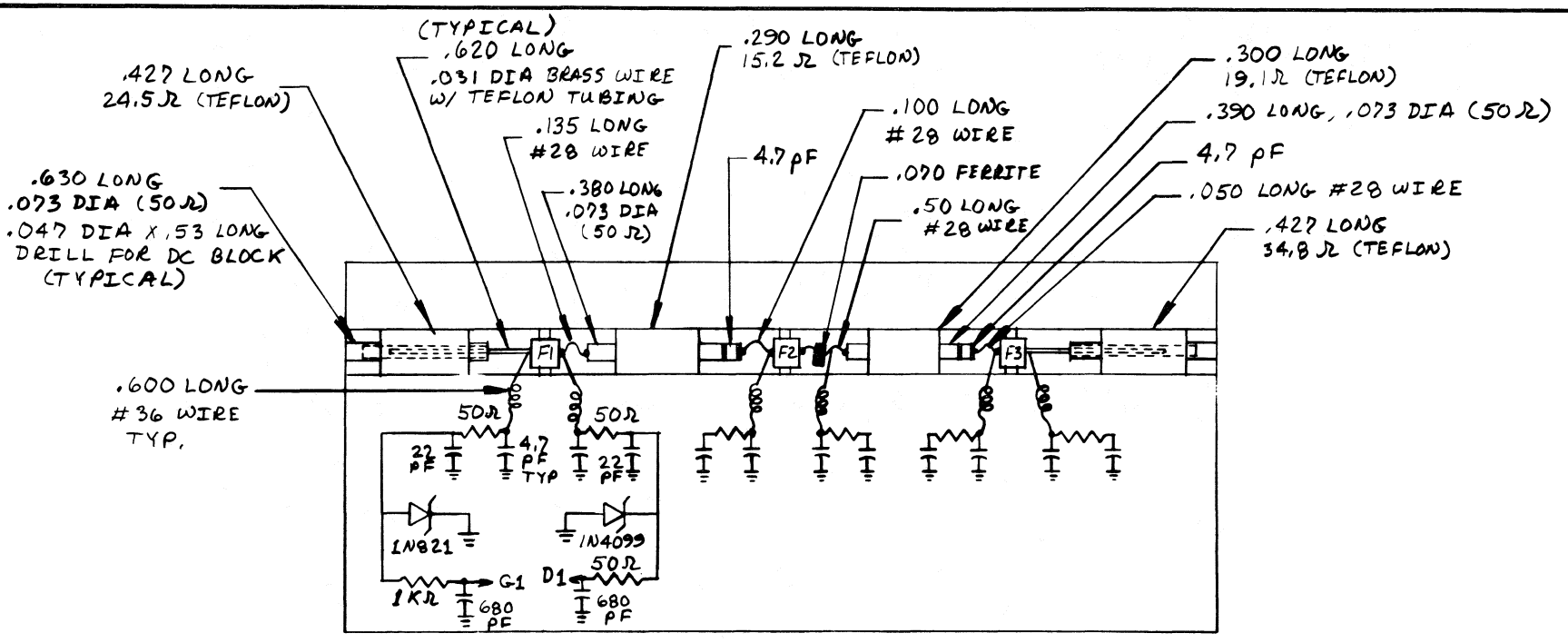
* - ON AMPLIFIERS WITH HEMT DEVICES, CENTER PIN IS LED POWER. GROUND OBTAINED THRU CONNECTOR BACKSHELL. OTHERWISE, CENTER PIN IS GROUND.

H. T. HALL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
3 PLACE DEC. (xxx) ±
2 PLACE DEC. (xx) ±
1 PLACE DEC. (x) ±

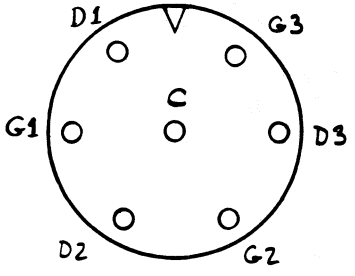
NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: 4.8 GHZ COOLED FETAMP	TITLE: INTERFACE DRAWING		
MATERIAL:	DRAWN BY: RON	DATE: 1/24/86	
FINISH:	DESIGNED BY:	DATE:	
	APPROVED BY:	DATE:	
SHEET NUMBER: 1/1	DRAWING NUMBER: A53205M 107	REV.	SCALE: 1:1



STAGES 2 AND 3
BIAS NETWORKS
IDENTICAL TO STAGE 1.

DC CONNECTOR



VIEW FROM INSIDE AMP CASE

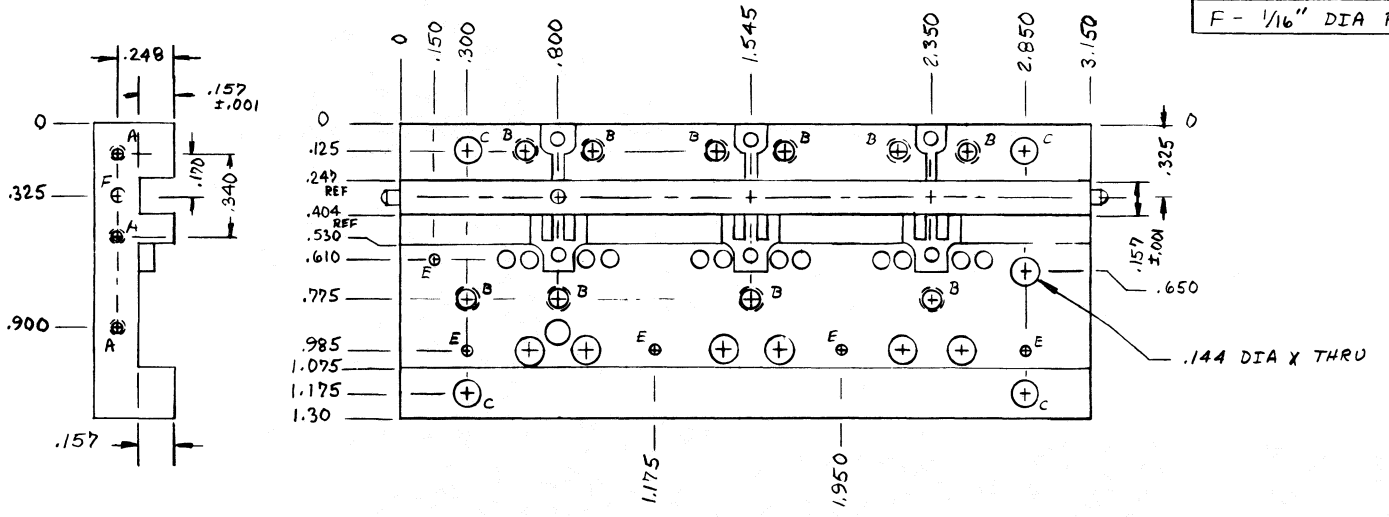
CONNECT C TO ANODE
OF LED IN HEMT AMPS,
GROUND OTHERWISE.

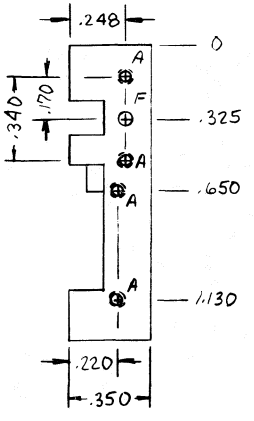
H. T. HALL

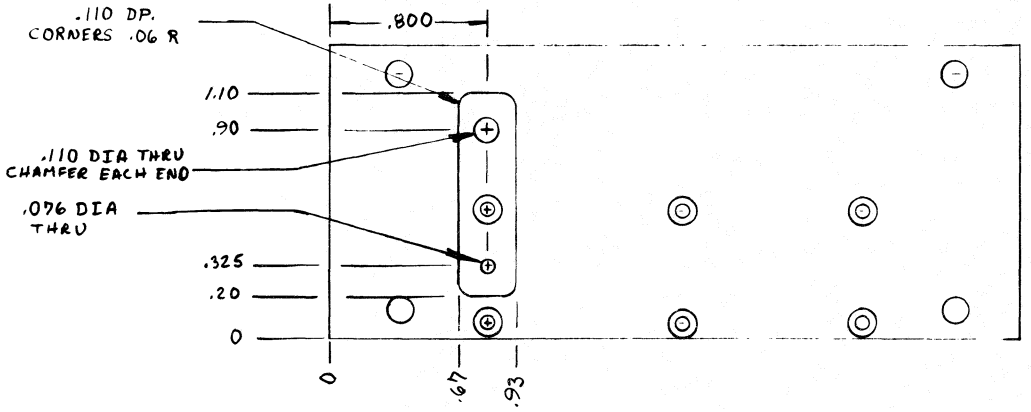
NATIONAL RADIO ASTRONOMY OBSERVATORY GREEN BANK, W. VA. 24944	
PROJ: 4.8GHz FETAMP	TITLE: SCHEMATIC
MATERIAL: ~	DRAWN BY: RON — DATE: 1/28/86
FINISH: ~	DESIGNED BY: — DATE:
	APPROVED BY: — DATE:
SHEET NUMBER: 1/1	DRAWING NUMBER: A532055001 — REV. — SCALE: ~

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
3 PLACE DEC. (xxx) ±
2 PLACE DEC. (xx) ±
1 PLACE DEC. (x) ±

A - 2-56 UNC-2B X .25 DP	(7 PLACES)
B - 4-40 UNC-2B X THRU	(10 PLACES)
C - .120 DIA THRU	(4 PLACES)
E - .0465 DIA X .10 DP	(5 PLACES)
F - 1/16" DIA PIN, PROTRUDE 1/16"	(2 PLACES)







NOTE: SEE DWG B53205M105 FOR DETAILS OF FET MOUNTING AREAS.

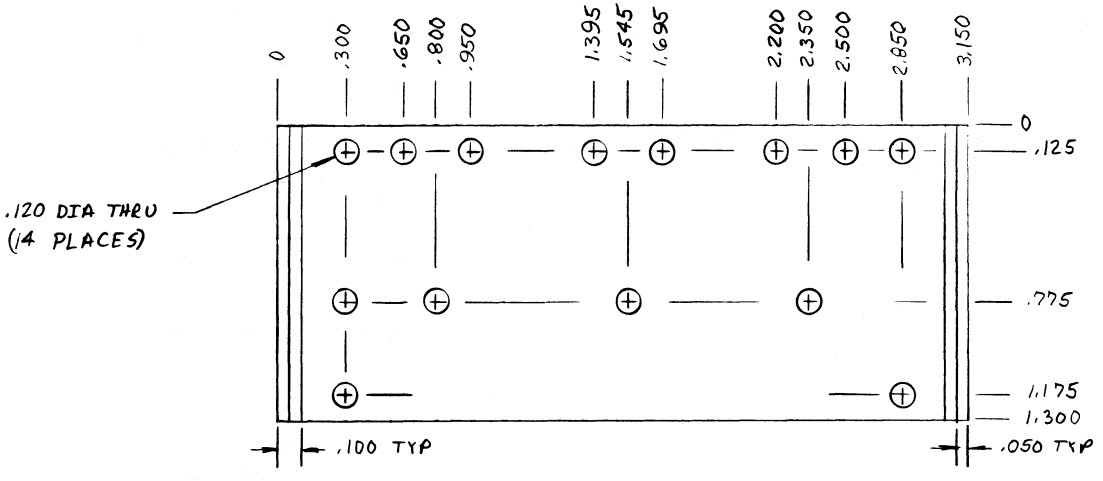
SURFACES 32

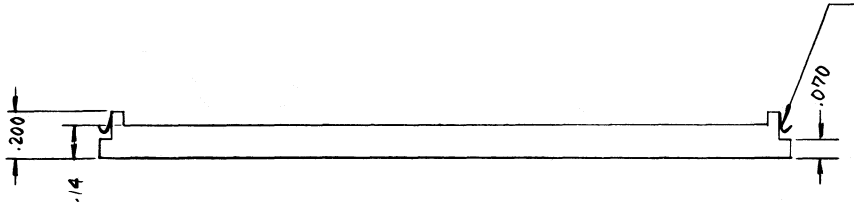
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±
3 PLACE DEC. (xxx) ± .003
2 PLACE DEC. (xx) ± .020
1 PLACE DEC. (x) ±

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: 5GHz FETAMP	TITLE: THREE STAGE BODY 1		
MATERIAL: OFHC COPPER	DRAWN BY: RDN	DATE: 2/27/85	
FINISH: 80 µin GOLD	DESIGNED BY:	DATE:	
	APPROVED BY:	DATE:	
SHEET NUMBER: 1/1	DRAWING NUMBER: B53205M101	REV. B 6/3/85	SCALE: NTS

H. T. HALL





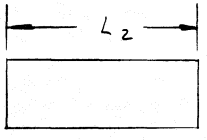
H. T. HALL

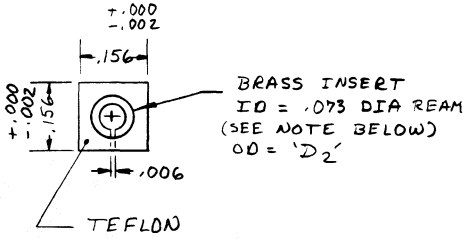
SURFACES 32

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±
3 PLACE DEC. (xxx) ± .005
2 PLACE DEC. (xx) ± .020
1 PLACE DEC. (x) ±

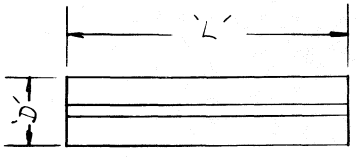
NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

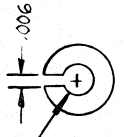
PROJ: 5 GHz FETAMP	TITLE: THREE STAGE COVER 1		
MATERIAL: OFHC COPPER		DRAWN BY: BON	DATE: 2/27/85
FINISH: 80 µin GOLD		DESIGNED BY:	DATE:
		APPROVED BY:	DATE:
SHEET NUMBER: 1/1	DRAWING NUMBER: B53205M102	REV. A 4/17/85	SCALE: NTS





DASH NO.	L_2	D_2	Z_{REF}	F_{REF}
-010	.310	.116	15.2	
-009	.290	.116	15.2	
-008	.270	.116	15.2	
-007	.427	.093	24.5	4.8
-006	.427	.073 (NO BRASS)	34.8	4.8
-005	.427	.102	21.0	4.8
-004	.427	.116	15.2	4.8
-013	.320	.106	19.1	
-012	.300	.106	19.1	
-011	.280	.106	19.1	





.073 DIA THRU (REAM)
SHOULD BE A SNUG, SLIP FIT
ON .073 DIA ROD AFTER PLATING.
CONTACT AT ENDS IMPORTANT.

MAT'L - BRASS

DASH NO.	'L'	'D'	Z_{REF}	F_{REF}
-003	.615	.113	24	4.8
-002	.615	.101	31	4.8
-001	.615	.084	41.8	4.8

DIA TOL = ±.001

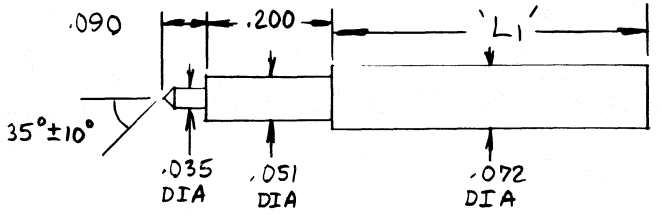
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±
3 PLACE DEC. (xxx) ± .005
2 PLACE DEC. (xx) ±
1 PLACE DEC. (x) ±

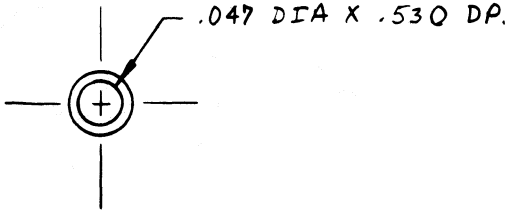
NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: 4.8 GHZ FETAMP
TITLE: TUNING SLUGS
MATERIAL: AS NOTED
DRAWN BY: RON DATE: 10/8/84
DESIGNED BY: DATE:
FINISH: 80 µin Cu / 40 µin Au
APPROVED BY: DATE:
SHEET NUMBER: 1/1
DRAWING NUMBER: B53205M103
REV. A 2/27/85
SCALE: 4:1

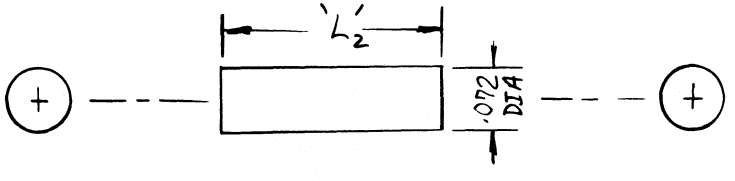
H. T. HALL

DASH NO	'L1'
-001	.570
-002	.590
-003	.610
-004	.630





IN/OUT LINE



INTERSTAGE LINE

-104	.420
-103	.400
-102	.390
-101	.370
DASH NO.	'L2'

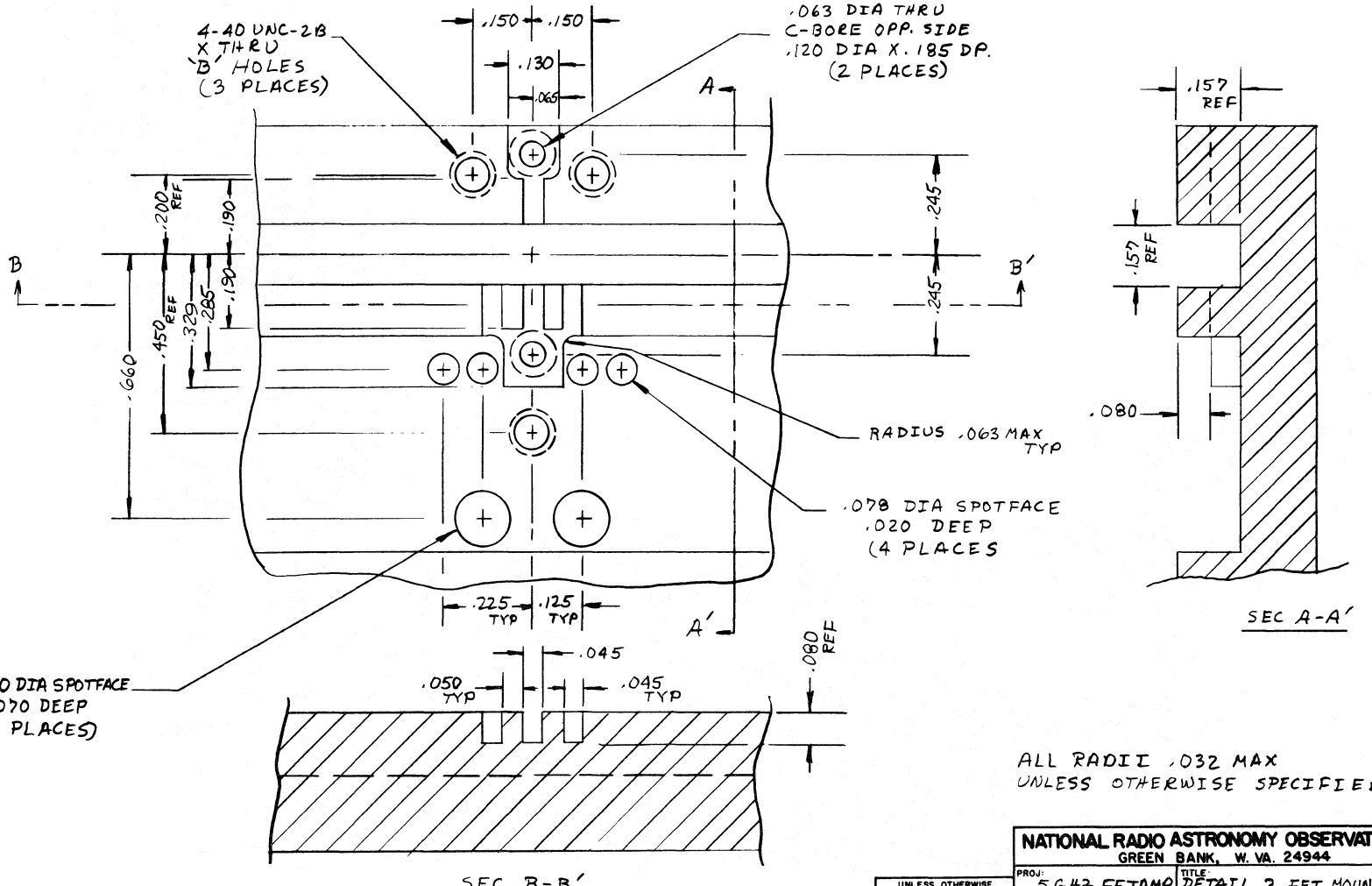
DIA TOL = ±.001

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES±
3 PLACE DEC.(xxx)± .003
2 PLACE DEC.(xx)±
1 PLACE DEC. (x)±

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: 5 GHz FETAMP	TITLE: 50 OHM LINES -2		
MATERIAL: BRASS		DRAWN BY: RON	DATE: 3/22/85
		DESIGNED BY:	DATE:
FINISH: 180µin CU/40µin AU		APPROVED BY:	DATE:
SHEET NUMBER: 1/1	DRAWING NUMBER: A53205M104	REV. 2 6/3/85	SCALE: NTS

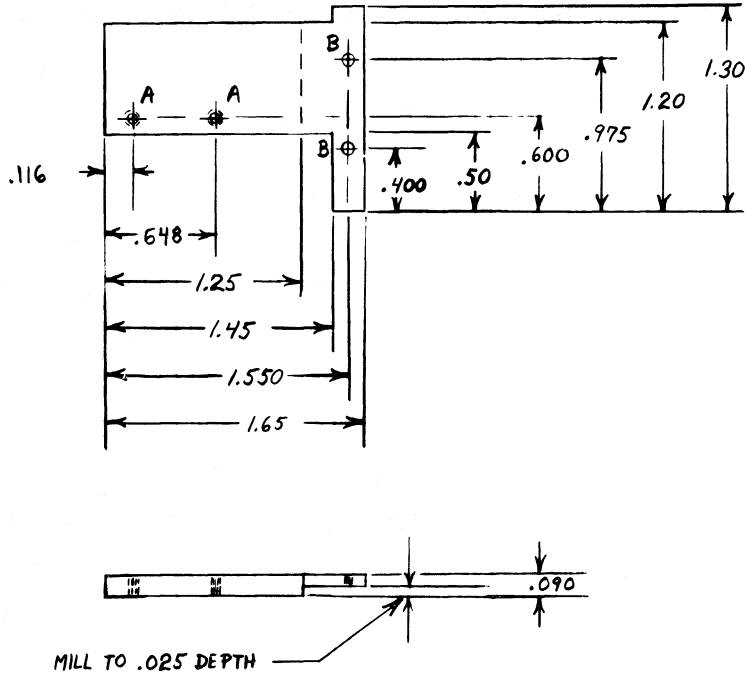
H.T. HALL



ALL RADII .032 MAX
UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	NATIONAL RADIO ASTRONOMY OBSERVATORY GREEN BANK, W. VA. 24944
TOLERANCES	PROJ: 5 GHz FETAMP — TITLE: DETAIL 2, FET MOUNTING
ANGLES ±	MATERIAL: ~ — DRAWN BY: RDN — DATE: 5/30/86
3 PLACE DEC. (xxx) ± .003	FINISH: ~ — DESIGNED BY: — DATE:
2 PLACE DEC. (xx) ±	APPROVED BY: — DATE:
1 PLACE DEC. (x) ±	SHEET NUMBER: — DRAWING NUMBER: B53205M 105 — REV. — SCALE: 2/1

K. T. HALL



A — 2-56 TAP THRU

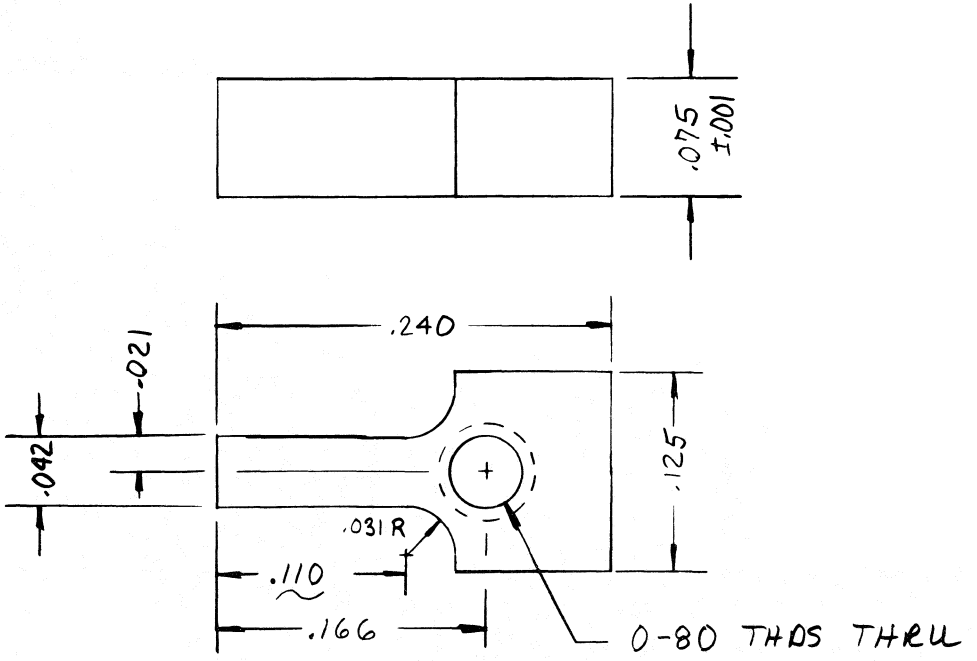
B — 2-56 CLEARANCE THRU

H. T. HALL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
3 PLACE DEC. (xxx) ± .005
2 PLACE DEC. (xx) ± .020
1 PLACE DEC. (x) ±

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: 5.0 GHz FET AMP	TITLE: CIRCULATOR COLD STRAP		
MATERIAL: .090 OFHC COPPER	DRAWN BY: SIMON		DATE: 5/30/85
FINISH: 80μ in GOLD	DESIGNED BY:		DATE:
	APPROVED BY:		DATE:
SHEET NUMBER:	DRAWING NUMBER: A53205M106	REV. C 6/3/85	SCALE: 1:1

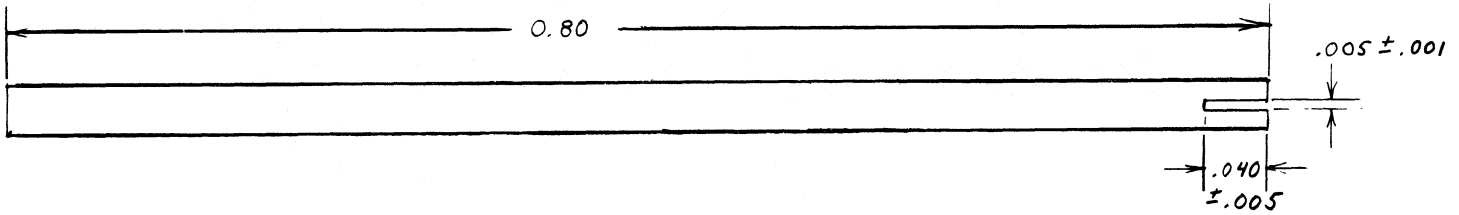


H. T. HALL

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ: FET DEVL	TITLE: TRANSISTOR STRAP II		
MATERIAL: 1/2 HARD BRASS	DRAWN BY: RON	DATE: 5/22/84	
FINISH: GOLD PLATE	DESIGNED BY:	DATE:	
	APPROVED BY:	DATE:	
SHEET NUMBER: 1/1	DRAWING NUMBER: 2.605-838-001	REV.	SCALE: 10:1

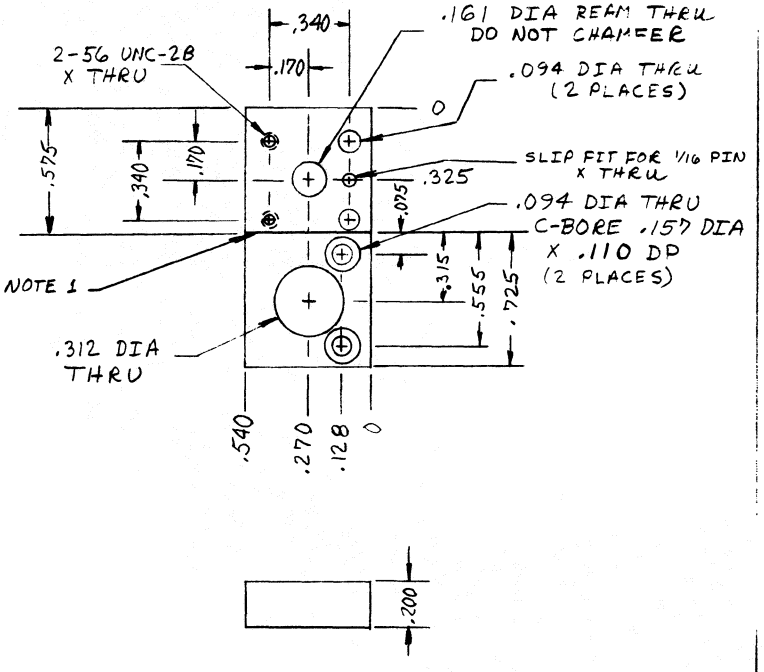
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
3 PLACE DEC. (xxx) ± .003
2 PLACE DEC. (xx) ±
1 PLACE DEC. (x) ±



H. T. HALL

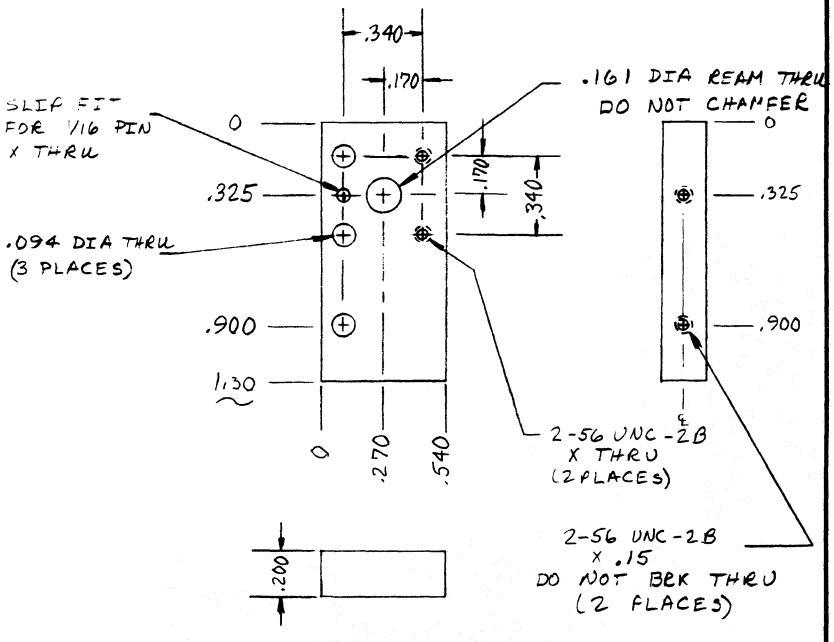
NATIONAL RADIO ASTRONOMY OBSERVATORY GREEN BANK, W. VA. 24944			
PROJ: 3 GHz FET	TITLE: DC BLOCK STUB		
MATERIAL: .031 DIA BRASS	DRAWN BY: RDN		DATE: 19 MAR 84
	DESIGNED BY:		DATE:
FINISH: 180μ in Cu, GOLD FLASH	APPROVED BY:		DATE:
SHEET NUMBER:	DRAWING NUMBER: 2.605-837-001	REV.	SCALE: 10:1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES ±
3 PLACE DEC. (xxx) ±
2 PLACE DEC. (xx) ± .020
1 PLACE DEC. (x) ±



-001

OUTPUT ENDPLATE



-002

INPUT ENDPLATE

NOTE1: DIVIDING LINE. ENDPLATE IS MADE IN TWO PARTS.

TOL .XX = ±.020 .XXX = ±.002	MATL OFHC COPPER	NRAO GREEN BANK, WV	
FINISH GOLD - 80 µin	SURFACE 32	SCALE: 2:1 / APPROVED BY: / DRAWN BY RDN	DATE: 6SEPT84 / REVISED 10/2/84
		3.2 GHz FETAMP, TWO STAGE 1 END PLATES	
		2.605-856-001, 002	DRAWING NUMBER