NATIONAL RADIO ASTRONOMY OBSERVATORY
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INTERFEROMETER 14.2 METER DIGITAL DATA LINK

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Dwayne R. Schiebel

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INTERFEROMETER 14.2 METER DIGITAL DATA LINK

Dwayne R. Schiebel

Introduction

The Digital Data Link consists of two systems: one which is located in Green Bank and one which is located on Point Mountain about 32 kilometers from Green Bank. A radio link enables digital data to be transmitted and received from the remote antenna. The DDP 116 can then read the received data or send data to the remote antenna.

Programming

To initiate a data transfer the link will interrupt the DDP 116 on interrupt line 14 (interrupt location 45). This interrupt should occur ten times a second. When the link receives data from the remote antenna the computer will be interrupted. Should the radio link drop out the computer will still receive a interrupt, but it will not be able to input data. When the DDP 116 receives the interrupt it has a maximum of 90 ms to output a commanded position and read thirteen words of data from the 14.2 m telescope.

INA 1017 Inputs up to thirteen data words received from the remote antenna. See Table I for format.

OTA 117 Outputs telescope commanded position. See Table V for format.

SKS 17 Skip if DDP 116 can input data.

SKS 117 Skip if DDP 116 can output data.

TABLE I

Bit Format Data from 14.2 m

Word	Function	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Range	Resolution
1	Indicated	ϕ	A														B	360° —	4.94385 s
2	Azimuth	ϕ	C			D												4.943 s	
3	Indicated	ϕ	A														B	360° —	4.94385 s
4	Elevation	ϕ	C			D												4.943 s	
5		ϕ	ϕ	ϕ	ϕ	ϕ	MUX ADDRESS			MULTIPLEXED DATA. SEE TABLE II.									
6		ϕ	ϕ	ϕ	ϕ	ϕ													
7		ϕ	ϕ	ϕ	ϕ	ϕ													
8	Front End Status	See Table III.																	
9	Control Panel	See Table IV.																	
10	Az Coarse Position	ϕ	400°	200°	100°	80°	40°	20°	10°	8°	4°	2°	1°	0.8°	0.4°	0.2°	0.1°		0.1°
11	El Coarse Position	ϕ																	0.1°
12	16 Bit TTL Data	E	Bits not assigned.																
13	Fast Analog Channel	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	S	X	X	X	X	X	X	± 5V		39 MV

A = 360°.

B = 0:01:19.1

C = 0:00:30.5

D = 0:00: 4.9

E = ϕ if remote antenna receives good data.

TABLE II

Multiplexed A/D Data from 14.2 m

Computer Word	Mux Address	Function	Range	Resolution
5	0	Barometric Pressure	572.0 - 699.5	0.5 MB
5	1	Dew Point	-64.0 - 63.5	0.5° C
5	2	Site Temperature	-64.0 - 63.5	0.5° C
5	3	Wind Speed	0 - 127.5	0.5 MPH
5	4	Wind Direction	0 - 510	2°
6	0	AZ Current	-64.0 - 63.5	0.5 A
6	1	AZ Error	-640.0 - 635.0	5 seconds
6	2	AZ Tach	-25.6 - 25.4	0.2°/min
6	3	Focus	0 - 73.95	0.29 cm
6	4	Trailer Temperature	-64.0 - 63.5	0.5° C
7	0	EL Current	-64.0 - 63.5	0.5 A
7	1	EL Error	-640.0 - 635.0	5 seconds
7	2	EL Tach	-25.6 - 25.4	0.2°/min
7	3	Slow Analog Ch. 1	$\pm$ 5 V	39 mV
7	4	Slow Analog Ch. 2	$\pm$ 5 V	39 mV

TABLE III

Bit Format Front End Control from 14.2 m

Bit	Function
1	100 kHz Lock.
2	1347.4 MHz Lock.

TABLE IV

Bit Format Control Panel from 14.2 m

Word	Function
1	Servo System OK Light: 0 = 0 K.
2	AZ CW Limit Light: 0 = In Limit.
3	AZ CCW Limit Light.
4	EL Up Limit Light.
5	EL Down Limit Light.
6	Stow Pin In Light: 0 = Pin In.
7	Stow Pin Out Light: 0 = Pin Out.
8	EL Axis Aligned Light: 0 = Aligned.
9	Accept Command Light: 0 = Accept.
10	Reject Command Light.
11	Brake Off Light.
12	Brake On Light.
13	Manual Light.
14	Computer Light.
15	
16	

TABLE V

Bit Format Commanded Position to 14.2 m

Word	Function	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Range	Resolution
1	AZ	ϕ	A														B	360° —	4.94385 s
2	Commanded	ϕ	C			D												4.943 s	
3	EL	ϕ	A														B	360° —	4.94385 s
4	Commanded	ϕ	C			D												4.943 s	

A = 360°

B = 00:01:19.1

C = 00:00:39.5

D = 00:00: 4.9

Electronics

The electronics can be divided into two systems. One system is the "Green Bank" system which sends 128 bits of information and receives 160 bits of information from the 14.2 m telescope. The other system is the "14.2 meter" system; it sends 160 bits of information to Green Bank and receives 128 bits of information.

A block diagram is provided for each system. This diagram could be used for quick reference to identify a particular card associated with its input or output data.

In general, the transmit section of each system contains a long shift register which is loaded with either digital data or some analog voltage converted-to-digital form. The conversion, loading and shifting is controlled by the card in slot 7. The receive section is a long shift register and data latch. The output data from this section will be in either digital or analog form. The receive section is also controlled by the card in slot 7.

Most cards in the system need no explanation. In the Green Bank system two busses are used: one to pass data to the DDP 116 (INBxx) and the micro bus which passes the data to the microprocessor. The 14.2 m system only has the micro bus.

One card worthy of note is the 14.2 m receive card, bits 1-48. This card converts the difference between commanded and indicated positions to an analog voltage. The list below is a rough estimate of voltage out for difference in.

Commanded 2.8° > indicated ... +10 V out

Commanded 2.8° < indicated ... -10 V out

For differences less than 2.8° the output will be about 4.88 mV for each 4.94 seconds of difference.

The microprocessor card is used to control two front panel displays which are provided to display data from both the transmit and receive sections of a system. The desired data display is selected by a digi-switch. A microprocessor (Motorola 6809) reads data in the shift registers and displays it in a meaningful format. The microprocessor card is the only card common to both systems except for the program stored in PROM's.

Microprocessor Program

This program reads the data in the shift registers and converts it to decimal or hexadecimal data to be displayed in the displays. Each display has an associated digit-switch to inform the program which data is requested. (See Table X.) In addition to displaying data, the program checks four words of position (indicated at GB and commanded at 14.2 m) for a most significant bit to be zero. If they are all zero, the program will set a data OK flip flop. This data OK, in addition to a hardware detection of sync enables data to be output from the link to the telescope and front end controls.

A special diagnostic mode can be entered by setting digi-switch A to 1F. In this mode, display A contains the number of data errors the program found since this counter was last reset. A plus sign in this display indicates that the counter has overflowed. Digi-switch B controls data that is displayed in display B and resets the block and error counters. Digi-switch B functions in the following manner:

Digi-Sw B = 00-0F	Displays last bad data block bits 1-120 in 8 bit chunks.
Digi-Sw B = 10	Resets error and block counters.
Digi-Sw B = 11	Displays receive block count; updates 10 times a second.

The indicated and commanded positions are displayed in hexadecimal. In order to be able to interpret this data, Appendix B is supplied to convert the two most significant bits to degrees, minutes, and seconds.

Tables VI and VII contain a card list for each system and Table VIII and IX are lists of particular bits used by the Green Bank system to control the front end and the telescope at Monterville.

Appendix A contains data sheets for the A/D and D/A used in these systems.

TABLE VI

Green Bank System

Slot	Function
4	Microprocessor card.
5	Transmit bits 49-128, 4 A/D channels, single bit data from control panel and front end and TTL data.
6	Transmit bits 1-48, commanded azimuth and elevation positions. Also interfaces with the DDP 116.
7	Transmit/receive control and bi-phase generator and decoder.
8	Receive bits 105-160, coarse indicated AZ/EL positions (in BCD), TTL data from 14.2 m, and one fast analog channel from 14.2 m.

TABLE VII

14.2 m System

Slot	Function
3	Microprocessor card.
4	Transmit bits 105-160, AZ/EL coarse indicated position (in BCD), TTL data in and fast analog data.
5	Transmit bits 73-104, single bit control data from front end and control panel.
6	Transmit bits 1-72, indicated AZ/EL positions and multiplexed analog data (weather and telescope).
7	Transmit/receive control and bi-phase generator and decoder.
8	Receive bits 81-128, single bit indication of front end and control panel from Green Bank and TTL data from Green Bank.
9	Receive bits 49-80, four analog channels.
10	Receive bits 1-48, commanded AZ/EL positions from DDP 116 at Green Bank.

TABLE VIII

Bit Format Front End Control to 14.2 m

Bit	Function
1	XR-XL IF
2	SR-SL IF
3	XR-SL IF
4	Paramps Off
5	Noise Mode
6	X Cal On
7	S Cal On

TABLE IX

Bit Format Control Panel to 14.2 m

Bit	Function
1	Power On
2	Power Off
3	Accept Command
4	Reject Command
5	EL Stow Pin Out
6	EL Stow Pin In
7	Brake Off
8	Brake On
9	Computer Control
10	Emergency Stop
11	Pots "Zero Off"
12	Telescope Lights On/Off

Credits

Credit should be given to the following for their help in this proejct: Ron Weimer for his suggestions and design of the transmit/receive control card; Rich Lacasse for his suggestions on the microprocessor card and help with its program; Bill Vrable and Jerry Turner for constructing the systems; Carolyn Dunkle for typing this report; and the Green Bank Machine Shop for building the chassis and engraving front panels.

Memonic List: Green Bank End

Memonic	Origin Slot	Function
AZI	10	Azimuth Motor Current Indication to Control Panel
BLØ-BL2	4	Blanking for Front Panel Display
CPIXX	J5	Single Bit Telescope Control Data to 14.2 m
CPXX	9	Single Bit Telescope Data from 14.2 m
$\overline{\text{DACK}}$	J7	From External Device to Reset TTL "DRDY"
DATA A	9	Rec. Data Out of Shift Register Bits 1-72
DATA B	8	Rec. Data Out of Shift Register Bits 1-104
$\overline{\text{DATA OK}}$	4	Received Data Checks Good
DATA OUT	6	Serial Data Out Bits 1-128 to Bi-Phase Generator
DATA OUT TO RF	7	Bi-Phase Data Out Bits 1-128
DISPLAY BUS	8	Coarse Display Data to Control Panel
DPØ-DP1	4	Decimal Point for Front Panel Display
DRDY	8	Tells External Device TTL Data is Ready
$\overline{\text{DRL}}$	6	Data Ready Indication to 116
DSP $\overline{\text{LD}}$	8	Latch Pulse for Control Panel Coarse Display
$\overline{\text{EAXX}}$	6	Enable A Bus (Data to 116)
$\overline{\text{EBXX}}$	4	Enable B Bus (Data to Micro-Processor)
ELI	10	Elevation Motor Current Indication to C.P.
FAST ANALOG	8	Analog Data from 14.2 Updates 10 Times a Second
FEIXX	J8	Single Bit Front End Control to 14.2 m
FEXX	9	Single Bit Data, Front End from 14.2 m
$\overline{\text{FULL}}$	7	Transfers Rec. Data from Shift Register to Latch
$\overline{\text{HOLD OUTPUT}}$	5	Keeps 116 from Outputting Data while SR is Shifting
$\overline{\text{HOLD TTL}}$	5	Keeps TTL Data from Changing during Shift
HZ 50	7	50 Hz Square Wave to RF Chassis
INB XX	8,9,10	Received Data to 116
INT	7	Force 116 Interrupt When GB Does Not Receive Data
LATCH SR	7	Latches Data in Shift Register Prior to Transmit
MICRO BUS X	5,6,8,9,10	Data to Micro-Processor
$\overline{\text{NMI}}$	7	Interrupts 116 when Shift Register Contains Data
$\overline{\text{ON 5V}}$	7	Enables Received Data to Front End & Control Panel
OTB XX	J1	Output Data from 116

Continued --

Memonic List: Green Bank End (continued):

Memonic	Origin Slot	Function
PIL 14	6	Interrupts 116 when Data is Ready
REC CLOCK	7	Clock to Receive Shift Register
REC DATA	BNC	Bi-Phase Received Data
$\overline{\text{REC INT}}$	7	Causes 116 to be Interrupted when Data is Ready
SA7.3 & 7.4	10	Spare Analog Data from 14.2 m
Send Data A	5	Data Out of Transmit Shift Register Bits 49-128
SGC, SGD	4	Sign for Front Panel Display
SR FULL	7	Opposite Phase of Full
SR REC DATA	7	Serial Data from 14.2 m
SR XMIT CLOCK	7	Transmit Shift Register Clock
START CONVERT	7	Starts A/D Conversion in GB Send Logic
TTL DATA	J7	Single Bit TTL Data to 14.2 m
TTL OUT	8	TTL Data from 14.2 m
WIND OUT	8	DC Voltage Indication of Wind Speed at 14.2 m
WSIX	10	Wind Speed at 14.2 m in Digital Form

Memonic List: 14.2 meter End

Memonic	Origin Slot	Function
A5-, A6-, A7-	J5	Analog Return for Multiplexed Analog Data
ANALOG X.X	J5	Analog Voltage for Multiplexed Analog Data
AZ POS ERR	10	Azimuth Position Error Voltage to Servo
AZ RATE	9	Manual Rate to Move Antenna from GB
AZ XX	J6	Azimuth Indicated Position
BLØ-BL2	3	Blanking for Front Panel Displays
CPIXX	J2	Single Bit Data from Telescope Control Panel
CPXX	8	Single Bit Control Panel Data from GB
$\overline{\text{DACK}}$	J1	Resets TTL Data Ready Condition
DATA B	9	Receive Serial Data Bits 1-48
DATA C	8	Receive Serial Data Bits 1-80
$\overline{\text{DATA OK}}$	3	Receive Data Checks OK
DATA OUT	6	Transmit Serial Data Bits 1-160
D DATA	J1	TTL Data In at 14.2 m
DISPLAY BUS XX	4	Data Bus to Coarse Display in Control Panel
DPØ-DP1	3	Decimal Point for Front Panel Display
DSP LDX	4	Load Pulse for Coarse Display Data
$\overline{\text{EBXX}}$	3	Enable B Bus (Data to Micro-Processor)
EL POS ERR	10	Elevation Position Error Voltage to Servo
EL RATE	9	Manual Elevation Rate to Move Antenna from GB
EL XX	J7	Indicated Elevation Position
FA 1/2	9	Fast Analog Data from Green Bank
FEIXX	J4	Single Bit Data from Front End
FEXX	8	Single Bit Front End Data from GB
$\overline{\text{FULL}}$	7	Transfers Data from Rec. Shift Register to Buffer
$\overline{\text{HOLD}}$	4	Hold TTL Data to Load Shift Register
LATCH SR	7	Latches Data in Transmit Shift Register
MICRO BUS X	4,5,6,8,9,10	Data Bus to the Micro-Processor
$\overline{\text{NMI}}$	7	Interrupts Micro-Processor to Take Data
$\overline{\text{ON 5V}}$	7	Enables Data to Control Panel and Front End

Continued --

Memonic List: 14.2 meter End (continued):

Memonic	Origin Slot	Function
RDY	8	Indicates TTL Data is Available
REC DATA	BNC	Bi-Phase Data from Receiver
SEND DATA A	5	Transmit Serial Data Bits 73-160
SEND DATA B	4	Transmit Serial Data Bits 105-160
SGC, SGD	3	Sign for Front Panel Displays
SR REC DATA	7	Serial Data to Rec. Shift Register
SR XMIT CLOCK	7	Clock for Transmit Shift Register
START CONV.	7	Starts A/D Conversion Prior to Transmit
TTLXX	8	Single Bit TTL Data from Green Bank
XMIT DATA	7	Bi-Phase Serial Data to Transmitter

TABLE X

Display Select

Digi-Switch	Function	Display Format
00	Indicated AZ Position	Hexidecimal
1	Indicated EL Position	Hexadecimal
2	Barometric Pressure	Millibar
3	Dew Point	Degrees Centigrade
4	Site Temperature	Degrees Centigrade
5	Wind Speed	MPH
6	Wind Direction	Degrees
7	AZ Current	Amps
8	AZ Error	Seconds
9	AZ Tach	Degrees/Minute
0A	Focus	CM
B	Control Room Temperature	Degrees Centigrade
C	EL Current	Amps
D	EL Error	Seconds
E	EL Tach	Degrees/Minute
0F	Slow Analog 1 & 2 from 14.2 m	Hexadecimal, SA1 = 2 MSD
10	Front-End Status from 14.2 m	Hexadecimal
1	Control Panel Status from 14.2 m	Hexadecimal
2	16 Bit TTL from 14.2 m	Hexadecimal*
3	Fast Analog from 14.2 m	Hexadecimal
4	Command AZ Pos	Hexadecimal
5	Commanded EL Pos	Hexadecimal
6	Fast Analog CH 1 & 2 to 14.2 m	Hexadecimal
7	AZ/EL Rate to 14.2 m	Hexadecimal
8	Control Panel Status at Green Bank	Hexadecimal
19	Front End Status at Green Bank	Hexadecimal
A	16 Bit TTL at Green Bank	Hexadecimal
B	AZ Servo Drive (only valid at 14.2 m)	Hexadecimal
C	EL Servo Drive (only valid at 14.2 m)	Hexadecimal
D	Spare	
E	Spare	
F	Special Diagnostic Mode.	

* MSB = Ø if 14.2 receives good data.

APPENDIX A

(1) Analog Devices Data Sheet, AD570, "Low Cost, Complete IC, 8-Bit A to D Converter".

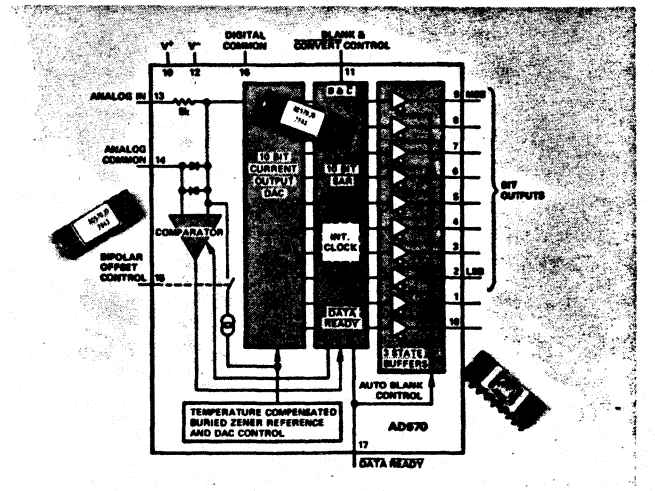
(2) Data Sheet HS DAC80, "Complete 12-Bit D/A Converter".

ANALOG DEVICES

Low Cost, Complete IC 8-Bit A to D Converter

AD570*

FEATURES
Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
0 to +70°C – AD570J
-55°C to +125°C – AD570S
Digital Multiplexing – 3 State Outputs
18 Pin Ceramic DIP
Low Cost Monolithic Construction



PRODUCT DESCRIPTION

The AD570 is an 8-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 25μs.

The AD570 incorporates the most advanced integrated circuit design and processing technology available today. I^2L (integrated injection logic) processing in the fabrication of the SAR function along with laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) and a temperature compensated, subsurface Zener reference insures full 8-bit accuracy at low cost.

Operating on supplies of +5V and -15V, the AD570 will accept analog inputs of 0 to +10V unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD570 executes a true 8-bit conversion with no missing codes in approximately 25μs.

The AD570 is available in two versions; the AD570J is specified for the 0 to 70°C temperature range, the AD570S for -55°C to +125°C. Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges and are packaged in 18-pin hermetically-sealed ceramic DIP's.

PRODUCT HIGHLIGHTS

1. The AD570 is a complete 8-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.8% (2LSB of 8 bits) is achieved without external trims.
2. The AD570 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD570 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V supplies. The device will also operate with a -12V supply.
6. The AD570S is also available with full processing to MIL-STD-883B, Class B. The single chip construction and functional completeness make the AD570 especially attractive for high reliability applications.
7. Every AD570 is subjected to long-term stabilization bakes, given a powered burn-in at +125°C, and temperature cycled ten times from -65°C to +150°C prior to final test to insure reliability and long-term stability. In addition, all units are tested 100% at the extremes of their respective temperature ranges for all parameters to guarantee full performance.

***Covered by Patent No. 3,940,760, other patents pending.**

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SPECIFICATIONS

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

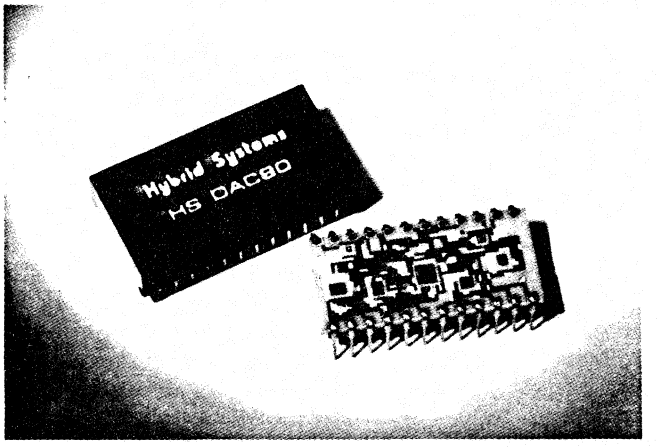
MODEL	AD570JD	AD570SD/AD570SD-883B[1]
RESOLUTION[2]	8 Bits	*
RELATIVE ACCURACY @ 25°C[2,3,4]	±1/2LSB max	*
T_{min} to T_{max}	±1/2LSB max	*
FULL SCALE CALIBRATION[4,5] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*
UNIPOLAR OFFSET (max)[4]	±1/2LSB	*
BIPOLAR OFFSET (max)[4]	±1/2LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)		
+25°C	8 Bits	*
T_{min} to T_{max}	8 Bits	*
TEMPERATURE RANGE	0 to +70°C	-55°C to +125°C
TEMPERATURE COEFFICIENTS[4]		
Guaranteed max Change		
T_{min} to T_{max}		
Unipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Bipolar Offset	±1LSB (88ppm/°C)	±1LSB (40ppm/°C)
Full Scale Calibration[6] (With 15Ω Fixed Resistor or 200Ω Trimmer)	±2LSB (176ppm/°C)	±2LSB (80ppm/°C)
POWER SUPPLY REJECTION[4]		
Max Change In Full Scale Calibration		
TTL Positive Supply		
+4.5V≤V+≤+5.5V	±2LSB max	*
Negative Supply		
-16.5V≤V-≤-13.5V	±2LSB max	*
ANALOG INPUT RESISTANCE	3kΩ min	*
	5kΩ typ	*
	7kΩ max	*
ANALOG INPUT RANGES		
(Analog Input to Analog Common)		
Unipolar	0 to +10V	*
Bipolar	-5V to +5V	*
OUTPUT CODING		
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary	*
LOGIC OUTPUT		
Bit Outputs and $\overline{\text{Data Ready}}$		
Output Sink Current	3.2mA min	*
(V_{OUT} = 0.4V max, T_{min} to T_{max})	(2TTL Loads)	*
Output Source Current (Bit Outputs)[7]		
(V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*
Output Leakage When Blanked	±40μA max	*
LOGIC INPUT		
Blank and Convert Input		
0≤V_{in}≤V+	±40μA max	*
Blank – Logic "1"	2.0V min	*
Convert – Logic "0"	0.8V max	*
CONVERSION TIME	15μs min	*
	25μs typ	*
	40μs max	*

Complete 12-Bit D/A Converter

FEATURES

- Low Cost
- 12-Bit Resolution
- Fast-Output Settling
- ±1/2 LSB Linearity
- Voltage or Current Output
- TTL and CMOS Compatible
- Wide Operating Supply Range

NEW!



DESCRIPTION

HS DAC80 is a low cost, general purpose 12-bit digital to analog converter. It consists of matched bipolar switches, a precision network, a low drift reference and a fast settling output amplifier (V Model only). The inputs are complementary-binary coded and can be driven by either TTL or CMOS logic up to +15 Volt. The input thresholds are standard TTL.

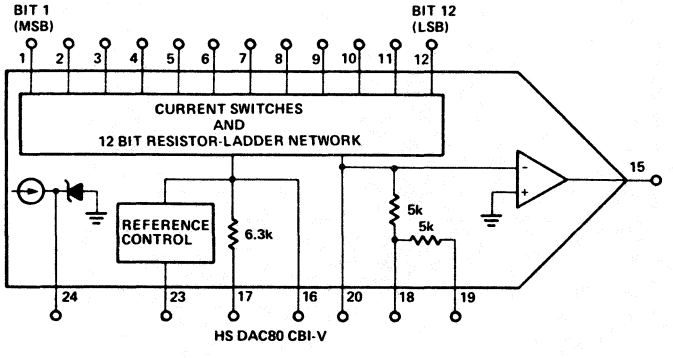
HS DAC80 comes in two versions, a voltage output model (HS DAC80-CBI-V) with pin programmable output ranges of ±2.5V, ±5V, ±10V, 0 to +5V and 0 to +10V, and a current output model (HS DAC80-CBI-I) with output ranges of either ±1mA or 0 to -2mA.

Centerpiece of the HS DAC80 is a bipolar monolithic fast settling MDAC. Special buffers are connected to its inputs for TTL and CMOS input compatibility. A low current, low drift, temperature compensated reference diode acts as voltage reference for the MDAC, and includes a control circuit which provides a gain adjustment feature.

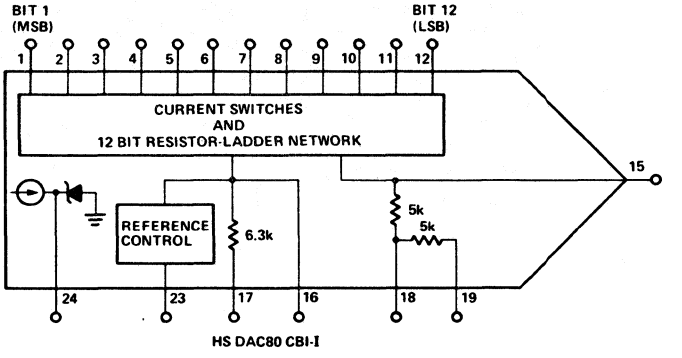
The on-chip thin film resistor ladder network is actively laser trimmed for output linearity error of less than 1/2 LSB. Output offset, gain and range scaling resistors are all factory trimmed for optimum performance.

HS DAC80 is packaged in a proprietary ceramic/plastic compound 24-pin DIP. The patented design of this package offers greatly increased sealing surface compared to "glued on lid" type packages; is leakproof, and will withstand all usual environmental hazards in its 0 to +70°C operating temperature range. In addition, no internal wires or components are in contact with any resins or epoxy, with substantial improvement in reliability as a result.

FUNCTIONAL DIAGRAMS



HS DAC80 CBI-V



HS DAC80 CBI-I

SPECIFICATIONS

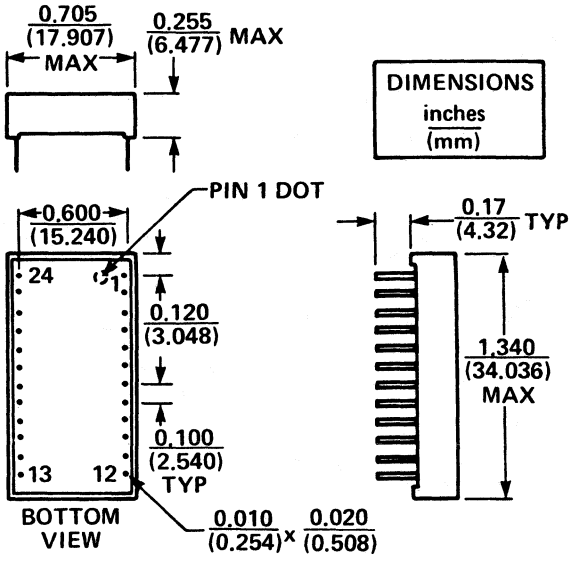
(T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	HS DAC80-CBI
DIGITAL INPUT	
Resolution	12-Bits
Coding	Complementary Binary/Offset Binary
Logic Levels	
Logical "1" (at +1μA)	+2V DC min, +15V DC max
Logical "0" (at -100μA)	0V DC min, +0.8V DC max
ACCURACY	
Linearity Error	±1/4LSB typ, ±1/2LSB[1] max
Differential Linearity Error	±1/2LSB typ, ±3/4LSB max
Gain Error[2]	±0.1% typ, ±0.3% max
Offset Error[2]	±0.05% FSR typ, ±0.15% FSR[3] max
Monotonicity Temp. Range	0 to +70°C
DRIFT[4] (0 to +70°C)	
Total Bipolar Drift (Includes Gain, Offset, and Linearity Drifts)	±25ppm FSR/°C max
Total Error Over 0 to +70°C[5]	
Unipolar	±0.08% FSR typ, ±0.15% FSR max
Bipolar	±0.06% FSR typ, ±0.12% FSR max
Gain	±15ppm/°C typ, ±30ppm/°C max
Exclusive of Internal Ref.	±10ppm/°C max
Unipolar Offset	±1ppm FSR/°C typ, ±3ppm FSR/°C max
Bipolar Offset	±7ppm FSR/°C typ, ±15ppm FSR/°C max
Differential Linearity Error 0 to +70°C	+1, -7/8 LSB max
Linearity Error 0 to +70°C	±1/2 LSB max
CONVERSION SPEED/V Models	
Settling Time to ±0.01% of FSR For FSR Change	
with 10kΩ Feedback	5μs typ
with 5kΩ Feedback	3μs typ
For 1 LSB Change	1.5μs typ
Slew Rate	10V/μs min, 18V/μs typ
CONVERSION SPEED/I Models	
Settling Time to ±0.01% of FSR For FSR Change	
10 to 100Ω Load	300ns typ
1kΩ Load	1μs typ
ANALOG OUTPUT/V Models	
Ranges	±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V
Output Current	±5mA min
Output Impedance (DC)	0.05Ω typ
Short Circuit Duration	Indefinite to Common
ANALOG OUTPUT/I Models	
Ranges	±1mA, 0 to -2mA typ
Output Impedance - Bipolar	3.2kΩ typ
Output Impedance - Unipolar	6.6kΩ typ
Compliance	±2.5V
INTERNAL REFERENCE VOLTAGE	+6.3V
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max
External-Use Current[6]	±200μA max
POWER SUPPLY SENSITIVITY	
+15V Supply	±0.02% FSR/% V_S max
-15V Supply	±0.002% FSR/% V_S max
POWER SUPPLY REQUIREMENTS[7]	
DAC80	±8V DC min ±15V DC typ ±16V DC max
Supply Drain	
+15 (Including 5mA Load)	30mA max
-15 (Including 5mA Load)	20mA max
+5V (Logic Supply)	Not required
TEMPERATURE RANGE	
Operating	0 to +70°C max
Storage	-55°C to +85°C

NOTES

1. Least Significant Bit (LSB).
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. With gain and offset errors adjusted to zero at +25°C.
6. Maximum with no degradation of specifications with constant load.
7. Power supply sensitivity may increase substantially at minimum supply voltages.

PACKAGE OUTLINE



PIN DIAGRAM

PIN	FUNCTION	
	I-Models	V-Models
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12 (LSB)	Bit 12 (LSB)
13	Not Required*	Not required*
14	-15V Supply	-15V Supply
15	I_{out}	V_{out}
16	Ref. Input	Ref. Input
17	Bipolar Offset	Bipolar Offset
18	Scaling Network	10V Range
19	Scaling Network	20V Range
20	N. C.	Summing Junction
21	Ground	Ground
22	+15V Supply	+15V Supply
23	Gain Adjust	Gain Adjust
24	6.3 $V_{Ref. Out}$	6.3$V_{Ref. Out}$

* The Logic Supply terminal is not connected internally.

APPENDIX B

Table to Convert from 2 MSD Hex Digits of Display to DD MM SS

TABLE TO CONVERT FROM 2MSD HEX DIGITS OF DISPLAY TO DD MM SS

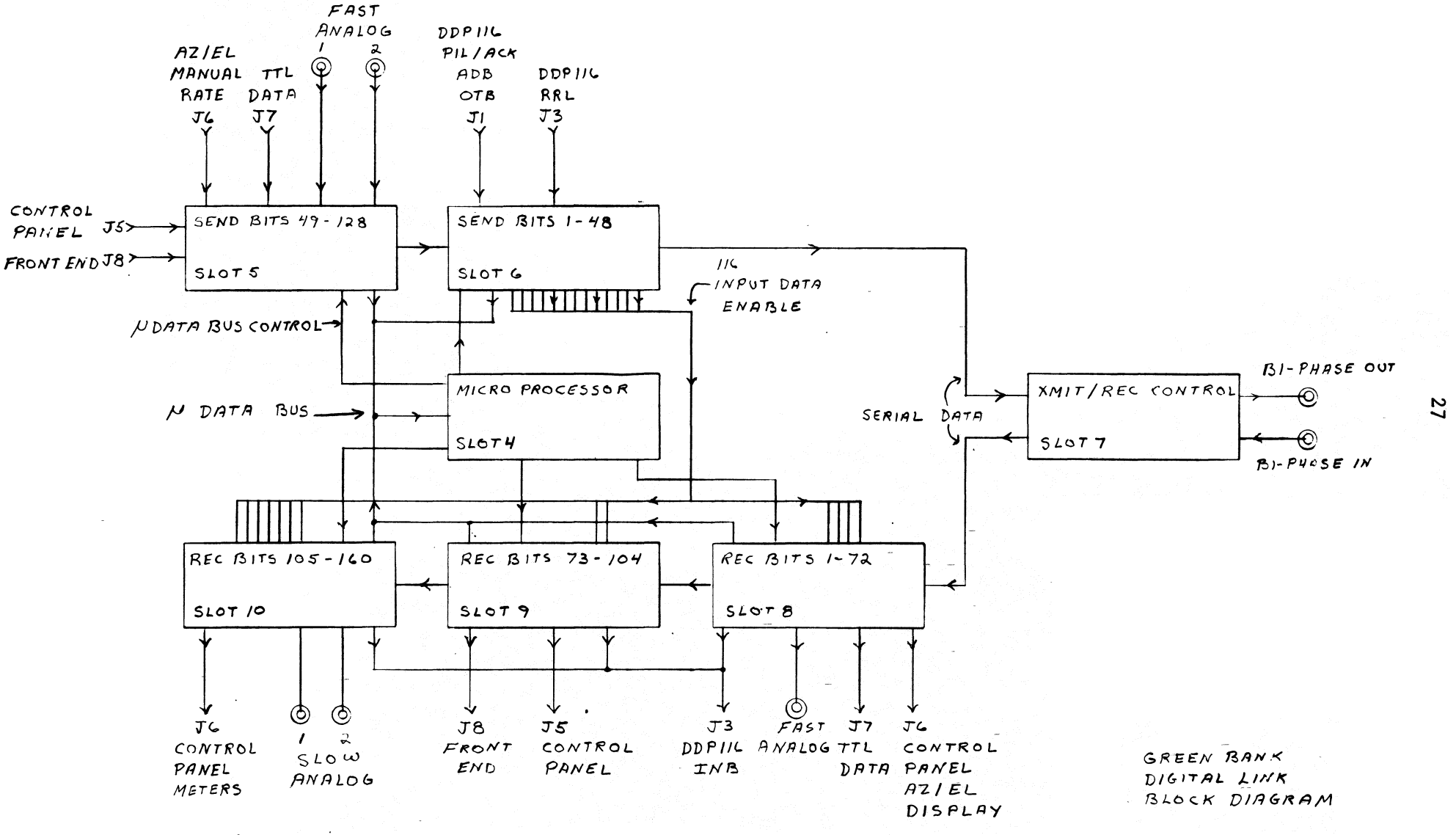
HEX	POSITION
01	005:37:30.00
02	011:15:00.00
03	016:52:30.00
04	022:30:00.00
05	029:07:30.00
06	033:45:00.00
07	039:22:30.00
08	045:00:00.00
09	050:37:30.00
0A	056:15:00.00
0B	061:52:30.00
0C	067:30:00.00
0D	073:07:30.00
0E	078:45:00.00
0F	084:22:30.00
10	090:00:00.00
11	095:37:30.00
12	101:15:00.00
13	106:52:30.00
14	112:30:00.00
15	118:07:30.00
16	123:45:00.00
17	129:22:30.00
18	135:00:00.00
19	140:37:30.00
1A	146:15:00.00
1B	151:52:30.00
1C	157:30:00.00
1D	163:07:30.00
1E	168:45:00.00
1F	174:22:30.00
20	180:00:00.00
21	185:37:30.00
22	191:15:00.00
23	196:52:30.00
24	202:30:00.00
25	208:07:30.00
26	213:45:00.00
27	219:22:30.00
28	225:00:00.00
29	230:37:30.00
2A	236:15:00.00
2B	241:52:30.00
2C	247:30:00.00
2D	253:07:30.00
2E	258:45:00.00
2F	264:22:30.00
30	270:00:00.00
31	275:37:30.00
32	281:15:00.00
33	286:52:30.00
34	292:30:00.00
35	298:07:30.00
36	303:45:00.00
37	309:22:30.00
38	315:00:00.00

TABLE TO CONVERT FROM 2MSD HEX DIGITS OF DISPLAY TO DD MM SS

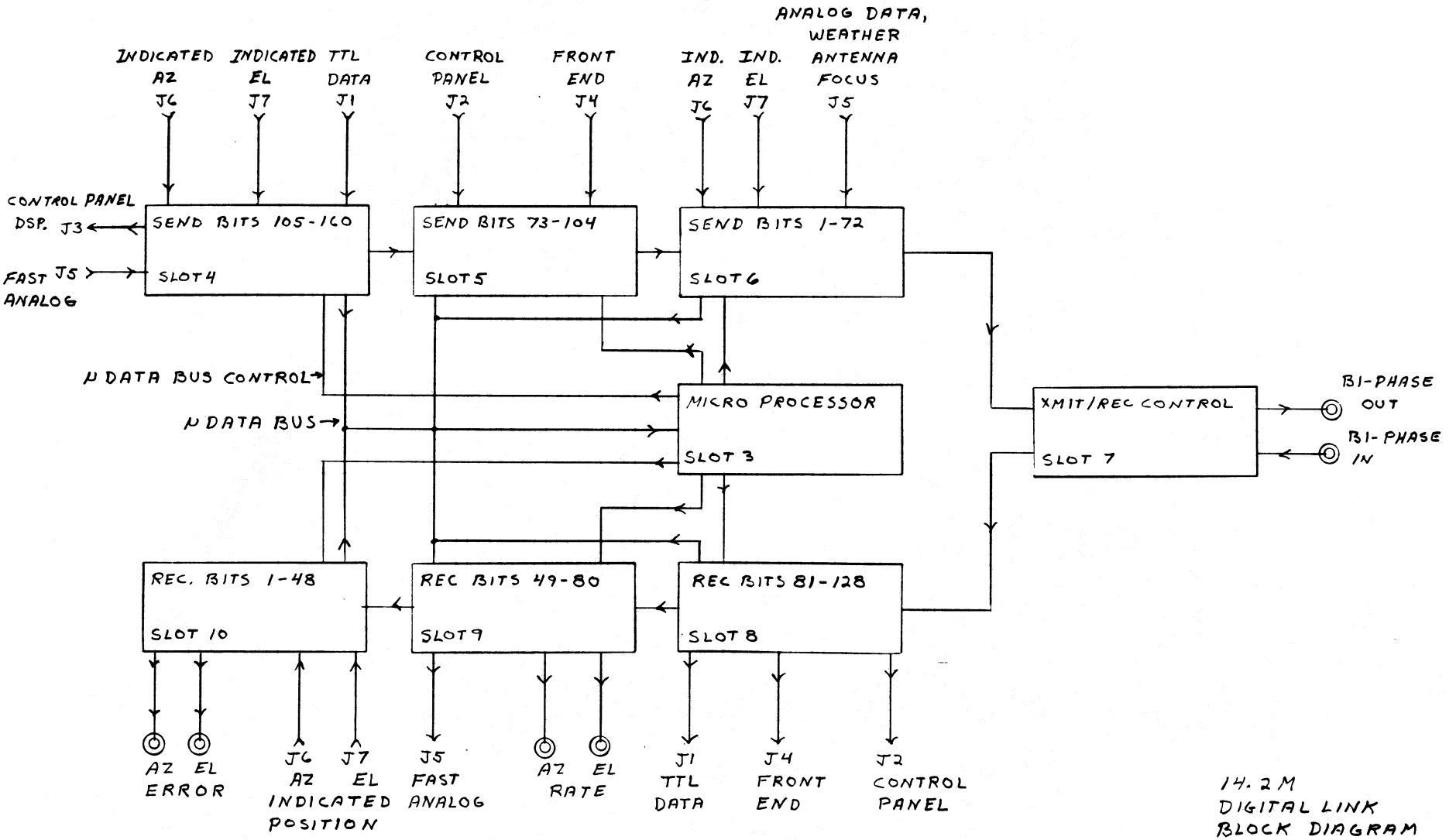
HEX	POSITION
39	320:37:30.00
3A	326:15:00.00
3B	331:52:30.00
3C	337:30:00.00
3D	343:07:30.00
3E	348:45:00.00
3F	354:22:30.00
40	360:00:00.00
41	365:37:30.00
42	371:15:00.00
43	376:52:30.00
44	382:30:00.00
45	388:07:30.00
46	393:45:00.00
47	399:22:30.00
48	405:00:00.00
49	410:37:30.00
4A	416:15:00.00
4B	421:52:30.00
4C	427:30:00.00
4D	433:07:30.00
4E	438:45:00.00
4F	444:22:30.00
50	450:00:00.00
51	455:37:30.00
52	461:15:00.00
53	466:52:30.00
54	472:30:00.00
55	478:07:30.00
56	483:45:00.00
57	489:22:30.00
58	495:00:00.00
59	500:37:30.00
5A	506:15:00.00
5B	511:52:30.00
5C	517:30:00.00
5D	523:07:30.00
5E	528:45:00.00
5F	534:22:30.00
60	540:00:00.00
61	545:37:30.00
62	551:15:00.00
63	556:52:30.00
64	562:30:00.00
65	568:07:30.00
66	573:45:00.00
67	579:22:30.00
68	585:00:00.00
69	590:37:30.00
6A	596:15:00.00
6B	601:52:30.00
6C	607:30:00.00
6D	613:07:30.00
6E	618:45:00.00
6F	624:22:30.00
70	630:00:00.00

TABLE TO CONVERT FROM 2MSD HEX DIGITS OF DISPLAY TO DD MM SS

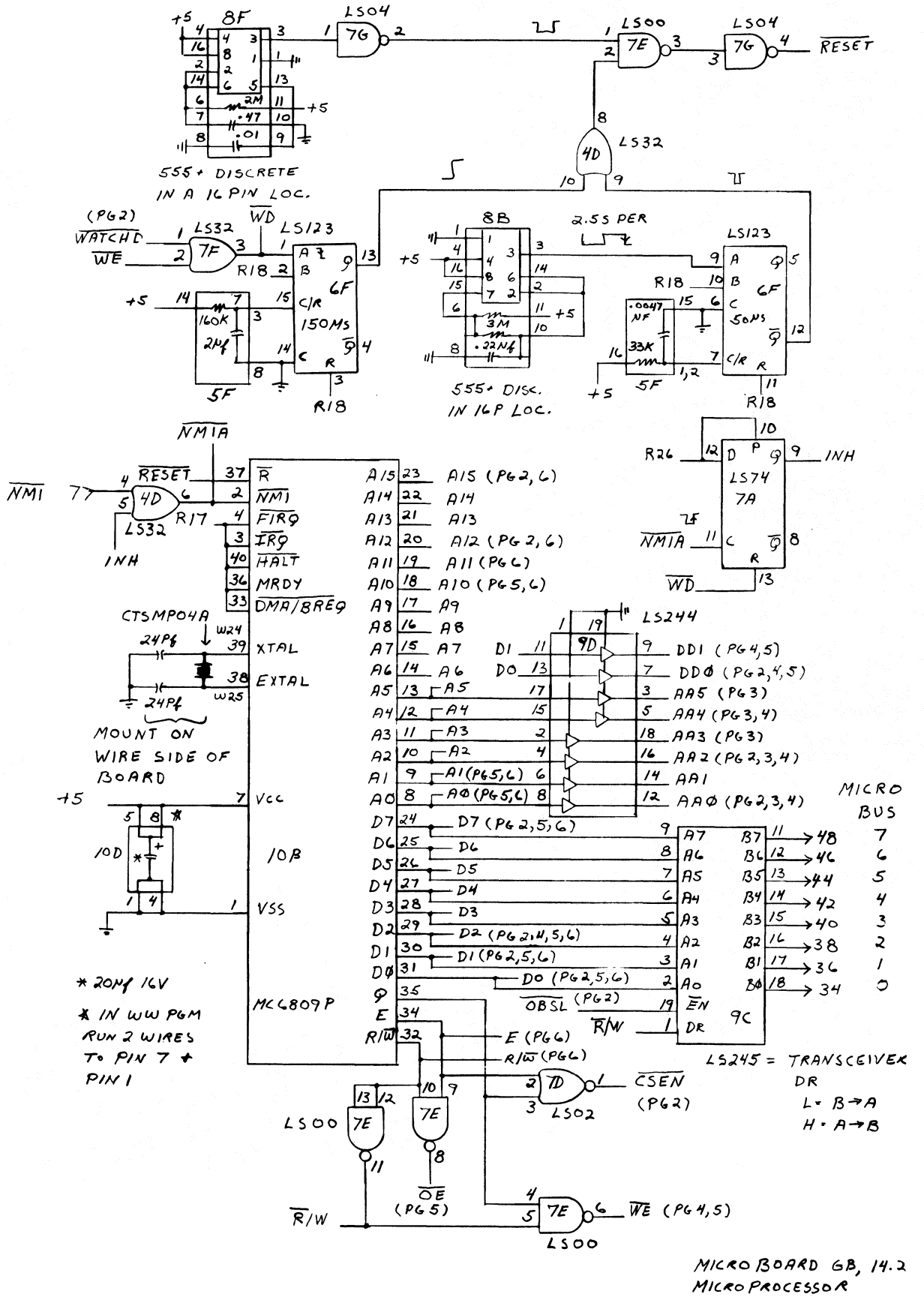
HEX	POSITION
71	635:37:30.00
72	641:15:00.00
73	646:52:30.00
74	652:30:00.00
75	658:07:30.00
76	663:45:00.00
77	669:22:30.00
78	675:00:00.00
79	680:37:30.00
7A	686:15:00.00
7B	691:52:30.00
7C	697:30:00.00
7D	703:07:30.00
7E	708:45:00.00
7F	714:22:30.00

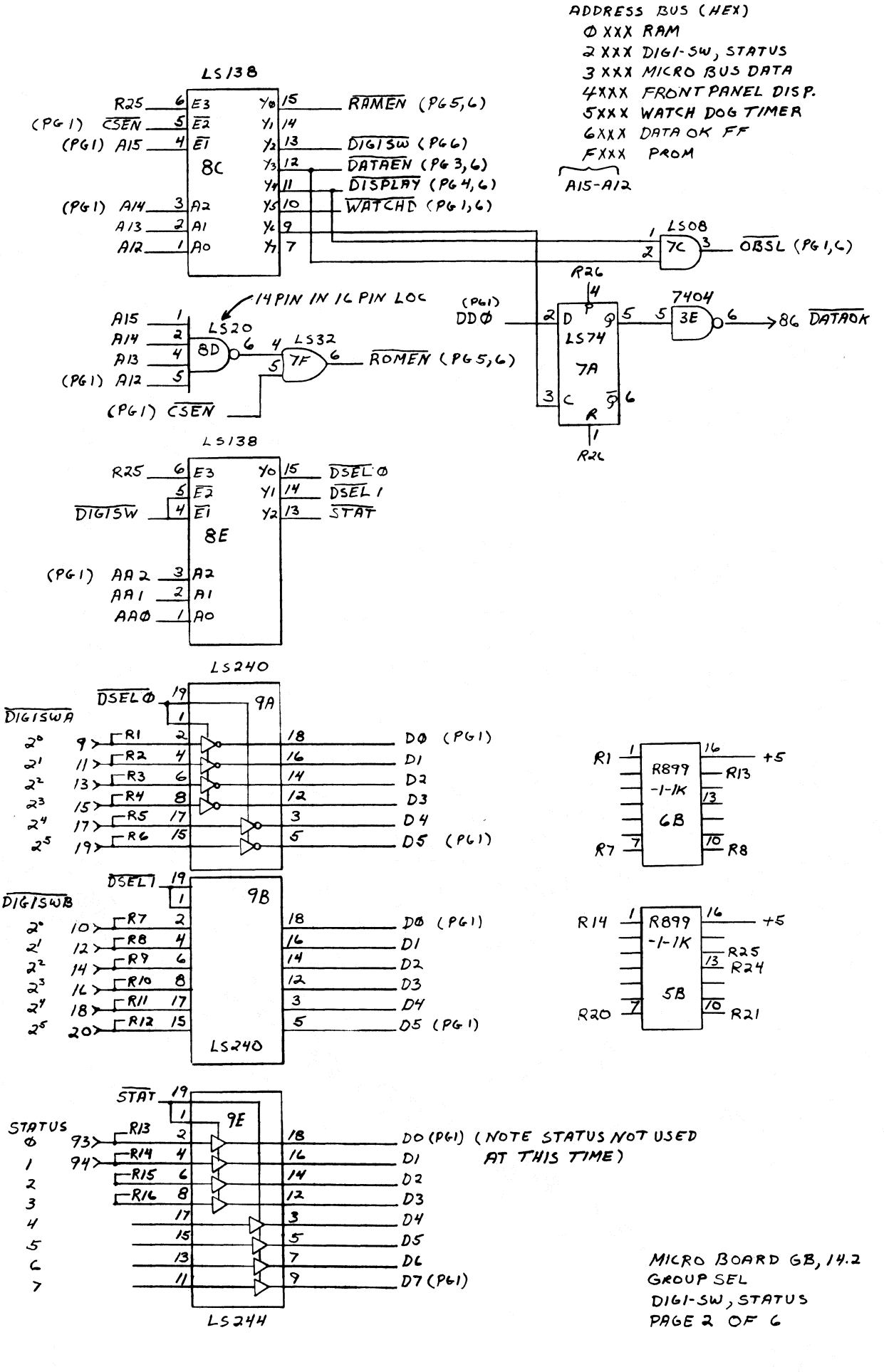


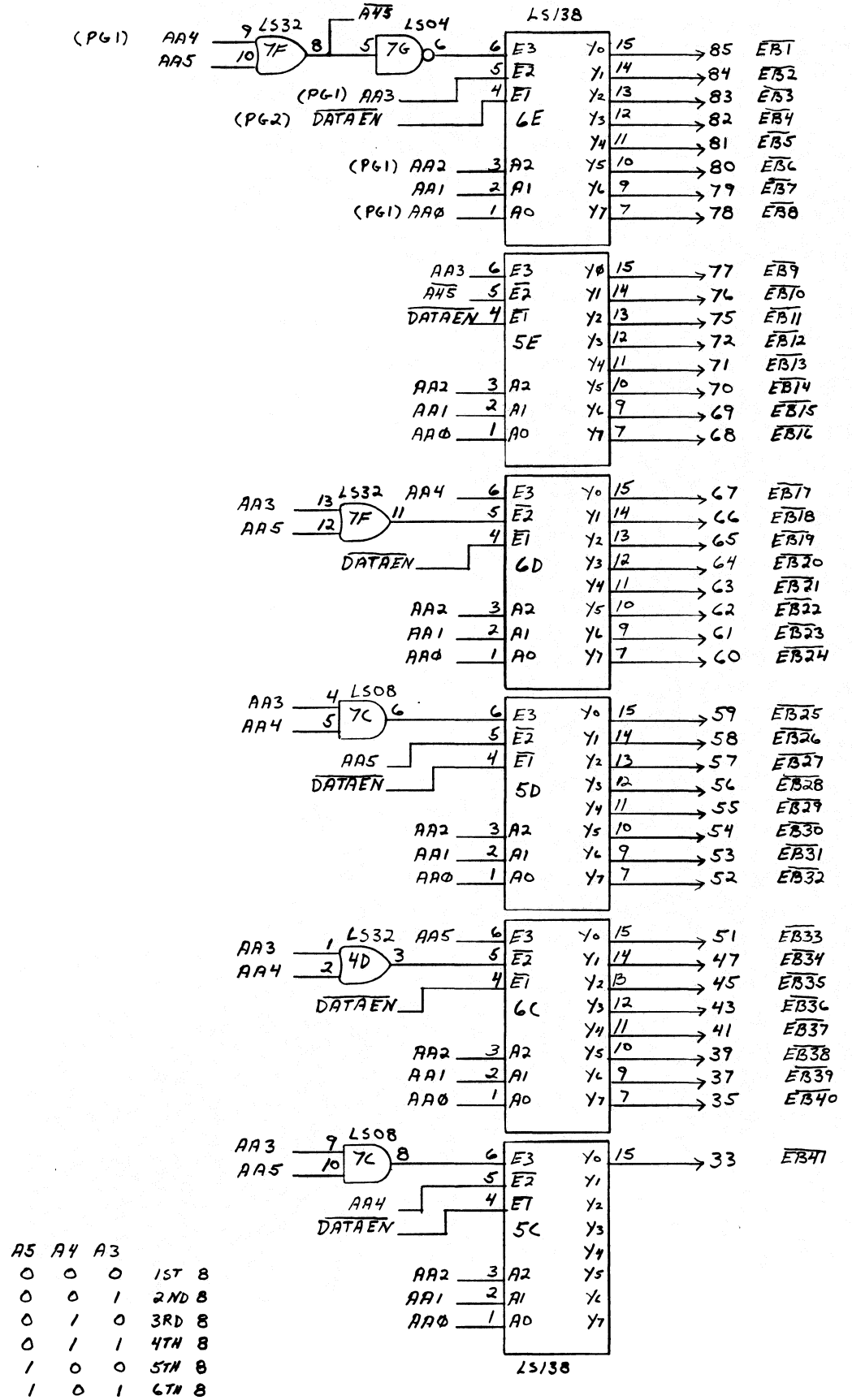
GREEN BANK
DIGITAL LINK
BLOCK DIAGRAM



14.2M
DIGITAL LINK
BLOCK DIAGRAM

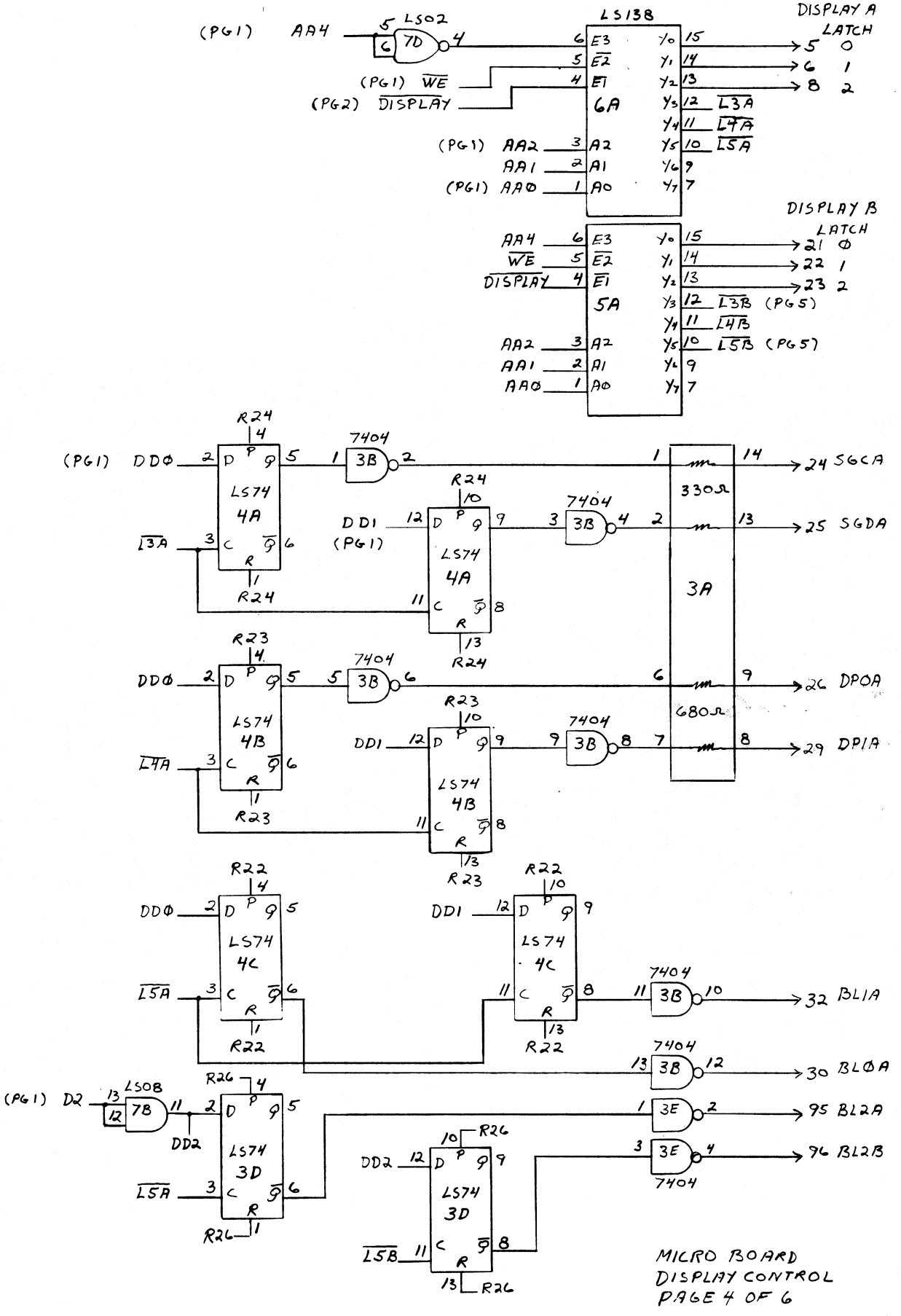

555+ DISCRETE
IN A 16 PIN LOC.
555+ DISC.
IN 16P LOC.
2.55 PER
MOUNT ON
WIRE SIDE OF
BOARD
* 20Mf 16V
* IN WW PGM
RUN 2 WIRES
TO PIN 7 &
PIN 1
LS245 = TRANSCEIVER
DR
L = B→A
H = A→B
MICRO
BUS
MICRO BOARD GB, 14.2
MICROPROCESSOR
PAGE 1 OF 6

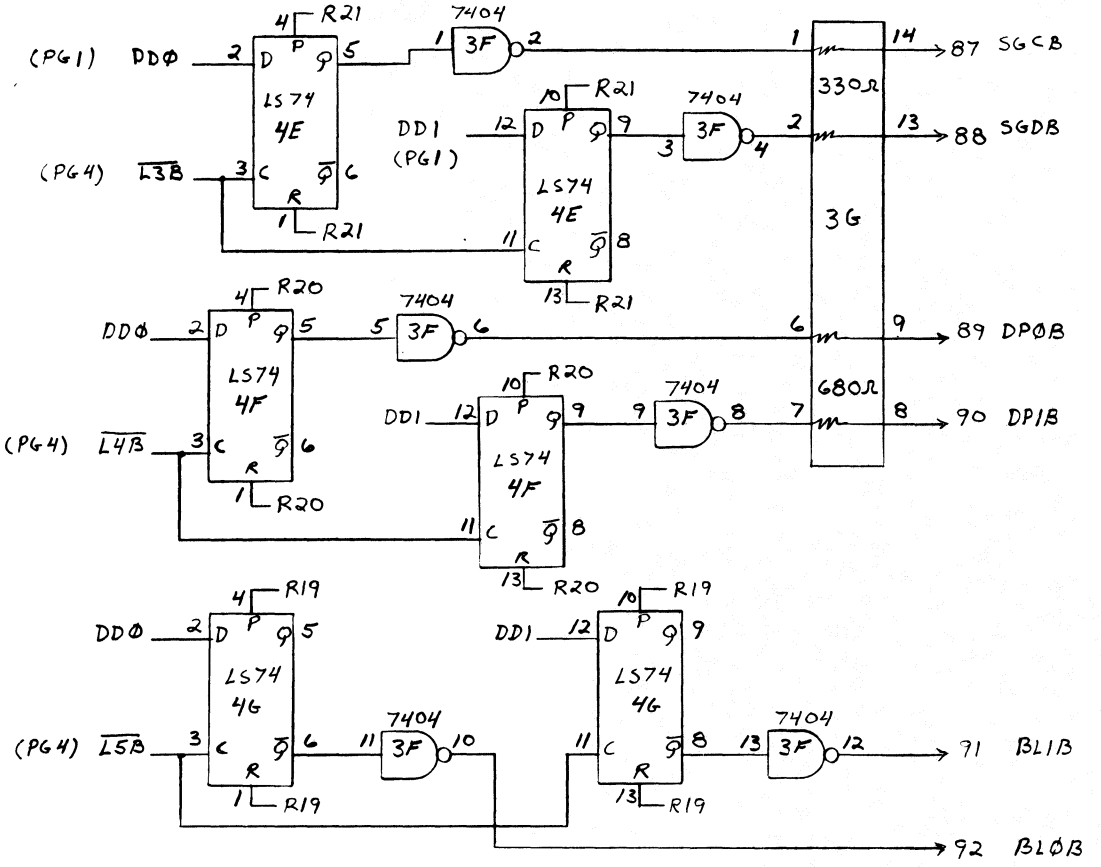

ADDRESS BUS (HEX)
0 XXX RAM
2 XXX DIGI-SW, STATUS
3 XXX MICRO BUS DATA
4XXX FRONT PANEL DISP.
5XXX WATCH DOG TIMER
6XXX DATA OK FF
FXXX PROM
A15-A12
LS138
8C
R25
(PG1) CSEN
(PG1) A15
(PG1) A14
A13
A12
RAMEN (PG5,6)
DIGISW (PG6)
DATAEN (PG3,6)
DISPLAY (PG4,6)
WATCHD (PG1,6)
LS08
7C
OBSL (PG1,6)
R26
14 PIN IN 16 PIN LOC
LS20
8D
LS32
7F
ROMEN (PG5,6)
(PG1) CSEN
(PG1) DD0
LS74
7A
7404
3E
86 DATAOK
LS138
8E
DIGISW
(PG1) AA2
AA1
AA0
DSEL0
DSEL1
STAT
LS240
9A
DIGISWA
DSEL0
D0 (PG1)
D1
D2
D3
D4
D5 (PG1)
R1
R2
R3
R4
R5
R6
R899
-1-1K
6B
R7
R8
+5
R13
9B
DIGISWB
DSEL1
LS240
R9
R10
R11
R12
5B
R14
R24
R25
R20
R21
9E
STAT
STATUS
R13
R14
R15
R16
D0 (PG1) (NOTE STATUS NOT USED AT THIS TIME)
D6
D7 (PG1)
LS244
MICRO BOARD 6B, 14.2
GROUP SEL
DIGI-SW, STATUS
PAGE 2 OF 6

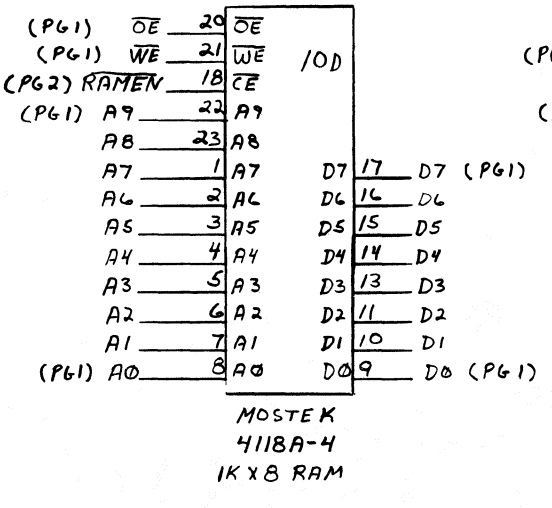


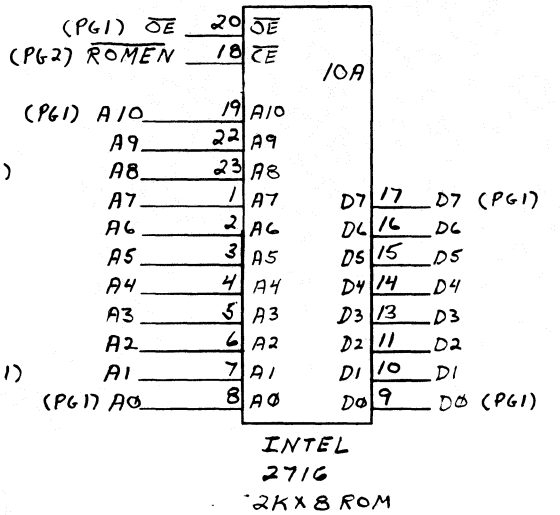
A5	A4	A3	
0	0	0	1ST 8
0	0	1	2ND 8
0	1	0	3RD 8
0	1	1	4TH 8
1	0	0	5TH 8
1	0	1	6TH 8

MICRO BOARD GB, 14.2
INPUT DATA ENABLE
PAGE 3 OF 6


DISPLAY A LATCH
DISPLAY B LATCH
LS138
LS02
7D
6A
5A
7404
3B
LS74
4A
4B
4C
3D
7B
LS08
3E
3A
330Ω
680Ω
R24
R23
R22
R26
(PG1) AA4
(PG1) WE
(PG2) DISPLAY
(PG1) AA2
AA1
(PG1) AA0
(PG1) DD0
DD1
(PG1) D2
L3A
L4A
L5A
L3B (PG5)
L4B
L5B (PG5)
24 SGCA
25 SGDA
26 DPOA
29 DPIA
32 BL1A
30 BL0A
95 BL2A
96 BL2B
MICRO BOARD
DISPLAY CONTROL
PAGE 4 OF 6



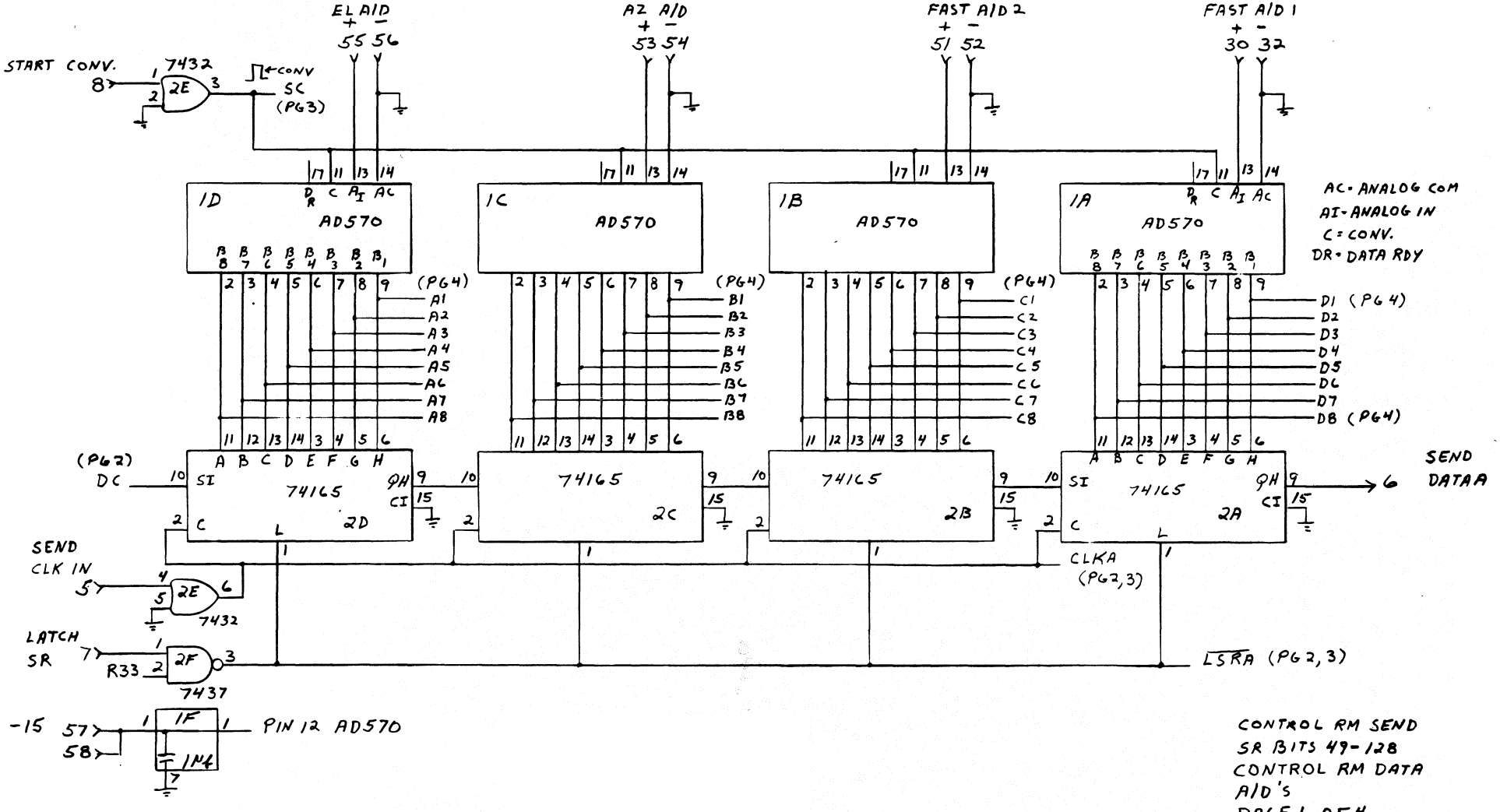


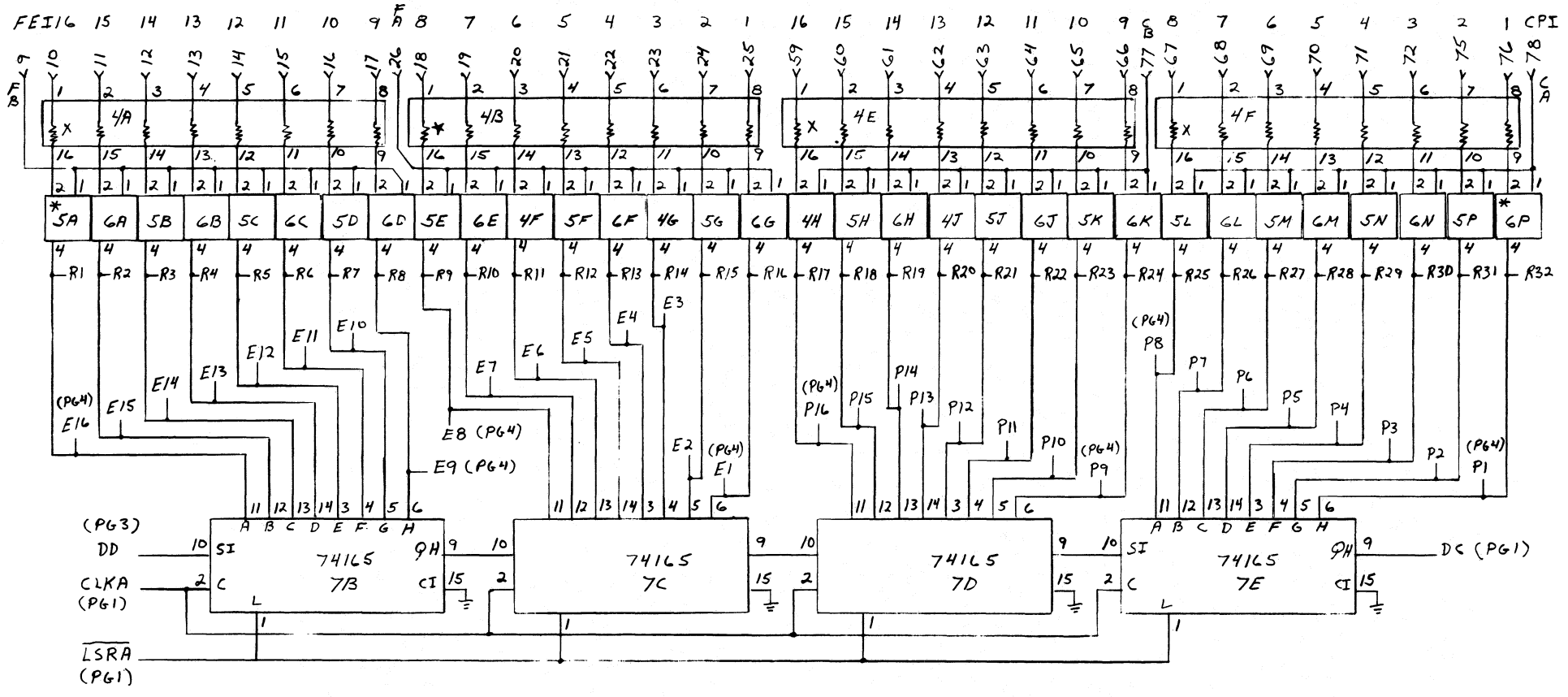


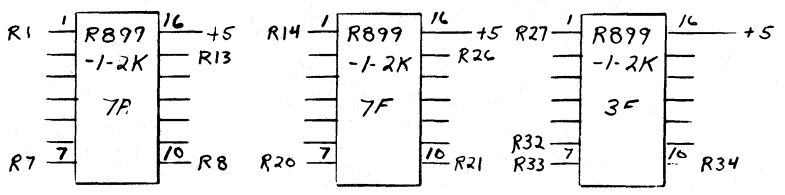
MICRO BOARD
DISPLAY/MEMORY
PAGE 5 OF 6

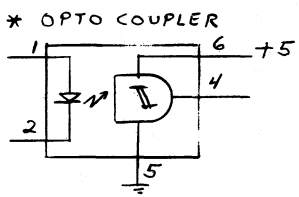
	SIGNAL	ANALYZER	BOARD PIN
(PG1)	A15	D15 (POD A)	Z16
	A14	D14	Z15
	A13	D13	Z14
	A12	D12	Z13
	A11	D11	Z12
	A10	D10	Z11
	A9	D9	Z10
	A8	D8	Z9
	A7	D7	Z8
	A6	D6	Z7
	A5	D5	Z6
	A4	D4	Z5
	A3	D3	Z4
	A2	D2	Z3
	A1	D1	Z2
(PG1)	A0	D0	Z1
	SPARE	Q TRIG	Z17
(PG1)	R/$\overline{W}$	Q CLK	Z18
(PG1)	E	CLK	Z19
	GND	GND	Z20
(PG1)	D7	D15 (POD B)	Z36
	D6	D14	Z35
	D5	D13	Z34
	D4	D12	Z33
	D3	D11	Z32
	D2	D10	Z31
	D1	D9	Z30
(PG1)	D0	D8	Z29
(PG2)	$\overline{RAMEN}$	D7	Z28
	$\overline{DIGISW}$	D6	Z27
	$\overline{DATAEN}$	D5	Z26
	$\overline{DISPLAY}$	D4	Z25
	$\overline{WATCHD}$	D3	Z24
	$\overline{OBSL}$	D2	Z23
(PG2)	$\overline{ROMEN}$	D1	Z22
	SPARE	D0	Z21
	SPARE	Q TRIG	Z37
(PG1)	R/$\overline{W}$	Q CLK	Z38
(PG1)	E	CLK	Z39
	GND	GND	Z40

MICRO BOARD
LOGIC ANALYZER
PAGE 6 OF 6


EL A/D
+ 55
- 56
A2 A/D
+ 53
- 54
FAST A/D 2
+ 51
- 52
FAST A/D 1
+ 30
- 32
START CONV.
8
7432
2E
CONV
SC
(PG3)
1D
AD570
1C
AD570
1B
AD570
1A
AD570
AC - ANALOG COM
AI - ANALOG IN
C = CONV.
DR = DATA RDY
(PG4)
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
C1
C2
C3
C4
C5
C6
C7
C8
D1 (PG4)
D2
D3
D4
D5
D6
D7
D8 (PG4)
(PG2)
DC
74165
2D
2C
2B
2A
SI
QH
CI
SEND DATAA
SEND CLK IN
5
2E
7432
CLKA (PG2,3)
LATCH SR
7
R33
2F
7437
LSRA (PG2,3)
-15
57
58
1F
1N4
PIN 12 AD570
CONTROL RM SEND
SR BITS 49-128
CONTROL RM DATA
A/D's
PAGE 1 OF 4







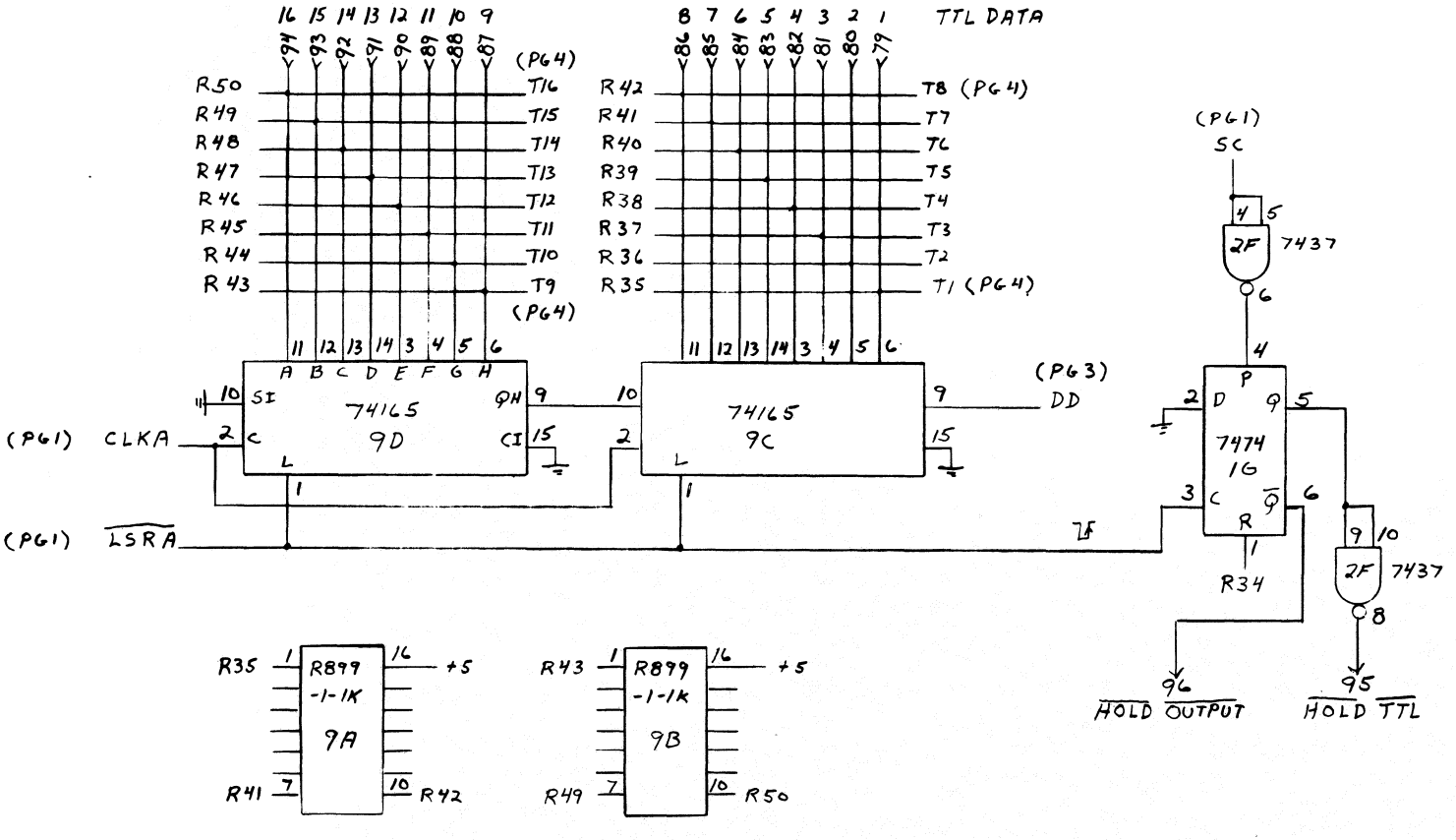
USED 32 PLACES
MOC 5008

✱ RESISTORS = 3.3K 1/4W

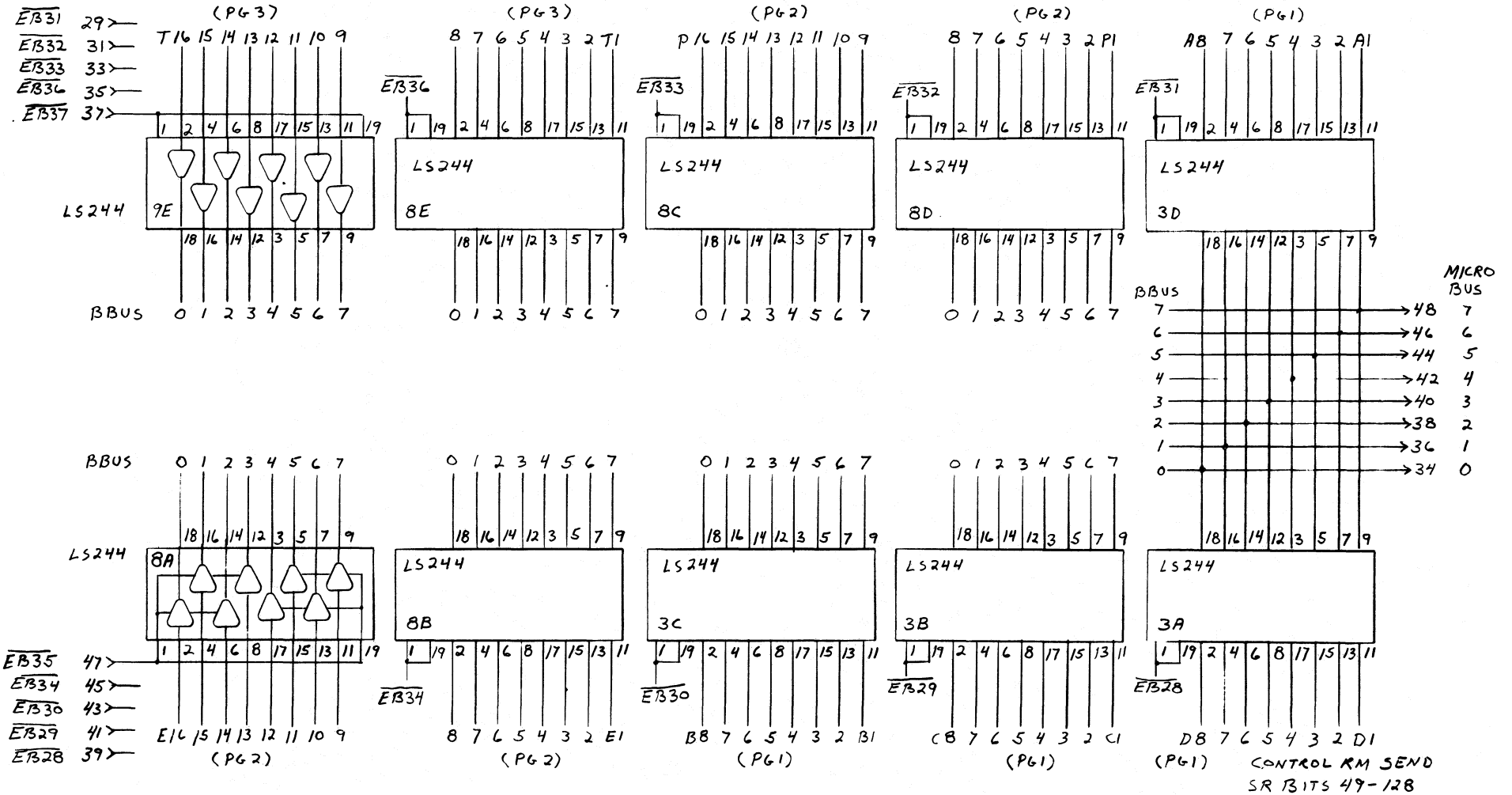
X RESISTORS = 470Ω 1/4W

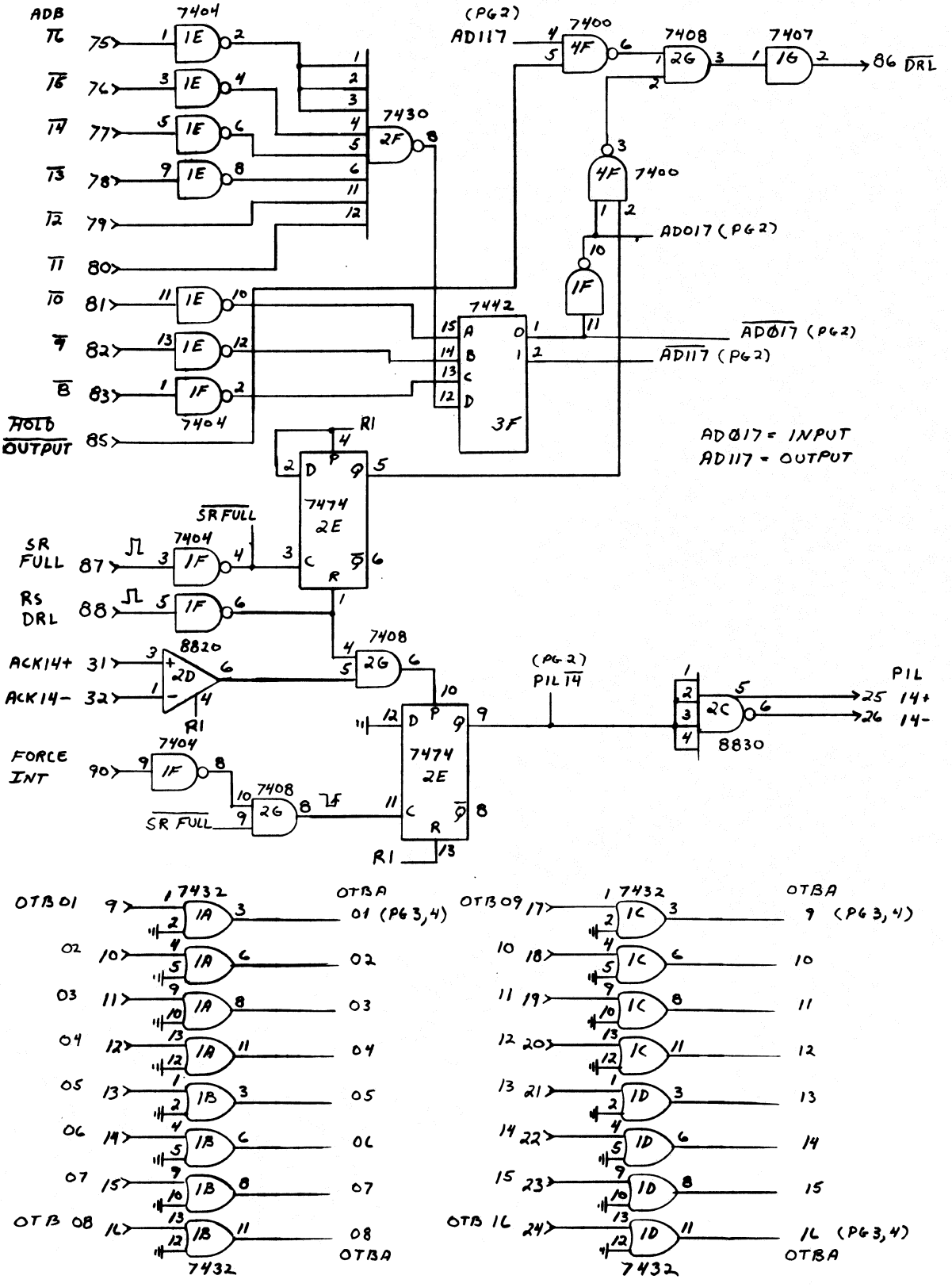
CURRENT IN TO COUPLER
GIVES 0V OUT = LOGIC 0

CONTROL RM SEND
SR BITS 49-128
CONTROL RM DATA
FRONT END
CONTROL PANEL
PAGE 2 OF 4

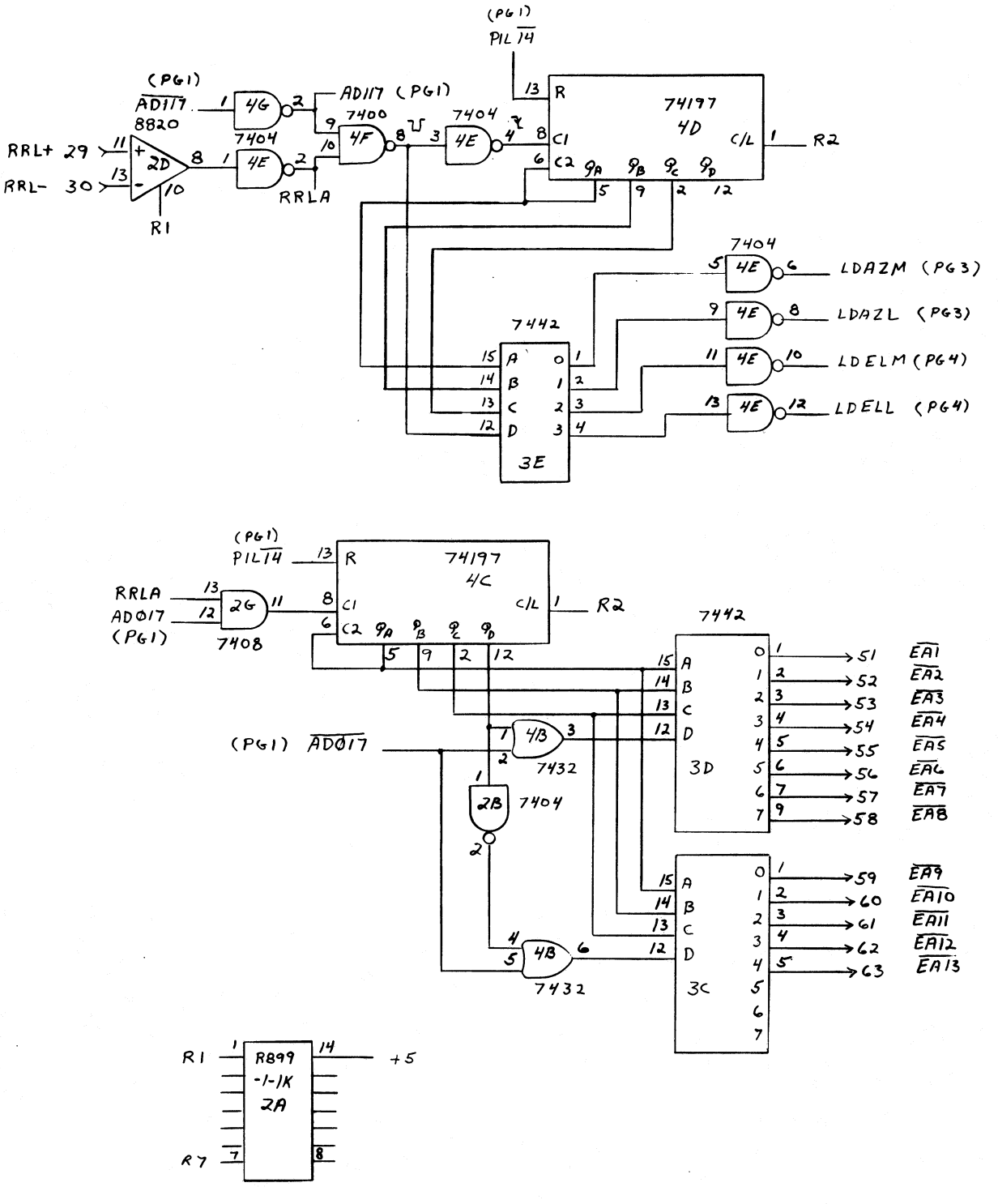


CONTROL RM SEND
SR BITS 49-128
CONTROL RM DATA
TTL
PAGE 3 OF 4

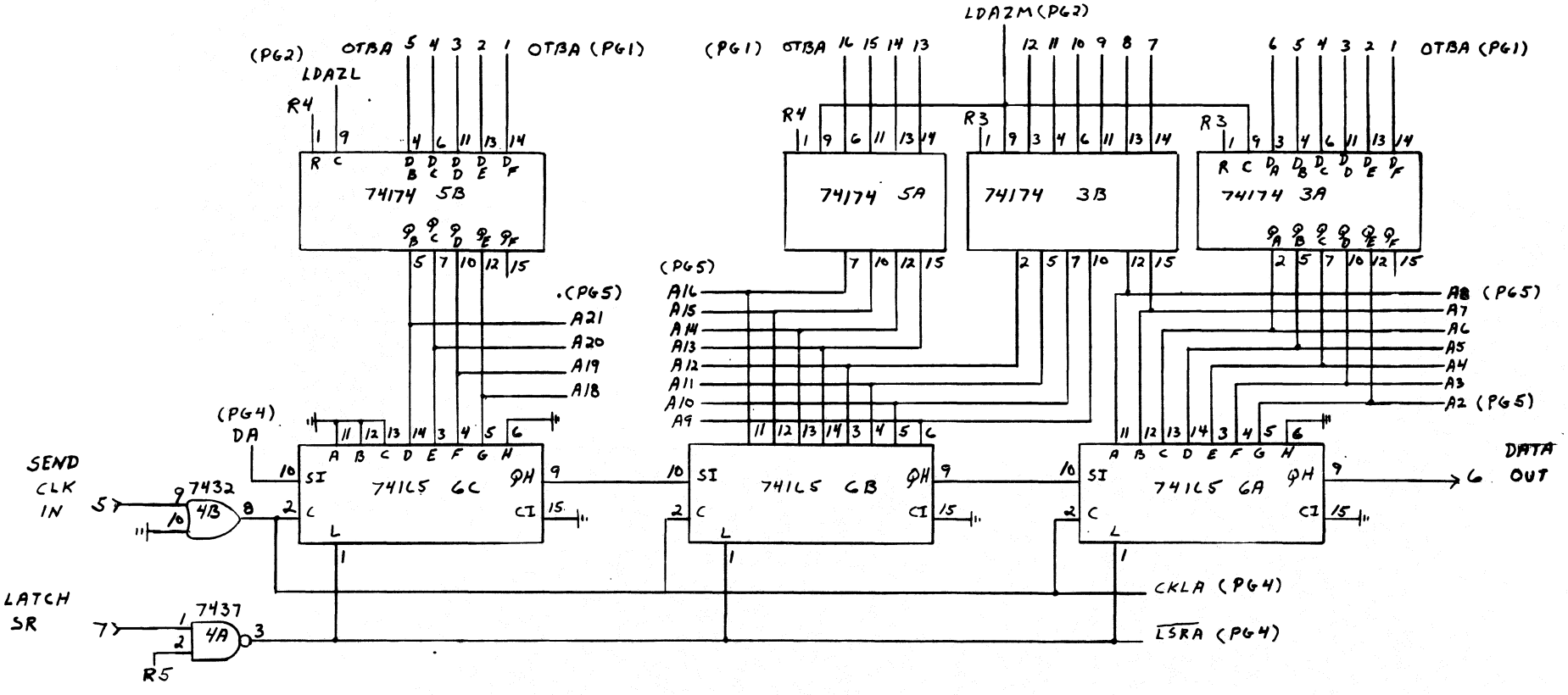

EB31 29
EB32 31
EB33 33
EB36 35
EB37 37
(PG3)
T 16 15 14 13 12 11 10 9
1 2 4 6 8 17 15 13 11 19
LS244
9E
18 16 14 12 3 5 7 9
BBUS 0 1 2 3 4 5 6 7
EB36
8 7 6 5 4 3 2 T1
LS244
8E
EB33
P 16 15 14 13 12 11 10 9
LS244
8C
EB32
8 7 6 5 4 3 2 P1
LS244
8D
EB31
A8 7 6 5 4 3 2 A1
LS244
3D
MICRO BUS
BBUS
7 → 48 7
6 → 46 6
5 → 44 5
4 → 42 4
3 → 40 3
2 → 38 2
1 → 36 1
0 → 34 0
EB35 47
EB34 45
EB30 43
EB29 41
EB28 39
E 16 15 14 13 12 11 10 9
(PG2)
8A
8 7 6 5 4 3 2 E1
8B
BB 7 6 5 4 3 2 B1
3C
CB 7 6 5 4 3 2 C1
3B
DB 7 6 5 4 3 2 D1
3A
CONTROL RM SEND
SR BITS 49-128
CONTROL RM DATA
MICRO BUS
PAGE 4 OF 4



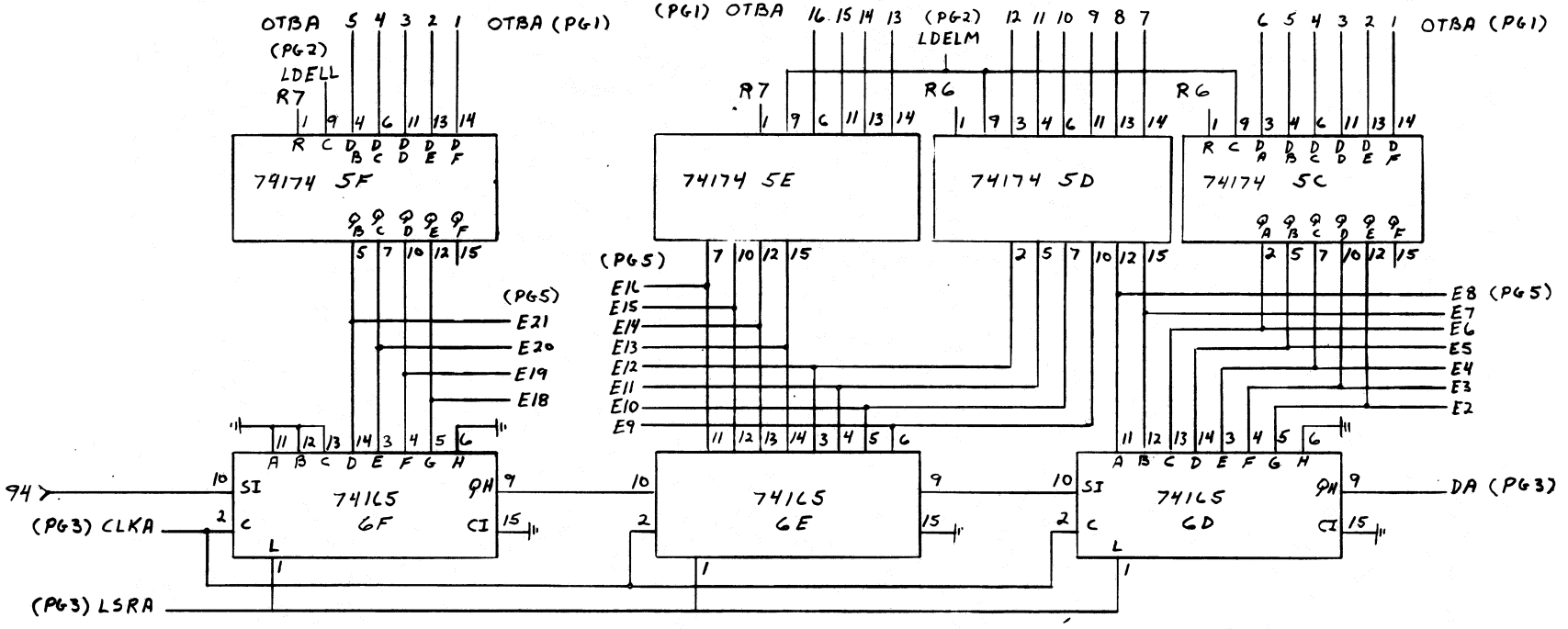
CONTROL RM SEND
SR BITS 1–48
116 INTERFACE
DRL, PIL, OTB BUFFER
PAGE 1 OF 5



CONTROL RM SEND
BITS 1-48
1/6 INTERFACE
I/O CONTROL
PAGE 2 OF 5

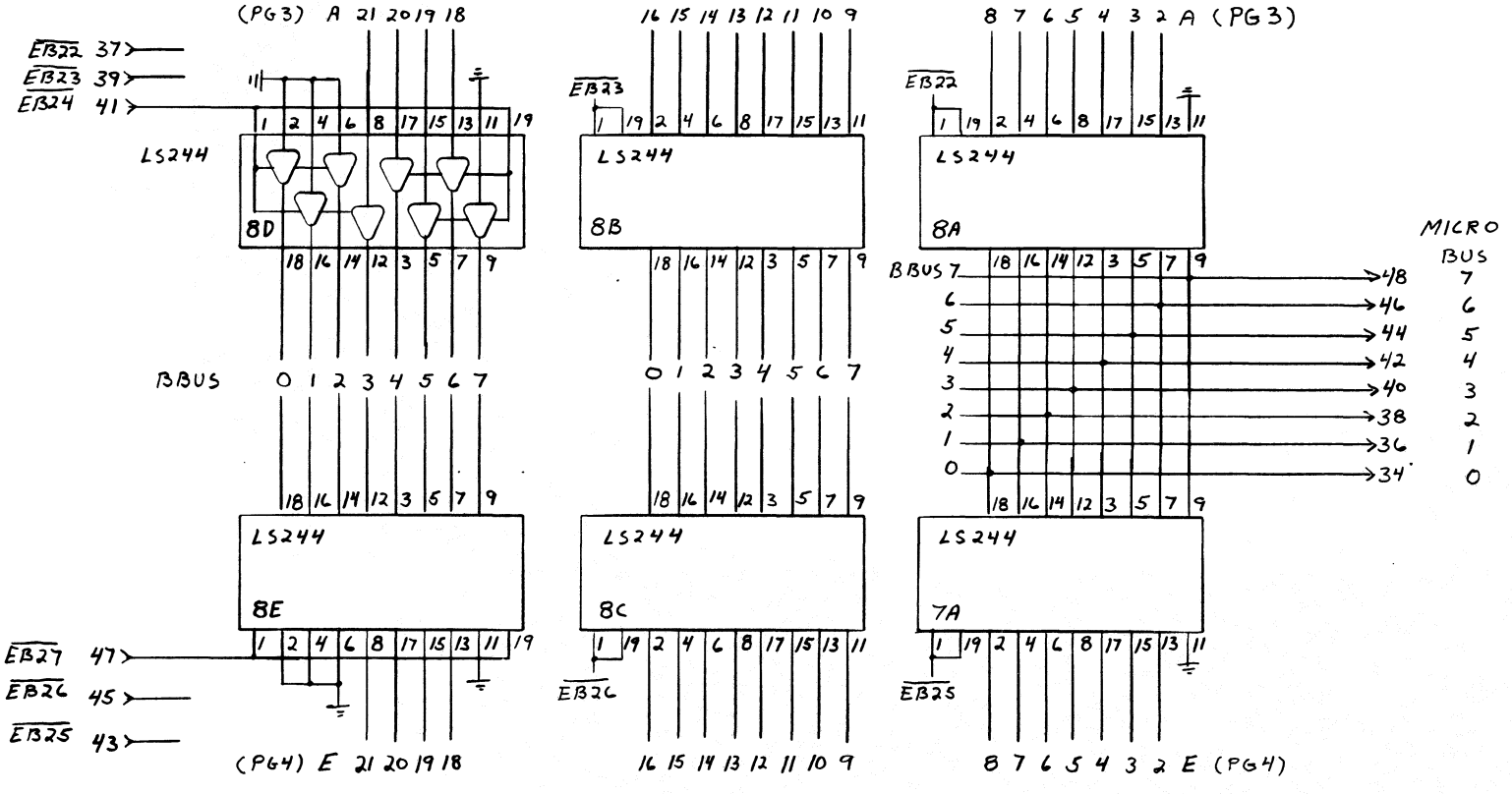


CONTROL RM SEND
SR BITS 1-48
I/L INTERFACE
AZIMUTH SR
PAGE 3 OF 5

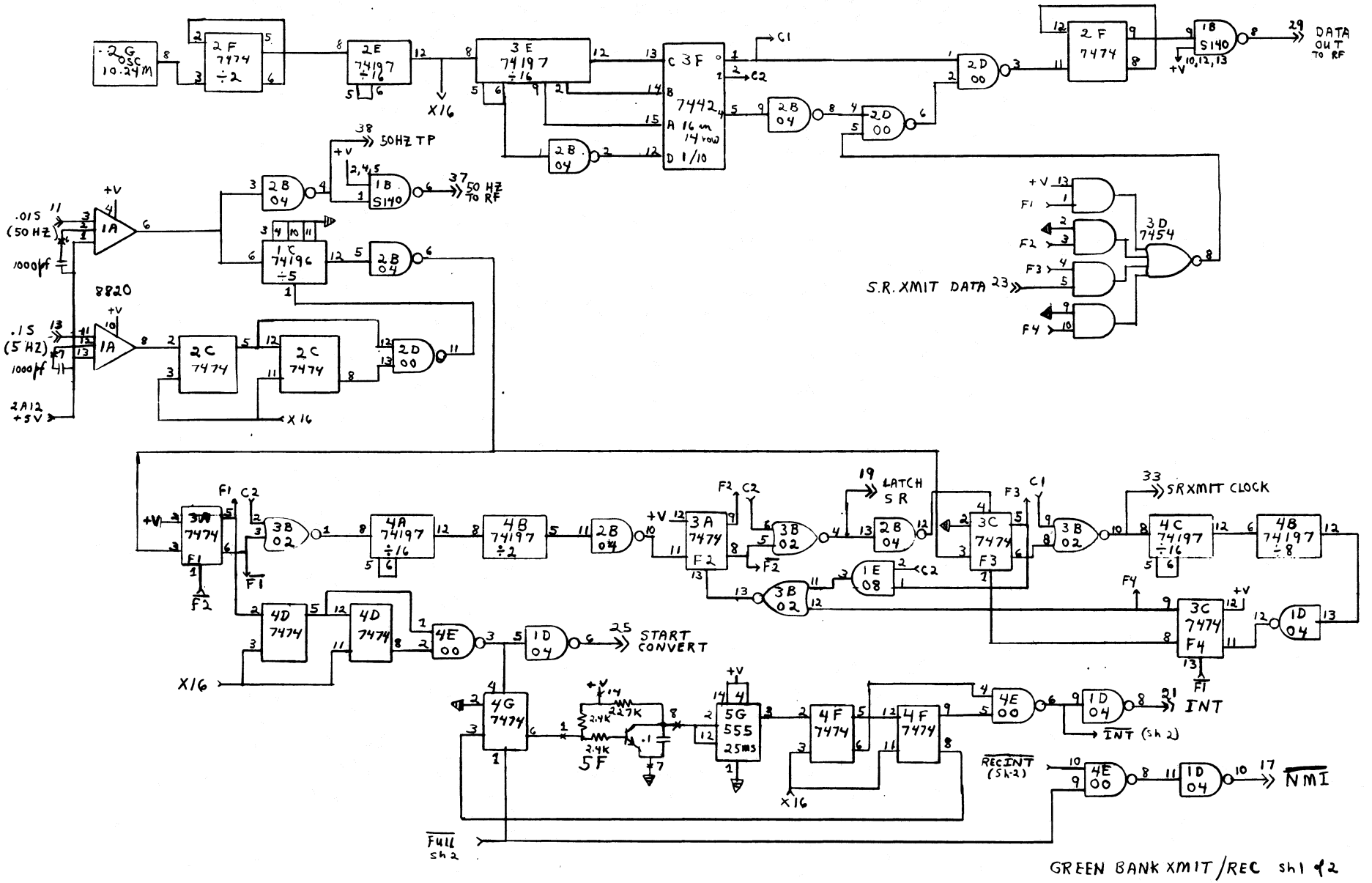


SEND DATA A

CONTROL RM SEND
SR BITS 1-48
I/C INTERFACE
ELEVATION SR
PAGE 4 OF 5

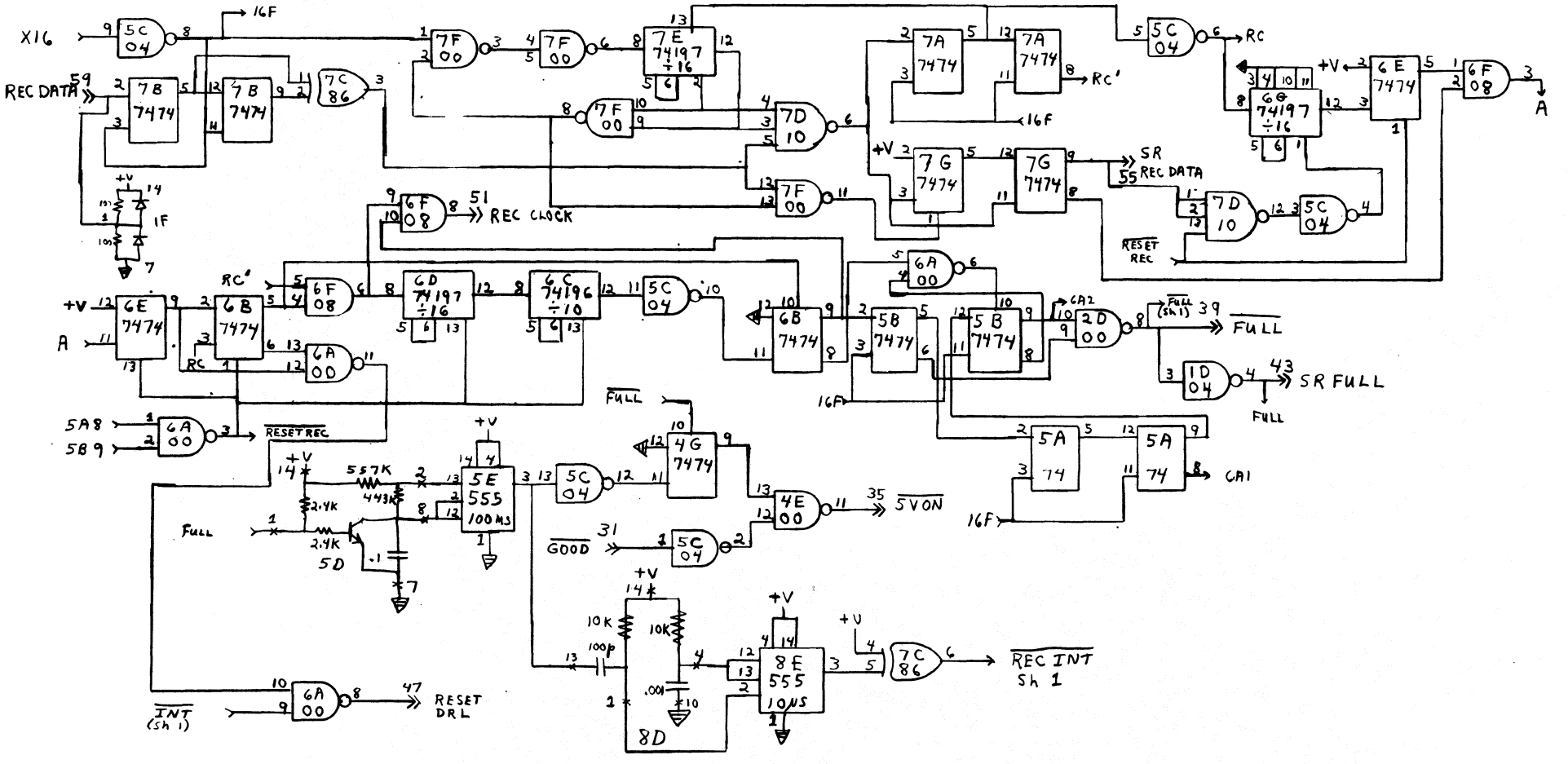


CONTROL RM SEND
SR BITS 1-48
I/C INTERFACE
MICRO BUS
PAGE 5 OF 5



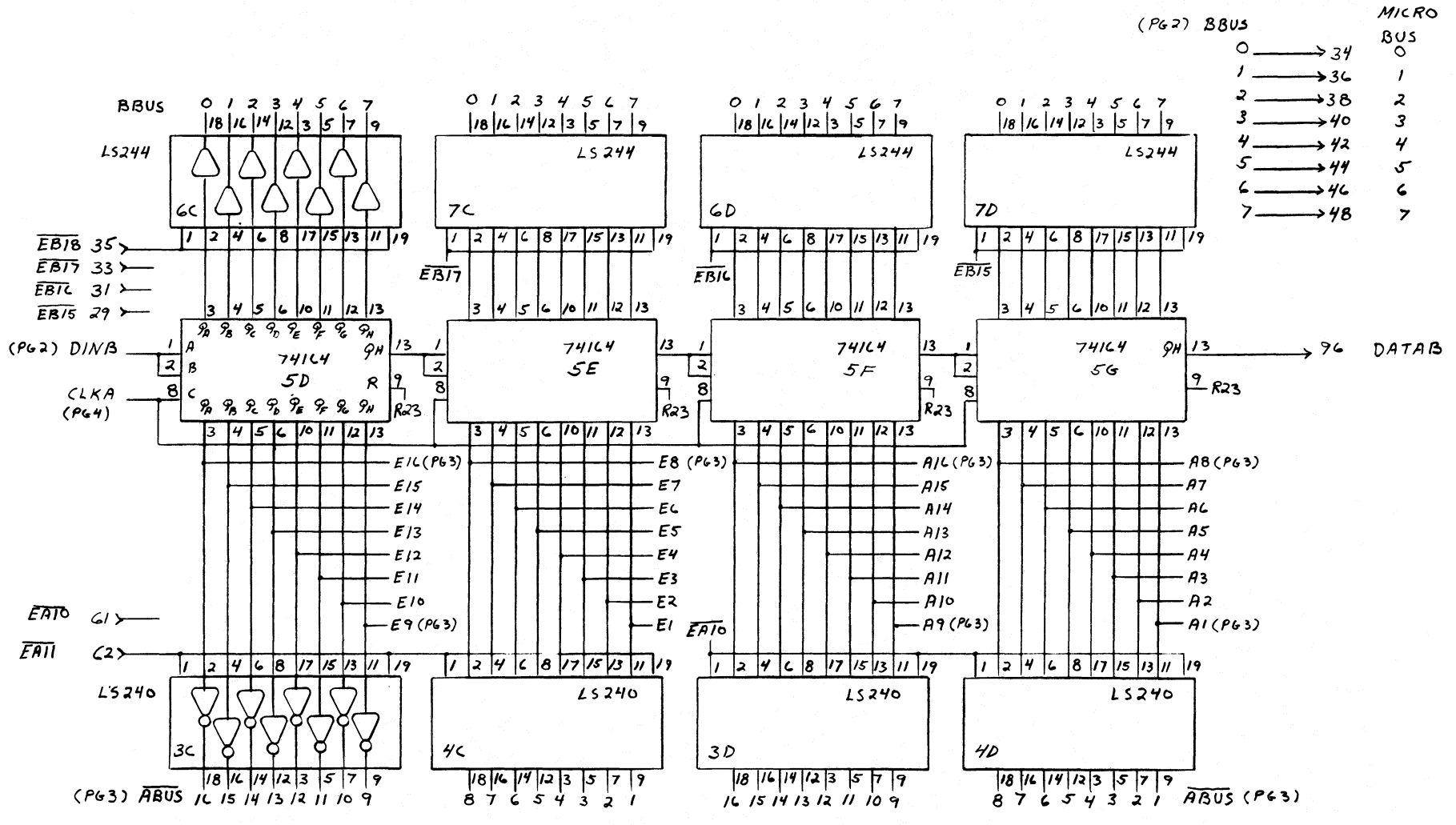
GREEN BANK XMIT/REC sh1 of 2

REV 02-09-84



GREEN BANK XMIT/REC sh 2 of 2

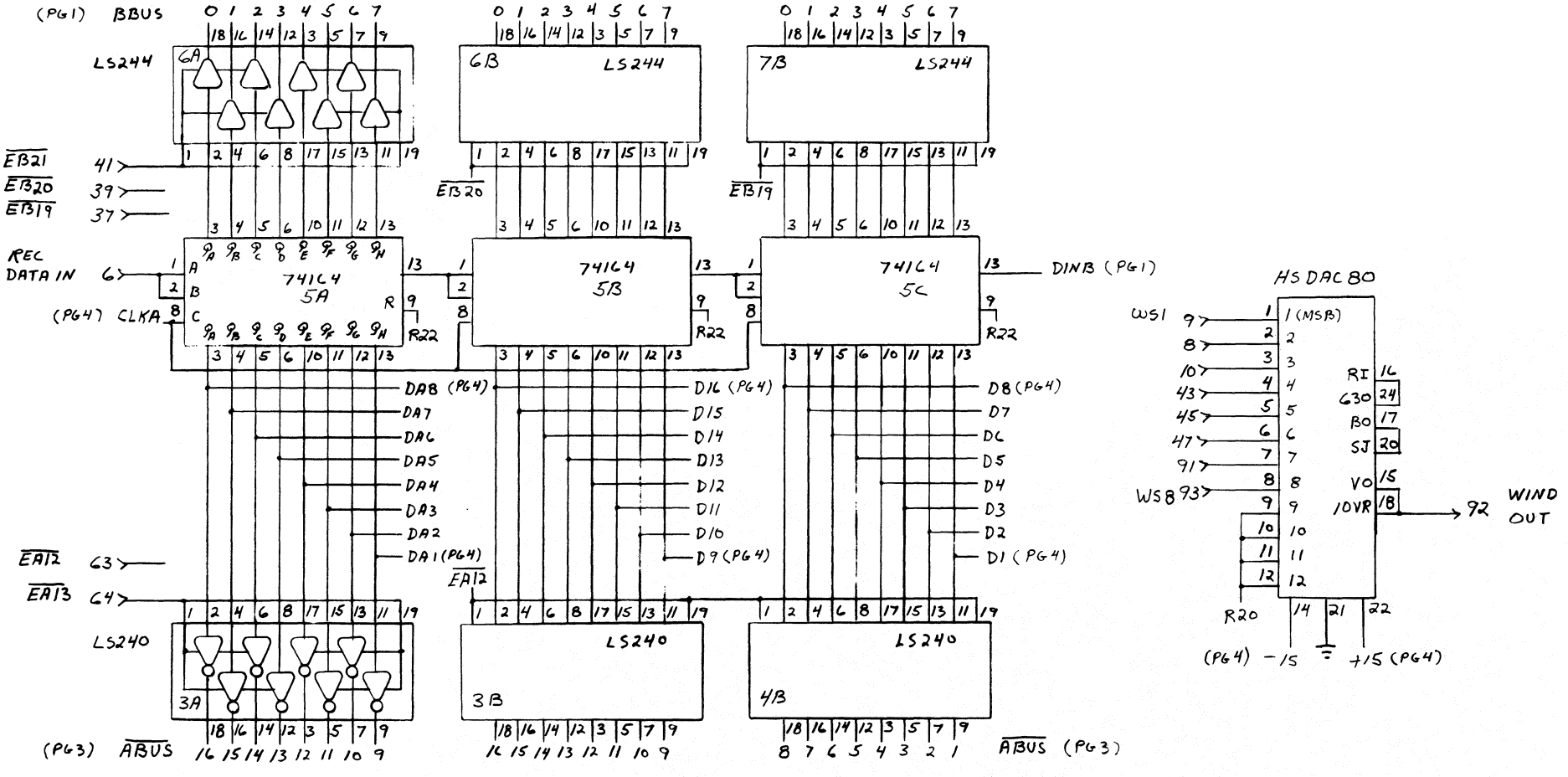
REV 02-09-84



$\overline{EA10}$ = A2 COARSE
$\overline{EA11}$ = E1 COARSE

NOTE: FOR DRAWING SIMIPLISITY OUTPUTS OF SR ARE SHOWN 3 - 4 TIMES

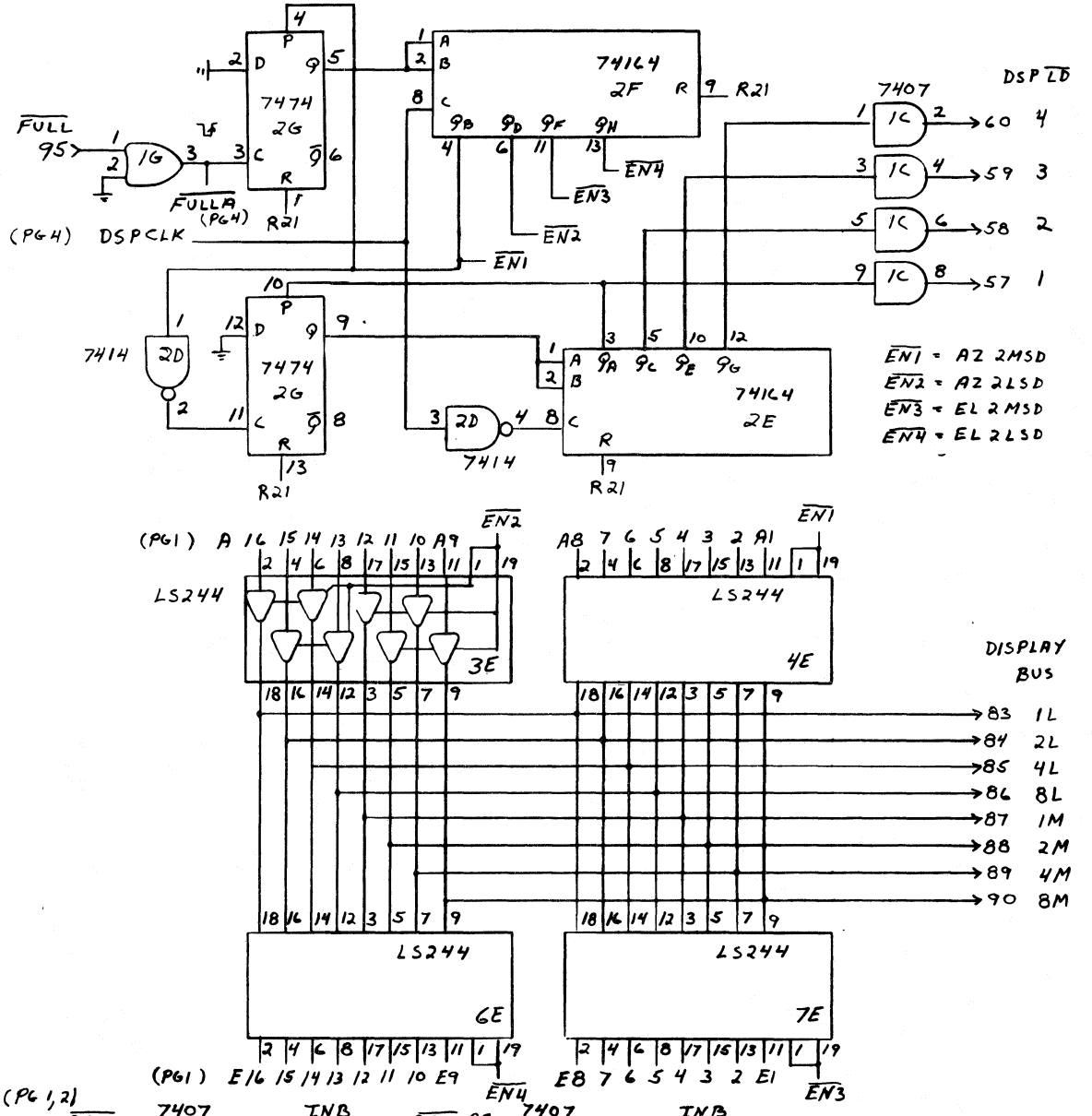
CONTROL RM REC.
SR BITS 105-160
PAGE 1 OF 4

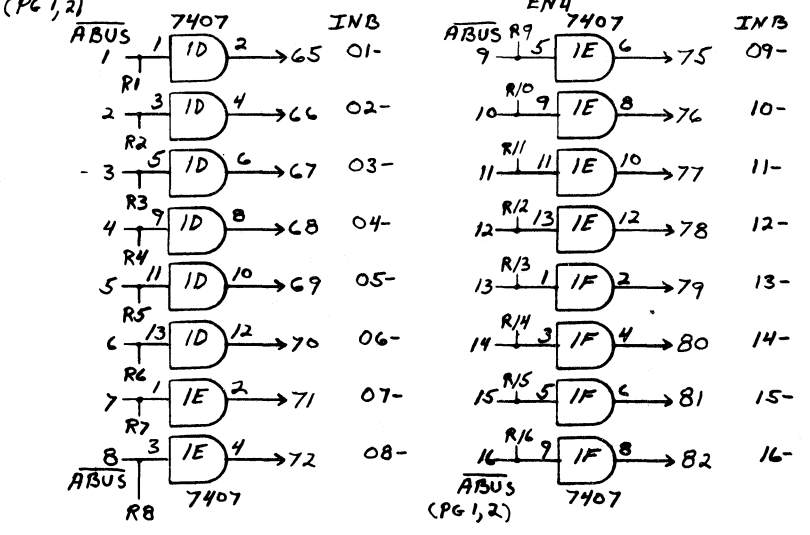


EA12 TTL DATA

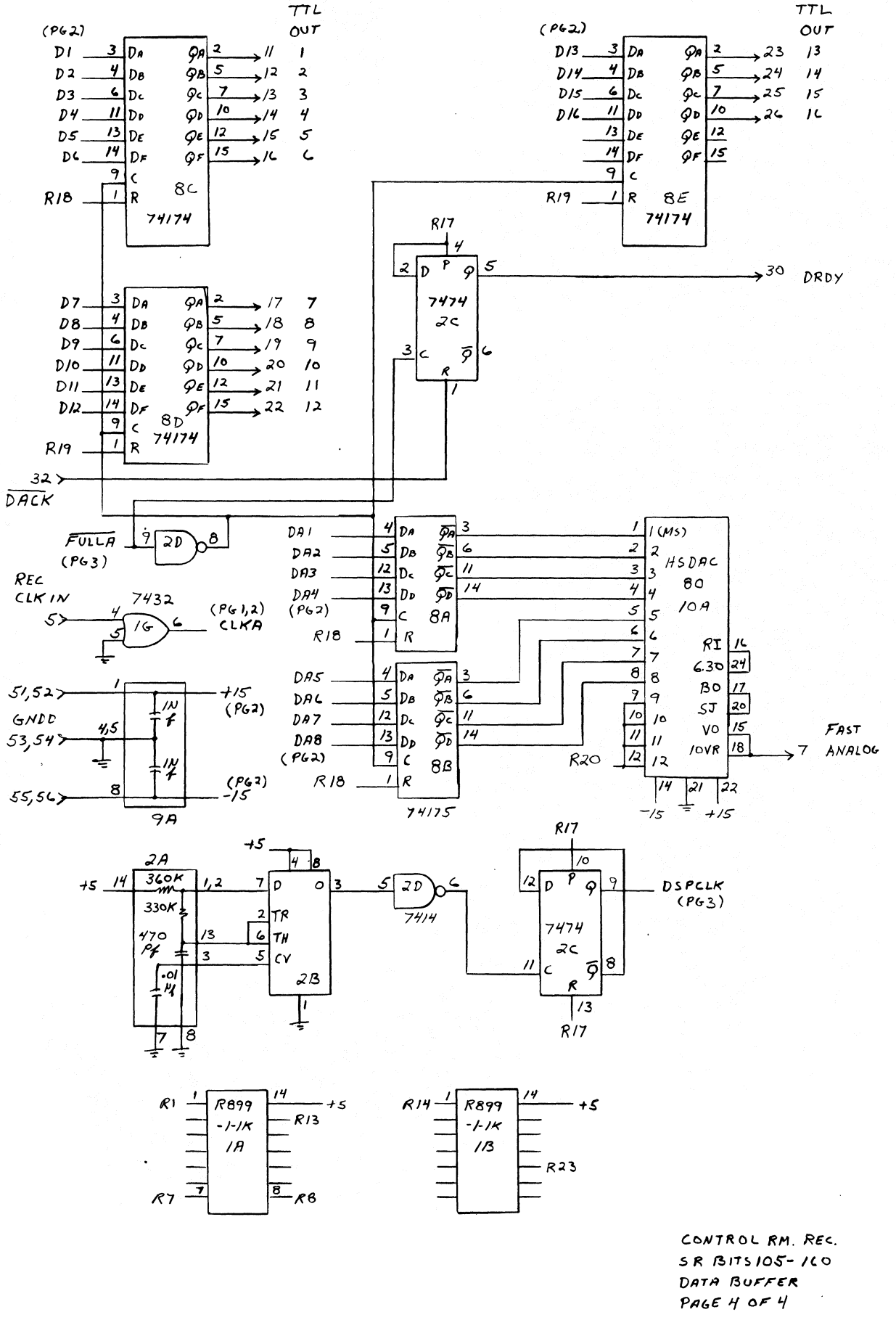
EA13 FAST A/D

CONTROL RM REC.
SR BITS 105- 160
PAGE 2 OF 4

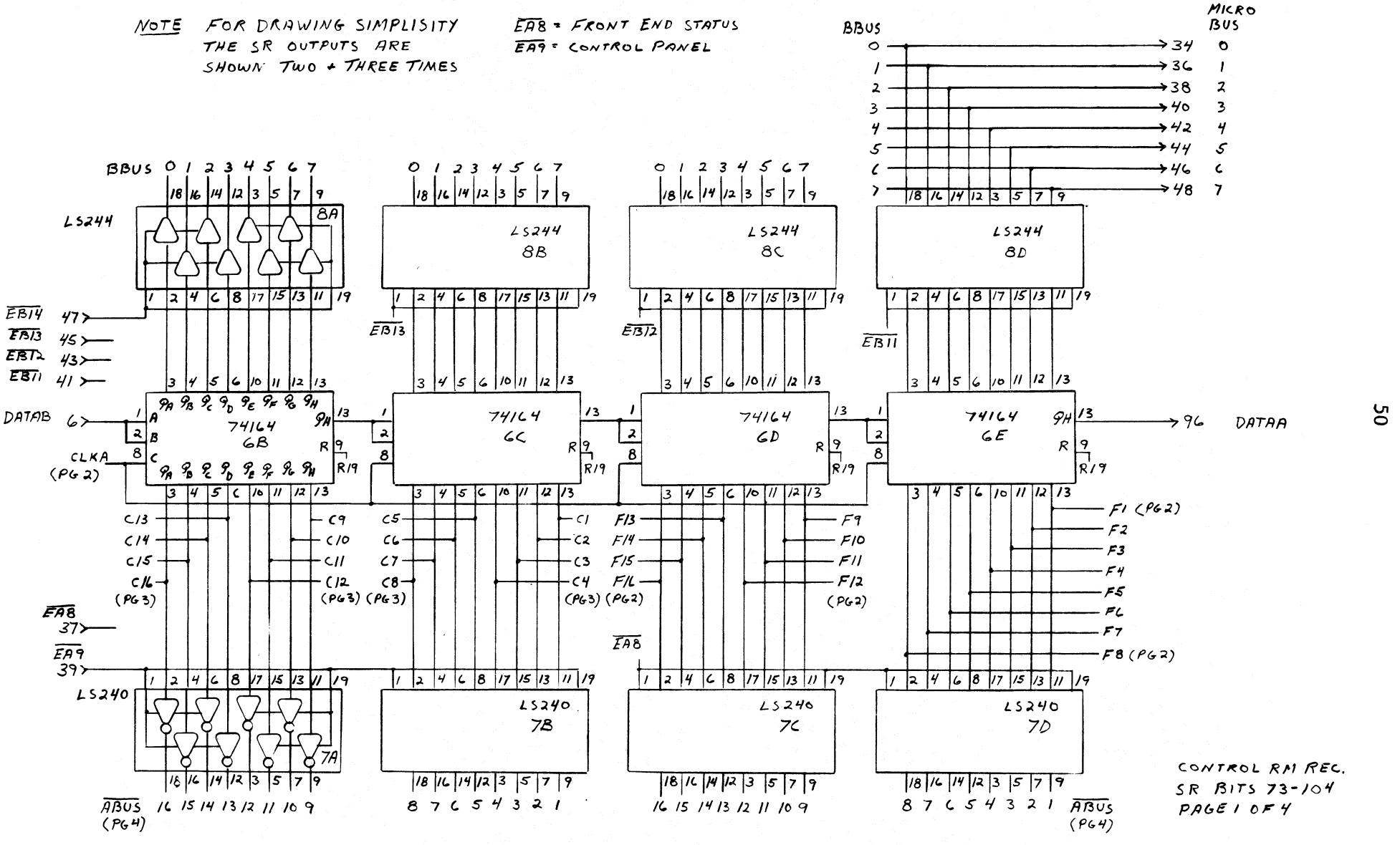


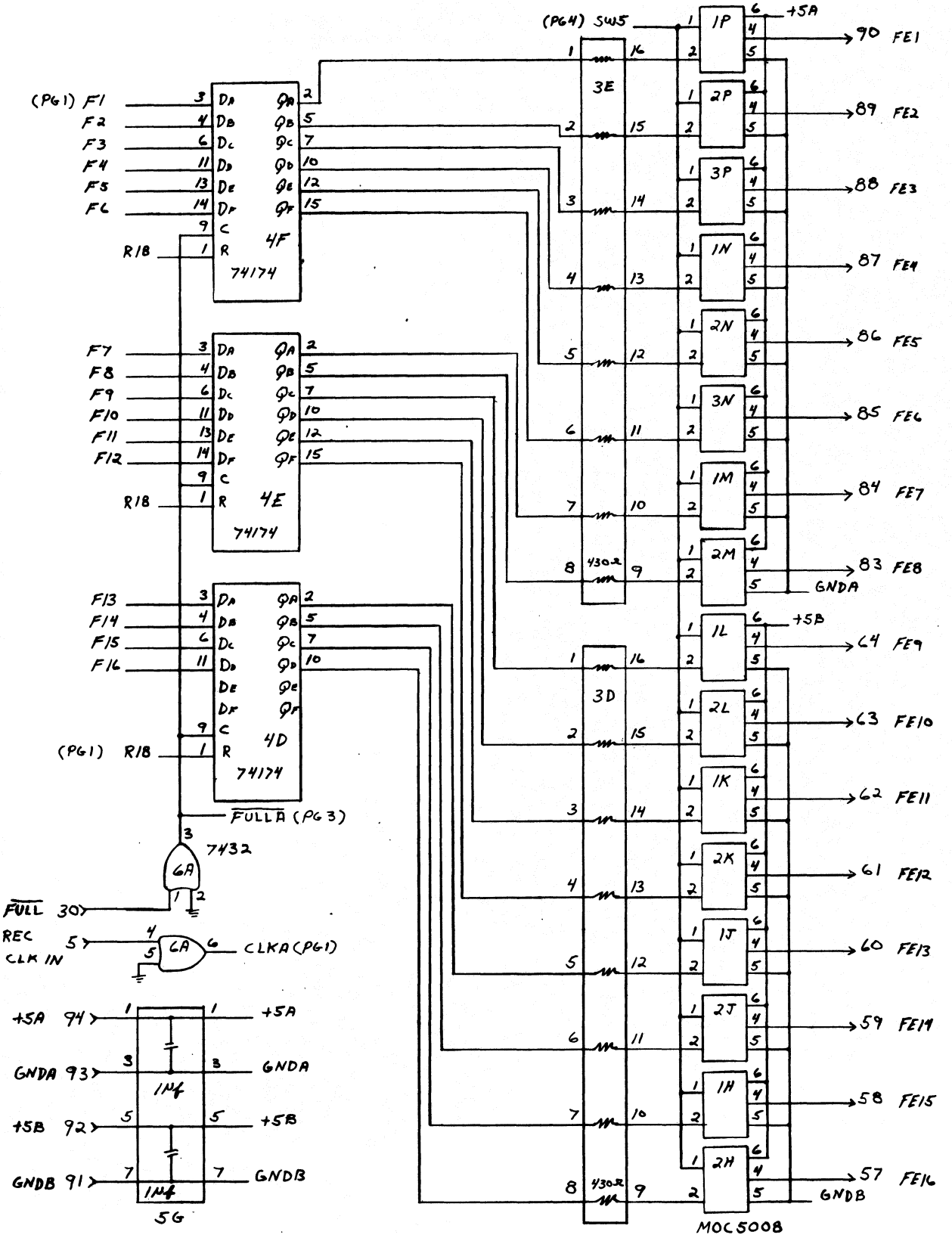


CONTROL RM. REC.
SR BITS 105-160
COARSE DISPLAY
PAGE 3 OF 4

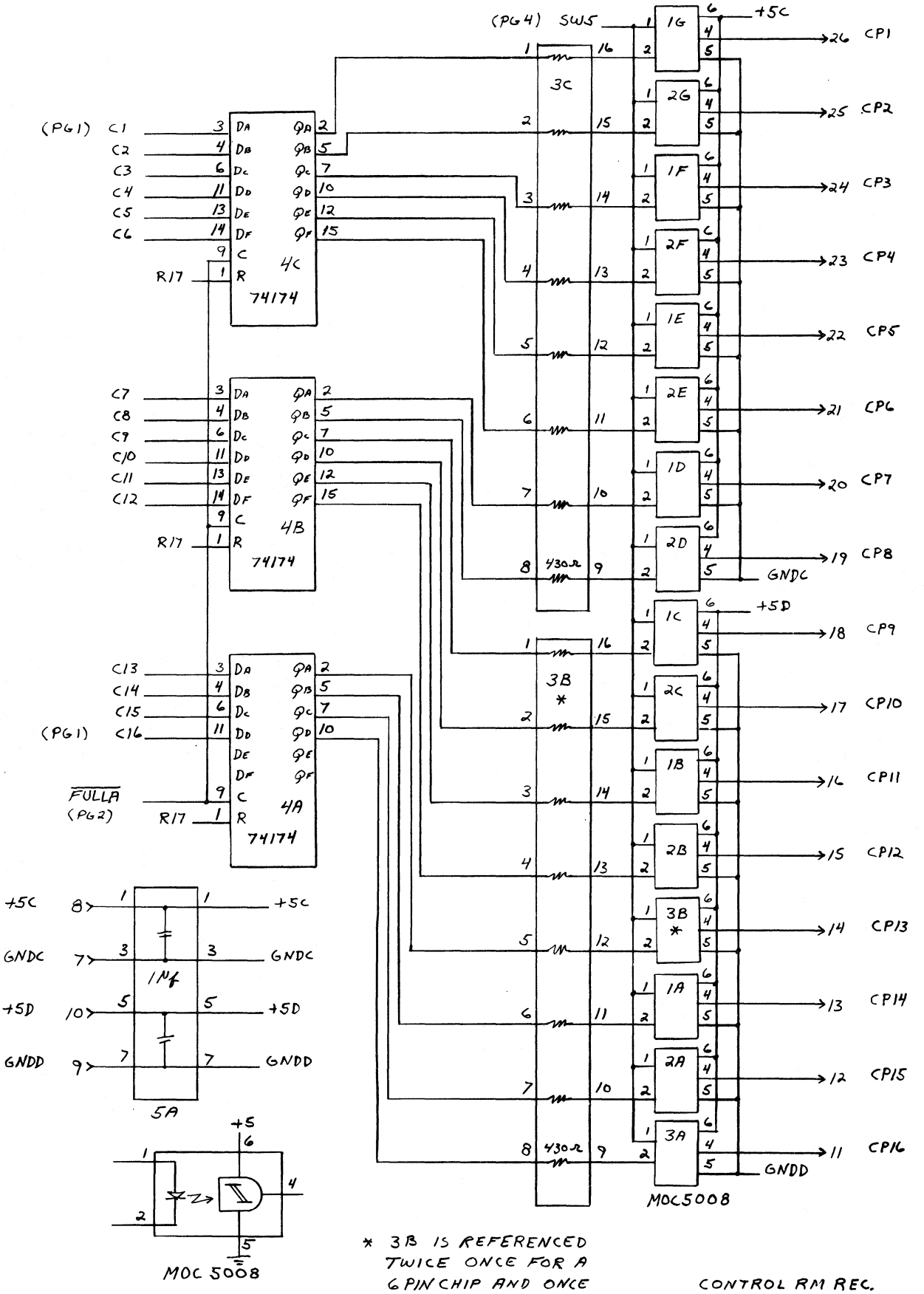


CONTROL RM. REC.
SR BITS 105-160
DATA BUFFER
PAGE 4 OF 4


NOTE FOR DRAWING SIMPLISITY THE SR OUTPUTS ARE SHOWN TWO & THREE TIMES
EA8 = FRONT END STATUS
EA9 = CONTROL PANEL
BBUS
MICRO BUS
LS244
8A
8B
8C
8D
74164
6B
6C
6D
6E
LS240
7A
7B
7C
7D
EB14
EB13
EB12
EB11
DATAB
CLKA (PG 2)
DATAA
EA8
EA9
ABUS (PG4)
CONTROL RM REC.
SR BITS 73-104
PAGE 1 OF 4

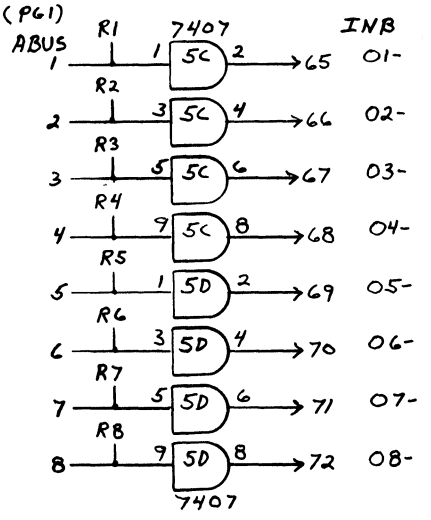


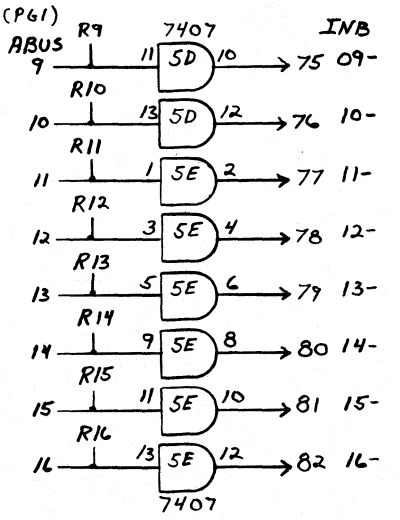
CONTROL RM REC
SR BITS 73-104
PAGE 2 OF 4

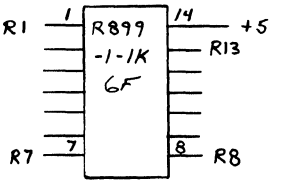


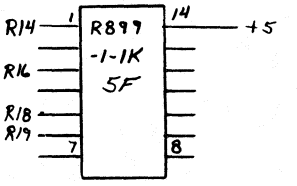
* 3B IS REFERENCED TWICE ONCE FOR A 6 PIN CHIP AND ONCE FOR A 16 PIN CHIP

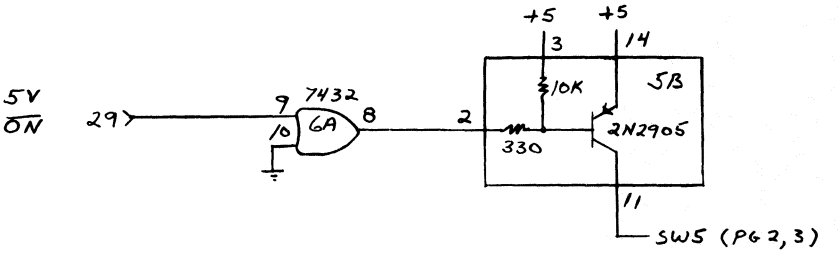
CONTROL RM REC.
SR BITS 73-104
PAGE 3 OF 4



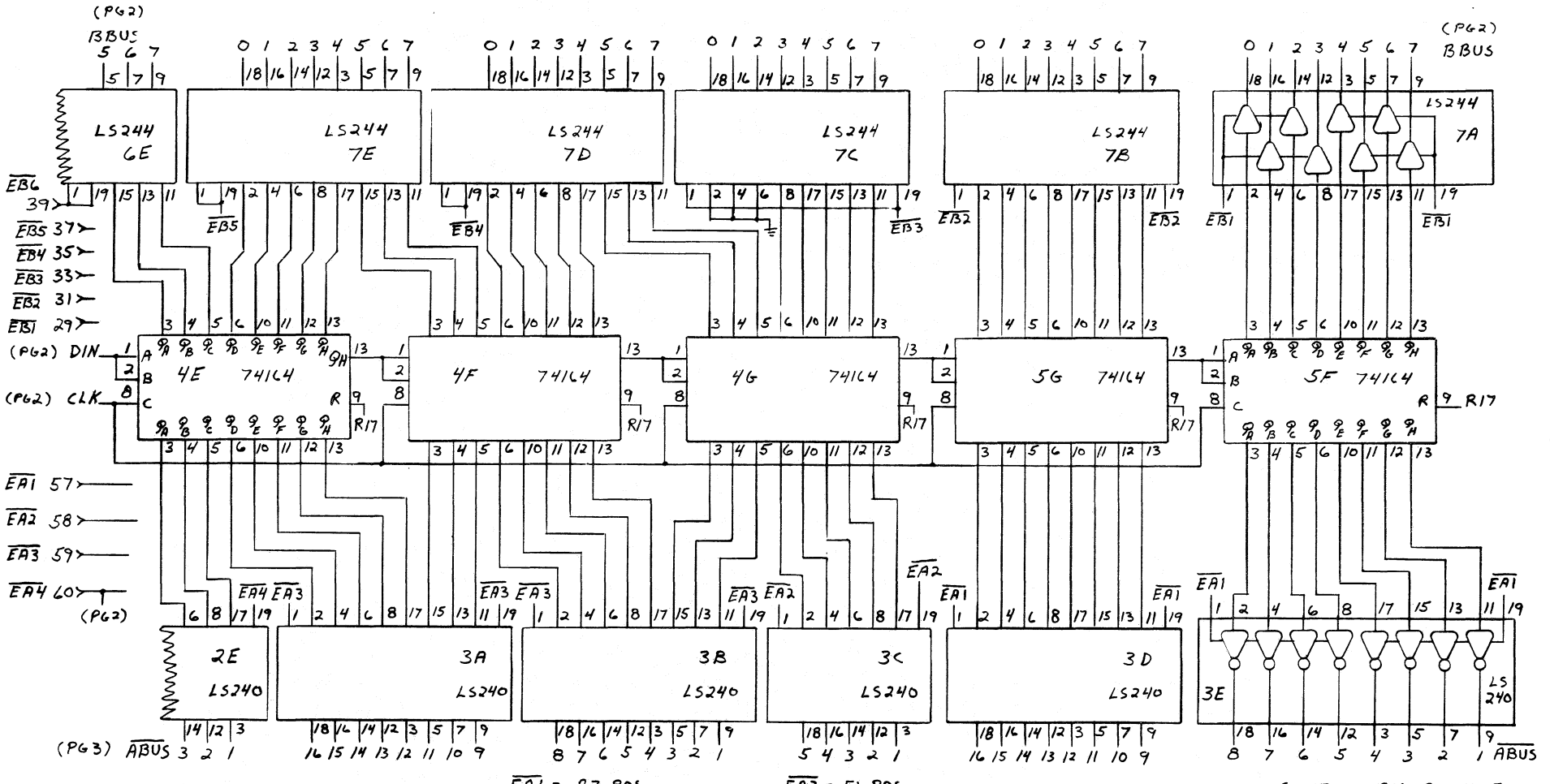


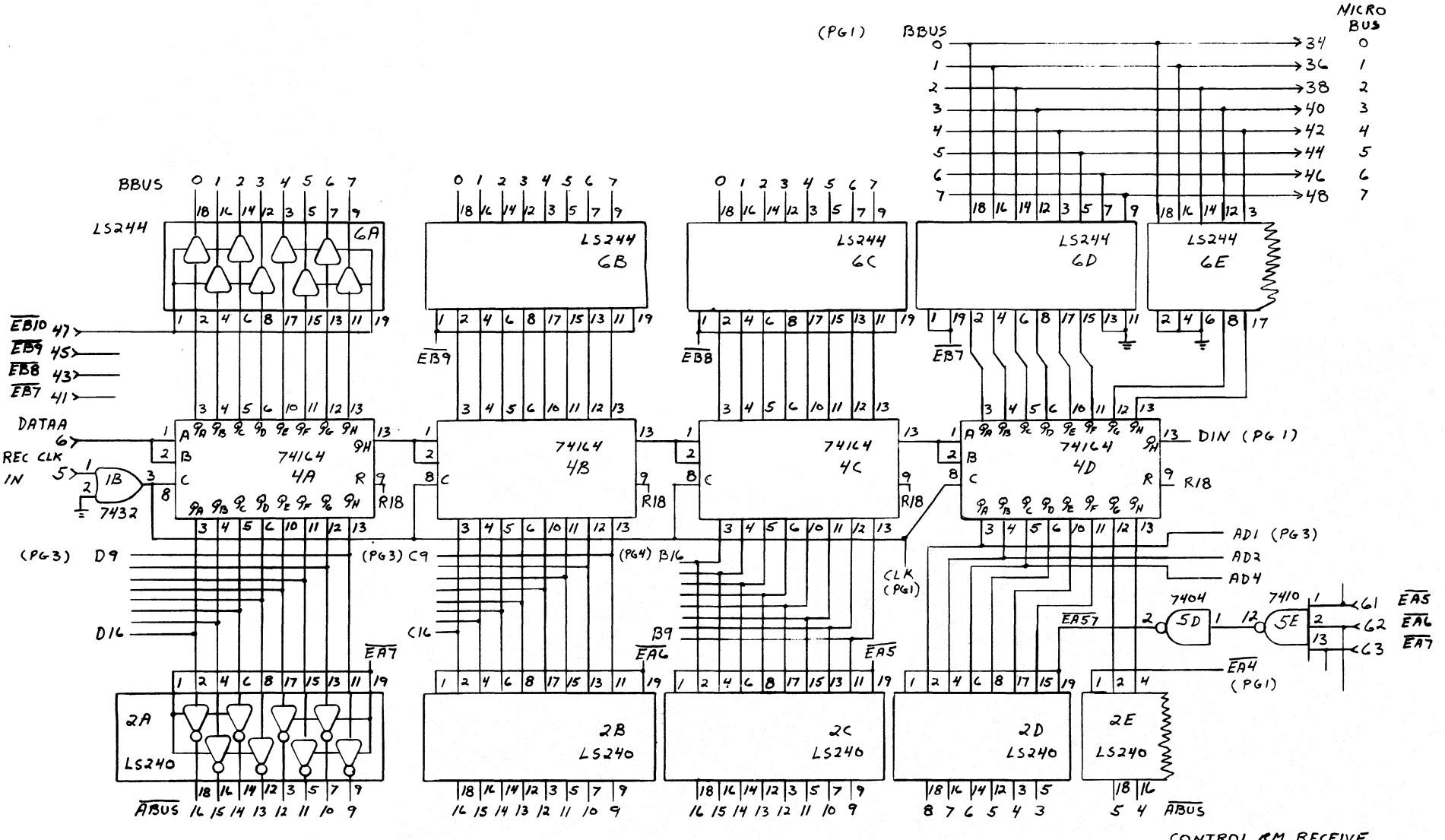


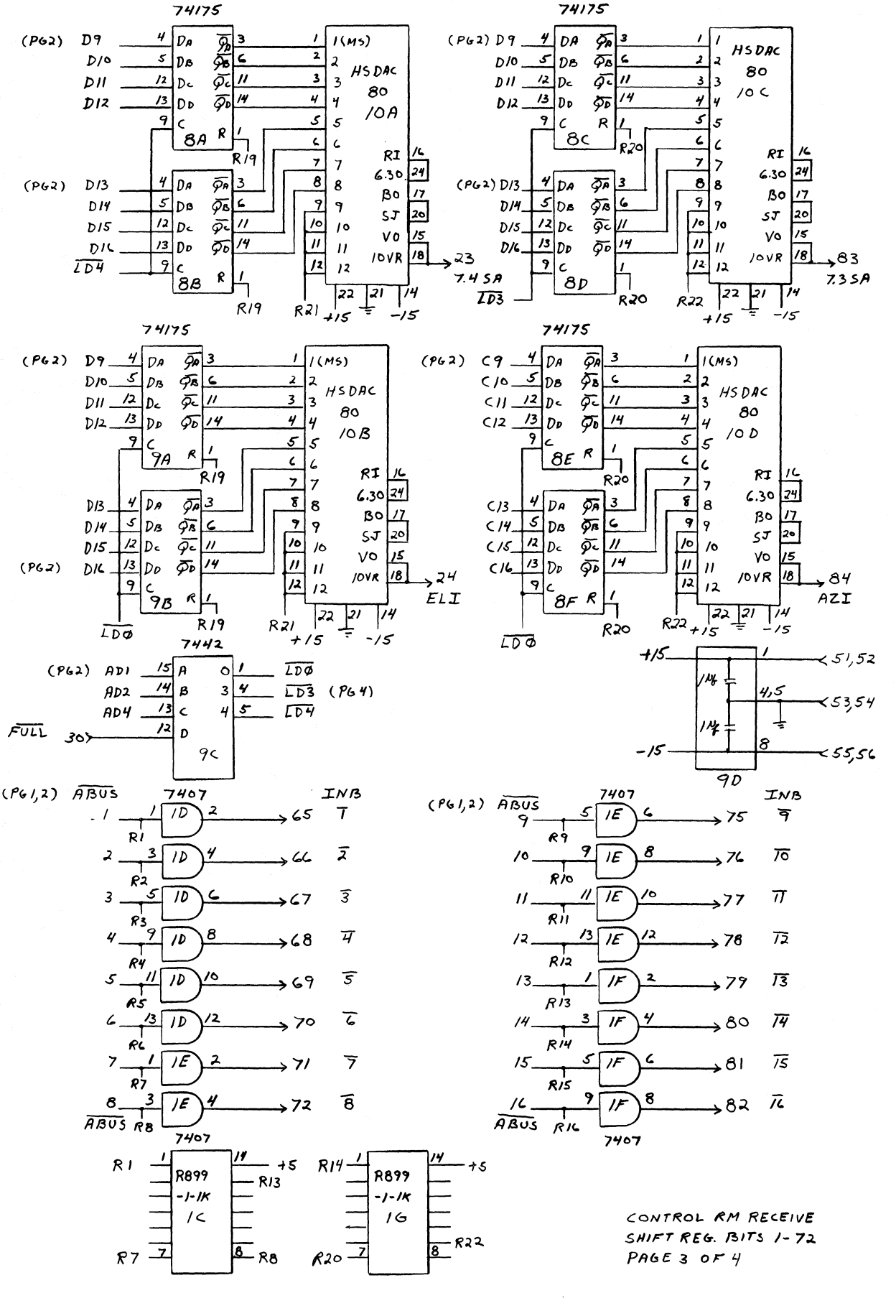


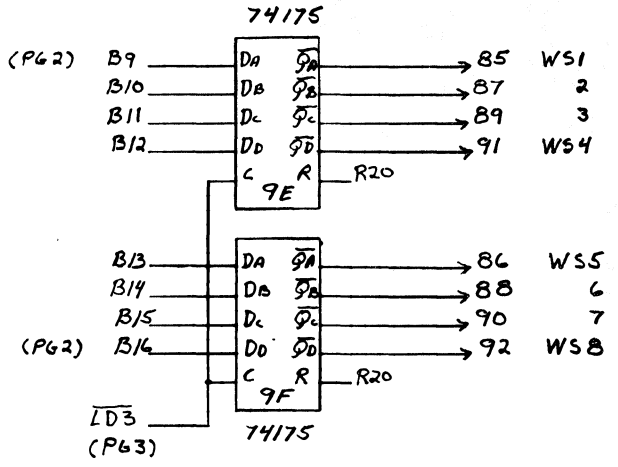


CONTROL RM REC.
SR BITS 73-104
PAGE 4 OF 4

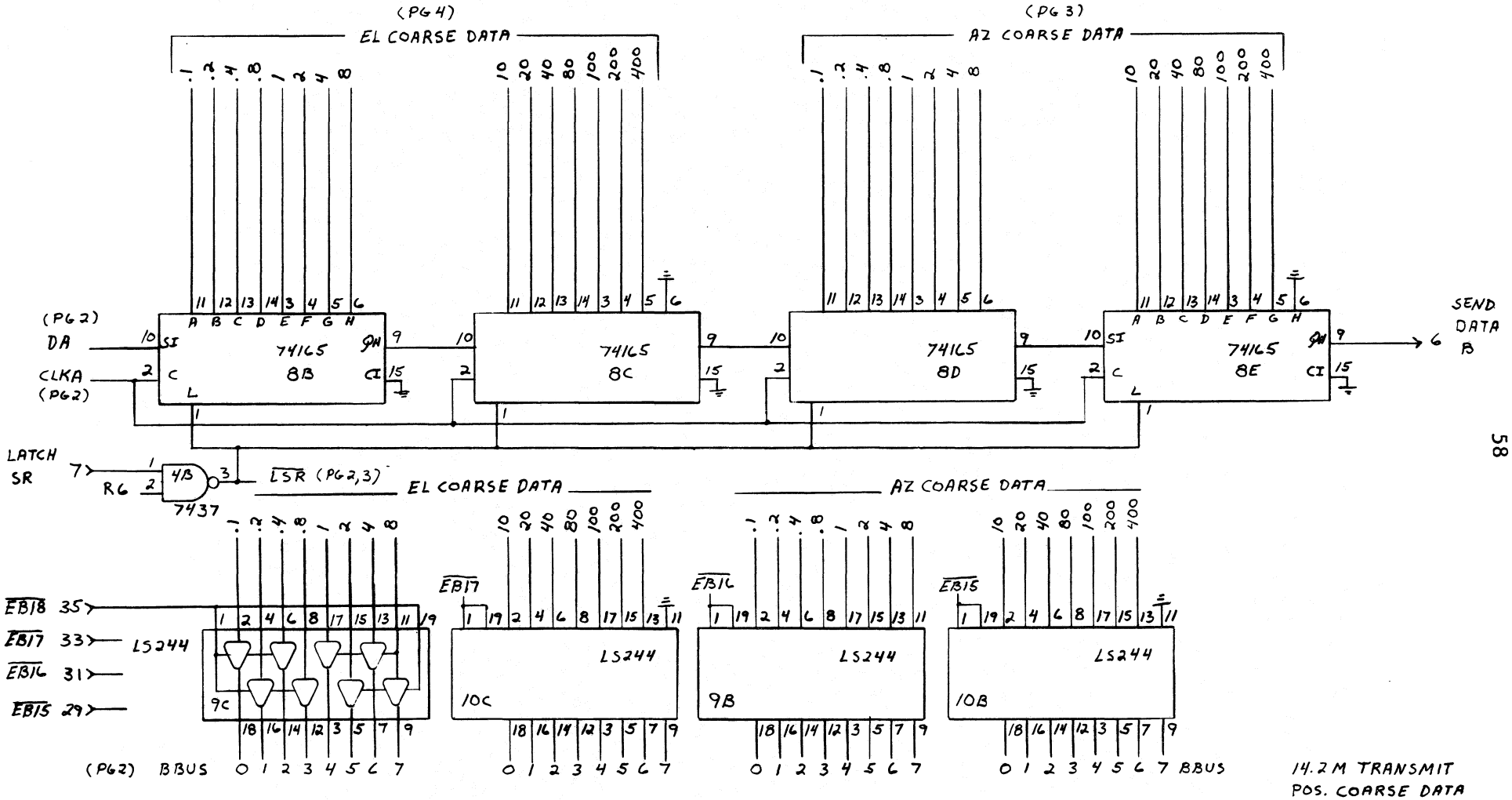

(PG2) BBUS
LS244 6E
LS244 7E
LS244 7D
LS244 7C
LS244 7B
LS244 7A
EB6 39
EB5 37
EB4 35
EB3 33
EB2 31
EB1 29
(PG2) DIN
(PG2) CLK
4E 74LC4
4F 74LC4
4G 74LC4
5G 74LC4
5F 74LC4
R17
EA1 57
EA2 58
EA3 59
EA4 60
(PG2)
2E LS240
3A LS240
3B LS240
3C LS240
3D LS240
3E LS240
(PG3) ABUS
NOTE FOR DRAWING SIMPLISITY THE SR OUTPUTS ARE SHOWN TWO AND THREE TIMES
EA1 = AZ POS
EA2 = AZ POS (5 LSB)
EA3 = EL POS
EA4 = EL POS (5 LSB)
CONTROL RM RECEIVE SHIFT REG BITS 1-72
PAGE 1 OF 4

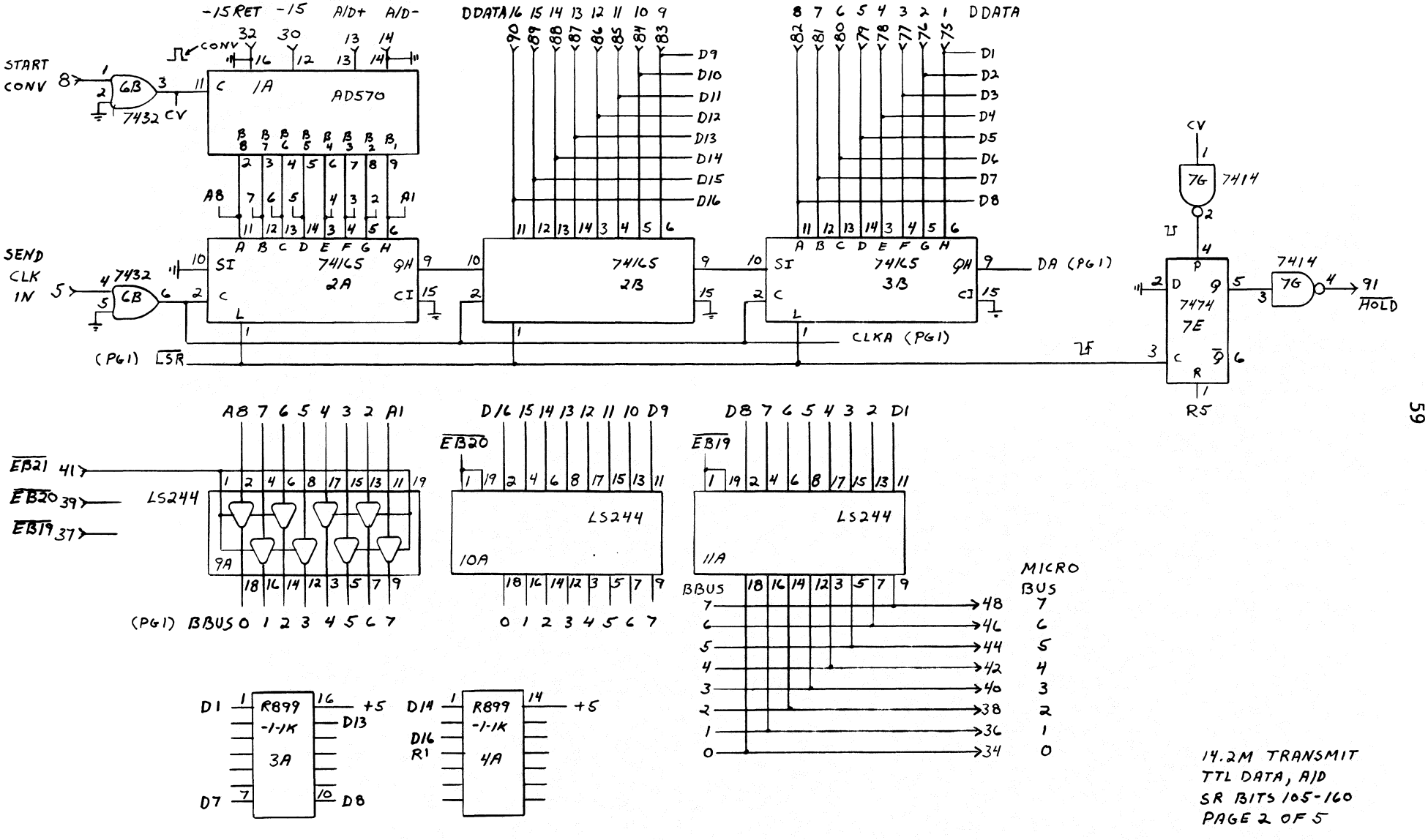

(PG1) BBUS
NICRO BUS
LS244 6A
LS244 6B
LS244 6C
LS244 6D
LS244 6E
EB10 47
EB9 45
EB8 43
EB7 41
DATAA
REC CLK IN
7432
74164 4A
74164 4B
74164 4C
74164 4D
R18
DIN (PG 1)
(PG3) D9
(PG3) C9
(PG4) B16
D16
C16
B9
CLK (PG1)
AD1 (PG3)
AD2
AD4
7404 5D
7410 5E
EA57
EA4 (PG1)
EA7
EA6
EA5
2A LS240
2B LS240
2C LS240
2D LS240
2E LS240
ABUS
EA4 = EL POS (5 LSB)
EA57 = ADDRESS FOR MUX WORDS 5-7
EA5 = MUX WORD 5
EA6 = MUX WORD 6
EA7 = MUX WORD 7
CONTROL RM RECEIVE
SHIFT REG BITS 1-72
PAGE 2 OF 4


74175
(PG2) D9
D10
D11
D12
(PG2) D13
D14
D15
D16
LD4
8A
8B
R19
R21
+15
-15
HSDAC 80 10A
RI
6.30
BO
SJ
VO
10VR
23
7.4 SA
LD3
8C
8D
R20
R22
HSDAC 80 10C
83
7.3 SA
74175
(PG2) D9
D10
D11
D12
(PG2) D13
D14
D15
(PG2) D16
LDØ
9A
9B
HSDAC 80 10B
24
ELI
74175
(PG2) C9
C10
C11
C12
C13
C14
C15
C16
8E
8F
HSDAC 80 10D
84
AZI
7442
(PG2) AD1
AD2
AD4
FULL
30
9C
LDØ
LD3
(PG4)
LD4
+15
-15
51,52
4,5
53,54
55,56
9D
(PG1,2) ABUS
7407
INB
R1
R2
R3
R4
R5
R6
R7
R8
65
66
67
68
69
70
71
72
R9
R10
R11
R12
R13
R14
R15
R16
75
76
77
78
79
80
81
82
R899
-1-1K
1C
1G
R13
R22
CONTROL RM RECEIVE
SHIFT REG. BITS 1-72
PAGE 3 OF 4

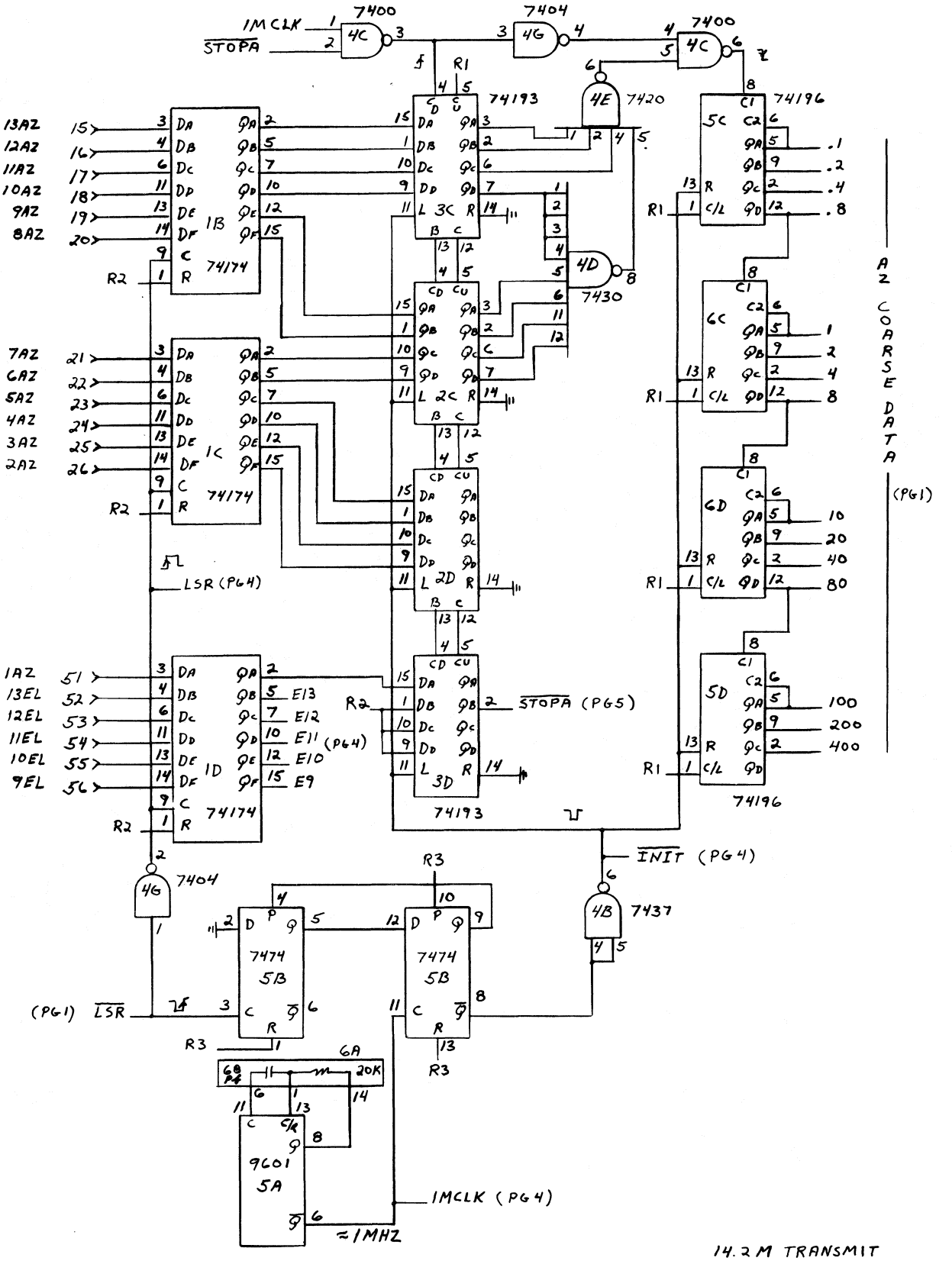


CONTROL RM RECEIVE
SHIFT REG BITS 1-72
PAGE 4 OF 4

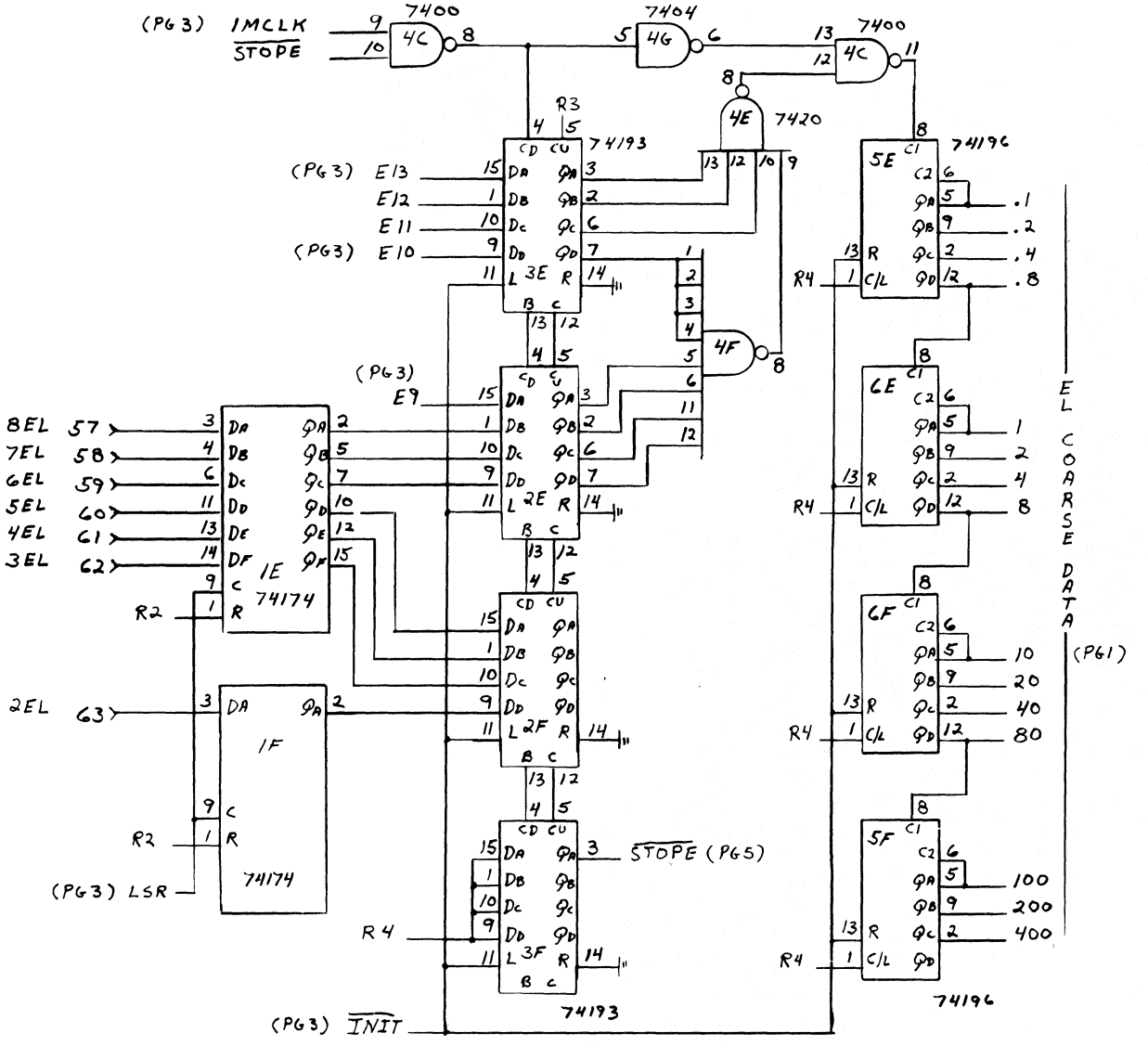

(PG 4)
EL COARSE DATA
.1 .2 .4 .8 1 2 4 8
10 20 40 80 100 200 400
(PG 3)
AZ COARSE DATA
.1 .2 .4 .8 1 2 4 8
10 20 40 80 100 200 400
(PG 2)
DA
CLKA
(PG 2)
74165
8B
74165
8C
74165
8D
74165
8E
SEND DATA B
LATCH SR
RG
7437
LSR (PG 2,3)
EL COARSE DATA
AZ COARSE DATA
EB18
EB17
EB16
EB15
LS244
9C
10C
9B
10B
(PG2) BBUS 0 1 2 3 4 5 6 7
14.2M TRANSMIT
POS. COARSE DATA
BITS 105-160
PAGE 1 OF 5



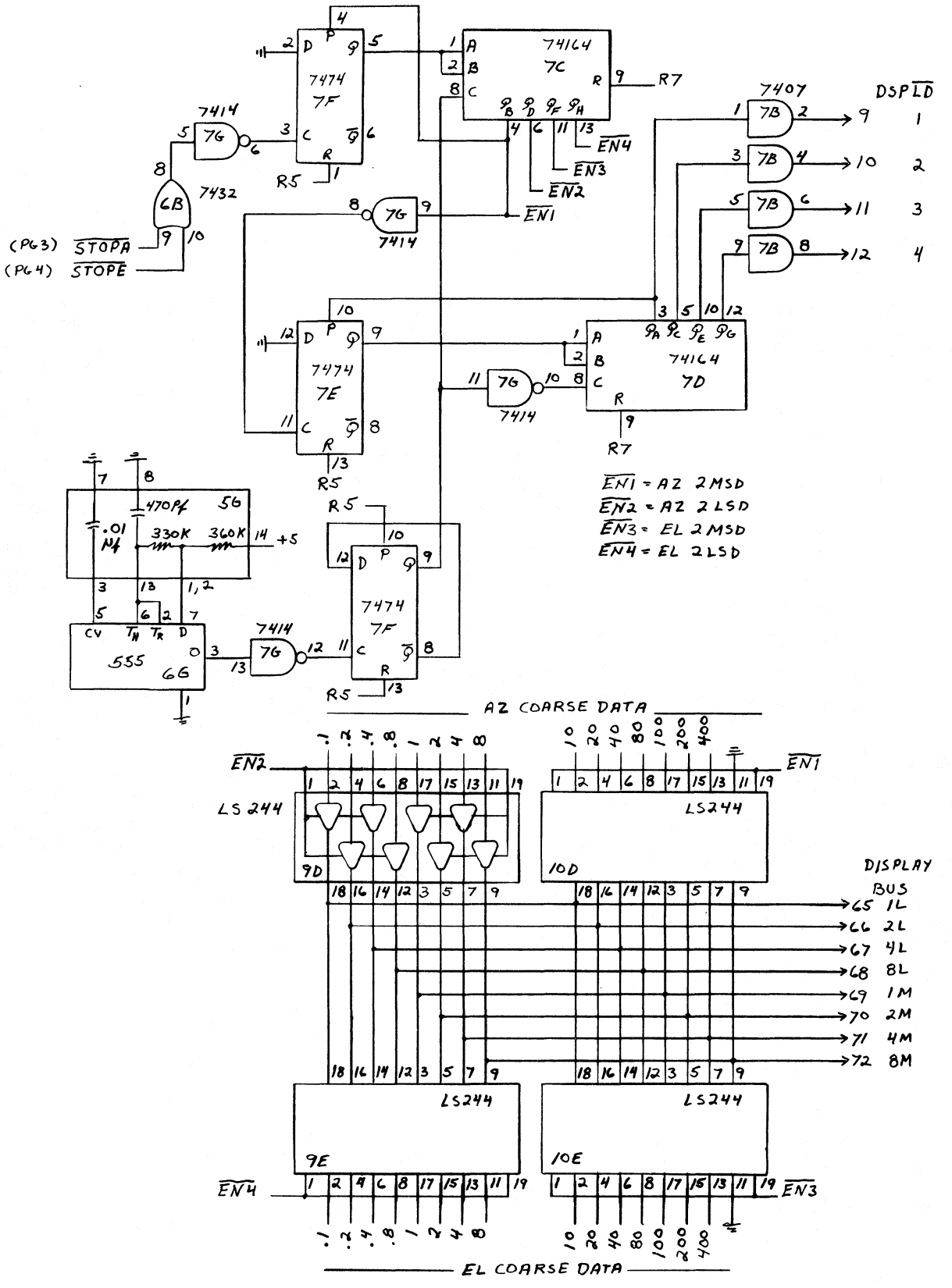
14.2M TRANSMIT
TTL DATA, A/D
SR BITS 105-160
PAGE 2 OF 5



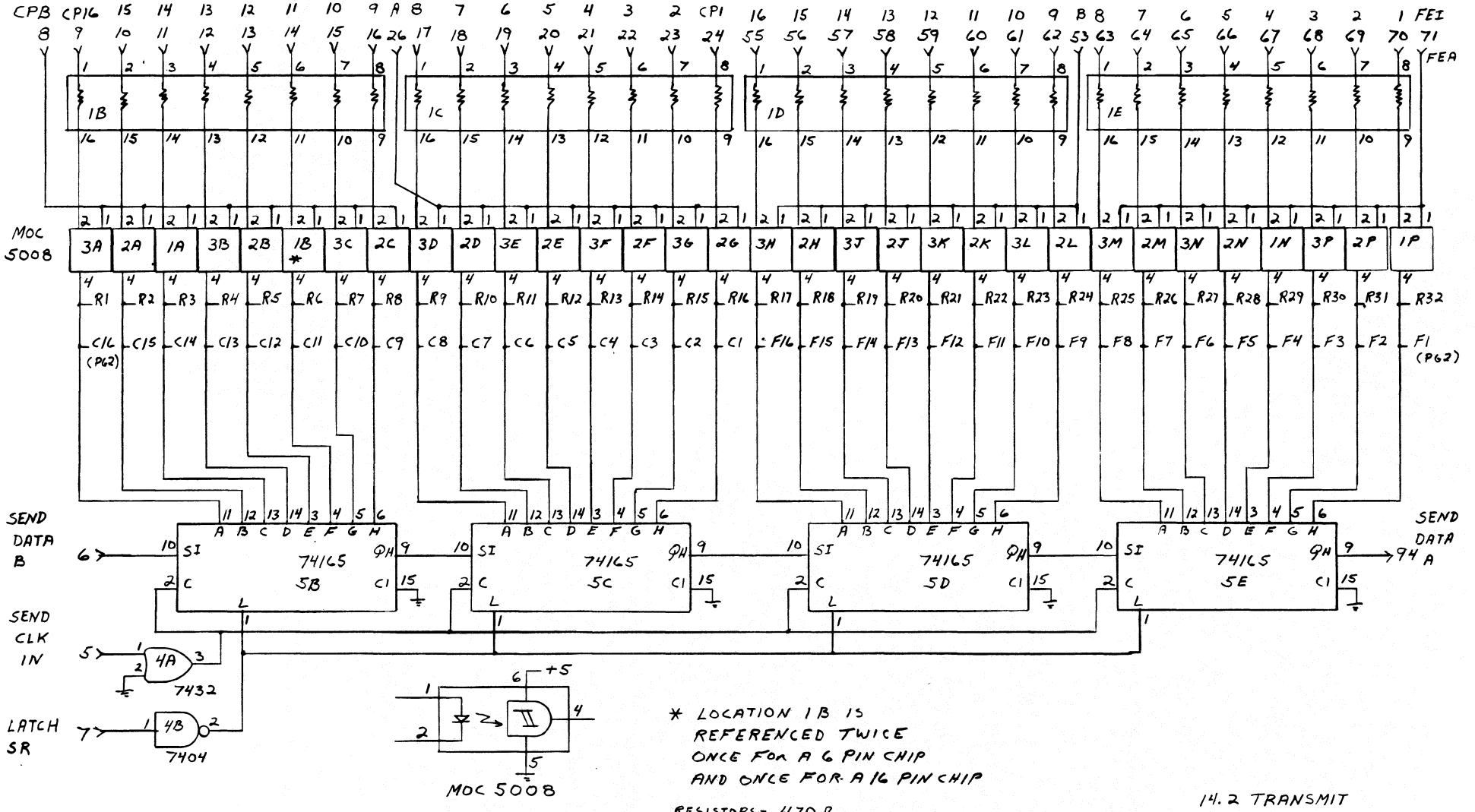
14.2M TRANSMIT
AZ CONVERT
SR BITS 105-160
PAGE 3 OF 5



14.2M TRANSMIT
EL CONVERT
SR BITS 105-160
PAGE 4 OF 5



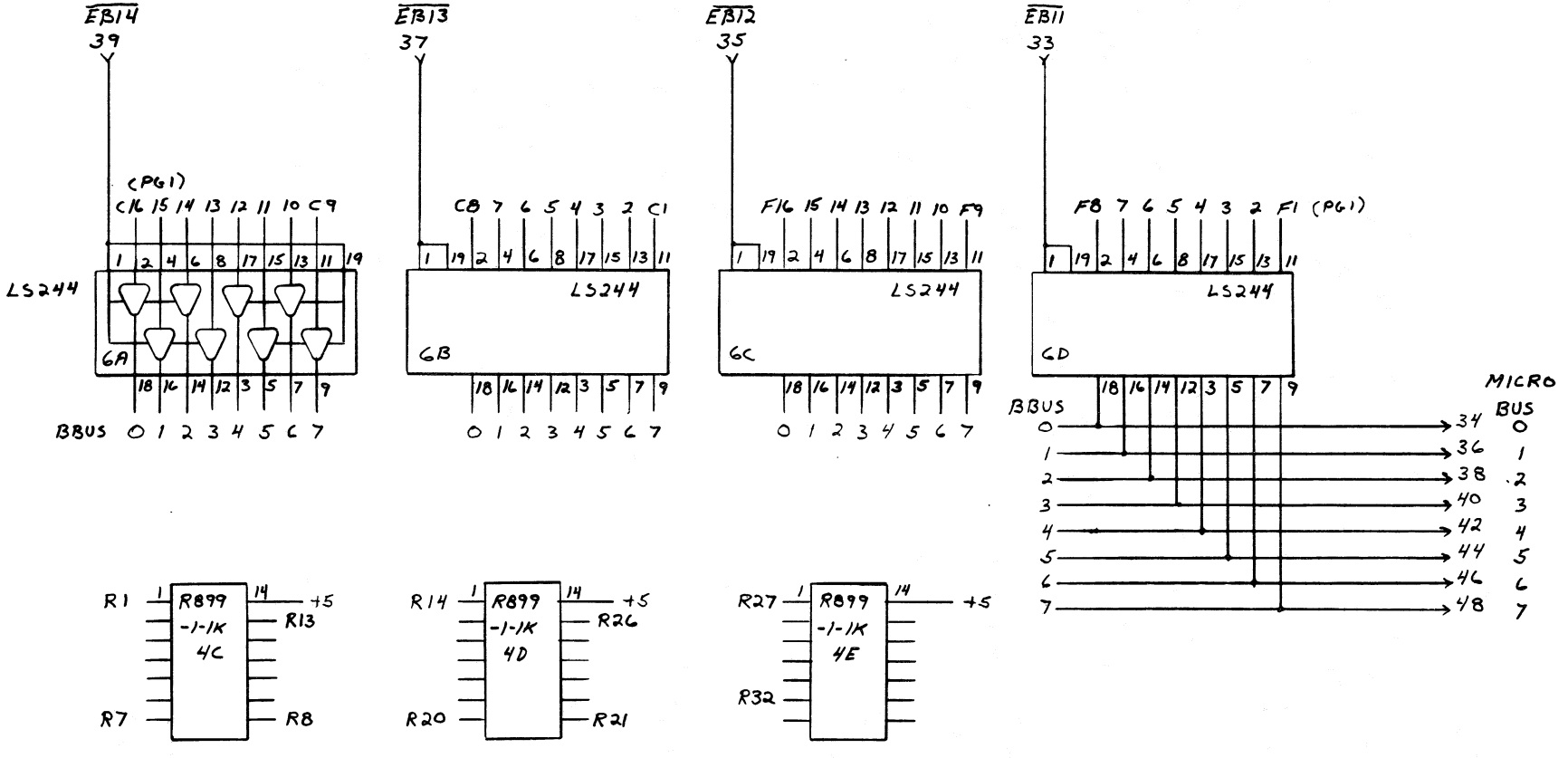
14.2 M TRANSMIT
LOCAL DSP
SR BITS 105-160
PAGE 5 OF 5



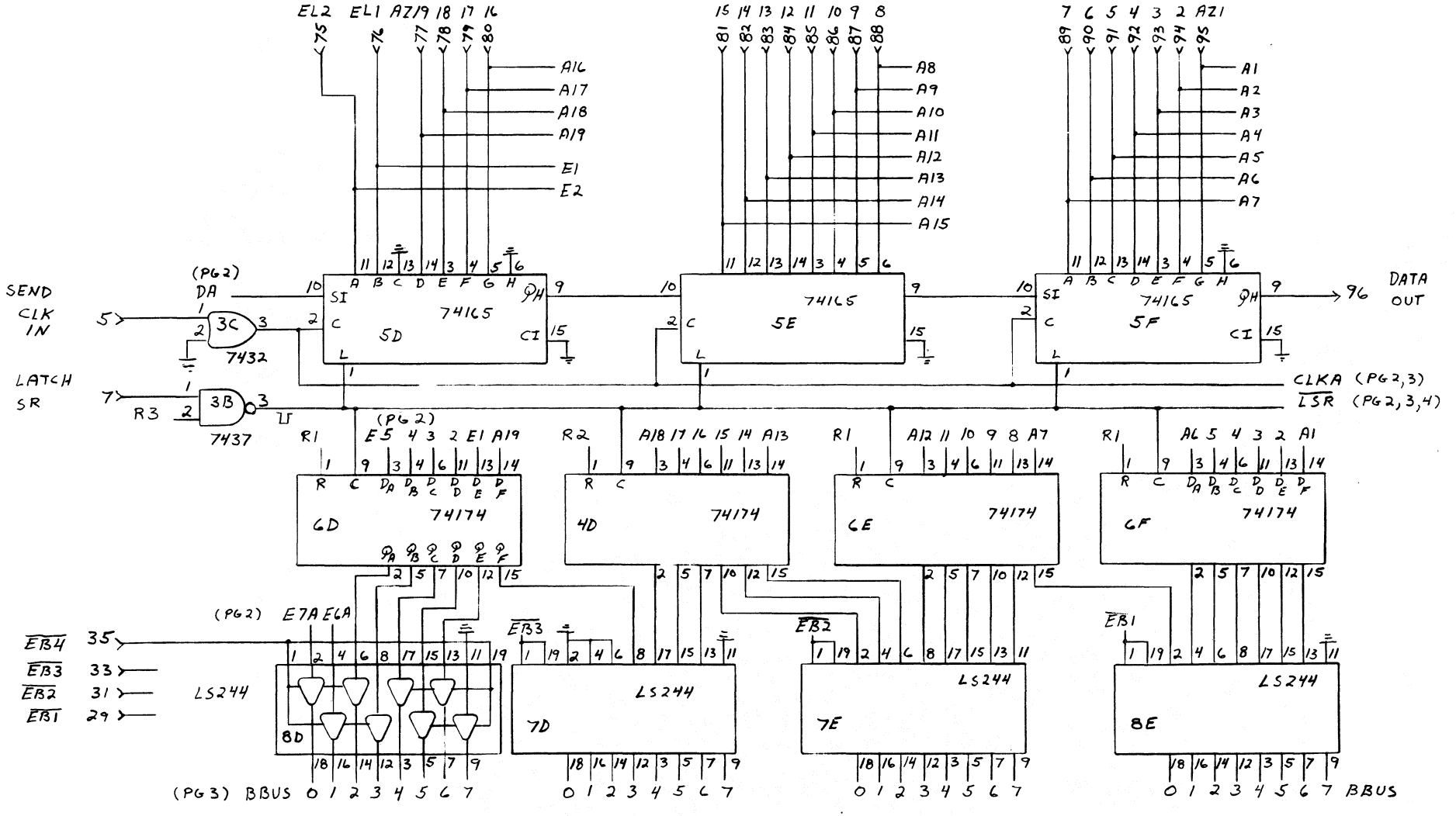
* LOCATION 1B IS REFERENCED TWICE ONCE FOR A 6 PIN CHIP AND ONCE FOR A 16 PIN CHIP

RESISTORS = 470Ω

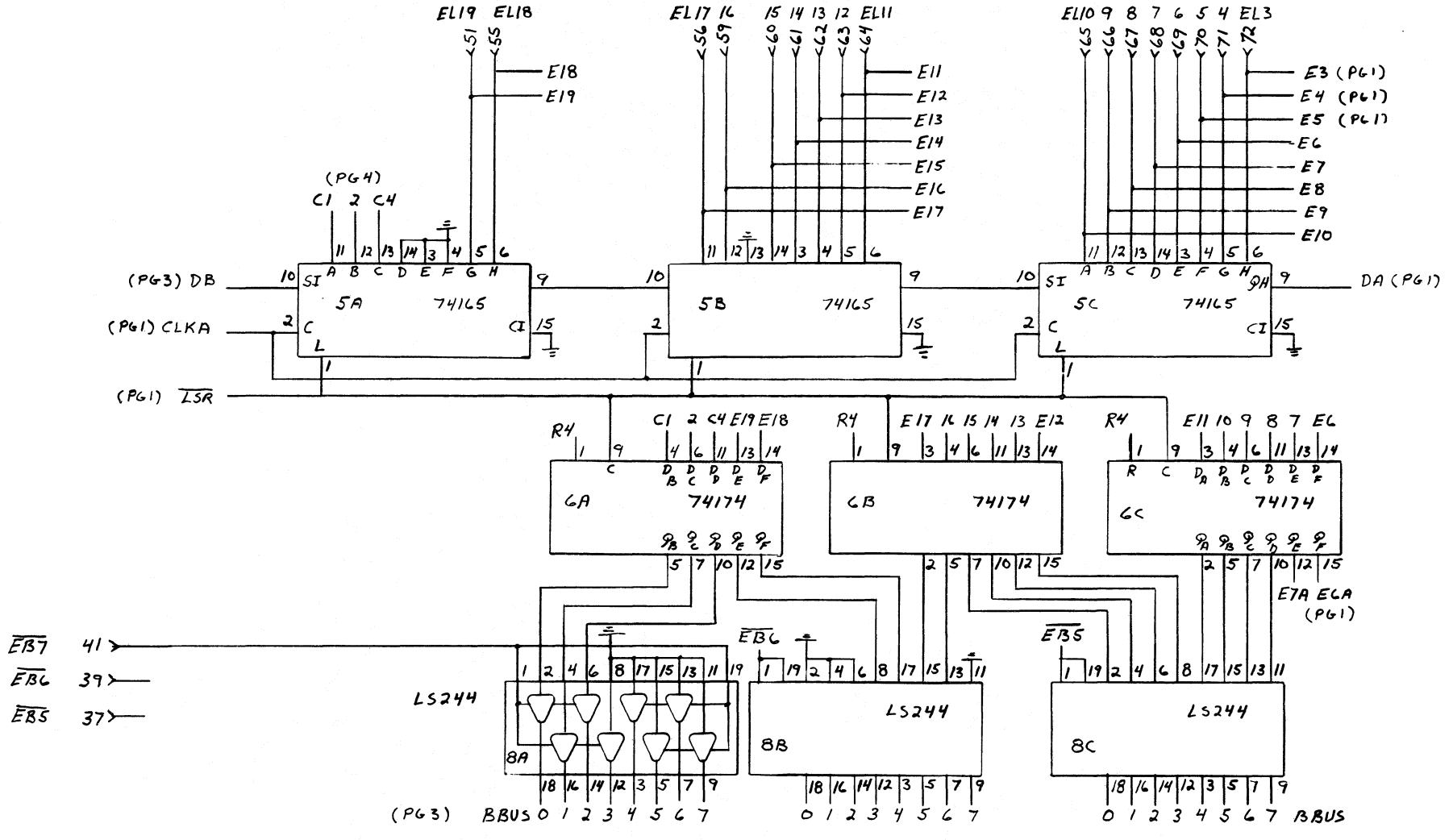
14.2 TRANSMIT
BITS 73-104
CONTROL PANEL
FRONT END
PAGE 1 OF 2



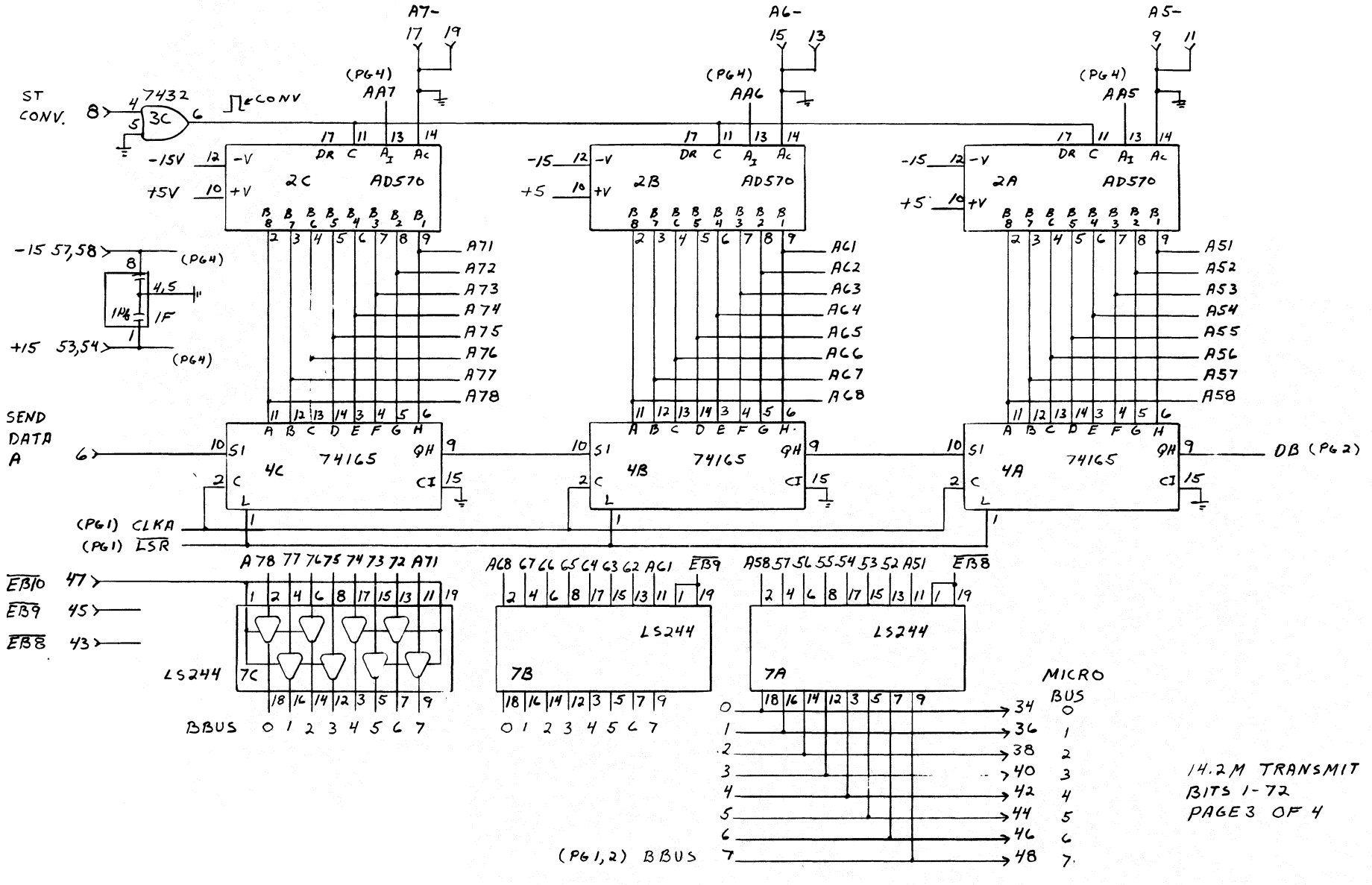
14.2 M TRANSMIT
BITS 73-104
PAGE 2 OF 2

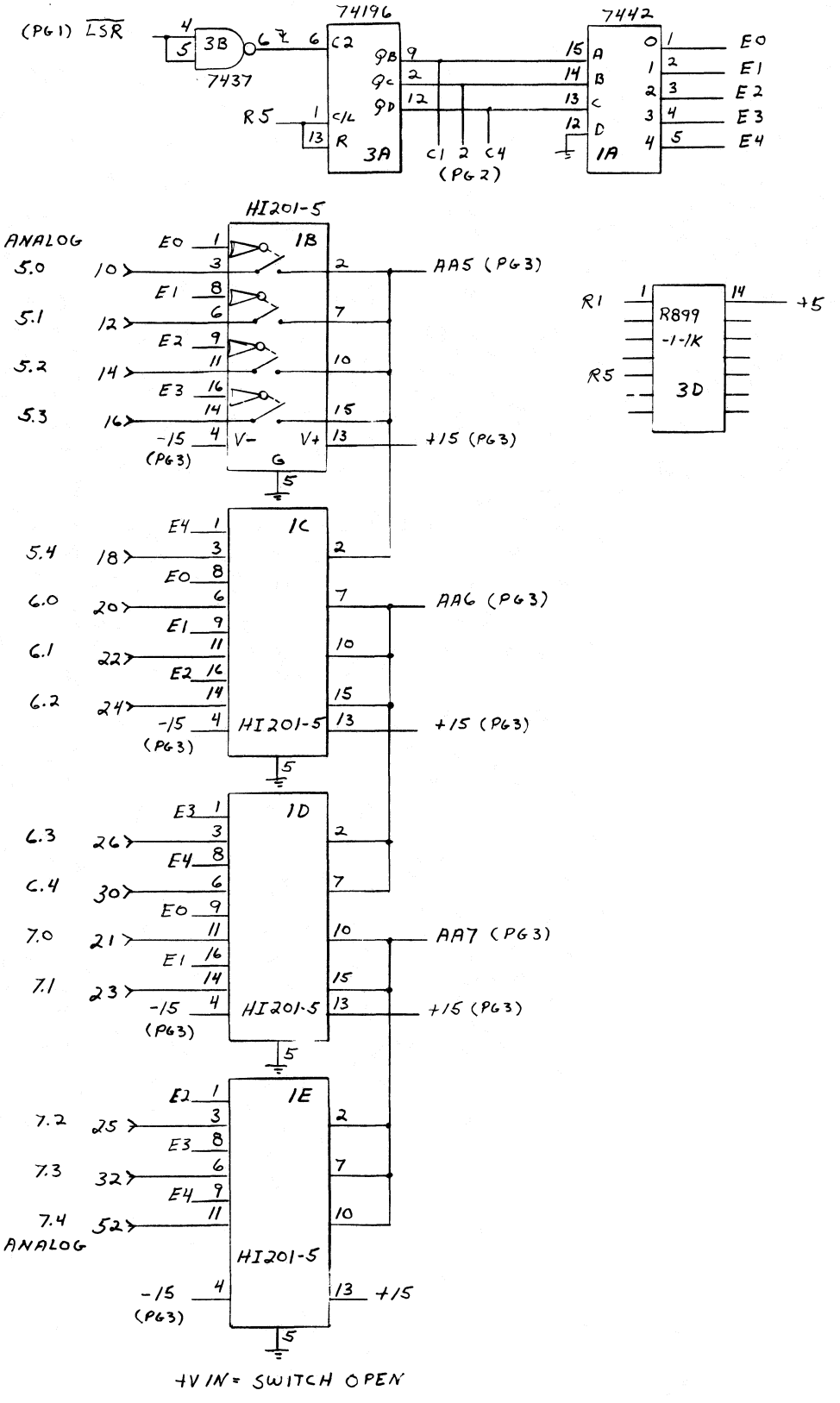


14.2 M TRANSMIT
BITS 1 - 72
PAGE 1 OF 4

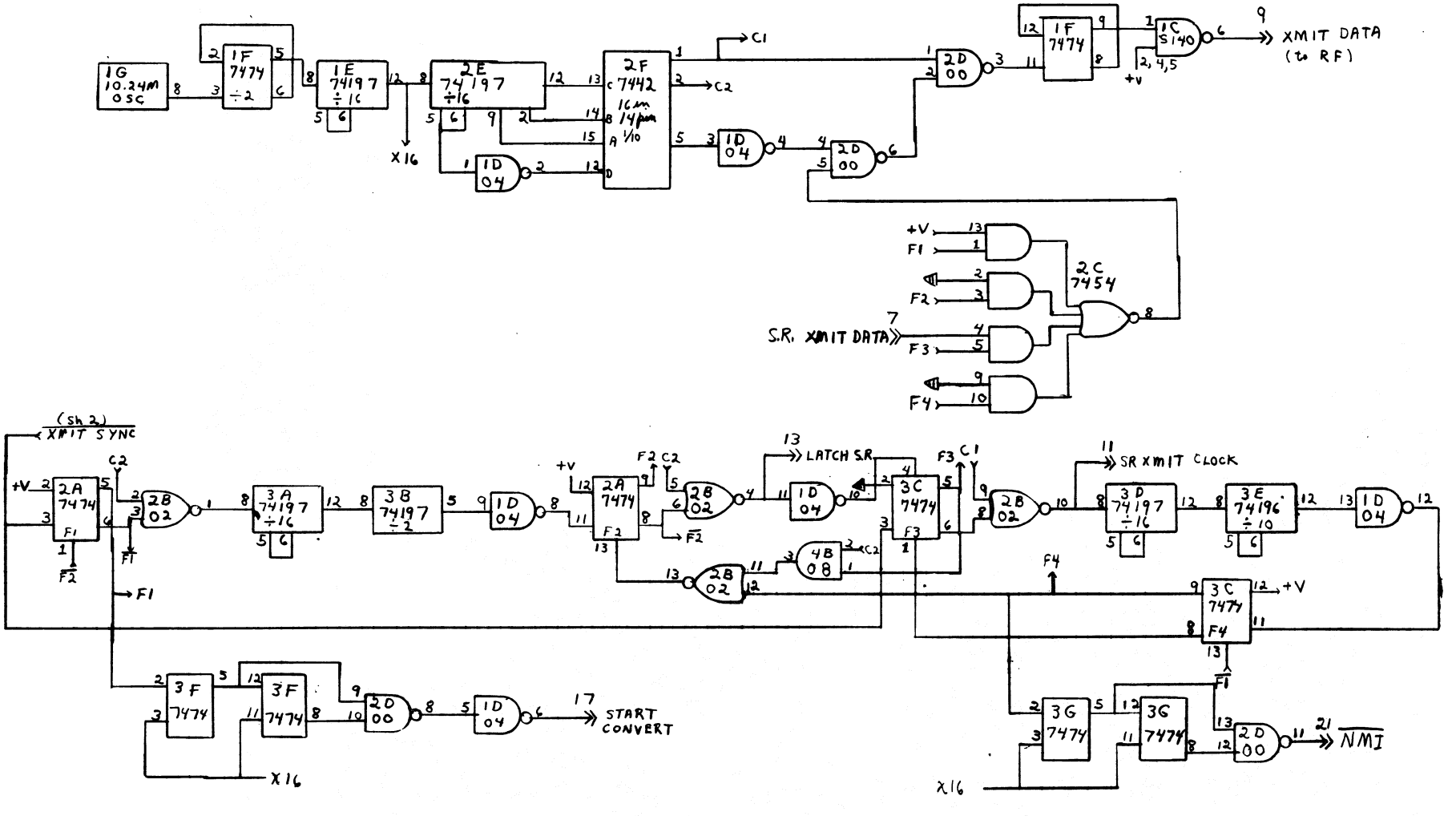


14.2 M TRANSMIT
BITS 1-72
PAGE 2 OF 4

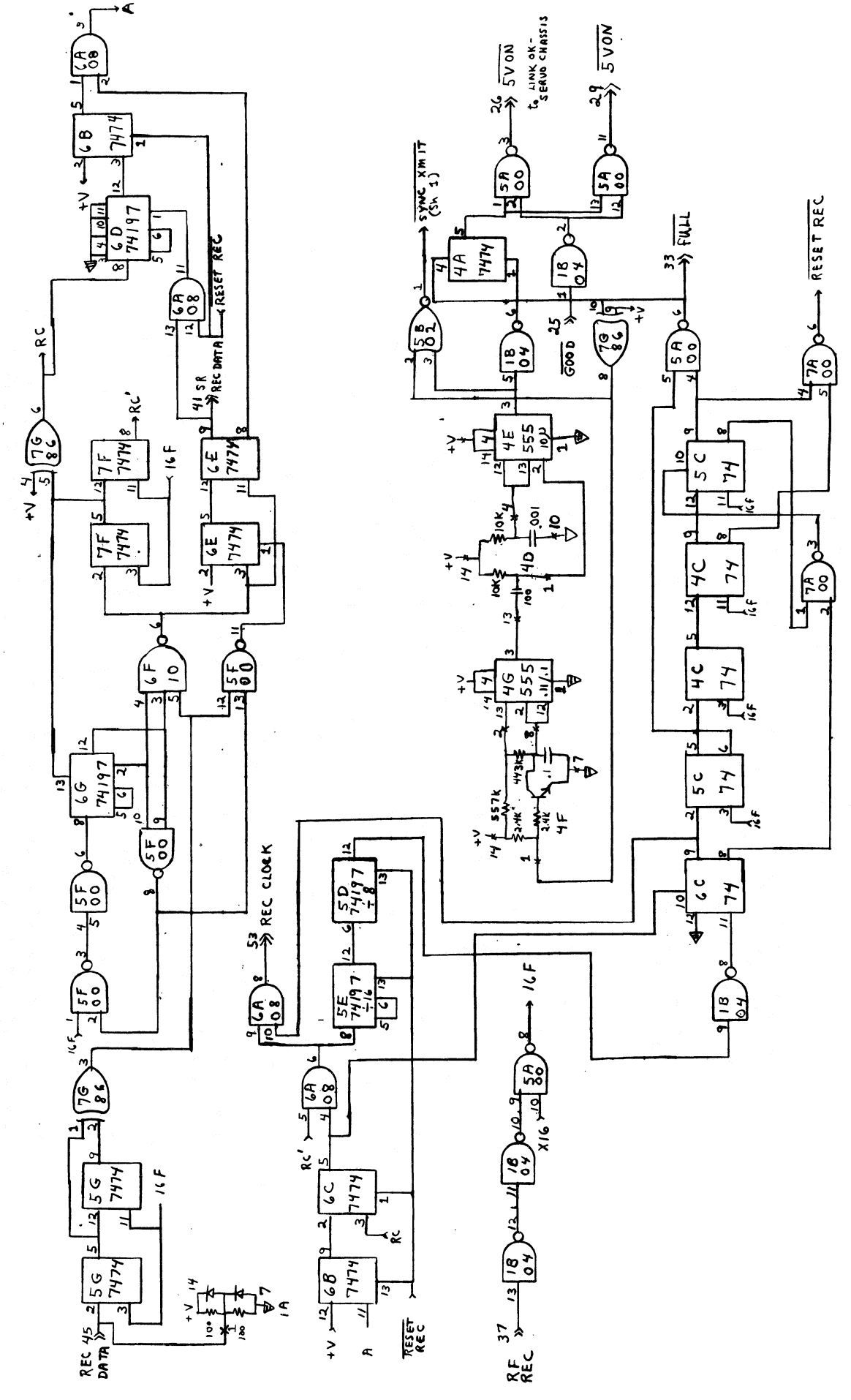

ST CONV.
7432
3C
ECONV
(PG4)
AA7
AA6
AA5
A7-
A6-
A5-
-15V
+5V
2C
2B
2A
AD570
74165
4C
4B
4A
SEND DATA A
(PG1) CLKA
(PG1) LSR
(PG4)
(PG2)
DB (PG2)
LS244
7C
7B
7A
EB10
EB9
EB8
BBUS 0 1 2 3 4 5 6 7
(PG1,2) BBUS
MICRO BUS
14.2M TRANSMIT
BITS 1-72
PAGE 3 OF 4

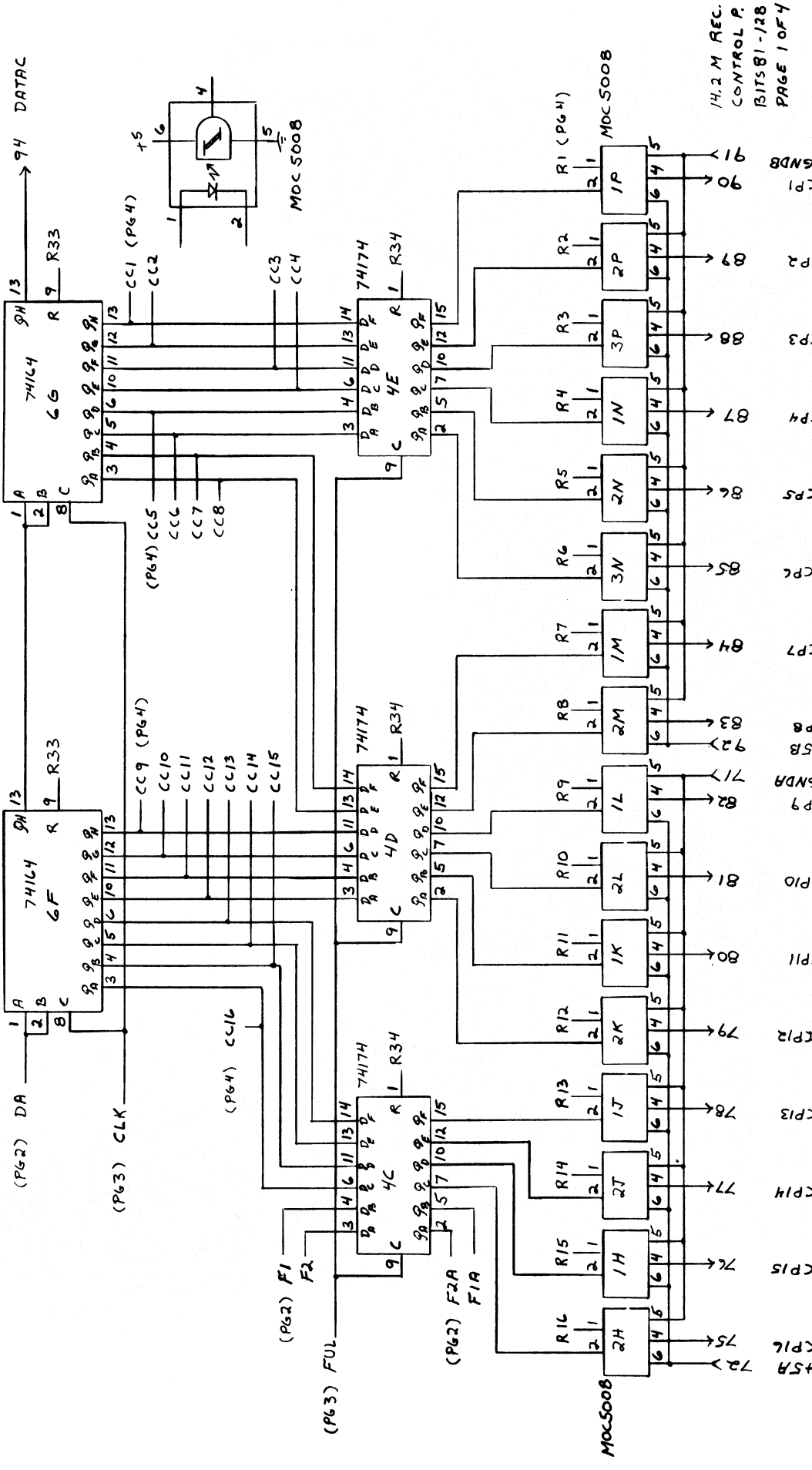


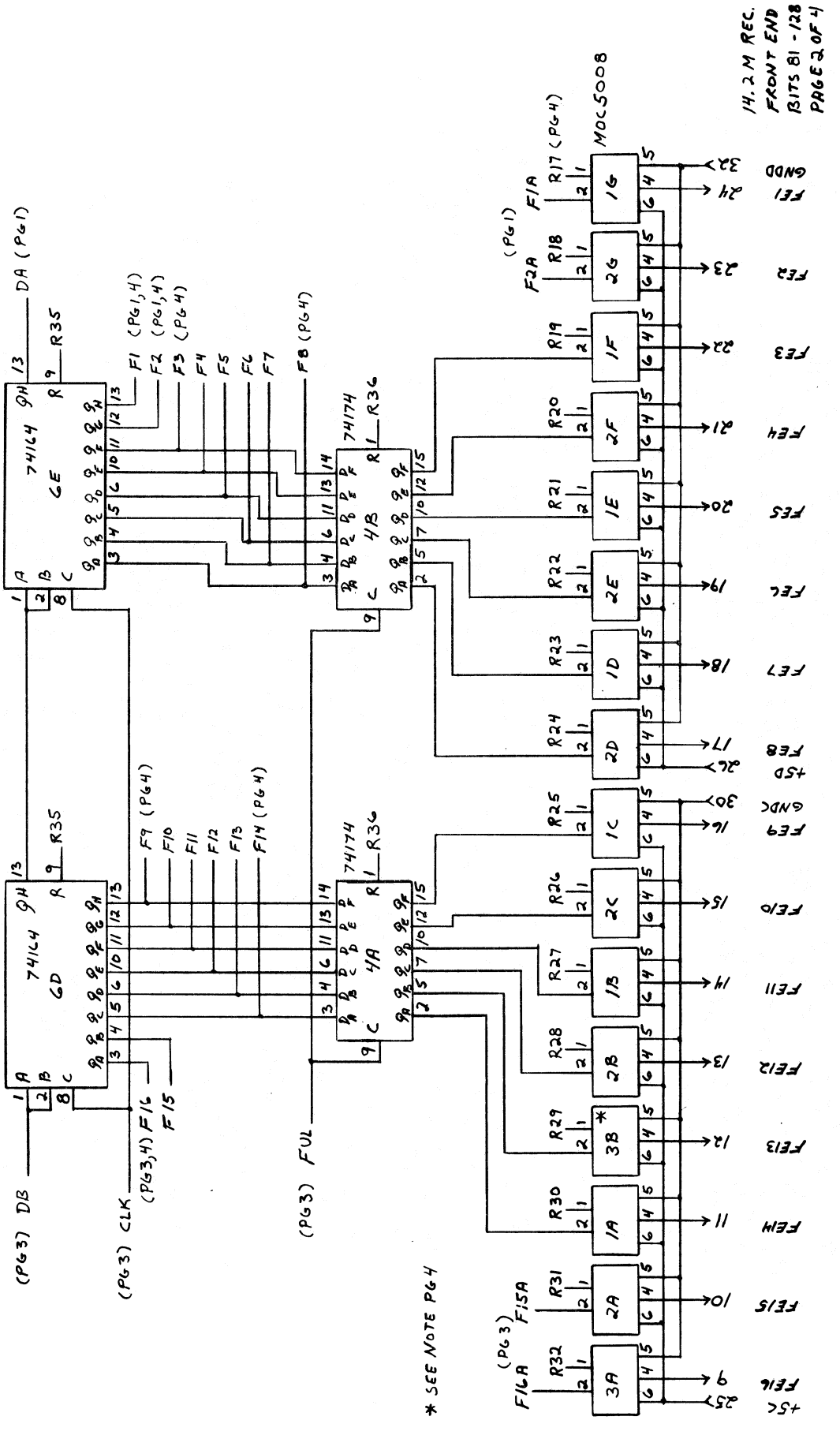
14.2 M TRANSMIT
BITS 1-72
ANALOG MUX
PAGE 4 OF 4

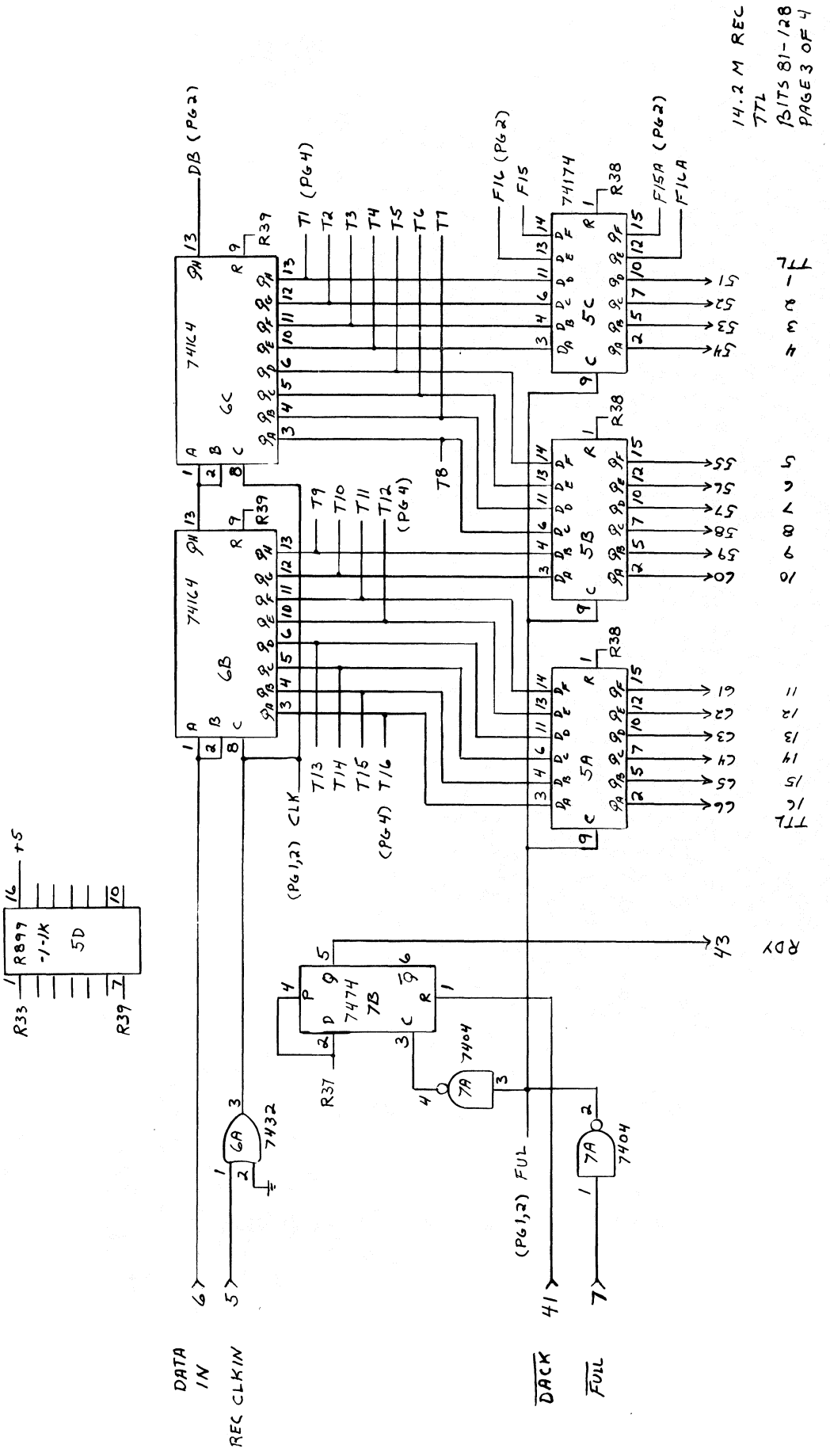


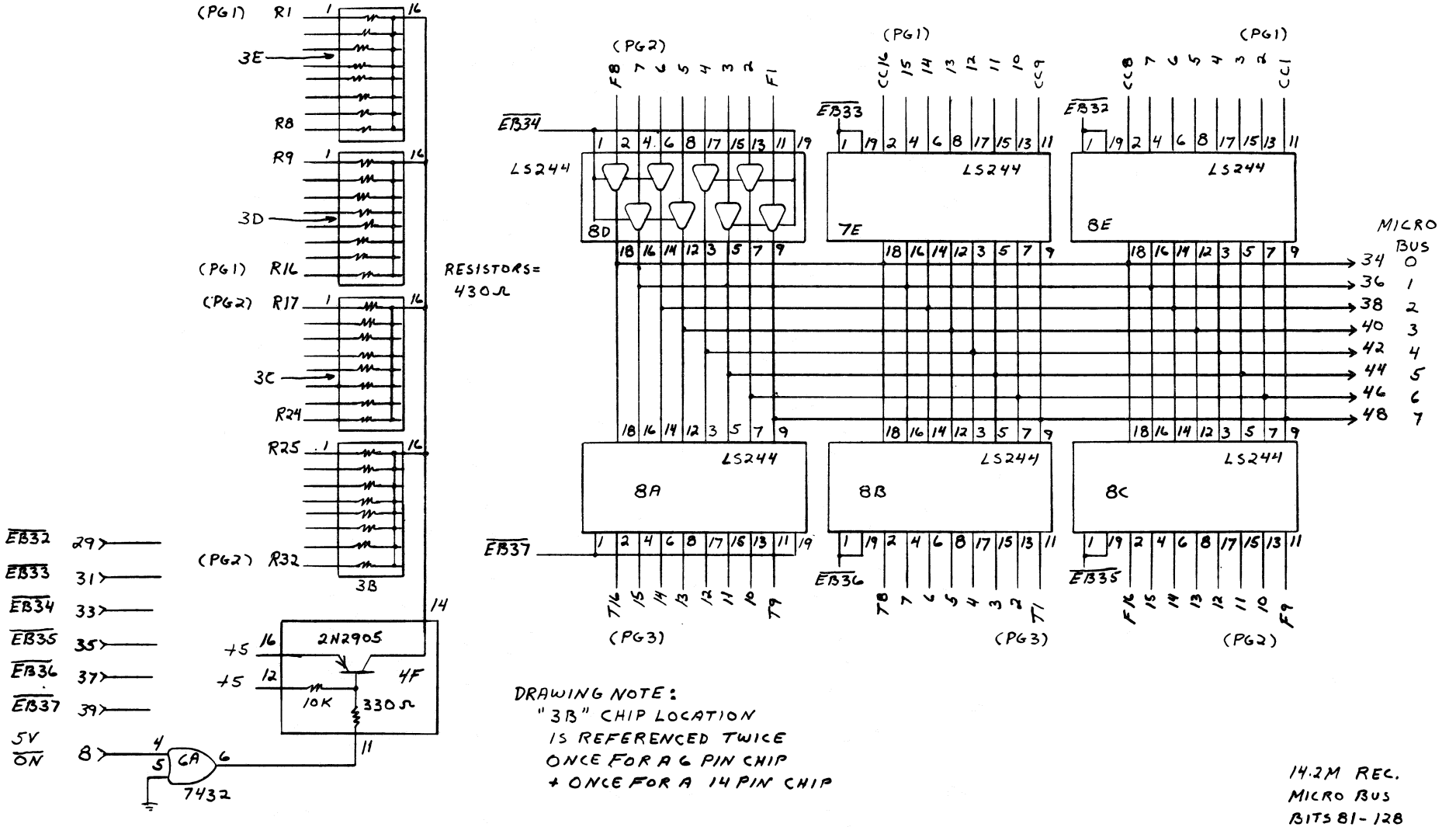
14.2 XMIT REC (Sh 1 of 2)
11-21-83

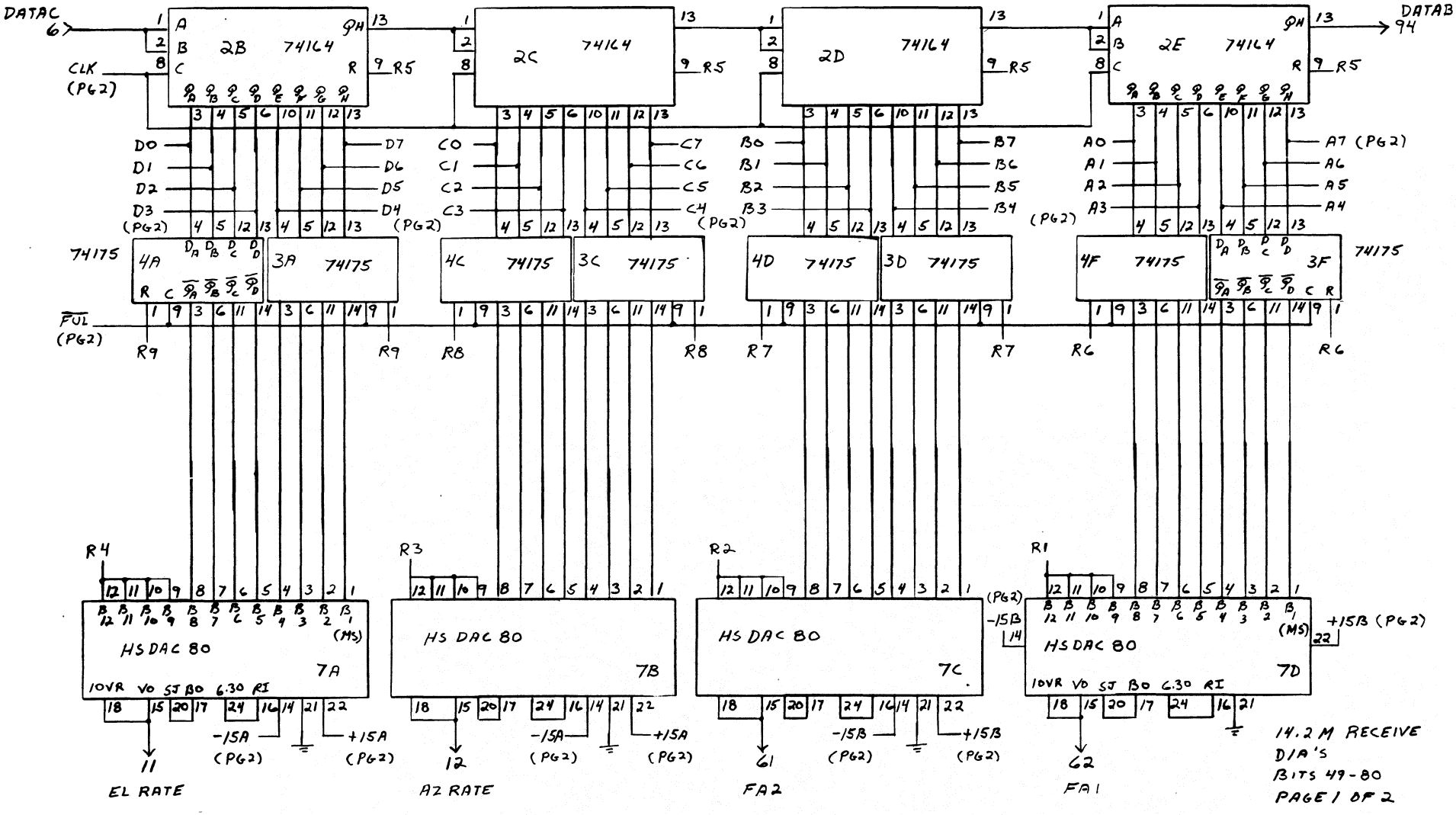

14.2 XMIT REC (SH 2 of 2)
12-8-83
REC DATA
RESET REC
REC CLOCK
RF REC
SYNC XMIT (SH 1)
5VON
LINK OK - SERVO CHASSIS
GOOD
FULL
RESET REC

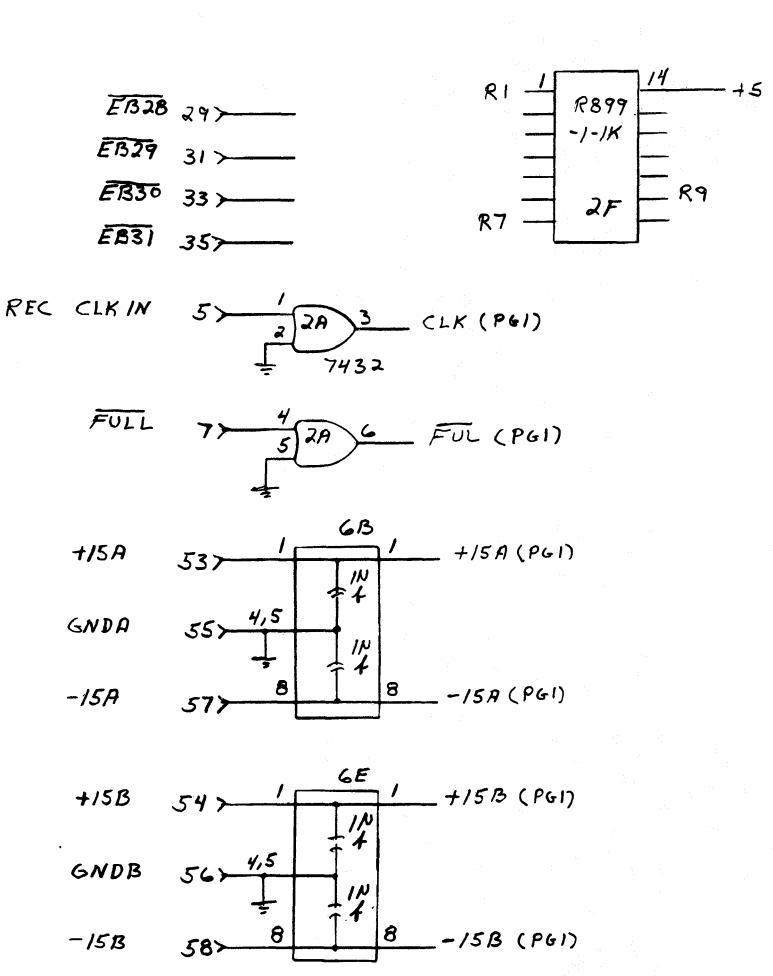

14.2 M REC.
CONTROL P.
BITS 81-128
PAGE 1 OF 4
94 DATAC
74164
6G
6F
74174
4E
4D
4C
MOC5008
R33
R34
R1 (PG4)
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
1P
2P
3P
1N
2N
3N
1M
2M
1L
2L
1K
2K
1J
2J
1H
2H
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP8
CP9
CP10
CP11
CP12
CP13
CP14
CP15
CP16
GNDB
GNDA
+5B
+5A
(PG2) DA
(PG3) CLK
(PG4) CC1
(PG4) CC2
(PG4) CC3
(PG4) CC4
(PG4) CC5
(PG4) CC6
(PG4) CC7
(PG4) CC8
(PG4) CC9
(PG4) CC10
(PG4) CC11
(PG4) CC12
(PG4) CC13
(PG4) CC14
(PG4) CC15
(PG4) CC16
(PG2) F1
F2
(PG3) FUL
(PG2) F2A
F1A

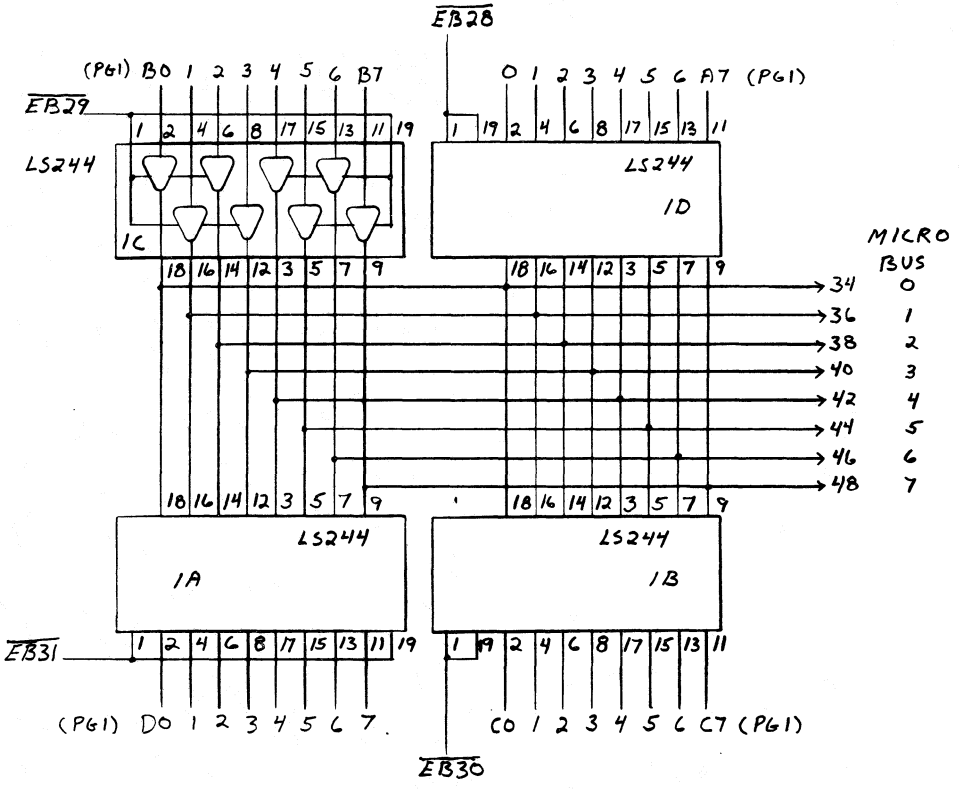

14.2 M REC.
FRONT END
BITS 81 - 128
PAGE 2 OF 4
MOC 5008
74164
6E
6D
74174
4B
4A
DA (PG1)
R35
R36
F1 (PG1,4)
F2 (PG1,4)
F3 (PG4)
F4
F5
F6
F7
F8 (PG4)
F9 (PG4)
F10
F11
F12
F13
F14 (PG4)
F15
F16
(PG3) DB
(PG3) CLK
(PG3,4)
(PG3) FUL
* SEE NOTE PG4
F1A
F2A
F15A
F16A
(PG1)
(PG3)
R17 (PG4)
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
1G
2G
1F
2F
1E
2E
1D
2D
1C
2C
1B
2B
3B
1A
2A
3A
GNDD
FE1
FE2
FE3
FE4
FE5
FE6
FE7
FE8
+5D
GNDC
FE9
FE10
FE11
FE12
FE13
FE14
FE15
FE16
+5C


14.2 M REC
TTL
BITS 81-128
PAGE 3 OF 4
DATA IN
REC CLKIN
DACK
FULL
RDY
TTL
DB (PG2)
F16 (PG2)
F15
F15A (PG2)
F16A
T1 (PG4)
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12 (PG4)
T13
T14
T15
T16
(PG4)
(PG1,2) CLK
(PG1,2) FUL
74164
6C
6B
74174
5C
5B
5A
7474
7B
7404
7432
6A
7A
R39
R38
R37
R33
R899
-1-1K
5D
+5

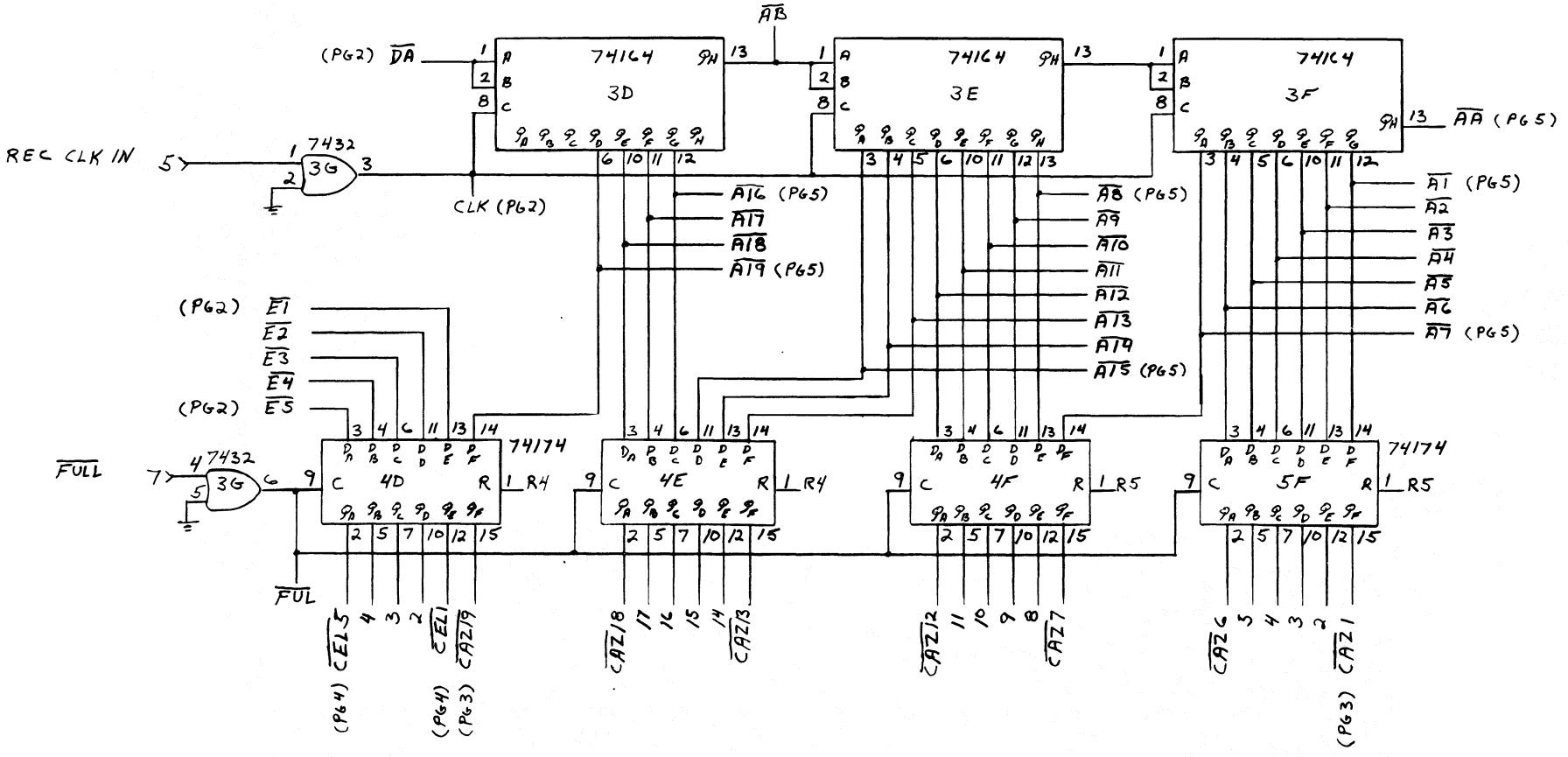

(PG1) R1
3E
R8
R9
3D
(PG1) R16
(PG2) R17
3C
R24
R25
(PG2) R32
3B
RESISTORS= 430Ω
(PG2)
(PG1)
(PG1)
LS244
8D
7E
8E
8A
8B
8C
MICRO BUS
34 0
36 1
38 2
40 3
42 4
44 5
46 6
48 7
(PG3)
(PG3)
(PG2)
EB32 29
EB33 31
EB34 33
EB35 35
EB36 37
EB37 39
5V ON 8
7432
2N2905
+5
+5
10K
330Ω
4F
DRAWING NOTE:
"3B" CHIP LOCATION
IS REFERENCED TWICE
ONCE FOR A 6 PIN CHIP
+ ONCE FOR A 14 PIN CHIP
14.2M REC.
MICRO BUS
BITS 81-128
PAGE 4 OF 4


DATAC
6
CLK
(PG2)
2B 74164
2C 74164
2D 74164
2E 74164
DATAB
94
R5
D0
D1
D2
D3
D4
D5
D6
D7
C0
C1
C2
C3
C4
C5
C6
C7
B0
B1
B2
B3
B4
B5
B6
B7
A0
A1
A2
A3
A4
A5
A6
A7 (PG2)
74175
4A
3A
4C
3C
4D
3D
4F
3F
FUL
(PG2)
R9
R8
R7
R6
R4
R3
R2
R1
HS DAC 80
7A
7B
7C
7D
10VR VO SJ BO 6.30 RI
(MS)
-15A
(PG2)
+15A
(PG2)
-15B
+15B (PG2)
11
EL RATE
12
AZ RATE
61
FA2
62
FA1
14.2 M RECEIVE
D/A'S
BITS 49-80
PAGE 1 OF 2

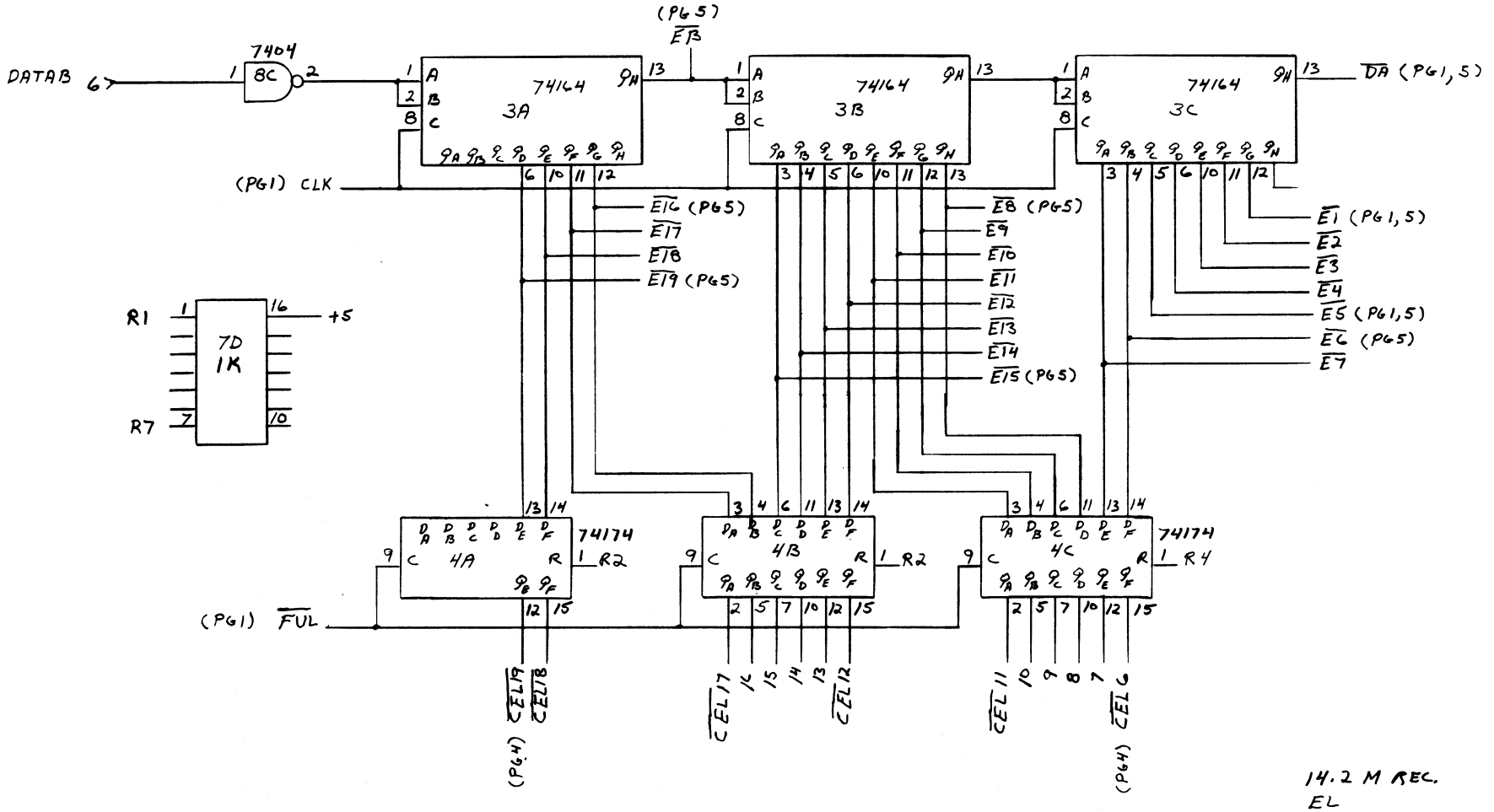




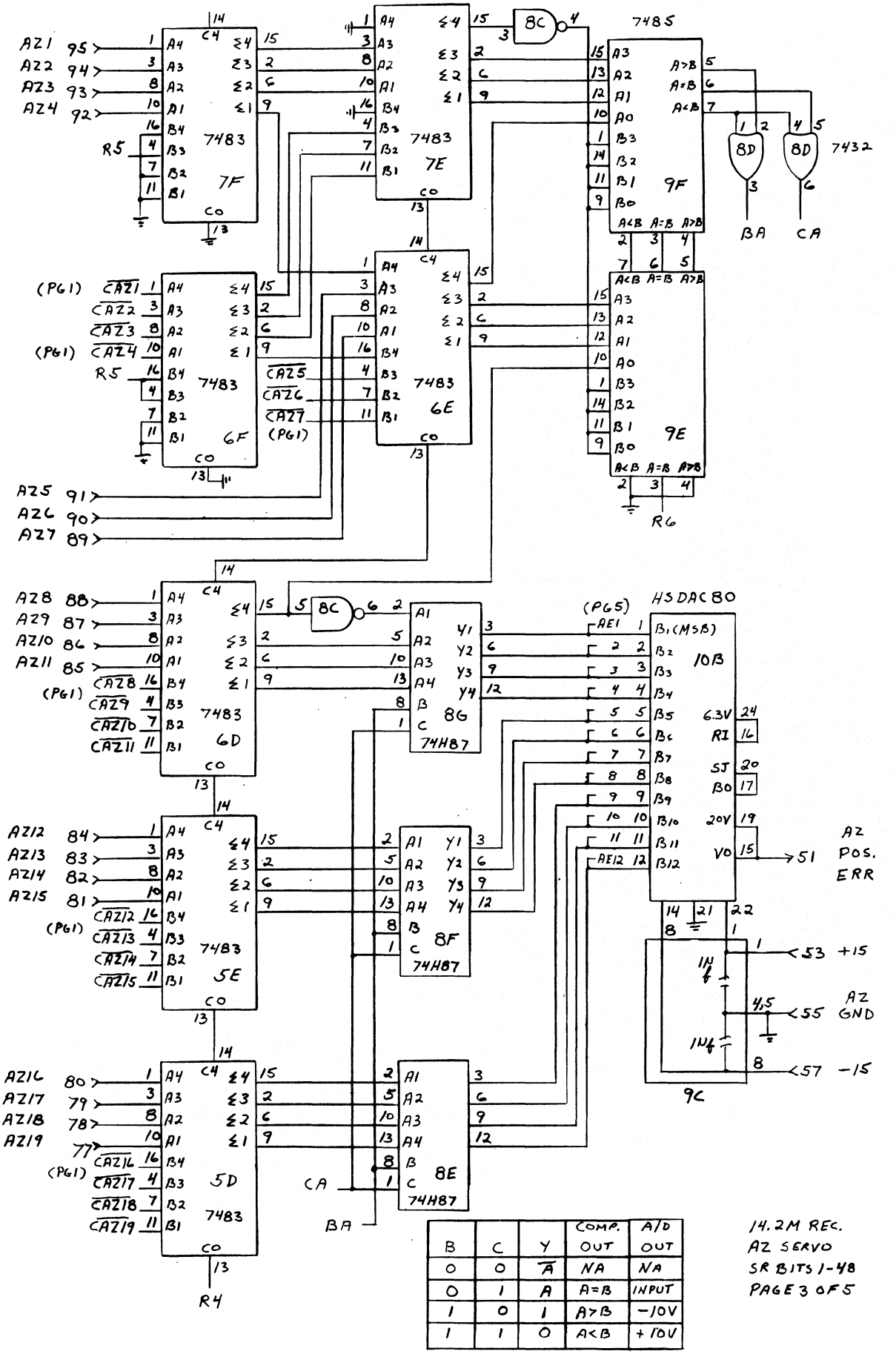
14.2 M RECEIVE
MICRO BUS
BITS 49-80
PAGE 2 OF 2



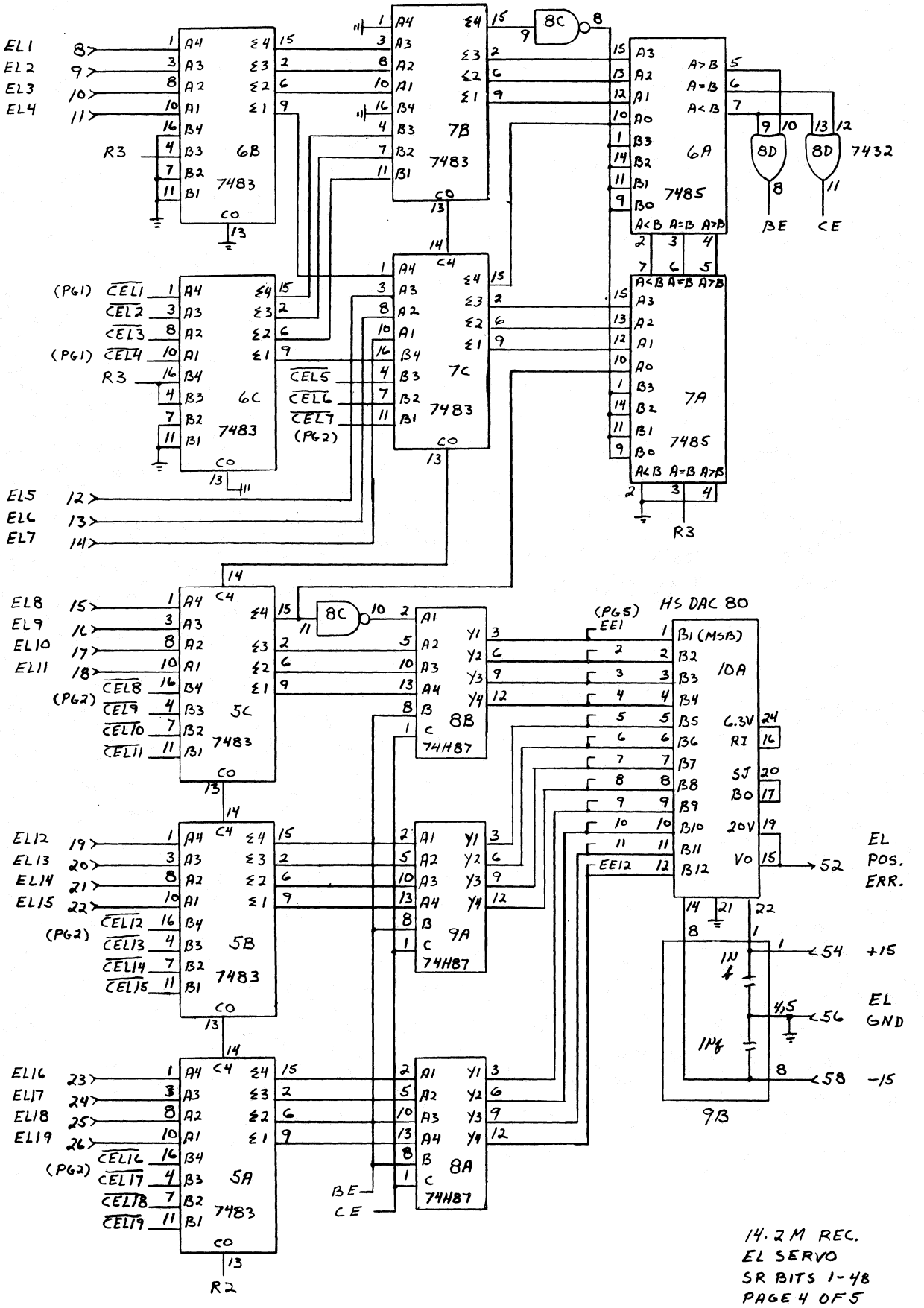
14.2 M REC.
AZ
SR BITS 1-48
PAGE 1 OF 5

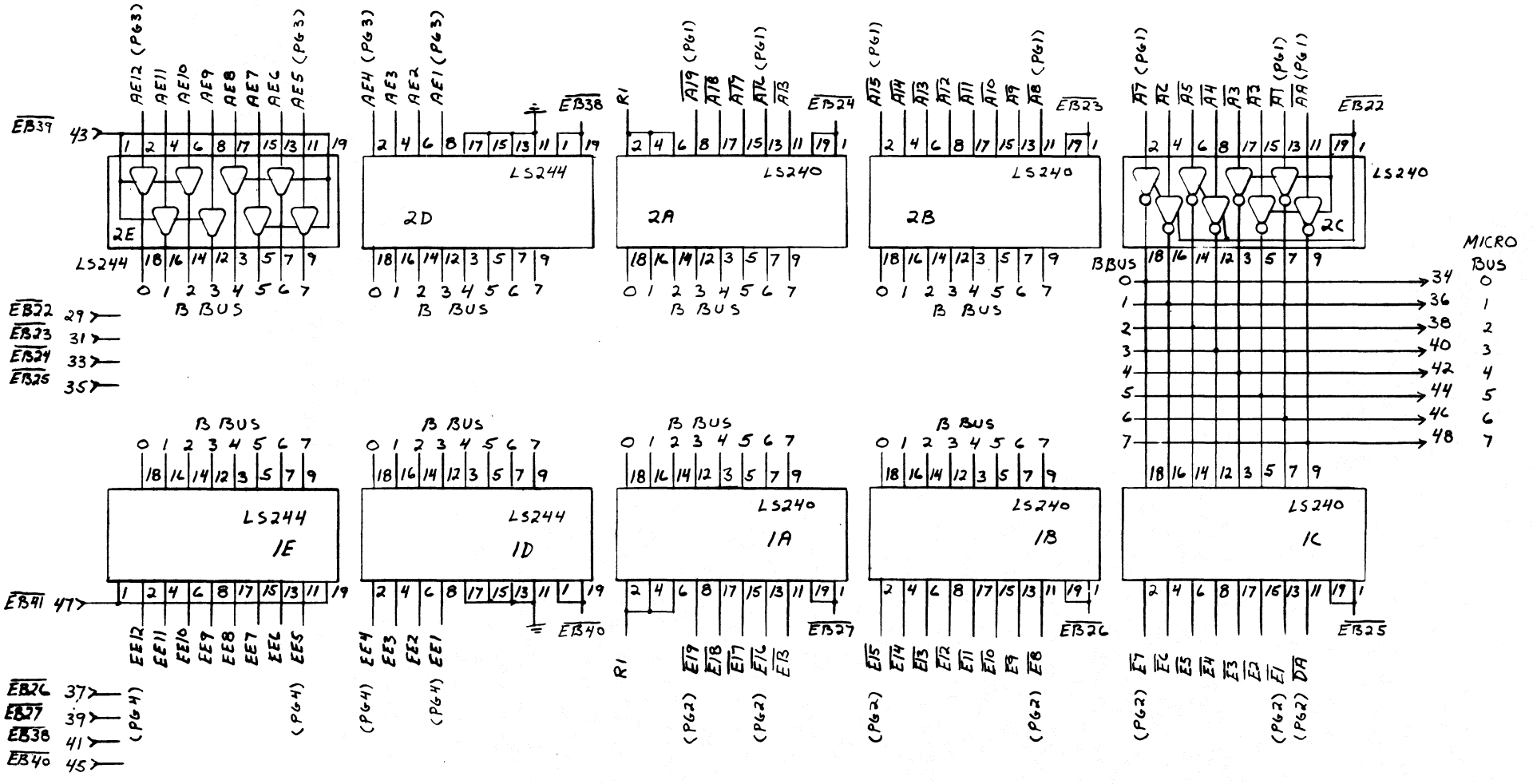


14.2 M REC.
EL
SR BITS 1-48
PAGE 2 OF 5



B	C	Y	COMP. OUT	A/D OUT
0	0	$\overline{A}$	NA	NA
0	1	A	A=B	INPUT
1	0	1	A>B	−10V
1	1	0	A<B	+10V


EL1
EL2
EL3
EL4
R3
6B
7483
7B
7483
8C
7432
8D
8D
BE
CE
6A
7485
7A
7485
R3
(PG1)
CEL1
CEL2
CEL3
(PG1)
CEL4
6C
7483
7C
7483
CEL5
CEL6
CEL7
(PG2)
EL5
EL6
EL7
EL8
EL9
EL10
EL11
(PG2)
CEL8
CEL9
CEL10
CEL11
5C
7483
8C
8B
74H87
(PG5)
EE1
EE12
HS DAC 80
10A
6.3V
RI
SJ
BO
20V
VO
52
EL POS. ERR.
54
+15
56
EL GND
58
-15
1N
1µf
9B
EL12
EL13
EL14
EL15
(PG2)
CEL12
CEL13
CEL14
CEL15
5B
7483
9A
74H87
EL16
EL17
EL18
EL19
(PG2)
CEL16
CEL17
CEL18
CEL19
5A
7483
8A
74H87
BE
CE
R2
14.2M REC.
EL SERVO
SR BITS 1-48
PAGE 4 OF 5


LS244
LS240
2D
2A
2B
2C
2E
1E
1D
1A
1B
1C
B BUS
BBUS
MICRO BUS
14.2 M REC
MICRO BUS
SR BITS 1-48
PAGE 5 OF 5