NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 246

FRONT-END DATA LINK
USERS' MANUAL

Richard J. Lacasse

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FRONT-END DATA LINK USERS' MANUAL
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FRONT END DATA LINK USERS' MANUAL

Richard J. Lacasse

1.0 Introduction

This manual is intended to supplement Electronics Division Internal Report No. 239, FRONT-END DATA LINK (FEDAL). It includes sufficient detail for a user to tailor a FEDAL to his application. In particular, the procedure for changing the analog input voltage limits and default initial digital outputs is described in detail. Firmware listings are provided, along with memory maps and a description of the program flow to provide a basis for custom user firmware. Also, test documents for each card and the chassis are included. Finally, FEDAL chassis wiring is specified. The user should become somewhat familiar with EDIR No. 239 before trying to understand the details below.

2.0 System Firmware

This section details the program flow for the V1.0-RJL FEDAL firmware. A memory map is included as an aid to custom programming. Finally, firmware listings are included.

2.1 Program Flow

Four programs control the FEDAL. The first of these, INIT, is normally entered following power-on. It is followed by MAIN, and MAIN may be interrupted by LINT or UACINT.

The INIT program initializes FEDAL analog outputs to 0 V and digital outputs to default values specified in ROM. It then tests the RAM, ROM, and ACIA's, setting status bits, if appropriate. Finally, it initializes the RAM and ACIA's, enables interrupts, and jumps to MAIN.
MAIN simply calls a number of subroutines to accomplish the following tasks: pulsing the auto-reset circuit and monitoring the link data lines (LPMON), acquiring, testing, and transmitting data (SYNCTR, ANACTR, DIGINT, ENDTR), and displaying received data (DISPLY). The MAIN program loops indefinitely until interrupted.

The LINT program is entered whenever the link ACIA interrupts the microprocessor to signal that a data byte has been received. LINT accepts and, if necessary, stores the byte. It keeps track of where in the data frame it is, and calculates a check-sum to compare with the transmitted one. Upon detection of a complete, good data frame it updates the dedicated user outputs.

The UACINT program is entered by interrupt whenever the user ACIA receives a byte. Since no user interface is defined, the program simply resets the interrupt request by reading from the ACIA. This program is included to provide a "hook" for a custom user program.

3.0 Memory Map

The FEDAL address space is divided as shown in Table 1. The reason certain devices, like the LINK ACIA, occupy a large address space is that only the five most significant address bits are decoded to select these devices. Detailed RAM and ROM maps are shown in Tables 2 and 3, respectively.
TABLE 1
Front-End Data Link Address Space

<table>
<thead>
<tr>
<th>Device</th>
<th>Address (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM</td>
<td>0000 to 03FF</td>
<td></td>
</tr>
<tr>
<td>AUTORESET</td>
<td>10XX</td>
<td></td>
</tr>
<tr>
<td>LINKACIA</td>
<td>18XX</td>
<td>00 - Control &amp; Status Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 - R/W Data Buf</td>
</tr>
<tr>
<td>OISWITCH</td>
<td>20XX</td>
<td>Link Input MUX Control</td>
</tr>
<tr>
<td>UACIA</td>
<td>28XX</td>
<td>00 -- Control &amp; Status Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 -- R/W Data Buf</td>
</tr>
<tr>
<td>ANALOG INPUT BOARD</td>
<td>48XX</td>
<td>00 -- MUX Latch</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 -- Start Convert</td>
</tr>
<tr>
<td></td>
<td></td>
<td>02 -- Status &amp; 4 MSB's (+ 2 Monitors)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>03 -- 8 LSB's</td>
</tr>
<tr>
<td>ANALOG OUTPUT SLOT 3</td>
<td>5000 :</td>
<td>MSB0</td>
</tr>
<tr>
<td></td>
<td>5001 :</td>
<td>LSN-0, MSN-1</td>
</tr>
<tr>
<td></td>
<td>5002 :</td>
<td>LSB1</td>
</tr>
<tr>
<td></td>
<td>5003 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5004 :</td>
<td>Analog Out 2 &amp; 3</td>
</tr>
<tr>
<td></td>
<td>5005 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5006 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5007 :</td>
<td>Analog Out 4 &amp; 5</td>
</tr>
<tr>
<td></td>
<td>5008 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5009 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>500A :</td>
<td>Analog Out 6 &amp; 7</td>
</tr>
<tr>
<td></td>
<td>500B :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>500C :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>500D :</td>
<td>Analog Out 8 &amp; 9</td>
</tr>
<tr>
<td></td>
<td>500E :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>500F :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5010 :</td>
<td>Analog Out 10 &amp; 11</td>
</tr>
<tr>
<td></td>
<td>5011 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5012 :</td>
<td>Digital Outputs 0 to 7</td>
</tr>
<tr>
<td></td>
<td>5013 :</td>
<td>Digital Outputs 8 to 15</td>
</tr>
</tbody>
</table>
Table 1 - Page 2

<table>
<thead>
<tr>
<th>Device</th>
<th>Address (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG OUTPUT SLOT 4</td>
<td>5800 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 :</td>
<td>Analog Output 12 &amp; 13</td>
</tr>
<tr>
<td></td>
<td>02 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>03 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>04 :</td>
<td>Analog Output 14 &amp; 15</td>
</tr>
<tr>
<td></td>
<td>05 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>06 :</td>
<td>Analog Output 16 &amp; 17</td>
</tr>
<tr>
<td></td>
<td>07 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>08 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>09 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0A :</td>
<td>Analog Output 18 &amp; 19</td>
</tr>
<tr>
<td></td>
<td>0B :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0C :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0D :</td>
<td>Analog Output 20 &amp; 21</td>
</tr>
<tr>
<td></td>
<td>0E :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0F :</td>
<td>Analog Output 22 &amp; 23</td>
</tr>
<tr>
<td></td>
<td>10 :</td>
<td>Digital Output 16 to 23</td>
</tr>
<tr>
<td></td>
<td>11 :</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12 :</td>
<td>Digital Output 24 to 31</td>
</tr>
</tbody>
</table>

<p>| ANALOG OUTPUT SLOT 5 | 6000 :        |                                          |
|                      | 01 :          | Analog Output 24 &amp; 25                     |
|                      | 02 :          |                                          |
|                      | 03 :          |                                          |
|                      | 04 :          | Analog Output 26 &amp; 27                     |
|                      | 05 :          |                                          |
|                      | 06 :          | Analog Output 28 &amp; 29                     |
|                      | 07 :          |                                          |
|                      | 08 :          |                                          |
|                      | 09 :          | Analog Output 30 &amp; 31                     |
|                      | 0A :          |                                          |
|                      | 0B :          |                                          |
|                      | 0C :          | Analog Output Monitor                     |
|                      | 0D :          | 0 &amp; 1 (Front Panel)                       |
|                      | 0E :          |                                          |
|                      | 0F :          | Analog Output Monitor                     |
|                      | 10 :          | 2 &amp; 3 (Rear Panel)                        |
|                      | 11 :          |                                          |
|                      | 12 :          | Internal Control Bits and Spares          |
|                      | 13 :          |                                          |</p>
<table>
<thead>
<tr>
<th>Device</th>
<th>Address (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOCAL DISPLAY (FRONT PANEL)</td>
<td>68XX</td>
<td>Local Display Latch</td>
</tr>
<tr>
<td>REMOTE DISPLAY (FRONT PANEL)</td>
<td>70XX</td>
<td>Remote Display Latch</td>
</tr>
<tr>
<td>DIGISWITCH 0</td>
<td>80XX</td>
<td>Controls AN.MON 0, Front Panel DVM</td>
</tr>
<tr>
<td>1</td>
<td>88XX</td>
<td>Controls AN.MON 1, Front Panel AVM</td>
</tr>
<tr>
<td>2</td>
<td>90XX</td>
<td>Controls AN.MON 2, User Monitor</td>
</tr>
<tr>
<td>3</td>
<td>98XX</td>
<td>Controls AN.MON 3, User Monitor</td>
</tr>
<tr>
<td>4</td>
<td>A0XX</td>
<td>MSB used to select limit or Digital Outputs</td>
</tr>
<tr>
<td>5</td>
<td>A8XX</td>
<td>Spare</td>
</tr>
<tr>
<td>TOGGLE SWITCH 0</td>
<td>B000</td>
<td>Digital Inputs 0 - 7</td>
</tr>
<tr>
<td>1</td>
<td>B001</td>
<td>Digital Inputs 8 - 15</td>
</tr>
<tr>
<td>2</td>
<td>B002</td>
<td>Digital Inputs 16 - 23</td>
</tr>
<tr>
<td>3</td>
<td>B003</td>
<td>Digital Inputs 24 - 31</td>
</tr>
<tr>
<td>ROM</td>
<td>F000 to FFFF</td>
<td></td>
</tr>
</tbody>
</table>
## TABLE 2

Memory (RAM) Detail
(Addr 0000 to 03FF)

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Spare</td>
<td></td>
</tr>
<tr>
<td>000F</td>
<td>Spare</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td>NIRTL</td>
<td>CH 0-7 One bit for each analog input channel.</td>
</tr>
<tr>
<td>0011</td>
<td>CH 8-15</td>
<td></td>
</tr>
<tr>
<td>0012</td>
<td>CH 16-23</td>
<td>A &quot;1&quot; means not in range specified.</td>
</tr>
<tr>
<td>0013</td>
<td>CH 24-31</td>
<td></td>
</tr>
<tr>
<td>0014</td>
<td>SPARE</td>
<td>Counter for Analog MUX.</td>
</tr>
<tr>
<td>0015</td>
<td>MUXCT</td>
<td></td>
</tr>
<tr>
<td>0016</td>
<td>SPARE</td>
<td>Local Status Word.</td>
</tr>
<tr>
<td>0017</td>
<td>STATUS</td>
<td></td>
</tr>
<tr>
<td>0018</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>0019</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>001A</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>001B</td>
<td>SYMOCT</td>
<td>LINT Sync Mode (Init. to 2).</td>
</tr>
<tr>
<td>001C</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>001D</td>
<td>HDRCT</td>
<td>LINT Header Byte Count</td>
</tr>
<tr>
<td>001E</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>001F</td>
<td>BYTECT</td>
<td>LINT Data Byte Count.</td>
</tr>
<tr>
<td>0020</td>
<td>RBUF0</td>
<td>A buffer for received data.</td>
</tr>
<tr>
<td>0021</td>
<td></td>
<td>(Approx. 16 spare locations.)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>006F</td>
<td>RBUF0</td>
<td>A second buffer for received data.</td>
</tr>
<tr>
<td>0070</td>
<td>RBUF1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00BF</td>
<td>RBUF1</td>
<td>Flag to select one of above buffers.</td>
</tr>
<tr>
<td>00C0</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>00C1</td>
<td>RBUFSE</td>
<td></td>
</tr>
<tr>
<td>00C2</td>
<td>SPARE</td>
<td>Computed CRC.</td>
</tr>
<tr>
<td>00C3</td>
<td>CRCCOM</td>
<td></td>
</tr>
<tr>
<td>00C4</td>
<td>SPARE</td>
<td>Bad frame counter.</td>
</tr>
<tr>
<td>00C5</td>
<td>BFRACT</td>
<td>&quot;FRAME READY&quot; flag.</td>
</tr>
<tr>
<td>00C6</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>00C7</td>
<td>FRRDY</td>
<td></td>
</tr>
<tr>
<td>00C8</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>00C9</td>
<td>REMSTA</td>
<td>Remote Status.</td>
</tr>
<tr>
<td>00CA</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>00CB</td>
<td>FSYNOK</td>
<td>First Sync OK.</td>
</tr>
<tr>
<td>00CC</td>
<td>SPARE</td>
<td></td>
</tr>
<tr>
<td>00CD</td>
<td>BSYNCT</td>
<td>Bad sync word ctr.</td>
</tr>
<tr>
<td>00CE</td>
<td>SPARE</td>
<td></td>
</tr>
</tbody>
</table>
Table 2 - Page 2

<table>
<thead>
<tr>
<th>Address</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00CF</td>
<td>ATEMP1</td>
</tr>
<tr>
<td>00D0</td>
<td>TIPLUS</td>
</tr>
<tr>
<td>00D1</td>
<td>CRCLOC</td>
</tr>
<tr>
<td>00D2</td>
<td>SPARE</td>
</tr>
<tr>
<td>00D3</td>
<td>LCOMER</td>
</tr>
<tr>
<td>00D4</td>
<td>SPARE</td>
</tr>
<tr>
<td>00D5</td>
<td>BLKDIS</td>
</tr>
<tr>
<td>00D6</td>
<td>SPARE</td>
</tr>
<tr>
<td>00D7</td>
<td>RCVDGD</td>
</tr>
<tr>
<td>00D8</td>
<td>SPARE</td>
</tr>
<tr>
<td>00D9</td>
<td>FROUT</td>
</tr>
<tr>
<td>00DA</td>
<td>SPARE</td>
</tr>
<tr>
<td>00DB</td>
<td>CHANI</td>
</tr>
<tr>
<td>00DC</td>
<td>SPARE</td>
</tr>
<tr>
<td>00DD</td>
<td>CH1NEXT</td>
</tr>
<tr>
<td>00DF</td>
<td>SPARE</td>
</tr>
<tr>
<td>00E1</td>
<td>CH0GD</td>
</tr>
<tr>
<td>00E2</td>
<td>CH0TST</td>
</tr>
<tr>
<td>00E3</td>
<td>CH1GD</td>
</tr>
<tr>
<td>00E4</td>
<td>CH1TST</td>
</tr>
<tr>
<td>00E5</td>
<td>SPARE</td>
</tr>
<tr>
<td>02FF</td>
<td>SPARE</td>
</tr>
<tr>
<td>0300</td>
<td>STACK</td>
</tr>
<tr>
<td>03FF</td>
<td>STACK</td>
</tr>
</tbody>
</table>
TABLE 3

ROM Memory Map

<table>
<thead>
<tr>
<th>Address</th>
<th>From</th>
<th>To</th>
<th>Routine or Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>F000</td>
<td>F131</td>
<td></td>
<td>INIT</td>
</tr>
<tr>
<td>F140</td>
<td>F153</td>
<td></td>
<td>MAIN</td>
</tr>
<tr>
<td>F170</td>
<td>F18A</td>
<td></td>
<td>DSWRD</td>
</tr>
<tr>
<td>F300</td>
<td>F303</td>
<td></td>
<td>UACINT</td>
</tr>
<tr>
<td>F500</td>
<td>F5AC</td>
<td></td>
<td>ANACTR</td>
</tr>
<tr>
<td>F7FD</td>
<td></td>
<td></td>
<td>CHECK SUM ADJUST WORD FOR 6A ROM.</td>
</tr>
<tr>
<td>F7FE</td>
<td>F7FF</td>
<td></td>
<td>6A ROM CHECK SUM.</td>
</tr>
<tr>
<td>F800</td>
<td>F87F</td>
<td></td>
<td>ANALOG LIMIT TABLE.</td>
</tr>
<tr>
<td>F880</td>
<td></td>
<td></td>
<td>CHECK SUM ADJUST WORD FOR 10A ROM.</td>
</tr>
<tr>
<td>F881</td>
<td>F882</td>
<td></td>
<td>10A ROM CHECK SUM.</td>
</tr>
<tr>
<td>F888</td>
<td>F88D</td>
<td></td>
<td>INITIAL DIGITAL OUTPUTS.</td>
</tr>
<tr>
<td>F890</td>
<td>F8CD</td>
<td></td>
<td>LIMCK</td>
</tr>
<tr>
<td>F8E0</td>
<td>F906</td>
<td></td>
<td>CONVRT</td>
</tr>
<tr>
<td>F910</td>
<td>FA39</td>
<td></td>
<td>LINT</td>
</tr>
<tr>
<td>FAE0</td>
<td>FAF8</td>
<td></td>
<td>LIMSET</td>
</tr>
<tr>
<td>FB00</td>
<td>FB1E</td>
<td></td>
<td>LXMIT</td>
</tr>
<tr>
<td>FB30</td>
<td>FB38</td>
<td></td>
<td>SYNCTR</td>
</tr>
<tr>
<td>FB40</td>
<td>FB53</td>
<td></td>
<td>DIGNIT</td>
</tr>
<tr>
<td>FB58</td>
<td>FB7F</td>
<td></td>
<td>ENDTR</td>
</tr>
<tr>
<td>FB88</td>
<td>FBCA</td>
<td></td>
<td>GET2</td>
</tr>
<tr>
<td>FCE0</td>
<td>FD99</td>
<td></td>
<td>DISPPLY</td>
</tr>
<tr>
<td>FDE0</td>
<td>FDE7</td>
<td></td>
<td>AOUT</td>
</tr>
<tr>
<td>FDF0</td>
<td>FE24</td>
<td></td>
<td>UPDATE</td>
</tr>
<tr>
<td>FE60</td>
<td>FF16</td>
<td></td>
<td>LPMON</td>
</tr>
<tr>
<td>FFF0</td>
<td>FFFF</td>
<td></td>
<td>INTERRUPT VECTORS</td>
</tr>
</tbody>
</table>
4.0 Data Communication Format

Table 4 depicts the format of the data stream on the link. The number of data bytes in the frame can be changed; however, the byte count (Byte #3) should be changed to reflect this. The LINT subroutine uses the byte count in accepting data, and so is flexible; however, certain programs that pick data out of the received frame and others which generate the frame are not so general. Care must be taken if changing the number or significance of the data bytes to change all affected subroutines.

TABLE 4

Data Communication Format

<table>
<thead>
<tr>
<th>Byte #</th>
<th>Contents (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7E</td>
<td>1st SYNC WORD</td>
</tr>
<tr>
<td>1</td>
<td>7E</td>
<td>2nd SYNC WORD</td>
</tr>
<tr>
<td>2</td>
<td>XX</td>
<td>STATUS</td>
</tr>
<tr>
<td>3</td>
<td>3B</td>
<td># OF BYTES/FRAME (HEX) OF DATA</td>
</tr>
<tr>
<td>4</td>
<td>XX</td>
<td>ANOUT 0-1 (TRANSMITTED ANALOG VOLTAGES)</td>
</tr>
<tr>
<td>5</td>
<td>XX</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>XX</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>.</td>
<td>ANOUT 2-3</td>
</tr>
<tr>
<td>8</td>
<td>.</td>
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</tr>
<tr>
<td>9</td>
<td>.</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>ANOUT 4-5</td>
</tr>
<tr>
<td>B</td>
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<tr>
<td>E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
<td>ANOUT 8-9</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>ANOUT 10-11</td>
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</table>
Table 4 - Page 2

<table>
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<tr>
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<th>Description</th>
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<tr>
<td>14</td>
<td>ANOUT 12-13</td>
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<tr>
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<tr>
<td>16</td>
<td>ANOUT 14-15</td>
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<tr>
<td>17</td>
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<tr>
<td>18</td>
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<td>19</td>
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<td>1A</td>
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<td></td>
</tr>
<tr>
<td>1D</td>
<td></td>
</tr>
<tr>
<td>1E</td>
<td></td>
</tr>
<tr>
<td>1F</td>
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<tr>
<td>20</td>
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<td>21</td>
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<td>28</td>
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<tr>
<td>29</td>
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<tr>
<td>2A</td>
<td>ANOUT 20-21</td>
</tr>
<tr>
<td>2B</td>
<td></td>
</tr>
<tr>
<td>1C</td>
<td></td>
</tr>
<tr>
<td>2D</td>
<td></td>
</tr>
<tr>
<td>2E</td>
<td>ANOUT 22-23</td>
</tr>
<tr>
<td>2F</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>XX DIGOUT MSB (TRANSMITTED DIGITAL INFO)</td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
</tr>
<tr>
<td>3A</td>
<td></td>
</tr>
<tr>
<td>3B</td>
<td></td>
</tr>
<tr>
<td>3C</td>
<td></td>
</tr>
<tr>
<td>3D</td>
<td></td>
</tr>
<tr>
<td>3E</td>
<td>CRC CHECK (Sum, mod 256, bytes 2 through 3D).</td>
</tr>
</tbody>
</table>
Table 4 - Page 3

Notes:

1. Each byte: 1 START BIT
   8 DATA BITS
   1 STOP BIT

   10 BITS TOTAL

   BIT TIME = 16 us

   "BYTE" TIME = 160 us

   FRAME TIME = 9.920 ms

   (This max data rate will not be met due to time consuming interrupt and acquisition programming.)

2. Two analog voltages, 12 bits each, are formatted into three bytes as follows:

   Byte #

<table>
<thead>
<tr>
<th>M</th>
<th>MSB</th>
<th>ANOUT N</th>
<th>MSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>M + 1</td>
<td>------</td>
<td>LSB</td>
<td>MSB</td>
</tr>
<tr>
<td>M + 2</td>
<td>------</td>
<td>ANOUT N+1</td>
<td>LSB</td>
</tr>
</tbody>
</table>
5.0 Firmware Listings

This section contains listings of all the routines in the V1.0-RJL FEDAL system. Each listing contains a header with a program description, a symbol definition table, and the code with embedded comments. Thus, it is self-documenting. The code is written in American Automation's version of Motorola 6809 Assembly Language.

LISTINGS FOLLOW.
ANACTR SUBROUTINE

FUNCTION: TRANSMITS STATUS, NUMBER OF BYTES, AND 32 ANALOG CHANNELS. CONTROLS THE ACQUISITION OF ANALOG INPUTS.

INPUT: STATUS WORD

OUTPUT: STATUS, NUMBER OF BYTES, AND 32 ANALOG CHANNELS TO LINK UART.

CALLS: LMIT, CONVRT, LIMCK, LIMSET

USES: D, U, X, Y, S-STACK

******************************************************************************

***************SYMBOL DEFINITIONS***************

LIMCK is a subroutine which checks the limits of the analog inputs.

LIMSET is a subroutine which sets a limit bit.

LXMIT is a subroutine which loads data to the link transmit buffer from reg. A.

CONVRT is a subroutine which initiates an A/D conversion and waits for a ready status. A time out by CONVRT is indicated to ANACTR by carry=1.

TEMP1 is a temporary storage location.

MUXCT is used to keep up with the channel to convert

MUXLT is the address of the MUX latch.
0042 A 0000 000400  MUXLT EQU  $400
0043  *
0044 A 0000 00003B  NUMBYT EQU  $3B
0045  *
0047 A 0000 00017  STATUS EQU  $17
0049  *
0050 A 0000 0000D1  CRCLOC EQU  $D1
0052  *
0053 A 0000 00001F  CHMAX EQU  $1F
0055  *
0056  ******************START OF PROGRAM**********************
0057  *
0058  *
0059 A 0000 4F  ANACTR CLRA
0060 A 0001 B74800  STA MUXLT 0 TO MUX LATCH
0061 A 0004 9715  STA MUXCT INIT MUXCT
0062 A 0006 9617  LDA STATUS XMIT STATUS
0063 A 0008 BD00  JSR LXMIT
0064 A 000B 97D1  STA CRCLOC
0065 A 000D 863B  LDA #NUMBYT XMIT NUMBER OF BYTES
0066 A 000F BDF00  JSR LXMIT
0067 A 0012 9BD1  ADDA CRCLOC
0068 A 0014 97D1  STA CRCLOC
0069 A 0016 8E007  LDX #007 WAIT FOR ANALOG SETTLING
0070 A 0019 301F  WAIT0 LEAX -1,X
0071 A 001B 26FC  ENE WAIT0
0072 A 001D BD8E0  CONV0 JSR CONVRT CONVERT 0 CHANNEL
0073 A 0020 20DC  BLT TOUT0 TIMED OUT?
0074 A 0022 4F  CLRA NO:
0075 A 0023 4C  INCA
0076 A 0024 B74800  STA MUXLT INCREMENT MUX LATCH
0077 A 0027 BDF00  JSR LIMCK CHECK LIMITS ON PREVIOUS CONV.
0078 A 002A 0C15  INC MUXCT MUXCT+1 TO MUXCT
0079 A 002C 2011  BRA ACON0 SKIP OVER YES
0080 A 002E 4F  TOUT0 CLRA YES:
0081 A 0032 4C  INCA INCREMENTMUX LATCH
0082 A 0033 B74800  STA MUXLT
0083 A 0033 BDFAE0  JSR LIMSET SET LIMIT BIT
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0034 A 0036 0C15 INC MUXCT
0035 A 0038 8E002 LDX #0002
0036 A 0038 301F WAIT1 LEAX -1,X
0037 A 003D 26FC BNE WAIT1
0038 A 003F 1F30 ACON0 TFR U:D SHIFT CONVERTED WORD
0039 A 0041 58 ASLB
003A A 0042 49 ROLA
003B A 0043 58 ASLB
003C A 0044 49 ROLA
003D A 0045 58 ASLB
003E A 0046 49 ROLA
003F A 0047 58 ASLB
0040 A 0048 49 ROLA
0041 A 0049 D7CF STB TEMP1 KEEP CONVERTED LSB'S
0042 A 004A BF000 JSR LIM SET TRANSMIT A DATA BYTE
0043 A 004E 9BD1 ADDA CRCLOC
0044 A 0050 97D1 STA CRCLOC
0045 A 0052 BDF81 CONV1 JSR CONVRT CONVERT NEXT CHANNEL
0046 A 0055 2000 BLT TOUT1 TIMED OUT?
0047 A 0057 9615 LDA MUXCT NO:
0048 A 0059 4C INC MUXCT
0049 A 005A 9BD1 STA CRCLOC
004A A 005B 97D1 STA MUXCT
004B A 005C 9ACF ORA TEMP1
004C A 005D 9500 JSR LIM SET SET LIMIT BIT
004D A 005E BDF81 TFR U:D UPDATE MUXCT
004E A 0060 0C15 INC MUXCT
004F A 0062 200B BRA ACON1 SKIP 'YES'
0050 A 0064 9615 TOUT1 LDA MUXCT YES:
0051 A 0066 4C INCA UPDATE MUXCT
0052 A 0067 B7480 STA MUXCT
0053 A 0068 0C15 INC MUXCT
0054 A 0069 1F30 ACON1 TFR U:D
0055 A 0071 9ACF ORA TEMP1
0056 A 0073 BDF81 JSR LIM SET TRANSMIT A DATA BYTE
0057 A 0076 9BD1 ADDA CRCLOC
0058 A 0078 97D1 STA CRCLOC
0059 A 007A 1F30 TFR U:D
005A A 007C 1F98 TFR B:A
005B A 007E BDF81 JSR LIM SET TRANSMIT ANOTHER DATA BYTE
005C A 0081 9BD1 ADDA CRCLOC
005D A 0083 97D1 STA CRCLOC
005E A 0085 BDF81 JSR CONVRT CONVERT NEXT CHANNEL
005F A 0088 201D BLT TOUT2 TIMED OUT?
<table>
<thead>
<tr>
<th>Line</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0126</td>
<td>A 008A 9615</td>
</tr>
<tr>
<td>0127</td>
<td>A 008C 4C</td>
</tr>
<tr>
<td>0128</td>
<td>A 008D B74800</td>
</tr>
<tr>
<td>0129</td>
<td>A 0090 811F</td>
</tr>
<tr>
<td>0130</td>
<td>A 0092 2F01</td>
</tr>
<tr>
<td>0131</td>
<td>A 0094 39</td>
</tr>
<tr>
<td>0132</td>
<td>A 0095 BDF899</td>
</tr>
<tr>
<td>0133</td>
<td>A 0098 0C15</td>
</tr>
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<td>0134</td>
<td>A 009A 7E003F</td>
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<tr>
<td>0139</td>
<td>A 00A5 2F01</td>
</tr>
<tr>
<td>0140</td>
<td>A 00A7 39</td>
</tr>
<tr>
<td>0141</td>
<td>A 00A8 BDFAE0</td>
</tr>
<tr>
<td>0142</td>
<td>A 00A9 0C15</td>
</tr>
<tr>
<td>0143</td>
<td>A 00AD 7E003B</td>
</tr>
<tr>
<td>0144</td>
<td>A 00AD 7E003B</td>
</tr>
</tbody>
</table>

LDA MUXCT NO:

STA MUXLT UPDATE MUX LATCH

CMPA #CHMAX SEE IF DONE

BLE ACON2 NO: SKIP

RTS YES: RETURN

ACON2 JSR LIMCK CHECK LIMIT

INC MUXCT MUXCT+1 TO MUXCT

JMP ACON0 LOOP UNTIL DONE

LDA MUXCT YES:

INCA INCREMENT MUX LATCH

STA MUXLT

CMPA #CHMAX SEE IF DONE

BLE ACON0 NO: SKIP

RTS YES: RETURN

ACON3 JSR LIMSET SET LIMIT BIT

INC MUXCT INCREMENT MUXCT

JMP WAIT1 LOOP UNTIL DONE

END
FUNCTION: LOAds D/A LATCHES

INPUT: START ADDR. OF LATCH IN Y
       START ADDR. OF DATA IN X
       NUMBER OF WORDS IN A

OUTPUT: DATA TO LATCHES

USES: A, Y, X

*********************************************************
1014 0001 ***************START OF PROGRAM***************

001 A 0000 EESI AGUT LDV X++ GET DATA FROM TABLE
002 A 0002 EFA1 STU Y++ STORE TO LATCH
003 A 0004 4A DECA
004 A 0005 2AF9 BNE AGUT LOOP UNTIL DONE
005 A 0007 39 RTS
006 END
CONVERT SUBROUTINE

FUNCTION: GETS THE ADC TO PERFORM A CONVERSION. TIMES OUT IN ABOUT 90 MICROSEC. IF ADC IS NOT READY, UPDATES THE ADC STATUS BIT IN THE STATUS WORD.

INPUT:NONE
OUTPUT: ADC OUTPUT MASKED TO 12 BITS IN D0; UPDATED STATUS WORD.
USES: D0

****************************************************************

ADCST EQU $4801
ABCOUT cf.!!! $4802
STATUS

RonVRT STA ADCST START CONVERT
LDA triF; ZERO STATUS BIT
ANDA STATUS
STA STATUS
LDU #03 SET. UP WAIT LOOP
WAITC LEAU -1,U WAIT
CMPU moo BLE TOUTC BRANCH IF TIMED OUT
LDD ADCOUT GET ADC WORD
BGE WAITC 0 MSBIT MEANS NOT READY
ANDA #$0F MASK OUT TO 12 BITS
TFR D0 U PUT RESULT IN U
RTS FLAG TIME-OUT TO CALLER

END

****************************************************************
* DIGINT SUBROUTINE

* FUNCTION: ACQUIRES AND TRANSMITS DIGITAL INPUTS

* INPUTS: 32 BITS FROM USER

* OUTPUTS: BITS TO LINK UART

* USES: A,Y:LIMIT

*******************************************************************************

*******************************************************************************

* LIMIT, A SUBROUTINE, INTERFACES WITH LINK UART

LIMIT EQU $FB00

*******************************************************************************

*******************************************************************************

********** Symbol Definition **********

****************************************************************************

TSAI INIT Y REG

*******************************************************************************

*******************************************************************************

********** Start of Program **********

*******************************************************************************
DISPLAY SUBROUTINE

FUNCTION: HANDLES FRONT PANEL AND USER ANALOG
MONITOR DISPLAY.

INPUT: FRONT PANEL ROTARY SWITCH,
FRONT PANEL AND USER DIGISWITCHES

OUTPUT: FRONT PANEL AND USER DISPLAYS

USES: D:LIN7,SET2,GSWRD

**SYMBOL DEFINITION**

SELW IS THE ADDR. OF THE FRONT PANEL ROTARY SEL. S4.

SELW EQU $E000

LSTEP IS THE LOCAL RESET ERROR COUNTER

LSTEP EQU $D000

LATCH IS THE LOCAL LED DISPLAY LATCH

LATCH EQU $C000

RLATCH IS THE REMOTE LED DISPLAY LATCH

RLATCH EQU $B000

RSTER0 IS THE ADDRESS OF THE RESET ERROR IN RBUF0

RSTER0 EQU $A9

RSTER1 IS THE ADDRESS OF THE RESET ERROR IN RBUF1

RSTER1 EQU $A0

RBUFSE IS THE DATA BUF POINTER

RBUFSE EQU $C1

LCOMER IS THE LOCALLY DETECTED COMMUNICATION ERROR COUNT

LCOMER EQU $D3
*COMER0 IS THE RBUF0 ADDR. OF COMM. ERROR
COMER0 EQU $58

*COMER1 IS THE RBUF1 ADDR. OF COMM. ERROR
COMER1 EQU $68

*STATUS IS THE LOCAL STATUS WORD
STATUS EQU $17

*REMTA IS THE REMOTE STATUS WORD
REMTA EQU $69

*BLKDIS IS USED TO KEEP UP WITH DISPLAY BLANKING

* BIT 0 IS USED TO BLANK THE FRONT PANEL DVM

* BIT 1 IS USED TO BLANK THE REMOTE LED STATUS DISPLAY

* THE DVM DISPLAY IS BLINKED WHEN BIT=0

* THE LED DISPLAY IS BLANKED WHEN BIT=1

*RBUF0 IS THE FIRST ADDRESS IN A RECEIVED REMOTE

* DATA BUFFER

*RBUF1 IS THE FIRST ADDRESS IN A RECEIVED REMOTE

* DATA BUFFER

*DSW0 IS THE ADDRESS OF THE FRONT PANEL DIGISWITCH

* ASSOCIATED WITH THE FRONT PANEL DVM

*DSW0 EQU $8000

*DSW2 IS THE ADDRESS OF THE USER DIGISWITCH ASSOCIATED

* WITH DSW2 ENABLE

* THE LSB OF ANOUT 2-8 AND

* THE MSB OF ANOUT 2-9

A029 EQU $600D
*AOCB IS THE LATCH CONTAINING THE MSB OF ANOUT 2-8
AO2E EQU $600C
*
*AO2B IS THE LATCH CONTAINING THE LSB OF ANOUT 2-10 AND
THE MSB OF ANOUT 2-11
A02B EQU $6010
*
*A02A IS THE LATCH CONTAINING THE MSB OF ANOUT 2-10
A02A EQU $600F
*
RCVDGD FLAGS THE FIRST GOOD DATA FRAME
RCVDGD EQU $17
*
GET2 IS A SUBROUTINE WHICH GETS TWO ANALOG VOLTAGES
GET2 EQU $F888
*
LIMOFF IS THE OFFSET OF THE LIMIT WORD IN THE
DATA TABLES.
LIMOFF EQU $34
*
TEMP1 IS A TEMPORARY STORAGE LOCATION
TEMP1 EQU $0F
*
DSWRD IS A SUBROUTINE WHICH RETURNS THE BINARY
VALUE OF THE DISISWITCH REQUESTED BY THE X REGISTER
DSWRD EQU $F170
*
**********************START OF PROGRAM**********************************
*
DISPLAY LDA #03 READ ROTARY SEL. SW.

ANDA SELSW
BEQ DISSIA DISPLAY STATUS IF = 0
LSRA
BEQ DISCOM DISPLAY COMERR IF = 1
STA LLATCH
TST RCVDGD ANY REMOTE DATA RECEIVED?
BEQ BLANKR IF NOT GO BLANK REMOTE DISP.
LDA #RSTER0 IS SO FIND AND DISPLAY RSTER0
A 0019 7608
A 001F 8EO3A9
A 001E A68A
A 0010 B7000
A 0023 263A
A 0045 9433
A 0027 B75000
A 002A 0007
A 0020 2721
A 0026 8E0058
A 0031 0D11
A 0033 2603
A 0035 8E0068
A 003A B77000
A 003D 291A
A 003F 7517
A 0041 B75000
A 0044 0007
A 0048 2757
A 0049 9F09
A 0044 B77000
A 0047 260A
A 004F 2603
A 004F 9405
A 0055 9705
A 0055 B75012
A 0058 3939
A 0059 36FD
A 005A 9415
A 005B 9705
A 005F B76012
A 0062 106E0010
A 0065 0011
A 0068 B704
A 006A 106E0076
A 006F 18F00CF
A 0071 9E8000
A 0074 BDF170
A 0077 1F89
A 0077 44
A 0084 2643
A 0085 9A05
A 0086 9705
A 0087 9705
A 008F 9415
A 0091 9705
A 0095 9705
A 009F 9415
A 00A0 106E0076
A 00A5 18F00CF
A 00A7 9E8000
A 00AA BDF170
A 00AA 1F89
A 00B7 44
BNE LOAD1
LDX #STER1
LOAD! LDA 0x
STA LATCH
BRA CONTI
DISCOM LDA LCOMER DISPLAY LOCAL COMM. ERR.
STA LATCH
LDA ROVDGD ANY REMOTE DATA RECEIVED?
BEO BLANKR IF NOT GO BLANK REMOTE DISPLAY
LDA #COMER0
TST RBUFSE IF SO FIND AND DISPLAY REMOTE COM. ERR.
BNE LOAD:
LDX #COMER1
LOAD2 LDA 0x
STA LATCH
BRA CONTI
DISSTA LDA STATUS DISPLAY STATUS
STA LATCH
TST ROVDGD
BEO BLANKR SEE IF ANY REMOTE DATA RECEIVED
LDA REMSTA IF SO DISPLAY
STA RATCH
BRA CONTI
* IF NOT, BLANK REMOTE DISPLAY AND UNBLINK DVM
BLANK R LDA 06
ORA BLKDID
STA BLKDID
STA DOUT4
RTS
CONTI LDA #FD UNBLANK DISPLAY
ANDA BLKDID
STA BLKDID
STA DOUT4
CONT3 LDV #RBUF0 TABLE ADDR. TO Y
TST RBUFSE
BNE CONT4
LDV #RBUF1
CONT4 STY TEMP1 SAVE RBUF VAL FOR LATER
LDX #DOW0 DSW ADDR TO X
JSR DSWRD GET SW VALUE IN BINARY
CONT6 TFR A B FIND LIMIT BIT
LSRA
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0168 A 0074 44 LSRA
0169 A 0074 44 LSRA
0170 A 0070 5E 34 ADDA #LIMOFF
0171 A 007E 01 66 LEAY A,Y ADDR. OF LIM WORD TO Y
0172 A 0080 04 07 ANDB #7 FIND THE BIT WITHIN THE WORD
0173 A 0082 5C INCB
0174 A 0083 4F CLRA
0175 A 0034 1A 01 ORCC #1
0176 A 0086 46 LOOP1 RGRA
0177 A 0087 5A DECB
0178 A 0088 2B 6C BNE LOOP1 LOOP TO POSITION BIT
0179 A 008A 05 44 BITA 0,Y
0180 A 008C 27 66 BEQ OK1 BRANCH IF WITHIN LIMITS
0181 A 008E 86 FE TOORIE LDA #FE
0182 A 0090 9A 05 ANDA BLKD15 OUT OF RANGE, BLINK DVM
0183 A 0092 0A 04 BRA CONT7
0184 A 0094 36 01 OK1 LDA #01 IN RANGE, DON'T BLINK DVM
0185 A 0096 9A 05 ORA BLKD15
0186 A 0098 87 05 CONT7 STA BLKD15
0187 A 009A B7 01 2 STA DOUT4
0188 A 007D 13 4F LDY TEMP1 RETRIEVE RBUF VALUE
0189 A 007F 50 FE 02 JSR GET2
0190 A 0043 FD 00 STD A029 OUTPUT BOTH FRONT PAN. VOLTAGES
0191 A 0045 96 CF LDA TEMP1
0192 A 0048 B7 00 STA A028
0193 A 004B 8E 00 LDX #DSW2 USER DSW ADDR. TO X
0194 A 00AE 0B 08 JSR GET2 GET REQUESTED VOLTAGES
0195 A 0081 FD 01 STD A028 OUTPUT USER MONITOR VOLTAGES
0196 A 0084 96 CF LDA TEMP1
0197 A 0086 B7 00 STA A02A
0198 A 0089 39 RTS
0199 END
**DSWRD 20 Dec 83 PAGE 001**

<table>
<thead>
<tr>
<th>Line</th>
<th>Code</th>
<th>Description</th>
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</tr>
<tr>
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<tr>
<td>0005</td>
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**Symbol Definition**

- TEN is the decimal number ten
- MAXBCD is the highest BCD switch value permitted
- MAXBIN is the highest binary value permitted

**START OF PROGRAM**

```
        DSWRD  LDA  6,X  INPUT DIGISWITCH
        COMA  UNCOMPLEMENT SWITCH
        CMPA  #MAXBCD
        BHI  OUT   RETURN MAX VAL. IF OUT OF RANGE
        TFR  A:B   BCD TO BINARY CONVERT
        ANDA  #$7F  BY SUCCESSIVE ADDITION
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        LSRB  GET   MSG IN B
        BNE  LOOP1
        RTS
        LOOP1  ADA  #$1F  DO SUCCESSIVE ADDS
        DEX
        BNE  LOOP1
        RTS
        LOOP1  ADA  #$1F  DO SUCCESSIVE ADDS
        DEX
        RTS
        LOOP1  ADA  #$1F  DO SUCCESSIVE ADDS
        DEX
        RTS
```

**END**
OW: ENTR SUBROUTINE


INPUT: NITBL, COMMERR, RSTER, CRCLOC

OUTPUT: ABOVE DATA TO LINK. LINK TIMEOUT CAN CHANGE STATUS WORD.

USES: A/Y LIMIT

**********************************************************44444***************

**************************************************

***********END of SYMBOL DEFINITION*********************

* NITBL IS THE ADDRESS OF THE FIRST ENTRY IN A 4 BYTE TABLE CONTAINING ANALOG LIMIT BITS.

NITBL EQU #10

* NIREND IS THE ADDRESS IF THE LAST ENTRY IN THIS TABLE

NIREND EQU #13

* LOCER IS USED TO COUNT COMMUNICATION ERRORS

LOCER EQU #13

* RSTER IS A HARDWARE COUNTER TO COUNT RESTART ERRORS

RSTER EQU #$3000

* CRCLOC IS THE LOCALLY GENERATED TRANSMIT CRC

CRCLOC EQU #$D1

* LIMIT IS THE LINK TRANSMIT SUBROUTINE

LIMIT EQU #$FB00

 ********************************************START OF PROGRAM********************************************
884:
0043 A 0000 18E0010 * ENTR
0044 A 0004 A6A0 LOUP1
0045 A 0006 BDF800 JSR LMIT XMIT LIMIT WORDS
0046 A 0008 9BD1 ADDA CRLOC UPDATE CRC
0047 A 000B 97D1 STA CRLOC
0048 A 000D 10C0013 CMPY #NIREND DONE?
0049 A 0011 2FF1 BLE LOUP1 NO: LOOP
0050 A 0013 9603 LDA LCOMER YES: CONTINUE
0051 A 0015 E0B00 JSR LMIT XMIT LCOMER
0052 A 0018 9BD1 ADDA CRLOC
0053 A 001A 97D1 STA CRLOC UPDATE CRC
0054 A 001C BAC000 LDA RSTER
0055 A 001F 6FB00 JSR LMIT XMIT RSTER
0056 A 0022 9401 ADDA CRLOC UPDATE CRC
0057 A 0024 BFB00 JSR LMIT XMIT CRC
0058 A 0027 39 RTS
0059 END
**GET2** SUBROUTINE

**FUNCTION:** Reads two consecutive digitswitches and fetches the requested analog voltages.

**INPUT:** Received data table address, in Y:

**DIGISWITCH ADDRESS IN X**

**OUTPUT:** First byte in TEMP1, second and third bytes in O REG.

**USES:** D, X, Y

***END OF SUBROUTINE***

**TEMP1** is a temporary storage location.

**DSWINC** is the increment in address between digitswitches.

**TIPLUS** is a temporary storage location immediately following TEMP1.

**DSWRD** is a subroutine which reads a digitswitch and forces it to #$1F if it is not in the range 00 to 21 decimal.

**DSWRD** EQU #$1F

**START OF PROGRAM**

**GET2** JSP DSWRD READ DIGISWITCH INTO A

**EVENT1** LDB #$03 UNPACK DATA

**RORA** SEE IF EVEN OR ODD

**ANDA** #$F

**ABOVE MASKS IN CASE CARRY WAS SET BEFORE ROTATE**

**AND INSTRUCTION HAS NO EFFECT ON CARRY!**

**ECC** EVEN BRANCH ON EVEN
*THE ABOVE INSTRUCTION PACKS THE DATA FOR OUTPUT

*TO THE DAC'S. FIRST BYTE IS LEFT IN TEMPI. AND

*THE SECOND AND THIRD ARE LEFT IN D
**************AMERICAN AUTOMATION ASSEMBLER**************

0001
0002 * INIT ROUTINE
0003 *                **********FUNCTION: PERFORM SELF-TESTS AND INITIALIZES FEDAL**********
0004 * INPUT: VARIOUS: FROM UNITS TESTED
0005 OUTPUT: VARIOUS: TO UNITS TESTD AND INITIALIZED
0006 CALLS: NONE
0007 CALLED BY: RESER INTERRUPT
0008
0009
0010
0011
0012
0013
0014 **********SYMBOL DEFINITION**********
0015
0016
0017 A 0000 00002800
0018 UACON EDU $2800
0019
0020 A 0000 00002801
0021 UACIA EDU $2801
0022
0023 A 0000 00001800
0024 LACON EDU $1800
0025
0026 A 0000 00001801
0027 LACIA EDU $1801
0028
0029 A 0000 00000000
0030 RAMST EDU $0000
0031
0032 A 0000 00000000
0033 RAMLGT EDU $400
0034
0035 A 0000 00000020
0036 RAMSTA EDU $20
0037
0038 A 0000 00000017
0039 STATUS EDU $17
0040
0041 A 0000 00001000
0042 ROMLGT EDU $1000
0442  * ROMST IS THE ROM START ADD.
0443 A 0000 00000000 ROMST EDU $F000
0445  *
0446  * CRC SUM IS THE STORED ROM CHECK SUM
0447 A 0000 00000000 CRC SUM EDU $9000
0448  *
0449  * ROMSTA IS THE ROM STATUS BIT
0450 A 0000 00000040 ROMSTA EDU $40
0451  *
0452  * ADCT1 IS AN ADC TEST WORD
0453 A 0000 00000000 ADCT1 EDU $30
0454  *
0455  * ADCT2 IS AN ADC TEST WORD
0456 A 0000 00000040 ADCT2 EDU $40
0457  *
0458  * ADCT3 IS AN ADC TEST WORD
0459 A 0000 00000000 ADCT3 EDU $30
0460  *
0461  * MUXL IS THE ADC MUX LATCH
0462 A 0000 00000000 MUXL EDU $4000
0463  *
0464  * ADOUT1 IS THE FIRST ADC BYTE
0465 A 0000 00004002 ADOUT1 EDU $4002
0466  *
0467  * ADOSTA IS THE ADC STATUS BIT
0468 A 0000 00000084 ADOSTA EDU $94
0469  *
0470  * OR IS AN ASCII CARRIAGE RETURN
0471 A 0000 0000004D OR EDU $9D
0472  *
0473  * PROMPT IS AN ASCII >
0474 A 0000 0000003E PROMPT EDU $3E
0475  *
0476  * WAIT1 IS A WAIT COUNT OF ABOUT 81 MILLISECONDS
0477 A 0000 00004000 WAIT1 EDU $4000
0478  *
0479  * WAIT2 IS A WAIT COUNT OF ABOUT 45 MICROSECONDS
0480 A 0000 00000003 WAIT2 EDU $3
0481  *
0482  * UARTST IS THE UART RESET WORD
0483 A 0000 00000017 UARTST EDU $17
ACIAS1 SETS UP THE ACIA FOR:

* 8 BIT, NO PARITY, 1 STOP, NO INTERRUPTS/16

ACIAS1 EQU $15

*TBEMPT MASKS THE TRANSMIT BUF EMPTY BIT ON ACIA'S

TBEMPT EQU $2

*LACSTA IS THE USER ACIA STATUS BIT

LACSTA EQU $8

*LACSTA IS THE LINK ACIA STATUS BIT

LACSTA EQU $48

*SYMCOT IS THE SYNC MODE COUNTER, INIT VALUE =2

SYMCOT EQU $18

*DA0, DA1, DAC AREA THE I/A CARD ADDRESSES

DA0 EQU $500
da1 EQU $580

da2 EQU $600

DALPS IS THE NUMBER OF LOOPS REQ'D IN DAC INIT

DALPS EQU $96

*TOSTAK IS THE INITIAL TOP OF STACK

TOSTAK EQU $0FE

*INTEN SETS LINK ACIA FOR:

INTEN EQU $95

*INTEN SETS USEF ACIA FOR:

INTEN EQU $95

DOFF IS THE OFFSET OF THE DIGITAL WORD IN THE DAC CARD

DOFF EQU $12

DWRD IS THE INITIAL DIGITAL WORD OUTPUT TABLE

DWRD EQU $F888

*
*INSEL IS THE LINK INPUT CHANNEL SELECT FLOP
*MAIN IS START ADDR. OF MAIN PROGRAM
*TEMP IS A TEMPORARY STORAGE LOCATION
*RICK IS THE LOCATION OF THE ROM CHECKSUM
*R2CK IS THE LOCATION OF THE RAM CHECKSUM
*FROUT IS A TEMPORARY STORAGE LOCATION
*RICK EQU $F7FE
*R2CK EQU $F681
*FROUT EQU $0000

INITIALIZED TO 1.

***************START OF PROGRAM***************

LDA #WARST DISABLE INTERRUPTS
STA LACON
LDY *D ADDRESS OF INIT. VALUES TO X

DAY #04TAB INIT DAC'S
LDU #$7FF7 Y GETS DAC ADDR. TABLE
LDY #0FF Y GET 0 VOLTS BITS
LDX #0Y ADDR. OF DAC TO Y
BIC D begun IF ADDR. = 0, THEN DONE
LDX #0ALPS SET LOOP COUNTER
LOOPB STU .X++ STORE TO DAC'S
STB .X+

DECA DEC .LOOP COUNTER
SNE LOOPB LOOP UNTIL = 0
LEAY .Y+ Y WHEN 0, POINT TO NEXT DAC CARD
BRA LOOPA AND LOOP
DATAB FDB DA# TABLE OF DAC ADDRESSES
FDB DA1
FDB DA2
FDB DA3
FDB 0000
DIGINI LDX #0WRT DIGITAL BITS INIT
LDY #0WAB TABLE OF INIT. VALUES TO X
**ROM TEST:** STORE AND VERIFY TWO BIT PATTERNS

```
0166 A 0331 EEA4  LOOPC   LDU  0:Y   DAC CARD ADSR TABLE TO Y
0169 A 0333 2709  BEQ   RAMST IF 0 TO U THE END OF DATA
0170 A 0335 E021  LDD   0++   GO TO NEXT TEST
0171 A 0337 EDC812  STD   RAMFU LOAD AND STORE INIT VALUES
0172 A 033A 3122  LEAV  2:Y   POINT TO NEXT ENTRY IN DATA
0173 A 033C 20F3  BRA   LOOPC AND KEEP LOOPING
0174
0175 A 033E CAAAA  RAMSTL LDY  #AAAA BIT PATTERN TO 0
0176 A 0441 8E0000  LOOP1 LDX  #RAMST RAM START ADDR. TO X
0177 A 0444 189E4000  LDY  #RAPST RAM LENGTH TO Y
0178 A 0448 E084  LOOP2 STD  0:1
0179 A 044A 10A3B1  CMPD  0+++ STORE AND VERIFY
0180 A 044D 260E  ENE   RAMERR FLAG ERROR IF NOT VERIFY
0181 A 044F 313E  LEAY  -2:Y
0182 A 0551 26F5  ENE   LOOP2 LOOP THRU ALL RAM
0183 A 0553 185F555  CMPD  ##5555 DONE TWO PATS, YET?
0184 A 0557 274A  BEQ   RAMOK YES: FLAG RAM OK
0185 A 0559 44  LSRA  NO: DO SECOND PATTERN
0186 A 055A 54  LSRB
0187 A 055B 20E4  BRA   LOOP1
0188 A 055D 8620  RAMERR LDA  #RMTST ON ERROR, SET STATUS BIT 5
0189 A 055F 9717  STA   STATUS
0190 A 0661 2003  BRA   ROMST GO TO NEXT TEST
0191 A 0663 4F  RAMOK CLR A NO ERROR, CLEAR STATUS
0192 A 0664 9717  STA   STATUS
0193
0194 A 0666 F57FE  ROMTST LDD  #ICK GET ROM CHECKSUM
0195 A 0669 F3F001  ADDC  #2CK SUM WITH F00 ROM CHECKSUM
0196 A 066C D0DF  STC   TEMP SAVE RESULT
0197 A 066E 10E1000  LDY  #ROLST ROM LENGTH TO Y
0198 A 0672 8EF000  LDY  #RAMST ROM START TO X
0199 A 0675 4F  CLRA   SUM ALL LOCATIONS
0200 A 0676 5F  CLR B
0201 A 0677 E805  LOOP3 ADDB  ++
0202 A 0679 2401  ECE   SKIP1 BRANCH IF NO CARRY
0203 A 067B 4C  INCA
0204 A 067C 313F  SKIP1 LEAY  -1:Y
0205 A 067E 26F7  BEQ   LOOP3 LOOP UNTIL DONE
0206 A 0680 109C0F  CMPD  TEMP SEE IF SUM CHECKS
0207 A 0683 2706  BEQ   ANST IF OK GO TO NEXT TEST
0208 A 0685 8640  LDA  #ROMSTA IF NOT OK SET ROM STATUS BIT
0209 A 0687 9A17  BRA   STATUS
```
STA STATUS

*ADC BOARD TEST: SEE THAT 2 CONTROL BITS

* GET IN AND OUT OF

ANTST CLRA STORE @ IN CONTROL BITS

STA MUXLT

LDA #ADCTI SEE IF THEY COME OUT OK

ANDA ADCTI MASK BITS AS WE WANT TO SEE

CMPA #ADCT2 SEE IF GET CORRECT RESULT

BNE ADERR IF ANY FLAG ERROR

CLR A NO A STORE @ IN CONTROL BITS

STA MUXLT

LDA #ADCTI MASK BITS

ANDA ADCTI

CMPA #ADCT3 SEE IF GET CORRECT RESULT

BNE ADERR IF ANY FLAG ERROR

BNE LACTST YES: GO TO NEXT TEST

LDA #ACIA STS: WAIT FOR EMPTY

STA LACTST

LDA #ACIA TEST

STA LACTST

LDA PROMPT TEST: DATA TO SEND

LDA ACIA STORE BYTE

BNE LACERR NO ERROR

BNE LACTST YES: WAIT FOR EMPTY

BNE LACTST ON EMPTY GO TEST LACIA

LEEP -1.4 MARK TIME

BNE LOOPU LOOP IF NO TIME OUT

BNE LOOPU LOOP IF NO TIME OUT

BNE LOOPU LOOP IF NO TIME OUT

LACERR LDA #ACIA ON ERROR, SET STATUS BIT

LACTST LDA STATUS

LACTST LDX #WAIT2 SET UP WAIT COUNT

LACTST LDX #WAIT2 SET UP WAIT COUNT

LACERR LDA #ACIA ON ERROR, SET STATUS BIT

LACTST STA LACIA

LACTST BITB LACIA

LACTST BITB LACIA

LACTST STA LACIA

LACTST BITB LACIA

LACTST LDX #WAIT2 SET UP WAIT COUNT

LACTST LDX #WAIT2 SET UP WAIT COUNT

LACERR LDA #ACIA ON ERROR, SET STATUS BIT

LACTST STA LACIA

LACTST BITB LACIA

LACTST BITB LACIA

LACTST STA LACIA

LACTST BITB LACIA

LACTST LDX #WAIT2 SET UP WAIT COUNT
*INITIALIZE ALL MEMORY TO ZERO EXPECT ROUT WHICH GOES TO ONE AND SYMOC WHICH GOES TO TWO AND STATUS WHICH IS PRESERVED AS IS:

LDA #01 FRUIT TO 1
STA FROUT

LDA #02 SYMOC TO 2
STA SYMOC

STA STATUS; RESTORE STATUS

LDA #03 READY USER ACIA
STA UACON

LDA #04 SIGNAL LOOKING FOR GOOD FRAME
STA STATUS

LDA #05 READY LINK ACIA
STA LACON

ANDC #AF REMOVE INTERRUPT MASKS

LDS #TOSTAK ENABLE NMI BY LDS

JMP MAIN
**LIMCK SUBROUTINE**

* CHECKS MIN/MAX LIMITS OF ANALOG VOLTAGES *

**INPUT:**

* U-REG FOR ANALOG VOLTAGE *
* MUXCT (LOC 15) TO COMPUTE BIT TO UPDATE *
* RANTBL: A TABLE, CONTAINING MIN/MAX VALUES *

**OUTPUT:**

* NIRTBL, A TABLE, GETS ONE BIT SET OR RESET *
* ALSO USES: A, X, Y *

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*Limck LDY #NIRTBL STATUS TABLE ADDR. TO Y *

LIMCK CLRA CALCULATE ADDR IN RANTBL

LIMCK D615 MUXCT

LIMCK 58 ASLB

LIMCK 58 ASLB

LIMCK C3F800 ADDD #RANTBL

LIMCK 1F01 TFR D.X ADDR. IN RANTBL TO X

LIMCK 9615 LDA MUXCT FIND POSITION OF BIT TO UPDATE

LIMCK 8407 ANDA #07 KEEP ONLY 3 LSB'S

LIMCK 4C INCA

LIMCK 5F CLRB

LIMCK 1A01 CRC C 01 SHIFT A BIT FROM C THRU B

LIMCK 56 LIMSH ROGB

LIMCK 4A DECA

LIMCK 26FC BNE LIMSH

LIMCK 43 COMA SEE IF LIMITS ARE PROGRAMMED

LIMCK A184 CMPA #X

LIMCK 270A BEQ IR BRANCH IF NOT

LIMCK 11A381 CMPU ,X++, CHECK LIMITS

LIMCK 2E10 BGT Nir

*Limck LDY #NIRTBL STATUS TABLE ADDR. TO Y

LIMCK CLRA CALCULATE ADDR IN RANTBL

LIMCK D615 MUXCT

LIMCK 58 ASLB

LIMCK 58 ASLB

LIMCK C3F800 ADDD #RANTBL

LIMCK 1F01 TFR D.X ADDR. IN RANTBL TO X

LIMCK 9615 LDA MUXCT FIND POSITION OF BIT TO UPDATE

LIMCK 8407 ANDA #07 KEEP ONLY 3 LSB'S

LIMCK 4C INCA

LIMCK 5F CLRB

LIMCK 1A01 CRC C 01 SHIFT A BIT FROM C THRU B

LIMCK 56 LIMSH ROGB

LIMCK 4A DECA

LIMCK 26FC BNE LIMSH

LIMCK 43 COMA SEE IF LIMITS ARE PROGRAMMED

LIMCK A184 CMPA #X

LIMCK 270A BEQ IR BRANCH IF NOT

LIMCK 11A381 CMPU ,X++, CHECK LIMITS

LIMCK 2E10 BGT Nir
AMERICAN AUTOMATION ASSEMBLER

0042 A 0024 11A364 CMPU 0,X
0043 A 0027 2D0B BLT NIR
0044 A 0029 9615 IR LDA MUXCT WITHIN RANGE OR UNPROGRAMMED
0045 A 002B 44 LSRA UPDATE THE APPROPRIATE BIT
0046 A 002C 44 LSRA
0047 A 002D 44 LSRA
0048 A 002E 53 COMB
0049 A 002F E4A6 ANDB A,Y
0050 A 0031 E7A6 STB A,Y
0051 A 0033 39 RTS
0052 A 0034 9615 NIN LDA MUXCT NOT WITHIN RANGE
0053 A 0036 44 LSRA UPDATE APPROPRIATE BIT
0054 A 0037 44 LSRA
0055 A 0038 44 LSRA
0056 A 0039 EAA6 ORB A,Y
0057 A 003A E7A6 STB A,Y
0058 A 003B 39 RTS
0059 A 003C 39 END
***LIMSET**

**FUNCTION:** SETS LIMIT BIT IN NIRTBL PER MUXCT

**INPUT:** MUXCT, SPECIFIES WHICH BIT TO SET

**OUTPUT:** THE SPECIFIED BIT IS SET IN NIRTBL

**USES:** A, B, X

**NIRTBL IS THE STARTING ADDRESS OF THE 'NOT IN RANGE' TABLE.**

**MUXCT IS USED TO KEEP TRACK OF THE CHANNEL TO CONVERT.**

-----------------START OF PROGRAM-------------------

**LIMSET**

LDX #NIRTBL STATUS TABLE ADDR. TO X

LDA MUXCT POSITION BIT

ANDA #07

INCA

CLRB

ORCC #1

LSSHFT RORB

DECA

BNE LSSHFT

LDA MUXCT STORE BIT

LSRA

LSRA

LSRA

ORB A,X

STB A,X

RTS

END
AMERICAN AUTOMATION ASSEMBLER

0001  ***********************************************
0002  * LINT SUBROUTINE *
0003  *
0004  *
0005  * FUNCTION: HANDLES RECEIVED DATA INTERRUPTS FROM *
0006  * LINK. *
0007  *
0008  * INPUT: LINK RECEIVED DATA AND MISC. MEMORY *
0009  *
0010  * OUTPUT: LINK DATA IN BUFFERS, REMOTE STATUS, AND *
0011  * MISC. MEMORY LOCATIONS. *
0012  *
0013  *
0014  *
0015  *
0016  ***********************************************
0017  *
0018  ***SYMBOL DEFINITIONS***
0019  *
0020  A 0000 0000019  LINTCT  EQU  $19
0021  *
0022  * LINTCT IS USED TO TELL MAIN MEMORY AN INTERRUPT OCCURRED
0023  *
0024  *
0025  A 0000 000001B  SYMCT  EQU  $1B
0026  *
0027  * SYMCT IS USED TO DEFINE THE SYNC MODE
0028  *
0029  *
0030  *
0031  *
0032  * RCVDAT  EQU  $1801
0033  *
0034  * RCVDAT IS THE ADDRESS OF THE LINK UART DATA BUF
0035  *
0036  *
0037  *
0038  *
0039  *
0040  *
0041  *

0001  ***********************************************
0002  * LINT SUBROUTINE *
0003  *
0004  *
0005  * FUNCTION: HANDLES RECEIVED DATA INTERRUPTS FROM *
0006  * LINK. *
0007  *
0008  * INPUT: LINK RECEIVED DATA AND MISC. MEMORY *
0009  *
0010  * OUTPUT: LINK DATA IN BUFFERS, REMOTE STATUS, AND *
0011  * MISC. MEMORY LOCATIONS. *
0012  *
0013  *
0014  *
0015  *
0016  ***********************************************
0017  *
0018  ***SYMBOL DEFINITIONS***
0019  *
0020  A 0000 0000019  LINTCT  EQU  $19
0021  *
0022  * LINTCT IS USED TO TELL MAIN MEMORY AN INTERRUPT OCCURRED
0023  *
0024  *
0025  A 0000 000001B  SYMCT  EQU  $1B
0026  *
0027  * SYMCT IS USED TO DEFINE THE SYNC MODE
0028  *
0029  *
0030  *
0031  *
0032  * RCVDAT  EQU  $1801
0033  *
0034  * RCVDAT IS THE ADDRESS OF THE LINK UART DATA BUF
*BYTECT IS THE DATA BYTE COUNTER
BYTECT EQU $1F

*RBUF is the starting address of a data buffer.
RBUF* EQU $20

*RBUF1 is the starting address of a data buffer.
RBUF1 EQU $70

*RBUFSE is a pointer to the active data buffer.
RBUFSE EQU $C1

*CRCOM is used to store the computed CRC.
CRCOM EQU $C3

*CRCCNT is used to count the number of bad CRC's.
CRCCOM EQU $C5

*REMSTA is used to store the remote status.
REMSTA EQU $C9

*FSYNO is used to flag a good first sync.
FSYNK EQU $CD

*STATUS is used to store the local status.
STATUS EQU $17

*BSYNCT is used to count the bad sync words.
BSYNCT EQU $CD

*FRDY is used to tell the main program that a complete, good frame has been received.
FRDY EQU $C7

*LOCOMER counts communication errors.
LOCOMER EQU $ID

*RCVPTR is an index used in storing received data.
RCVPTR EQU $DF

*UPDATE is a subroutine that updates the analog and digital outputs after receipt of a good frame.
**********START OF PROGRAM**********************
0124  A 004F 2712  BEQ  CRCTST  YES: GO TEST CRC
0127  A 0051 00F  LDB  RCVPTR  RCV'D DATA STORE INDEX TO B
0128  A 0053 8E0020  LDX  #RBUFF  NO: SELECT BUF FOR DATA STORE
0129  A 0056 00C1  TST  RBUFFE
0130  A 0058 2703  BEQ  STROCV
0131  A 005A 8E0079  LDX  #RBUFF1
0132  A 005D A785  STPCV  STA  BX  STORE DATA
0133  A 005F 0CDF  INX  RCVPTR  INC THE INDEX
0134  A 0061 00F1  DEC  BYTECT  UPDATE BYTECT
0135  A 0063 96C3  ADDA  CRCROM  UPDATE CRC
0136  A 0065 97C3  STA  CRCROM
0137  A 0067 7E0127  A  JMP  OUT
0138  A 006A 91C3  CRCTST  CMPA  CRCROM  RCV'D CRC=COMPUTED?
0139  A 006C 271C  BEQ  GCR  YES BRANCH
0140  A 006E 8602  DCPC  LDA  #02  SEE IF <2 BAD
0141  A 0070 91C5  CMPA  BCROCT
0142  A 0072 2E0D  BGT  LT2BAD  YES BRANCH
0143  A 0074 8603  LDA  #03  NO: RESYNC
0144  A 0076 971B  STA  SYMCTX
0145  A 0078 9001  LDA  #01  SET STATUS BIT
0146  A 007A 9417  ORA  STATUS
0147  A 007C 9717  STA  STATUS
0148  A 007E 7E0127  A  JMP  OUT
0149  A 0081 0C5  LT2BAD  INC  BCROCT  UPDATE BAD CRC COUNT
0150  A 0083 8604  LDA  #04  SET UP TO RECEIVE SYNC
0151  A 0085 971D  STA  HDRCT  (DON'T FLAG DATA READY)
0152  A 0087 7E0127  A  JMP  OUT
0153  A 008A 8604  GCR  LDA  #04  GOOD CRC
0154  A 008C 971D  STA  HDRCT  UPDATE HDRCT
0155  A 008E 0C05  CLR  BCROCT  CLEAR BAD CRC COUNTER
0156  A 0090 9617  LDA  STATUS
0157  A 0092 86FE  ANDA  #0FE  CLEAR 'LOOKING FOR SYNC'
0158  A 0094 9717  STA  STATUS  STATUS BIT
0159  A 0096 00C1  TST  RBUFFE  UPDATE BUFFER POINTER
0160  A 0098 270F  BEQ  SEO
0161  A 009A 00C1  CLR  RBUFFE
0162  A 009C 00C1  TST  BSYRCT  UPDATE DATA?
0163  A 009E 2606  BNE  NONEW  NO: GO JUMP OUT
0164  A 00A0 8E0070  LDX  #RBUFF1  YES: POINT TO DATA
0165  A 00A2 BC0F  JSR  UPDATE  GO UPDATE
0166  A 00A4 7E0127  A  NONEW  JMP  OUT
0167  A 00A6 00C1  SEO  INC  RBUFFE
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0168 A 00AB 00CD TST BSYNCT UPDATE DATA?
0169 A 00AD 00DE BNE NONEW2
0170 A 00AF 00E9 LDX #0DF0 YES: POINT TO DATA
0171 A 00B2 00F0 JSR UPDATE UPDATE
0172 A 00B5 0127 A NONEW2 JMP OUT
0173 A 00B6 02EF1 HOrCT1 LDA RDVDAI
0174 A 00BB 04A DECA STORE BYTE COUNT
0175 A 00BC 071F STA BYTCT
0176 A 00BE 0C4 INCA UPDATE CRC
0177 A 00BF 0CB3 ADA CRCOM
0178 A 00C1 07C3 STA CRCOM
0179 A 00C3 0A1D DEC HDRCT UPDATE HDRCT
0180 A 00C5 0BBF CLR RCVPTR INITIALIZE RCV BUF POINTER
0181 A 00C7 0127 A JMP OUT
0182 A 00CA 0181 HOrCT2 LDA RDVDAI RECEIVE STATUS
0183 A 00CB 07C9 STA REMSTA
0184 A 00CC 0A1D DEC HDRCT UPDATE HDRCT
0185 A 00CD 07C3 STA CRCOM INIT CRC COUNT
0186 A 00DE 0552 BRA OUT
0187 A 00DF 0181 HOrCT3 LDA RDVDAI SECOND Sync?
0188 A 00E0 018E CMPA #$5E
0189 A 00E1 02E9 BNE BSYN3 NO-BRANCH
0190 A 00E2 06A3 DEC HDRCT YES:
0191 A 00E3 00CD TST FSYNOK WAS FIRST Sync OK?
0192 A 00E4 02E2 BNE FSYNBD NO-Branch OUT
0193 A 00E5 00CD CLR BSYNCT YES CLEAR BAD Sync COUNTER
0194 A 00E6 02E1 FSYNBD BRA OUT
0195 A 00E7 0003 BSYN3 INC LOUMER
0196 A 00E8 0652 LDA #02 SEE HOW MANY BAD SYNCS
0197 A 00EE 07C0 CMPA BSYNCT 2 OR MORE: RESYNC
0198 A 00EC 2065 BLE RESYN3
0199 A 00EF 00CD INC BSYNCT LESS THAN 2:
0200 A 00F0 0A1D DEC HDRCT JUST UPDATE COUNTERS
0201 A 00F2 2033 BRA OUT
0202 A 00FA 0462 RESYN3 LDA #02 SET Sync Mode =2
0203 A 00F6 071B STA SYMCT
0204 A 00FB 0601 LDA #1 SET STATUS BIT=1
0205 A 00FA 0A17 ORA STATUS
0206 A 00FC 0717 STA STATUS
0207 A 00FE 2227 BRA OUT
0208 A 0100 0181 HOrCT4 LDA RDVDAI FIRST Sync?
0209 A 0103 017E CMPA #$7E
<table>
<thead>
<tr>
<th>Line</th>
<th>Address</th>
<th>Operation</th>
<th>Immediate</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0210</td>
<td>A 0105</td>
<td>BNE</td>
<td>BSYN4</td>
<td>NO, BRANCH</td>
</tr>
<tr>
<td>0211</td>
<td>A 0107</td>
<td>CLR</td>
<td>FSYNOK</td>
<td>YES, UPDATE COUNTERS</td>
</tr>
<tr>
<td>0212</td>
<td>A 0109</td>
<td>DEC</td>
<td>HDRC</td>
<td></td>
</tr>
<tr>
<td>0213</td>
<td>A 010B</td>
<td>BRA</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>0214</td>
<td>A 010D</td>
<td>INC</td>
<td>BSYN4</td>
<td>Flag BAD Sync</td>
</tr>
<tr>
<td>0215</td>
<td>A 010F</td>
<td>INC</td>
<td>FSYNOK</td>
<td>Increment Communication ERRORS</td>
</tr>
<tr>
<td>0216</td>
<td>A 0111</td>
<td>LDA</td>
<td>#02</td>
<td>More than 2 BAD_SYNCS?</td>
</tr>
<tr>
<td>0217</td>
<td>A 0113</td>
<td>CMPA</td>
<td>BSYN4</td>
<td></td>
</tr>
<tr>
<td>0218</td>
<td>A 0115</td>
<td>BLE</td>
<td>RESYN4</td>
<td>YES, RESYN4</td>
</tr>
<tr>
<td>0219</td>
<td>A 0117</td>
<td>INC</td>
<td>BSYN4</td>
<td>No, UPDATE COUNTERS</td>
</tr>
<tr>
<td>0220</td>
<td>A 0119</td>
<td>DEC</td>
<td>HDRC</td>
<td></td>
</tr>
<tr>
<td>0221</td>
<td>A 011B</td>
<td>BRA</td>
<td>OUT</td>
<td></td>
</tr>
<tr>
<td>0222</td>
<td>A 011D</td>
<td>RESYN4</td>
<td>LDA</td>
<td>SET SYNC MODE =2</td>
</tr>
<tr>
<td>0223</td>
<td>A 011F</td>
<td>STA</td>
<td>SYMOK</td>
<td></td>
</tr>
<tr>
<td>0224</td>
<td>A 0121</td>
<td>LDA</td>
<td>#01</td>
<td>SET STATUS BIT</td>
</tr>
<tr>
<td>0225</td>
<td>A 0123</td>
<td>ORA</td>
<td>STATUS</td>
<td></td>
</tr>
<tr>
<td>0226</td>
<td>A 0125</td>
<td>STA</td>
<td>STATUS</td>
<td></td>
</tr>
<tr>
<td>0227</td>
<td>A 0127</td>
<td>OUT</td>
<td>ANDC</td>
<td>#AF, ENABLE INTERRUPTS</td>
</tr>
<tr>
<td>0228</td>
<td>A 0129</td>
<td>RTI</td>
<td>END</td>
<td></td>
</tr>
<tr>
<td>0229</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**FUNCTION: PULSES AUTO-RESET CIRCUIT TO PREVENT**

**INPUT: FROUT = 1 INDICATES A GOOD DATA**

**FRAME HAS BEEN RECEIVED, UNF**

**THE LAST TIME FRMA WAS RECEIVED.**

**IT SERVES AS A COUNTER TO COUNT**

**PROGRAM LOOPS UNTIL A GOOD FRAME.**

**OUTPUT: CHANNEL STATUS WORDS: CHGO-CH11.**

**CHGO-CH11.**

**USES: CALLS: NONE**

**CALLED BY MAIN**

* ***SYMBOL DEFINITION***

---

**FRONT COUNTS MAIN PROGRAM LOOPS WITHOUT A GOOD FRAME**

**FRONT ECU #09**

**STATUS IS THE LOCAL STATUS WORD**

**STATUS ECU #17**

**CHAN IS A MEMORY IMAGE OF THE SELECTED LINK CHANNEL**

**CHAN ECU #0E**

**INSEL IS THE LINK INPUT CHANNEL SELECT FLOP**

**INSEL ECU #2000**

**RSTDIS IS THE AUTO RESET ADDRESS**

**RSTDIS ECU #1000**

**CHGO IS THE CHANNEL GOOD FLAG**

**CHGO ECU #E1**
0042 *CH0TST IS THE CHANNEL 0 TESTED FLAG
0043 A 0000 00000E2 CH0TST EQU $E2
0045 *
0046 *CH1TST IS THE CHANNEL 1 GOOD FLAG
0047 A 0000 00000E3 CH1GT EQU $E3
0048 *
0049 *CH1TST IS THE CHANNEL 1 TESTED FLAG
0050 A 0000 00000E4 CH0TST EQU $E4
0051 *
0052 **********START OF PROGRAM**************
0453 *
0054 A 0000 071000 STA RTDIS PULSE AUTO RESET
0055 A 0000 0008 TST FROUT FROUT = 0 ?
0056 A 0005 2745 BEO FROUT YES BRANCH
0057 A 0007 2D48 BLT FROUT INC: FROUT >/=128 ?
0058 *
0059 A 0000 0CD9 INC FROUT NO: COUNT
0060 A 0000 39 RTS RETURN
0061 *
0062 A 0000 0DD9 FROUT TST CHAN: CHAN 0 ON ?
0063 A 0001 2729 BEO CHAN1 YES:BRANCH
0064 A 0018 4F CLRA NO: SET CH1 GOOD: TESTED
0065 A 0011 4C INCA
0066 A 0012 97E3 STA CH1DO
0067 A 0014 97E4 STA CH1DI
0068 A 0014 0DE2 TST CH0ST CHAN 0 TESTED ?
0069 A 0013 2600 BNE CH011 YES:BRANCH
0070 A 0014 4F CLRA NO: TC0: CH 0
0071 A 0015 570E STA CHAN
0072 A 0018 7200 STA INSEL
0073 A 0010 0CD9 INC FROUT
0074 A 0022 39 RTS
0075 *
0076 A 0028 0DE1 CH0TST TST CH0D0 CHANNEL 0 GOOD ?
0077 A 0029 2600 BNE CH0G1 YES: BRANCH
0078 A 0027 8616 ROUT1 LDA #FI8 NO: SET BAD CHAN STATUS
0079 A 0029 9A17 CRA STATUS
0080 A 0028 9717 STA STATUS
0081 A 0020 0CD9 INC FROUT COUNT
0082 A 002F 39 RTS
0083 *
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0064 A 0038 B6EF CH001 LDA #B6F RESET BAD CHANNEL STATUS
0065 A 0032 9417 ANDA STATUS
0066 A 0034 5717 STA STATUS
0067 A 0036 0CD9 INC FRONT COUNT
0068 A 0038 39 RTS
0069
0070 A 0033 4F CH001: CLRA SET CH 0 GOOD TEST
0071 A 003A 4C INCA
0072 A 003E 97E1 STA CH001
0073 A 003D 97E2 STA CH011
0074 A 003F 0DE4 TST CH001 CHAN 1 TESTED?
0075 A 0041 2608 BNE CH01 YES BRANCH
0076 A 0043 B72000 STA INSEL NOT TEST CHAN 1
0077 A 0046 97D9 STA CHAN1
0078 A 0048 0CD9 INC FRONT
0079 A 004A 39 RTS
0080
0081 A 004B 0DE3 CH01: TST CH001 CHAN 1 GOOD?
0082 A 004D 26E1 BNE CH01 YES BRANCH
0083 A 004F 2606 BRA ROUT1 NO SET BAD CHANNEL STATUS BIT
0084
0085 A 0051 00DB ROUT1 TST CHAN1 CHAN 1 ON?
0086 A 0053 2704 BEO CHAN1 NO YES BRANCH
0087
0088 A 0055 0DE2 TST CH011 CHAN 2 TESTED?
0089 A 0057 2604 BNE CH01 YES BRANCH
0090 A 0059 4F CLRA NO! SWITCH TO CH 1
0091 A 005A 97DB STA CHAN1
0092 A 005C B72000 STA INSEL
0093 A 005E 4C INCA
0094 A 0060 9709 STA FRONT FRONT = 1
0095 A 0062 39 RTS
0096
0097 A 0063 0DE1 CH012 TST CH01 NO CHAN 0 GOOD?
0098 A 0065 2619 BNE CH00 YES BRANCH
0099 A 0067 4F CLRA NO! SWITCH TO CH 0
0100 A 0068 97DB STA CHAN1
0101 A 006A B72000 STA INSEL
0102 A 006D 97E1 ROUT2 STA CH000 RESET ALL FLAGS
0103 A 006F 97E2 STA CH01
0104 A 0071 97E3 STA CH01
0105 A 0073 97E1 STA CH011

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0126 A 0075 8001 LDA #01 SET FROUT=1
0127 A 0077 97DB STA FROUT
0128 A 0079 8611 LDA #11 SET BAD CHAN AND LOOKING
0129 A 0079 9A17 ORA STATUS FOR SYNC STATUS BITS
0130 A 007D 9717 STA STATUS
0131 A 007F 39 RTS
0132 *
0133 A 0080 4F CHO1: CLRA
0134 A 0081 97DB STA CHAN1 SWITCH TO CHAN 0
0135 A 0083 B200 STA INSET
0136 A 0086 97DB STA FROUT SET IF FOR FROUT=1
0137 A 0088 97E3 STA CH1D INDICATE CH 1 BAD
0138 A 008A 4C INCA INDICATE CH 1 BAD
0139 A 008B 97E4 STA CH1T
0140 A 008D 2986 BRA BOUT1 SET BAD CHAN STATUS
0141 *
0142 A 008F 00E4 CH1T1: TST CH1T1: CH 1 TESTED?
0143 A 0090 250A BNE CH1T2 YES: BRANCH
0144 A 0093 4F CLRA NO: SWITCH TO CH 1
0145 A 0094 4C INCA
0146 A 0095 97DB STA CHAN1
0147 A 0097 B200 STA INSEL
0148 A 009A 97DB STA FROUT FROUT=1
0149 A 009C 39 RTS
0150 *
0151 A 009D 00E3 CH1T2: TST CH1T2: CHANNEL 1 GOOD?
0152 A 009F 250A BNE CH1T2: YES: BRANCH
0153 A 00A1 4F CLRA NO: SWITCH TO CH 1
0154 A 00A2 4C INCA
0155 A 00A3 97DB STA CHAN1
0156 A 00A5 B200 STA INSEL
0157 A 00A6 4F CLRA GC: RESET ALL FLAGS
0158 A 00A9 20C2 BRA BOUT2 AND SET BAD CHAN STATUS
0159 *
0160 A 00A9 4F CH1T2: CLRA SET UP FOR FROUT=1
0161 A 00AC 97DB STA FROUT
0162 A 00AE 97E1 STA CH1D INDICATE CH 0 BAD
0163 A 00B0 4C INCA
0164 A 00B1 97E2 STA CH1T2 SET CH 0 BAD
0165 A 00B3 97DB STA CHAN1 SWITCH TO CHAN 1
0166 A 00B5 B200 STA INSEL
0167 A 00BE 16FF00 LBRRA BOUT1 SET BAD CHAN STATUS
0168 END
0001    0002    0003    0004    0005    0006    0007    0008    0009    0010    0011    0012    0013    0014    0015    0016
0017    0018    0019    0020    0021    0022    0023    0024    0025    0026    0027    0028    0029    0030    0031
0032    0033    0034    0035    0036    0037    0038    0039    0040    0041    0042    0043    0044
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*******************************************************************************
* * LXMIT SUBROUTINE *
* * FUNCTION: PUTS A BYTE IN THE LINK UART DATA BUF. *
* * TIMES OUT IF UART IS NOT READY SOON *
* * ENOUGH. UPDATES STATUS BIT 3. *
* * INPUT: BYTE IN A REG. *
* * OUTPUT: BYTE INTO LINK UART DATA BUF. IF NO *
* * TIME-OUT; UPDATED STATUS BIT *
* * USES: R1 *
* *
*******************************************************************************
* *STATUS IS USED TO KEEP LOCAL STATUS INFO *
* *
* LUCON IS LINK UART CONTROL REG. *
* LUDAT IS LINK UART DATA REG. *
* *
*******************************************************************************/

**START OF PROGRAM**

LXMIT LDX #8000 SET UP TIME-OUT CTR.
LDX #1000 TEST UART READY
LDB #10 TEST UART READY
XWAIT BITB LUCON
BNE SEND
LEAX -$1X BRANCH IF NOT READY
EAX XWAIT
XOUT LDB #$E TIME-OUT STATUS UPDATE
ORL STATUS
STB STATUS
RTS
SEND STA LUDAT SEND DATA
LDB #$F7 UPDATE STATUS
ANDB STATUS
STB STATUS
RTS
END
**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
**CALLS:**

**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
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**USES:** A.X
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**USES:** A.X
**CALLED BY LPMAN
**CALLS:**

**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
**CALLS:**

**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
**CALLS:**

**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
**CALLS:**

**FUNCTION:** TESTS ALTERNATE LINK CHANNEL. IF DATA IS *
**RECEIVED, AN SWI TO LINT SUBROUTINE IS **
**EXECUTED TO PROCESS IT**

**INPUT:** CHANNEL CONTAINING INPUT CHANNEL ACTIVE
**OUTPUT:** CHAINI, CONTAINING INPUT CHANNEL ACTIVE

**USES:** A.X
**CALLED BY LPMAN
**CALLS:**
AMERICAN AUTOMATION ASSEMBLER

142 A 0006 0002 TST CHANI
0043 A 0008 2601 PNE CONT1
344 A 000A 4C INCA
0045 A 0008 070B CONT1 STA CHANI STORE CHAN. IMAGE IN MEM.
0046 A 003D B7000 STA INSEL SWITCH CHAN SEL FLOP
6047 A 0010 8601 LDA #1 SET UP TEST
0048 A 0012 BE753 LDX #WAIT
0049 A 0015 001F LOOP1 LEAX -1;X CHECK TIME OUT
1050 A 0017 2706 BEQ TOUT
0051 A 0019 B5000 BITA LINCON DATA RECEIVED?
4052 A 001C 27F7 BEQ LOOP1 IF NO, LOOP UNTIL TIME OUT
0053 A 001E 3F SWI IF YES GO PROCESS
4054 A 001F 3605 TOUT LDA #LISTEN ENABLE INTERRUPT IN LINK ACIA
6055 A 0021 B7F00 STA LINCON
4056 A 0024 3F RTS LINCON
4057
************* MAIN ROUTINE *************

* FUNCTION: CONTROLS PROGRAM FLOW *
* INPUT: NONE *
* OUTPUT: NONE *
* USES: NONE *
* CALLS: LPMON, SYNCTR, ANACTR, DIGINT, ENDTR, DISPLAY *
* CALLED BY NONE (ENTRY FROM INIT ROUTINE) *

************* SYMBOL DEFINITION *************

* LP MON IS A SUBROUTINE WHICH MONITORS VARIOUS PARAMETERS *
* ONCE THRU EACH MAIN PROGRAM LOOP *

A 0000 0000FE60 LPMON EQU $FE60

* SYNCTR IS A SUBROUTINE WHICH TRANSMITS THE SYNC WORDS *
A 0000 0000FB30 SYNCTR EQU $FB30

* ANAC TR IS A SUBROUTINE WHICH TRANSMITS STATUS NUMBER *
* OF BYTES AND ANALOG VALUES, AS WELL AS CONTROLS *
* AND MONITORS ANALOG ACQUISITION *
A 0000 0000F500 ANAC TR EQU $F500

* DIGINT IS A SUBROUTINE WHICH ACQUIRES AND TRANSMITS *
A 0000 0000FB40 DIGINT EQU $FB40

* ENDTR IS A SUBROUTINE WHICH TRANSMITS ALL THE STUFF *
* AT THE END OF THE DATA FRAME *
A 0000 0000FB58 ENDTR EQU $FB58

* DISPLAY IS A SUBROUTINE WHICH UPDATES FRONT PANEL AND *
* USER MONITOR DISPLAY *
A 0000 0000FCE0 DISPLAY EQU $FCE0

* UPDATE IS A SUBROUTINE WHICH UPDATES USER OUTPUTS WHEN
AMERICAN AUTOMATION ASSEMBLER  MAIN  29 Dec 83  PAGE 002

0042  A 0000 0000FDF0  * A VALID FRAME IS RECEIVED
0044  UPDATE EDU FDF0
0045  *
0046  ****************************START OF PROGRAM*****************************
0047  *
0048  0049  A 0000 0DFE60  MAIN JSR LMN
0049  A 0003 0DF640  JSR SW
0049  A 0000 0DF500  JSR ANACT
0050  A 0000 0DF400  JSR DISC
0051  A 0000 0DFB58  JSR ENTRA
0052  A 003F 0DFC1A  JSR DISPL
0053  A 0012 0FDCE  SPA MAIN
0054  END
**SYNCTR SUBROUTINE**

**FUNCTION:** Transmits the link sync bytes

**INPUT:** None

**OUTPUT:** Sync words to link UART

**USES:** A, LXMIT

**SYMBOL DEFINITIONS**

*SYNCDW IS THE LINK SYNC WORD*

SYNCDW EQU $7E

*LXMIT IS THE LINK HANDLER SUBROUTINE*

LXMIT EQU $FB00

**START OF PROGRAM**

SYNCTR LDA #SYNCDW
JMP LXMIT
JSR LXMIT LOAD AND TRANSMIT SYNC WORD
**UACINT**, SUBROUTINE

**FUNCTION:** Handles User ACIA Interrupts

**INPUT:** FRAM HSFR ACIA

**OUTPUT:** NONE

**USES:** A

**CALLS:** NONE

**CALLED BY:** User Interface (Entry from User ACIA Interrupt)

**SYMBOL DEFINITION**

- **UACRB** is the User ACIA Read Buffer

**START OF PROGRAM**

1. Read User Interface to Clear Interrupt
2. LDA UACFB
3. RTI
4. END
* UPDATE SUBROUTINE *

* FUNCTION: UPDATES USER ANALOG AND BINARY OUTPUTS *
* INPUTS: DATA IN A RECEIVED DATA BUFFER *
* TBDY FLAG TO SIGNAL DATA AVAILABLE *
* DIGITS TO SELECT BETWEEN DIGITAL OUTPUTS *
* 16 TO 31 AND LIMIT BITS 0 TO 15 *
* OUTPUTS: 31 ANALOG SIGNALS *
* DIGITAL OUTPUTS 0 TO 15 *
* DIGITAL OUTPUTS 16 TO 31 OR ANALOG LIMIT *
* USES: A, X, Y, U *

******************************************************************************

0020 1.
0021 Offr.
0022 A 0000 00000C7 FBDY EQU $C7
0023 *
0024 A 0000 00000D7 RCVD0 EQU $D7
0025 *
0026 *
0027 A 0000 00000C7 RBUF0 EQU $29
0028 *
0029 A 0000 0000020 RBUF1 EQU $70
0030 *
0031 A 0000 0000070 RBUF2 EQU $50
0032 *
0033 A 0000 0000061 RBUF3 EQU $61
0034 *
0035 A 0000 0000061 RBUF4 EQU $61
0036 *
0037 A 0000 0000061 RBUF5 EQU $61
0038 *
0039 A 0000 0000061 RBUF6 EQU $61
0040 *
0041 *
AOUT2 is the start addr. of the third analog out card.

AOUT is the start addr. of the subroutine which loads
the analog output latches.

AOUTL is the addr. of the latches for DOUT 0 - 15

AOUTL is the addr. of the latches for DOUT 16 - 31

DOUTL is the offset of the digital words in the memory

DOUTL is used to count main program loops without

A good frame output. It is reset by this routine

If this routine outputs a new frame

FRONT is used to count main program loops without

A bit 7 is used to indicate limit bit or digital output

Front buffer.

Start of program

Update

BNE

INC

CONT.

LDY

#AOUT3

OUTPUT to analog card 0

LDA

#09:

Tell how many words to output

JSR

AOUT

LDA

#09:

Output to analog card 1

JSR

AOUT

LDA

#09:

Output to analog card 2

LDA

#09:

Test DSW4 to find out

LDA

#09:

Point to limit bits

STU

OUTPUT one or the other

CLR

Indicate a good frame received

RTS

END
6.0 How to Put in the Right Checksum

This section assumes the user is familiar with the use of a PROM programmer, and with hexadecimal notation. Access to a hexadecimal calculator such as Dwayne Schiebel's may be helpful.

Three locations in each ROM are saved for storing the ROM checksum and checksum adjust. Let A be the location for checksum adjust, B be the location for checksum MSB, and C be the location for the LSB.

Values to plug into A, B, and C are found as follows:
1. Get the ROM program into the programmer's RAM.
2. Set locations A, B, and C to zero (0080-0082 in 10A ROM, 07FD-07FF in 6A ROM).
3. Do a checksum on 0000 to 07FF.
4. Let the resulting two LSD's be called Z, and the next two LSD's be called Y; e.g., if the programmer gives 0467F2 as a checksum, Z = F2 and Y = 67.
5. If \( Y + Z = 0 \), then \( A = B = C = 00 \).
   If \( 0 < Y + Z \leq 100_\text{H} \), then
   \[
   \begin{align*}
   B &= Y + 1 \\
   C &= Z \\
   A &= 100_\text{H} - (B + C)
   \end{align*}
   \]
   else
   \[
   \begin{align*}
   B &= Y + 2 \\
   C &= Z \\
   A &= 200 - (B + C)
   \end{align*}
   \]
(All arithmetic done in hexadecimal.)
7.0 How to Enter Analog Limits

This section assumes the user is familiar with the use of a PROM programmer, and with hexadecimal notation. Access to a hexadecimal calculator such as Dwayne Schiebel's may be useful.

Minimum and maximum limits can be programmed into ROM 10A for each analog input. Input voltages that exceed these voltages cause a limit bit to be set. These limit bits, in turn, cause the front panel DVM to blink when the appropriate channel is selected; the limit bits for channels 0 to 15 can also be passed on to the user, instead of digital outputs 16 to 31.

These limits are programmed as follows. First, the appropriate value for the limit must be calculated. Assume it is V volts, where V is a decimal number between -10 and +9.996 volts. Calculate

\[ N_D = \left(\frac{(V + 10)}{20}\right) \times 4096 \]

Then change \( N_D \) to a hexadecimal number, \( N_H \) and round, if necessary, to an integer. (Dwayne Schiebel and others have calculators that will make this conversion at the touch of a button.) Let XYZ be the three character hex representation of \( N_H \). It is programmed into two consecutive bytes of ROM as follows:

<table>
<thead>
<tr>
<th>Byte #</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>( \emptyset ) X</td>
</tr>
<tr>
<td>N + 1</td>
<td>Y Z</td>
</tr>
</tbody>
</table>

The byte to min/max channel mapping is specified in Table 5.

Once the min/max values are known they can be programmed by reading ROM 10A V1.0-RJL into the ROM programmer and changing the appropriate bytes. Then the checksum should be changed,
as described in Section 6.0. Finally, a new ROM can be programmed, or the old one erased and reprogrammed. A new and different label should be used to identify it.

**TABLE 5**  
Analog Voltage Limit Locations in Rom 10A

<table>
<thead>
<tr>
<th>Byte #</th>
<th>Channel</th>
<th>Min</th>
<th>Max</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0, 1</td>
<td>0</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>2, 3</td>
<td>0</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>4, 5</td>
<td>1</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>6, 7</td>
<td>1</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>8, 9</td>
<td>2</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>A, B</td>
<td>2</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>C, D</td>
<td>3</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>F, F</td>
<td>3</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>10, 11</td>
<td>4</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>7C, 7D</td>
<td>31</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>7E, 7F</td>
<td>31</td>
<td></td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
7.1 Example

Assume we want to change the default min and max values from the V1.0-RJL standard to -5 and +5 volts, respectively for channel 17. Calculate

\[
((-5 + 10)/20) \times 4096 = 1024_{10} = 400_{16}
\]

\[
((+5 + 10)/20) \times 4096 = 3072_{10} = C00_{16}
\]

Interpolating from Table 4, channel 17 max corresponds to bytes 44_{16} and 45_{16} and channel 17 min to bytes 46_{16} to 47_{16}.

Read ROM 10A V1.0-RJL into the PROM Programmer. Change the contents of the above-mentioned four locations as follows:

<table>
<thead>
<tr>
<th>Byte # (Hex)</th>
<th>Contents (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>44</td>
<td>0C</td>
</tr>
<tr>
<td>45</td>
<td>00</td>
</tr>
<tr>
<td>46</td>
<td>04</td>
</tr>
<tr>
<td>47</td>
<td>00</td>
</tr>
</tbody>
</table>

Find and enter the new checksum as described in Section 6.0 and program a new ROM.

8.0 Changing Default Power-On Digital Outputs

This section assumes the user is familiar with the use of a PROM programmer and with the hexadecimal number system.

The FEDAL Digital Outputs go to specified default values shortly after power-on. In V1.0-RJL firmware the default is all logic high. (Of course, after a good data frame is received these outputs are updated.) It is not too hard to conceive of applications in which certain switch settings are desirable immediately after power-on. This can be effected by modifying these default values.
The defaults are modified as follows. Table 6 specifies the default values table located in ROM 10A. Each output is assigned one bit in this table, and changing a bit is as easy as reprogramming the byte in which it resides, and then updating the checksum as described in Section 6.0.

8.1 Example

Suppose we want outputs 6, 12, and 30 to default to logic low and all the rest to logic high. We need to program

\[
\begin{align*}
10111111_2 & = BF_{16} \text{ into location } 88 \\
11101111_2 & = FF_{16} \text{ into location } 89 \\
10111111_2 & = BF_{16} \text{ into location } 8B
\end{align*}
\]

of ROM 10A, and then update the ROM checksum.

<table>
<thead>
<tr>
<th>TABLE 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Digital Output Locations in ROM 10A.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Byte # (Hex)</th>
<th>Default Output # (decimal) (MSB .......... LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>88</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>89</td>
<td>15 14 13 12 11 10 9 8</td>
</tr>
<tr>
<td>8A</td>
<td>23 22 21 20 19 18 17 16</td>
</tr>
<tr>
<td>8B</td>
<td>31 30 29 28 27 26 25 24</td>
</tr>
</tbody>
</table>
9.0 Test Procedures

This section includes test procedures for the three Front-End Data Link (FEDAL) boards and the chassis. Card schematics, parts lists, and layouts, however, are not included. These can be found on pages 26 to 62 of the FEDAL report, EDIR No. 239.
TEST PROCEDURES

FEDAL-In Card
FEDAL-MP Card
FEDAL Output Card Tests
FEDAL Chassis
TEST PROCEDURE FOR FEDAL-IN CARD

R. Lacasse

June 10, 1983

1. Remove all cards and power supply connections from the front end data tester.

2. Put the blank, wired, FEDAL-IN card in the input slot.

3. Test for shorts between the tester's supply inputs.

4. Verify continuity between:
   A. +15 V supply input and: B34, C52, G17, G33, H16, H18, H24, J18, J30, J33, Z48, Z55.
   D. +5 V supply input and: B01, B12, B23, D01, D09, F02, 1112, 1113, 1114, L07, L09.
   E. 5 V RTN supply and: C10, C21, C32, E07, E15, F12, F13, G09, L10.

5. Remove the card and install all its components per the layout on page 4.

6. Connect supplies to the tester.

7. Turn on the supplies and measure the currents consumed by the tester with no cards inserted.

8. Plug in the card and measure the incremental currents, consumed by the card. The currents should be in the following ranges:

<table>
<thead>
<tr>
<th>Supply</th>
<th>Minimum (mA)</th>
<th>Maximum (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5 V</td>
<td>103</td>
<td>245</td>
</tr>
<tr>
<td>+15 V</td>
<td>44</td>
<td>72</td>
</tr>
<tr>
<td>-15 V</td>
<td>44</td>
<td>72</td>
</tr>
</tbody>
</table>

9. Install the "Test 6" ROM into location 10A of the FEDAL-MP board. Install the FEDAL-MP board and FEDAL-IN cards into their proper slots in the front end data link chassis. Remove the top of the chassis for easy access to the FEDAL-IN board.
10. Install "clothes-pins" on both MUX-16's, locations 3B and 3C. Remove the 240 ohm resistor between H31 and J31. Install one end of a 1 KΩ, 1/8 W, 5% resistor into J31; leave the other end of the resistor sticking up.

11. Turn the power on and verify the presence of low-going 0.75 μsec pulses on 3A12, 3A13, 3A14, 3A15. Verify the presence of a TTL low on 2B06. Measure the width of the TTL-high part of the waveform at 2B01. It should be ≤ 25 μsec, typically, 20 μsec.

12. Trim the gain and offset of the ADC 80 as described in this section. The gain and offset pots are located as shown on the component layout, page 4. Use the voltage calibrator supply (Digitec, Model 311) to apply -9.9976 volts to channel zero of the MUX by connecting the positive supply output to 3B19 and the negative output to end of the 1 KΩ resistor that was left sticking up. (Use the "REVERSE" feature of the 311 to get the negative voltage.) The inverted ADC output is displayed on the FEDAL chassis' status display and the channel to be monitored is selected with the top digiswitch on the front panel. Select channel 00. Adjust the offset pot so that the display flickers between 0000 and 0001. Apply +9.9927V with the Digitec and adjust the gain pot so that the display flickers between 0FFE and 0FFF. Double check both pot settings and re-adjust if necessary. Verify that an input of 0.0000 V gives a reading of 0800 ± 1.

13. Verify the channel select logic as follows:
   A. Select channel 00 with the digiswitch.
   B. With no signal applied to 3B19, the display should not have a stable reading.
   C. Then apply +5.000 V from the Digitec to 3B19. The display should become stable and read 0C00 ± 1.
   D. Repeat this test for channels 1-31. Corresponding MUX pins are shown in Table 1 on page 3.

14. Measure the inter-channel isolation of the MUXes as follows:
   A. Monitor channel zero with 3B19 connected to 3B12 with an EZ-hook. The display should read 0800 ± 1.
   B. Apply +10 V from the Digitec to 3B20. The reading should change by, at most, 1.
   C. Now apply -10 V. The reading should again change by, at most, 1. (Ideally, it should not change at all.)
   D. Repeat this test for the MUX at 3C: connect 3C19 to 3C12; apply ±10 V to 3C20 and verify the display change as above, monitoring channel 16.
15. Measure the slew rate of the INA-101 amplifier. Using a signal generator, apply a square wave, that goes from +10 V to -10 V with frequency of about 1 kHz, to 3B19. Ground of the signal generator should be on the end of the 1 kΩ test resistor that was left sticking up. Select channel 00 with the digitwitch. Monitor PIN 14 on the ADC-80 with a scope. Verify that the settling time, including the ramp and ringing, on both transitions is less than 150 μsec.

16. Replace the 240 Ω resistor.
TEST PROCEDURE FOR FEDAL-MP CARD

R. J. Lacasse

June 23, 1983
Revised: 7/18/83 and 8/23/83

1. Remove all cards and power supply connections from the front-end data link tester (FEDALT).

2. Put the blank, wired, FEDAL-MP card in the µP slot. (If discrete components are already inserted, they may be left in, with the exception of 3G and 8F.)

3. Test for shorts between the FEDALT's supply inputs.

4. Verify continuity between:

<table>
<thead>
<tr>
<th>+5 V and B 1, 33, 47</th>
</tr>
</thead>
<tbody>
<tr>
<td>C 42, 14</td>
</tr>
<tr>
<td>D 1, 20, 24, 47</td>
</tr>
<tr>
<td>E 33, 38, 42</td>
</tr>
<tr>
<td>F 17, 29, 32, 34, 47</td>
</tr>
<tr>
<td>G</td>
</tr>
<tr>
<td>H 47</td>
</tr>
<tr>
<td>J 38</td>
</tr>
<tr>
<td>K 9, 11, 13, 23, 25, 27, 47</td>
</tr>
<tr>
<td>L 2, 5</td>
</tr>
<tr>
<td>M 47</td>
</tr>
<tr>
<td>N</td>
</tr>
<tr>
<td>P</td>
</tr>
<tr>
<td>R</td>
</tr>
<tr>
<td>S 1, 10, 12, 21, 33, 41</td>
</tr>
<tr>
<td>T 1, 9, 12, 20, 51</td>
</tr>
<tr>
<td>U 2, 10, 14, 20, 33, 41</td>
</tr>
<tr>
<td>V 12, 16, 17</td>
</tr>
<tr>
<td>W 2, 5, 44</td>
</tr>
<tr>
<td>X</td>
</tr>
<tr>
<td>Y 29</td>
</tr>
<tr>
<td>Z</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>+15 V and B 14</th>
</tr>
</thead>
<tbody>
<tr>
<td>J 29</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>+15 V RTN and B 15, 18</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 V RTN and B 15, 18</td>
</tr>
<tr>
<td>-15 V and B 17</td>
</tr>
<tr>
<td>J 33</td>
</tr>
</tbody>
</table>
5. Remove the card and install all its components per the layout on page 5. The 2716 ROM at location 6A should be labeled F000; the 2716 ROM at location 10A should be labeled TEST 7. Double check the component layout and orientation.

6. Connect supplies to the tester.

7. Turn on the supplies and measure the currents consumed by the tester with no cards inserted. Adjust the supply voltages if required to ± 0.1 V of nominal.

8. **Current Consumption Test.** Power off.

   Plug the card into the MP slot. Power on. Measure the incremental currents consumed by the card. These should be in the following ranges:

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5 V</td>
<td>600</td>
<td>800</td>
<td>1500</td>
</tr>
<tr>
<td>+15 V</td>
<td>5</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>-15 V</td>
<td>5</td>
<td>8</td>
<td>15</td>
</tr>
</tbody>
</table>

9. **Power on Reset Test.** Power off.

   Replace the 0.22 μF capacitor at 9B16 to 9B01 with a 15 μF capacitor, plus side to pin 16. Monitor 9A13 with a scope set to 0.5 sec per horizontal division and 2 V per vertical division. When +5 V power is turned on, a 1.0 ± 0.2 sec positive pulse should be seen on this pin. If not, reference schematic sheet 2. Replace the 0.22 μF capacitor.

10. **User Baud Rate Generator Test.**

    Verify a square wave with 52.1 ± 2 μsec period at 4B03 and 4B04. If not, see schematic sheet 10.

11. **Twelve Volt Regulator Test**

    Verify +12 V DC ± 1 V at 4K08 (75150), and -12 V DC ± 1 V at 4K05. If not, see schematic sheet 11.

12. **Three Volt Regulator Test.**

    Verify +3 V DC ± 0.5 V at 3G04 (100 Ω). If not, see schematic sheet 12.

13. **1 MHz Clock Test.**

    Verify 1 MHz square wave at 10B34, 10B35. If not, see schematic sheet 1.

14. **Signal Level and Timing Tests.**

    Remove all boards from the front-end data link chassis (FEDALC). Insert the board under test into the "MP" slot. Place select switch on the front panel to status. Power on. Verify a TTL logic high on 10B 2, 3, 4, 37. Verify reasonable TTL logic switching signals on 10B 8 through 23.
14. (Continued):

Place the select switch in Restart Errors position. Verify the following timing. (Times in nanoseconds, always trigger on scope channel 1.)

Reference schematic sheets 1, 8, 9, if necessary.

15. Enable Signal Test.
Place the select switch in Status.
Verify a 0.75 ± 0.02 µsec pulse on 5F07. Trigger on this waveform. Use the second scope channel to verify similar pulses, each occurring about 19 µsec later than the previous one on:

5F: 9, 10, 11, 12, 13, 14, 15
3F: 7, 9, 10, 11, 12, 15
1F: 7, 9, 10, 11, 12, 13, 14
2F: 14, 13, 12

Reference schematic sheets 15 and 16 if necessary.
16. **Digiswitch and Display Tests.**

Verify that the value on the digiswitches associated with the front panel DVM is displayed on the "Remote" LED display. Try a few values and see that they are all displayed correctly. Do the same for the lower digiswitches, associated with the analog meter; they should be displayed on the "Local" LED display. If not, see schematic sheet 12.

17. **Restart Error Counter Test.**

Place LED display select switch in the restart error position. Turn power off. Replace the .47 µF capacitor at 9B09-9B08 with a 15 µF capacitor, with positive on capacitor to 9B09. Turn power on. The remote display should read 00. Turn power off. Replace the 200 K resistor at 9B07-9B10 with a 100 K resistor. Turn power on. The remote display should count cyclicly from 00 to FF. If not, see schematic sheet 2. Replace the .47 µF capacitor and 200 KΩ resistor.

18. **User UART Test.**

Place LED display select switch in Communication Error position. Jumper pin 2 to pin 3 on the rear panel RS232 connector. Verify that the DVM digiswitches are displayed on the remote LED's. View the transmitted data on the jumpered pins. Verify a two level waveform, with the positive excursion ≥ 6 V and the negative excursion ≤ 6 V. If not, see schematic sheets 10, 11.

19. **Link UART Tests.**

Turn power off.

Remove rear panel jumpers on the digital I/O Elco connector, if present. Install a FEDAL-OUT card on the bottom slot. Install the F800 ROM into 10A. Power on. Verify switching waveforms on the FEDAL-MP connector, pins 55, 56, 57, 58. Verify a roughly 1 Hz TTL switching waveform on 2E07 and 2F07 (6N137's). Verify that the remote status LED's are blanked. Power off. Reference schematic sheets 3 and 5 if required.

20. **Link Receiver Tests.**

Jumper A to C, B to D, E to J, and F to K on the rear panel digital I/O Elco connector. Power on. Verify a switching waveform on 2E06. Verify that both MV50's on the board light. Verify that with the select switch in any of the three positions, both remote and local displays read 00.

21. **Auto-Reset Test.**

Verify .75 µsec pulses with 20 ± 2 msec period on 9C01. Reference schematic sheet 2 if required.
TEST PROCEDURE FOR
FRONT-END DATA LINK OUTPUT CARD TESTS

R. Lacasse
August 23, 1983

1. If connected to the supplies, disconnect the front-end data link tester from the supplies.

2. Separate digital wires on rows G and V from analog wires on rows H and W. Pins 17 and 20 on the DACs are especially sensitive.

3. Remove all cards from the FEDAL tester. Insert the FEDAL out card to be tested in output slot 0, with component side oriented per labels on the tester.

4. Check for shorts between supplies.

5. Use an ohm meter or buzzer to verify the following supply connections:

   +15 V to:
   - Row B: Pin 41
   - Row H: Pins 4, 18, 32, 46
   - Row L: Pins 4, 18, 32, 46
   - Row W: Pins 4, 18, 32, 46

   -15 V, on version 1.2 boards (-15 V decoupling caps plugged in on component side):
   - Row B: Pin 42
   - Row H: Pins 3V, 12, 19V, 26, 35V, 40, 51V, 54
   - Row L: Pins 12, 26, 40, 54
   - Row W: Pins 3V, 12, 19V, 26, 35V, 40, 51V, 54

   -15 V, on version 1.3 boards (-15 V decoupling caps wrapped on wire side):
   - Row B: Pin 42
   - Row H: Pins 12, 26, 40, 54
   - Row J: Pins 9, 23, 37, 51
   - Row L: Pins 12, 26, 40, 54
   - Row W: Pins 12, 26, 40, 54

   15 V RTN, on version 1.2 boards:
   - Row B: Pins 38, 39
   - Row C: Pins 41, 42
   - Row H: Pins 5, 70, 19, 23G, 33, 39G, 47, 55G
   - Row L: Pins 5, 19, 33, 47
   - Row P: Pins 7G, 23G, 39G, 55G
   - Row W: Pins 5, 7G, 19, 23G, 33, 39G, 47, 55G
15 V RTN, on version 1.3 boards:

Row B: Pins 38, 39  
Row C: Pins 41, 42  
Row H: Pins 5, 19, 33, 47  
Row J: Pins 8, 22, 36, 50  
Row L: Pins 5, 19, 33, 47  
Row W: Pins 5, 19, 33, 47

+5 V to:

Row B: Pins 2, 11, 20, 29, 40, 45  
Row D: Pins 1, 12, 23, 45  
Row F: Pins 1, 12, 23, 34, 45  
Row P: Pins 1, 12, 23, 34, 45  
Row S: Pins 1, 12, 23, 34, 45  
Row U: Pins 1, 12, 23, 45

5 V RTN to:

Row C: Pins 9, 18, 27, 36, 38, 39, 54  
Row E: Pins 10, 21, 32, 54  
Row G: Pins 10, 21, 32, 43, 54  
Row R: Pins 10, 21, 32, 43, 54  
Row T: Pins 10, 21, 32, 43, 54  
Row V: Pins 10, 21, 32, 54

6. Remove the card from the tester. Connect the supplies. Turn the supplies on and verify that less than 50 milliamps are drawn by the tester with no cards plugged in.

7. Insert card under test, with no components inserted, into slot Out-0. Verify that supply current does not increase.

8. Remove the card and insert all discrete components. Plug the card back in, and verify that the currents do not change. If they do change, a polarized cap may be in backwards, or a capacitor may be shorted.

9. Turn power off, and install the remainder of the components. Remember to cut off pin 23 on the DAC 80's.

10. Turn power on and verify the following currents (above tester requirements):

   +15 volts ...... 200 mA to 360 mA  
   -15 volts ...... 160 mA to 240 mA  
   +5 volts ...... 400 mA to 900 mA

   If any of these are out of range, find the faulty component, or see if any components are plugged in backwards. Current consumption by chip is as follows:
10. Continued:

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LS138</td>
<td>6.3</td>
<td>typ. 10 max (5 V only)</td>
</tr>
<tr>
<td>LS240</td>
<td>20</td>
<td>typ. 44 max (5 V only)</td>
</tr>
<tr>
<td>LS377</td>
<td>20</td>
<td>typ. 35 max (5 V only)</td>
</tr>
<tr>
<td>HS DAC80</td>
<td>0.0</td>
<td>typ. 0 max (+5 V)</td>
</tr>
<tr>
<td>HS DAC80</td>
<td>30</td>
<td>typ. 36 max (+15 V)</td>
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<tr>
<td>HS DAC80</td>
<td>18</td>
<td>typ. 24 max (-15 V)</td>
</tr>
</tbody>
</table>

11. Turn power off. Insert "Test 3" ROM into the microprocessor board and plug this board into its socket. Turn power back on.

12. Connect scope channel 1 to FEDAL OUT board, pin C5. Trigger scope on channel 1. Verify the presence of 0.75 microsecond, low-going pulses on this pin. If not, see that it is present on FEDAL OUT pin A-39. If it is, FEDAL OUT wiring is at fault. If not, something is wrong with the microprocessor board.

13. Verify the presence of 0.5 microsecond pulses on:

Row B: Pins 4, 5, 6, 12, 13, 14, 15, 21, 22, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 35, 36

Row C: Pins 26, 35

If not, check wiring and address bits A0 to A4 per sheet 1 of the schematic.

14. Verify that the LED's on the tester's test board, locations B7, 12, respond to the toggle switches at locations B8, 13. If not, check wiring per bottom half of sheet 1 of schematic.

15. Ground the scope probe on 15 V TRN, at pin B38. Verify the presence of smooth, negative going ramps that go from +10 V to -10 V in about 780 milliseconds, from each of the DAC's. These ramps can be found on the test board location B01. Pins 1 thru 12 correspond to ANAOUT-0 thru 11 on the schematic sheets 2 thru 7. If the ramps are not smooth, bits are getting lost between the input buffer at 1E (sheet 1) and the DAC's (sheets 2 thru 7), or the DAC's are faulty. With the scope set at a sweep rate of 0.1 sec per div., 5 V per div., internal rising edge triggered, and input DC coupled, the entire ramp can be viewed. Increasing the sweep rate to 200 microseconds per division, 10 millivolts per division, same trigger, and viewing the test points through a 1000 pF capacitor, allows viewing of the small steps in the ramp. Since they are viewed through a 1000 pF capacitor, they appear as small, positive going ramps. The step size should be about 4.9 millivolts in amplitude and 200 microseconds in duration. The "thick grass" hash around the ramps should not be more than 10 to 15 millivolts peak. If it is, digital wires may be coupling into analog wires and should be rearranged, or additional supply decoupling may be required. Large spikes at the transitions are expected; the grass we are concerned about is between the transitions only.
 TEST PROCEDURE FOR
FRONT-END DATA LINK CHASSIS

R. Lacasse

August 22, 1983

Introduction

This test procedure is to be used to debug Front-End Data Link Chassis using a set of cards that are known to be good. Thus, most problems should be attributable to wiring errors. A wiring list is included in Appendix A for reference.

1. Set-Up

   a. Locate the chassis to be tested on two 1" x 1" x 1' pieces of wood to allow air to circulate under the bottom cover.

   b. Connect the chassis to the Front-End Data Link Tester by means of the four multiconductor cables.

   c. Connect a 5 volt supply to the tester and power on. Verify that it supplies ≤ 500 mA.

   d. Connect the resistors at B26 and B27 on the tester to the 15 V Ret. binding post.

   e. Connect AC power to the chassis. Lower the chassis front panel. Power on and measure the supply voltages on the terminal board. Terminal assignments are shown on page A-9. Supplies should be within 10 millivolts of nominal. If not, adjust the supplies

2. Supply Bus Tests

   Power off. Remove the part of the rear cover that protects the connector pins. Power on. Verify the presence of +5 V on pins 2 and 100, 0 V on pins 1, 99, and 69, +15 V on pin 61, and -15 V on pin 65 of each slot.

3. Supply Current Tests

   Power off. Insert a tested set of cards into the card cage. Power on and verify the following supply currents on the terminal board, using a Simpson multimeter or equivalent:

<table>
<thead>
<tr>
<th>Supply</th>
<th>Typ (A)</th>
<th>Max (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5 V</td>
<td>2.7</td>
<td>4.0</td>
</tr>
<tr>
<td>+15 V</td>
<td>0.8</td>
<td>1.2</td>
</tr>
<tr>
<td>-15 V</td>
<td>0.5</td>
<td>0.8</td>
</tr>
</tbody>
</table>
4. **Link Continuity Tests**

   a. Verify that, with the chassis' front panel select switch in STATUS position, both local and remote displays read 00.

   b. Power off. Remove the component carrier at A15 on the tester. Power on. The Status Display should read

   
   Local .... 01
   Remote ... Blank

   for about one second. Then it should read all zeros.

   c. With power on, pull the component carrier at A6. The local display should read 01 in about 1 second.

   d. Replace A6 and A15. The display should go to all zeros immediately.

5. **Digital I/O Test**

   Set Digi-Switch 4 on the TESTER to 70. Verify that the LED's in location B7, B12, B17 and B22 respond to the switches in locations B8, B13, B18, and B23. If not, check the wiring to the Digital I/O connector.

6. **Analog I/O Tests**

   Leave all analog inputs (B26 and B27) tied to 15 V RTN through the 10 KΩ resistors. Apply a 20 V p-p, 1 Hz, sinusoid directly (i.e., on the other side of the resistor) to each of the analog inputs in turn. Verify that the sampled version of the signal appears on the appropriate analog output and that the analog output goes to 0 V when the signal is applied to the next input channel. Analog I/O is summarized in Table 1.

7. **User Limit Tests**

   a. Select channel 00 on the chassis front panel monitor with the digi-switch. Connect a variable DC supply, referenced to 15 V RTN, to Analog Input 0 (B2601). The front panel meter should read the supply voltage. When the supply voltage is turned up to ≥ 9.98 V, ±.02 V, the front panel meter should blink.

   b. Set switch 4 on the Tester to 80. Verify that the LED at B1708-B1709 is off when the front panel meter blinks, and on when it does not (i.e., as the DC input supply is adjusted over and under the limit). Verify the same for analog input channels 1-15. The mapping of channels to LED's is shown in Table 3.

8. **Chassis Temperature**

   After at least a 30 minute warmup period, measure the air temperature inside the chassis in between the cards and in the vicinity of the supplies. The temperature should be ≤ 45°C.

9. **Burn the unit in for 4 to 7 days and repeat steps 1 through 8.**
### TABLE 1: Analog I/O Locations

<table>
<thead>
<tr>
<th>Channel</th>
<th>Analog Input</th>
<th>Analog Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>B26-01</td>
<td>B01-01</td>
</tr>
<tr>
<td>1</td>
<td>-02</td>
<td>-02</td>
</tr>
<tr>
<td>2</td>
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<td>B02-01</td>
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<tr>
<td>13</td>
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<td>B27-01</td>
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<td>B03-01</td>
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<td>-15</td>
<td>-07</td>
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<tr>
<td>31</td>
<td>-16</td>
<td>-08</td>
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</table>

### TABLE 2: Tester Limit LED Locations vs. Analog Input

<table>
<thead>
<tr>
<th>Analog Input</th>
<th>Limit LED Location</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td>B17-08</td>
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<tr>
<td>1</td>
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<tr>
<td>2</td>
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<td>7</td>
<td>-01</td>
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<tr>
<td>8</td>
<td>B22-08</td>
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</tr>
<tr>
<td>14</td>
<td>-02</td>
</tr>
<tr>
<td>15</td>
<td>-01</td>
</tr>
</tbody>
</table>
APPENDIX A

FRONT END DATA LINK CHASSIS WIRING
GENERAL INFORMATION:
1-CONNECTOR DESIGNATIONS:
   S1 THROUGH S5: CARD CAGE WIRE WRAP 100 PIN CONNECTORS, WITH S1 AT TCP
   TB: TERMINAL BOARD ON FLOOR OF CHASSIS
   P1 THROUGH P5: REAR PANEL ELCC AND D CONNECTORS WITH P1 AT TCP
   P6: FRONT PANEL TOP DIGISWITCH, MOST SIGNIFICANT DIGIT
   P7: FRONT PANEL TOP DIGISWITCH, LEAST SIGNIFICANT DIGIT
   F8: FRONT PANEL BOTTOM DIGISWITCH, MOST SIGNIFICANT DIGIT
   P9: FRONT PANEL BOTTOM DIGISWITCH, LEAST SIGNIFICANT DIGIT
   P10: FRONT PANEL DIGITAL PANEL METER CONNECTOR
   P11: FRONT PANEL ANALOG PANEL METER CONNECTORS
   D1: FRONT PANEL DISPLAY, LEFT-MOST DIGIT
   D2: FRONT PANEL DISPLAY, SECOND DIGIT FROM LEFT
   D3: FRONT PANEL DISPLAY, THIRD DIGIT FROM LEFT
   D4: FRONT PANEL DISPLAY, RIGHT-MOST DIGIT
   Sw: FRONT PANEL DISPLAY SECTOR SWITCH, PER SEPARATE SCHEMATIC.
2-INSTALL DIGES ON FRONT PANEL DIGISWITCHES
3-INSTALL ALL BUS-BARS ON CARD CAGE, AND CHECK RESISTANCE BETWEEN PARS.
4-DO THE REST OF THE WIRING IN ANY CONVENIENT ORDER.
5-BUZZ OUT ALL WIRING.
6-KEEP ANALOG WIRING AWAY FROM DIGITAL WIRING. SIGNALS NAMES WHOSE
   FIRST LETTER IS 'A' ARE ANALOG SIGNALS.
MEMBER NAME: FEDALhI

GENERAL INFORMATION

1-SLOTS ARE NUMBERED 1 THROUGH 5 FROM TOP TO BOTTOM.

2-PINS ARE CALLED COLUMNS: SX-YZ, WHERE X IS THE SLOTT NUMBER, 1 THROUGH 5, AND YZ IS THE PIN NUMBER.
   FOR EXAMPLE S4-38 REFERS TO SLOTT 4 PIN 38.

3-A "B" IN THE TO/FRONT COLUMN MEANS THAT THE SIGNAL ON THAT PIN IS BUSSED VERTICALLY THROUGH THE CARD CAGE.
   FOR EXAMPLE, A "B" IN COLUMN 5 MEANS THAT ALL PINS 5 AND 6 IN THE CARD CAGE ARE BUSSED TOGETHER WITH A BUS BAR. PIN 6 IS INCLUDED BECAUSE IT IS OPPOSITE PIN 5 AND THERE IS NO WAY TO BUS PINS 5 TOGETHER WITHOUT ALSO INCLUDING PINS 6.

4-A "NI" IN THE TO/FRONT COLUMN MEANS THAT THE SIGNAL ON THAT PIN IS BUSSED VERTICALLY THROUGH THE CARD CAGE FROM THE ODD PINS OF SLOTT 2 DOWNWARD, I.E., SLOTT 1 AND THE EVEN PINS OF SLOTT 1 ARE NOT INCLUDED IN THIS BUS.

5-A LOWER CASE LETTER IS INDICATED BY A "LESS THAN" SIGN, "<".
   FOR EXAMPLE LOWER CASE L IS PRINTED <L.
<p>| NAME | PIN | TC/FRCM  | | NAME | PIN | TC/FRCM |
|------|-----|----------| | | | |
| 5V RET | 1 | RUNION GND BUS | | *5V | 2 | RUNION VCC BUS |
| 5V RET | 3 | RUNION GND BUS | | *5V | 4 | RUNION VCC BUS |
| C7-  | 5 | G | | C7-  | 6 | B |
| C6-  | 7 | G | | C6-  | 8 | B |
| C5-  | 9 | G | | C5-  | 10 | B |
| C4-  | 11 | G | | C4-  | 12 | B |
| C3-  | 13 | G | | C3-  | 14 | B |
| C2-  | 15 | G | | C2-  | 16 | B |
| C1-  | 17 | G | | C1-  | 18 | B |
| C0-  | 19 | G | | C0-  | 20 | B |
| 21 | | | | 22 | |
| 23 | | | | 24 | |
| 25 | | | | ADCSEL-  | 26 | 51-26 |
| 5V RET | 27 | RUNION GND BUS | | 5V RET | 28 | RUNION GND BUS |
| A1-  | 29 | G | | A1-  | 30 | B |
| AO-  | 31 | G | | AO-  | 32 | B |
| G-  | 35 | G | | G-  | 36 | B |
| 37 | | | | 38 | |
| ANIN-0 | 39 | P1-C | | ANIN-1 | 40 | P1-C |
| ANIN-2 | 41 | P1-C | | ANIN-3 | 42 | P1-C |
| ANIN-4 | 43 | P1-C | | ANIN-5 | 44 | P1-C |
| ANIN-6 | 45 | P1-C | | ANIN-7 | 46 | P1-C |
| 47 | | | | 48 | |
| 5V RET | 49 | RUNION GND BUS | | 5V RET | 50 | RUNION GND BUS |
| 51 | | | | 52 | |
| ANIN-8 | 53 | P1-C | | ANIN-9 | 54 | P1-C |
| ANIN-10 | 55 | P1-C | | ANIN-11 | 56 | P1-C |
| ANIN-12 | 57 | P1-C | | ANIN-13 | 58 | P1-C |
| ANIN-14 | 59 | P1-C | | ANIN-15 | 60 | P1-C |
| +15V | 61 | G | | +15V | 62 | B |
| 63 | | | | 64 | |
| -15V | 65 | B | | -15V | 66 | B |
| PSEUDO GND | 67 | J1-C | | | 68 | |
| 1V RET | 69 | B | | 1V RET | 70 | B |
| 71 | | | | 72 | |
| 5V RET | 73 | RUNION GND BUS | | 5V RET | 74 | RUNION GND BUS |
| 75 | | | | 76 | |
| ANIN-16 | 77 | P1-C | | ANIN-17 | 78 | P1-C |
| ANIN-18 | 79 | P1-C | | ANIN-19 | 80 | P1-C |
| ANIN-20 | 81 | P1-C | | ANIN-21 | 82 | P1-C |
| ANIN-22 | 83 | P1-C | | ANIN-23 | 84 | P1-C |
| ANIN-24 | 85 | P1-C | | ANIN-25 | 86 | P1-C |
| ANIN-26 | 87 | P1-C | | ANIN-27 | 88 | P1-C |
| ANIN-28 | 89 | P1-C | | ANIN-29 | 90 | P1-C |
| ANIN-30 | 91 | P1-C | | ANIN-31 | 92 | P1-C |
| 93 | | | | 94 | |
| 95 | | | | 96 | |
| 5V RET | 97 | RUNION GND BUS | | 5V RET | 98 | RUNION VCC BUS |
| 5V RET | 99 | RUNION GND BUS | | 5V RET | 100 | RUNION VCC BUS |</p>
<table>
<thead>
<tr>
<th>NAME</th>
<th>PIN</th>
<th>TC/FROM</th>
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</thead>
<tbody>
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### Slot 3 Wiring

**Name** | **Pin** | **Pin**
--- | --- | ---
SV REF | 1 | RUNICN GND BUS
SV REF | 3 | RUNICN GND BUS
C7 | 5 | B
C6 | 7 | B
C5 | 9 | B
C4 | 11 | B
C3 | 13 | B
C2 | 15 | B
C1 | 17 | B
C0 | 19 | B
A4- | 21 | N1
A3- | 25 | N1
A2- | 27 | N1
SV REF | 28 | RUNICN GND BUS
A1- | 29 | B
A0- | 31 | B
A0- | 33 | B
A0- | 35 | B
A0- | 37 | B
CUT2 | 39 | S2-37
CUT15-C | 41 | P3-<W
CUT13-C | 43 | P3-<Y
CUT11-C | 45 | P3-AA
CUT9-C | 47 | P3-C
CUT7-C | 49 | RUNICN GND BUS
CUT5-C | 53 | P3-HH
CUT3-C | 55 | P3-KK
CUT1-C | 57 | P3-MM
+15V | 61 | B
+15V | 63 | B
-15V | 65 | B
-15V | 66 | B
SV REF | 69 | B
A0- | 71 | P4-A
SV REF | 73 | RUNICN GND BUS
A0- | 77 | P4-E
A0- | 79 | P4-J
A0- | 81 | P4-L
A0- | 83 | P4-N
A0- | 85 | P4-R
A0- | 87 | P4-U
A0- | 89 | P4-H
A0- | 91 | P4-Y
A0- | 93 | P4-<A
A0- | 95 | P4-<C
SV REF | 97 | RUNICN GND BUS
SV REF | 99 | RUNICN GND BUS

**Notes:**
- **SV REF** points to various wiring connections.
- **CUT** points to specific connections involving the CUT pin.
- **A** and **SV REF** refer to various grounding points.
- **15V** points to various power connections.
- **P** points to specific connections involving the P pin.
| NAME        | PIN | TC/FRCM | | NAME        | PIN | TC/FRCM |
|-------------|-----|---------| | | | |
| 5V RET 1    | 1   | RUNION GND BUS | | 1+5V 2 | RUNION VCC BUS |
| 5V RET 3    | 3   | RUNION GND BUS | | 1+5V 4 | RUNION VCC BUS |
| C7          | 5   | B | | 1C7 6 | P |
| C6          | 7   | B | | 1C6 8 | B |
| C5          | 9   | B | | 1C5 10 | B |
| C4          | 11  | B | | 1C4 12 | P |
| C3          | 13  | B | | 1C3 14 | B |
| C2          | 15  | B | | 1C2 16 | A |
| C1          | 17  | B | | 1C1 18 | P |
| C0          | 19  | B | | 1C0 20 | P |
| A4-         | 21  | N1 | | 1A4- 22 | N1 |
| A3-         | 23  | N1 | | 1A3- 24 | N1 |
| A2-         | 25  | N1 | | 1A2- 26 | N1 |
| 5V RET 27   | 27  | RUNION GND BUS | | 15V RET 28 | RUNION GND BUS |
| A1-         | 29  | B | | 1A1- 30 | B |
| A0-         | 31  | B | | 1A0- 32 | B |
| A-          | 33  | | | 34 | |
| G-          | 35  | B | | 1G- 36 | B |
| 37 | | | | 38 | |
| CUTSEL1-39 | S2-39 | | | 40 | |
| CCUT15-41  | P3-C | | | 42 | P3-D |
| CCUT13-43  | P3-E | | | 44 | P3-F |
| CCUT11-45  | P3-F | | | 46 | P3-J |
| CCUT9-47   | P3-K | | | 48 | P3-L |
| 5V RET 49   | 49  | RUNION GND BUS | | 5V RET 50 | RUNION GND BUS |
| CCUT7-51   | P3-M | | | 52 | P3-N |
| CCUT5-53   | P3-P | | | 54 | P3-R |
| CCUT3-55   | P3-S | | | 56 | P3-T |
| CCUT1-57   | P3-U | | | 58 | P3-V |
| 59 | | | | 60 | |
| +15V 61     | B | | | 62 | B |
| 63 | | | | 64 | |
| -15V 65     | B | | | 66 | B |
| 67 | | | | 68 | |
| 15V RET 69  | B | | | 70 | B |
| ANOUT-71   | P4-K | | | 72 | P4-L TWIST 71-72 |
| 5V RET 73   | RUNION GND BUS | | 74 | RUNION GND BUS |
| ANOUT 1-75  | P4-M | | 76 | P4-N TWIST 75-76 |
| ANOUT2-77   | P4-P | | 78 | P4-R TWIST 77-78 |
| ANOUT3-79   | P4-S | | 80 | P4-T TWIST 79-80 |
| ANOUT4-81   | P5-A | | 82 | P5-B TWIST 81-82 |
| ANOUT5-83   | P5-C | | 84 | P5-D TWIST 83-84 |
| ANOUT6-85   | P5-E | | 86 | P5-F TWIST 85-86 |
| ANOUT7-87   | P5-J | | 88 | P5-K TWIST 87-88 |
| ANOUT8-89   | P5-L | | 90 | P5-M TWIST 89-90 |
| ANOUT9-91   | P5-N | | 92 | P5-P TWIST 91-92 |
| ANOUT10-93  | P5-R | | 94 | P5-S TWIST 93-94 |
| ANOUT11-95  | P5-U | | 96 | P5-V TWIST 95-96 |
| 5V RET 97   | RUNION GND BUS | | 98 | RUNION VCC BUS |
| 5V RET 99   | RUNION GND BUS | | 100 | RUNION VCC BUS |
### SLCT 5 Wiring

**SLCT NAME: CUT2**

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**LOCAL/REMOTE DISPLAY WIRING LIST**

**DEFINITION OF SYMBOLS:**

**DIGIT NUMBERING AS VIEWED FROM OUTSIDE THE CHASSIS:**

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**EXAMPLE:** C3-4 REFERS TO PIN 4 ON THE THIRD DIGIT FROM THE LEFT

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|                     |     | 5 V Supply Return
|                     |     | DPM-A1                  |
|                     |     | Card Cage 5 V Return Bus|
|                     |     | LED Displays, Pin 6     |
| 15 V Ret            | 3   | TB-2                    |
|                     |     | 15 V Supply Return
|                     |     | Card Cage 15 V Return Bus|
| +5 V                | 4   | +5 V Supply             |
|                     |     | DPM-A2                  |
|                     |     | Card Cage +5 V Bus      |
|                     |     | LED Displays, Pin 7     |
| +15 V               | 5   | +15 V Supply            |
|                     |     | Card Cage +15 V Bus     |
| -15 V               | 6   | -15 V Supply            |
|                     |     | Card Cage -15 V Bus     |
| Spare               | 7   |                         |
| AC Neutral          | 8   | Front Panel Power Switch|
|                     |     | +5 V Supply             |
|                     |     | ± 15 V Supply           |
| AC Hot              | 9   | Rear Panel AC Connector |
|                     |     | +5 V Supply             |
|                     |     | ± 15 V Supply           |

### Digital Panel Meter Connector Wiring

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>DPM-</th>
<th>From/To</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 V Ret</td>
<td>A1</td>
<td>TB-2</td>
</tr>
<tr>
<td>+5 V</td>
<td>A2</td>
<td>TB-4</td>
</tr>
<tr>
<td>Mon. -Ø</td>
<td>A14</td>
<td>Mon Ø BNC; S5-89 Twisted</td>
</tr>
<tr>
<td>15 V Ret</td>
<td>A15</td>
<td>BNC Ret; S5-90</td>
</tr>
<tr>
<td>Decimal Pt.</td>
<td>B7</td>
<td>B10</td>
</tr>
</tbody>
</table>

--- Others Not Used ---
Analog Panel Meter Wiring

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>APM</th>
<th>From/To</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mon-1</td>
<td>+</td>
<td>S5-91; Mon 1 BNC</td>
</tr>
<tr>
<td>15 V Ret</td>
<td>-</td>
<td>S5-92; BNC Ret</td>
</tr>
</tbody>
</table>

Select Switch Wiring

```
SELSWEN- (S2-72)  C  P7-1
    1  (LSB)
    2  (MSB)
    3
```

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