NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT No. 242

DIGITAL CONTINUUM RECEIVER HARDWARE

DWAYNE R. SCHIEBEL

JANUARY 1984

NUMBER OF COPIES: 150

DIGITAL CONTINUUM RECEIVER HARDWARE

Dwayne R. Schiebel

After using and modifying the present Digital Standard Receiver it was felt that instead of duplicating this receiver it would be better to build a new receiver. There were several changes incorporated in the new receiver. Some of these changes are listed below:

1. Higher resolution of a phase period, 15.5 μs instead of 1 ms.

2. Phases Ø and 2 will have the same period and phases 1 and 3 will have the same period.

3. Blanking time can be set for one part in sixty-four of a phase period, and can be set for two different times -- one for signal and one for reference.

4. A new switching signal can be generated under calculator control. This signal can switch in advance of the receiver switching signal.

5. Chart recorder channels have been reduced from eight to six; two of the channels have 12-bit resolution and the other four have 8-bit resolution.

6. There are four calibration channels; each channel can fire on any one of four phases.

Programming

The new receiver was designed to give the programmer more flexibility in his control of the receiver. This receiver can be controlled by the HP9826 or the HP9825 desk top computer. The program instructions that follow are for the 9826.

In order for the 9826 to output data to the Digital Continuum Receiver, the program will first have to set a counter to the correct count. This can be accomplished as follows:

```
Let DSR = 12
Control DSR,2;2
Output DSR using "#,W";X (X = Ø - 12)
Control DSR,Ø;1
Control DSR,2;Ø
```

Data can be output with consecutive output commands starting with the highest number and counting down to zero. The words would be output as below:

Word	
Ø	Data to host computer (as many words as necessary)
1	D/A 1 (12 bits). (See note 4.)
2	D/A 2 (12 bits). (See note 4.)
3	D/A 3 and 4 (two channels of 8 bit D/A) (See note 5.)
4	D/A 5 and 6. (See Note 5.)
5	Cal Control. (See Note 1.)
6	#Chs, #Phases, Sig/Ref Adv. (See Note 2.)
7	Blanking. (See Note 3.)
8	Cycles/Integration.
9	Period for Phase Ø and 2 2^0 - 2^{15}
10	Period for Phase Ø and 2 2^{16}- 2^{21} left justified. (See Note 6.)
11	Period for Phase 1 and 3 2^0 - 2^{15}. (See Note 6.)
12	Period for Phase 1 and 3 2^{16}- 2^{21} left justified. (See Note 6.)

Note 1 There are four channels of cal; a 16-bit word is required to control all four channels. A one is output to turn the cal on. At power on cal state is undetermined. The following table lists the cal control.

2^0	Phase Ø CH Ø	2^8	Phase Ø CH 2
2^1	1	2^9	1
2^2	2	2^{10}	2
2^3	3	2^{11}	3
2^4	Phase Ø CH 1	2^{12}	Phase Ø CH 3
2^5	1	2^{13}	1
2^6	2	2^{14}	2
2^7	3	2^{15}	3

Note 2

2^0	Sig Adv LSB (one part in 64 of phase Ø and 2)
2^1	
2^2	
2^3	
2^4	
2^5	
2^6	Ref Adv LSB (one part in 64 of phase 1 and 3)
2^7	
2^8	
2^9	
2^{10}	
2^{11}	
2^{12}	Number of Phase Periods LSB
2^{13}	" " " "
2^{14}	Number of Channels LSB
2^{15}	" " "

Note 3

2^0 Blanking (one part in 64 of Phase Ø and 2) Signal
2^1
2^2
2^3
2^4
2^5
2^6 Blanking (one part in 64 of Phase 1 and 3) Reference
2^7
2^8
2^9
2^{10}
2^{11}

Note 4

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	
0	1	1	1	1	1	1	1	1	1	1	1	*
0	0	0	0	0	0	0	0	0	0	0	0	**
1	0	0	0	0	0	0	0	0	0	0	0	***

* +Full scale
** 0 V
*** -Full scale

Note 5

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	***
---	---	---	D/A 3 & 5	---	---	---	---	---	---	D/A 4 & 6	---	---	---	---	---	

* +Full scale
** 0 V
*** -Full scale

Note 6 The actual phase period output is the phase period minus one. For example, if you output all zeros, you would have a period of 15.5 us.

Various conditions can be controlled within the receiver as follows:

```
Control DSR,2;1
Output DSR using "#,W";Z (see below)
Control DSR,0;1
Control DSR,2;0
```

Output word Z can control from one to three functions at one time:

2^0 | 0 = Reset Fifo
2^1 | 1 = Force End of Scan
2^2 | 2 = No Reset, No End of Scan
3-7 = Not Used
2^3 = Reset Error Status
2^4 = Reset Time Base Counters

The host computer will be interrupted when the 9826 executes the following:

```
Control DSR,2;3
Control DSR,0;1
Control DSR,2;0
```

Receiver data can be input by an "Enter" statement. To read all four channels, a total of 32 words must be input. The data format is listed below:

First Word	Phase 3 MS	Channel 4
	3 LS	
	2 MS	
	2 LS	
	1 MS	
	1 LS	
	0 MS	
	0 LS	

The other three channels are input in sequence (3,2,1) in the same manner as channel 4. The two words for each phase has the following format:

Calculator Bits:

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
Ø	Ø	Ø	2^{27}	-	-	-	-	-	-	-	-	-	-	-	2^{15}	MS Data
Ø	2^{14}	-	-	-	-	-	-	-	-	-	-	-	-	-	2^0	LS Data

After the data has been input, a status word is available from the time the last data word is read until the start of the next integration period. If an error condition exists, it will remain until the program resets the error status. If the program reads this status word, it should normally reset the status word after the start of the scan. The following information is contained in the status word.

2^0 = Ø Receiver 1 Error (VCO too high or integration
2^1 = Ø Receiver 2 Error counter overflow)
2^2 = Ø Receiver 3 Error
2^3 = Ø Receiver 4 Error
2^4 = Ø Missed Reading a Sample
2^5 = Ø Timing is External

Under normal conditions the status word should be 63, if an error developes that status bit will be zero. Status bit 2^5 will be zero as long as the timing is on external, and is unaffected by reset status.

Digital Electronics

The digital electronics is composed of six different types of wire-wrap cards. The following is a brief descriptioin of each card's function:

Card 1 (Slot 3)

The first page of this drawing contains the phase period counters. These counters are loaded with a count depending on which odd or even phase the receiver is on.

Page two of the drawings contain storage--for phase periods, blanking times and advance signal and reference time.

On the left hand side of page three is contained the blanking time generator. The right hand side contains the advanced reference signal.

Page four contains the phase counter and decoder. There are two signals of importance that exit this card:

$\overline{\text{Cycle}}$ Decrements Cycle/Integration Counter on Card 4.

$\overline{\text{2 Cycle}}$ Decrements Center of Integration Counter on Card 4.

Card 2 (Slots 4, 5, 6, & 7)

The first page of this card contains tri-state switches that apply data to the 9826 input bus. These switches are controlled by signals originating on card 4.

The remaining pages contain the integration counters.

Card 3 (Slot 8)

The top of page one of this card contains output data buffers to the host computer. The bottom of the page contains two 8-bit D/A's.

The second page and top of the third page contains four D/A's, two 8-bit and two 12-bit.

The four channel cal generator is at the bottom of page 3.

Card 4 (Slot 9)

This card's main function is communication with the 9826. Page one of this card is involved in generating various control functions. The top of the second page contains the logic that controls the input data to the 9826, while the bottom controls output data. The very bottom of page two contains logic that enables the status word to be applied to the 9826 input bus.

The cycle per integration counter will be found at the top of page three. The logic at the bottom of this page is used to control the integration counters and to skip one receiver cycle after setup data has been output.

Page four contains the host computer interrupt logic. This logic generates three interrupts, center of integration, data and end of scan. The D flip-flop in the lower right of the page disables error checking between scans.

The hex inverters at the top of page five buffer the output bus of the 9826. The logic at the bottom of the page places receiver status on the calculator status lines and interrupts the calculator at start of scan.

Card 5 (Slot 10)

The top half of the first page of Card 5 contains optical-isolated gates. These gates are connected to the receiver voltage controlled oscillator. At present a Teledyne Philbrick 4707 voltage to frequency converter is being used. Blanking is applied to the VCO signal before it goes to the integrator counters (Card 2). The bottom of this page contains logic that interfaces external switching, calibration, and blanking to the digital logic.

The logic on page two is used to check the VCO frequency. When the VCO reaches about 4.1 MHz an error will be indicated. The

D flip-flop at the bottom of the page is used to prevent the error checking logic from getting a false counter overflow condition at integrator reset time.

The top two-thirds of page three has logic that sets a error condition on a one to zero transition out of the last stage of the integrator counters. The logic at the bottom of the page applies status information to the 9826 input bus.

Page four contains logic for front panel indication of receiver error and VCO input level.

Card 6 (Slot 11)

The first page of Card 6 contains logic to driver front panel light emitting diodes and a power supply monitor at the bottom of the page. The signal "PSTS" can be checked by the 9826 to see if the digital logic has power applied.

The last page of this set of drawings contains drivers for calibration, switching, advanced switching, blanking and all four phases.

Diagnostics

A diagnostic disk has been prepared for this system. To use the diagnostics, insert the disk and turn on power. Instructions will be displayed on the CRT. Test 3 is a useful test of the integration counters. With a known frequency in on the test box, this program computes the integrator count and displays the difference. A full test, reading receiver data and sending dummy data to the host computer is available in Test 5.

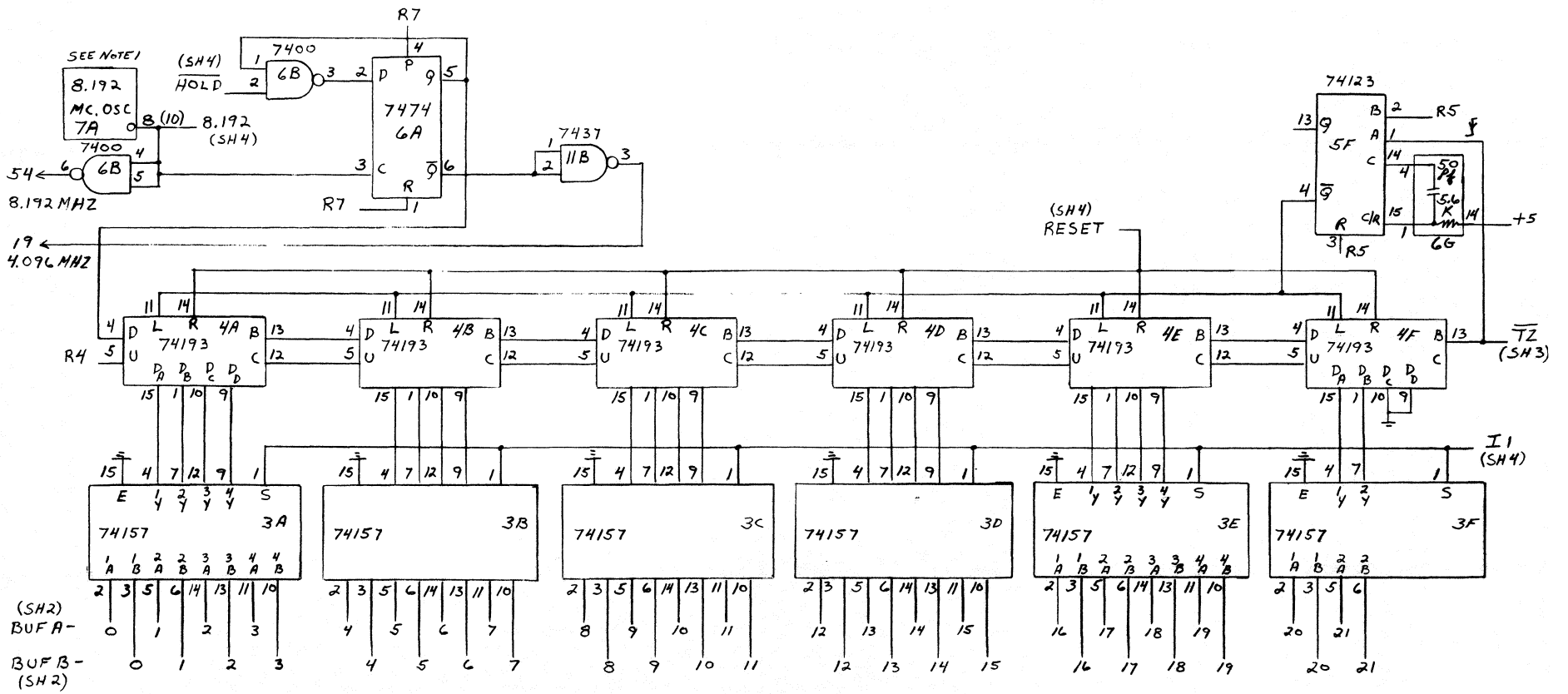
Credits

Credit is given to R. Weimer and R. Fisher for their help in designing this system. The construction of this project was performed by W. Vrable and J. Turner. The chassis was built by the Green Bank Machine Shop.

Memonic List

Memonic	Origin Slot	
ADV SIG	3	Advanced Switching Signal
BLØ	9	Loads Blanking Time
BLTM OUT	3	Combined Internal & External Blanking
CA X	10	Blanked VCO Signal
CAL $\overline{\text{CH X}}$	8	Calibration Signal
CHSEL	9	Input Word Channel Select
CRX	8	Analog Out to Chart Recorder
$\overline{\text{CTLX}}$	8	Control Signals from Calculator
$\overline{\text{CYCLE}}$	3	One Cycle of Receiver
$\overline{\text{2 CYCLE}}$	3	Twice the Frequency of Cycle
$\overline{\text{DACXX}}$	9	Data Strobe for D/A
DAR X	9	Calculator Input Counter Decoded
$\overline{\text{DAVAIL}}$	9	Data is available for Calculator
DØ-15	9	Buffered Calculator Output Data
DIØ-15	4-7, 10	Calculator Input Bus
$\overline{\text{DO}}\overline{\text{Ø}}\text{-}\overline{\text{15}}$	Calculator	Data Out of Calculator
DOUT CX	4-7	Carry from Last Integrator Stage
DOA X	8	Data to Host Computer
$\overline{\text{EIR}}$	9	Interrupt to Calculator
ENB ERR	9	Inhibits Error Condition Between Scan
END	Host Comp.	End Scan from Host Computer
HDSTB	9	Data Strobe for Host Computer
I1A I2A	3	Phase Counter before Decode
INT BLM	3	Internal Blanking

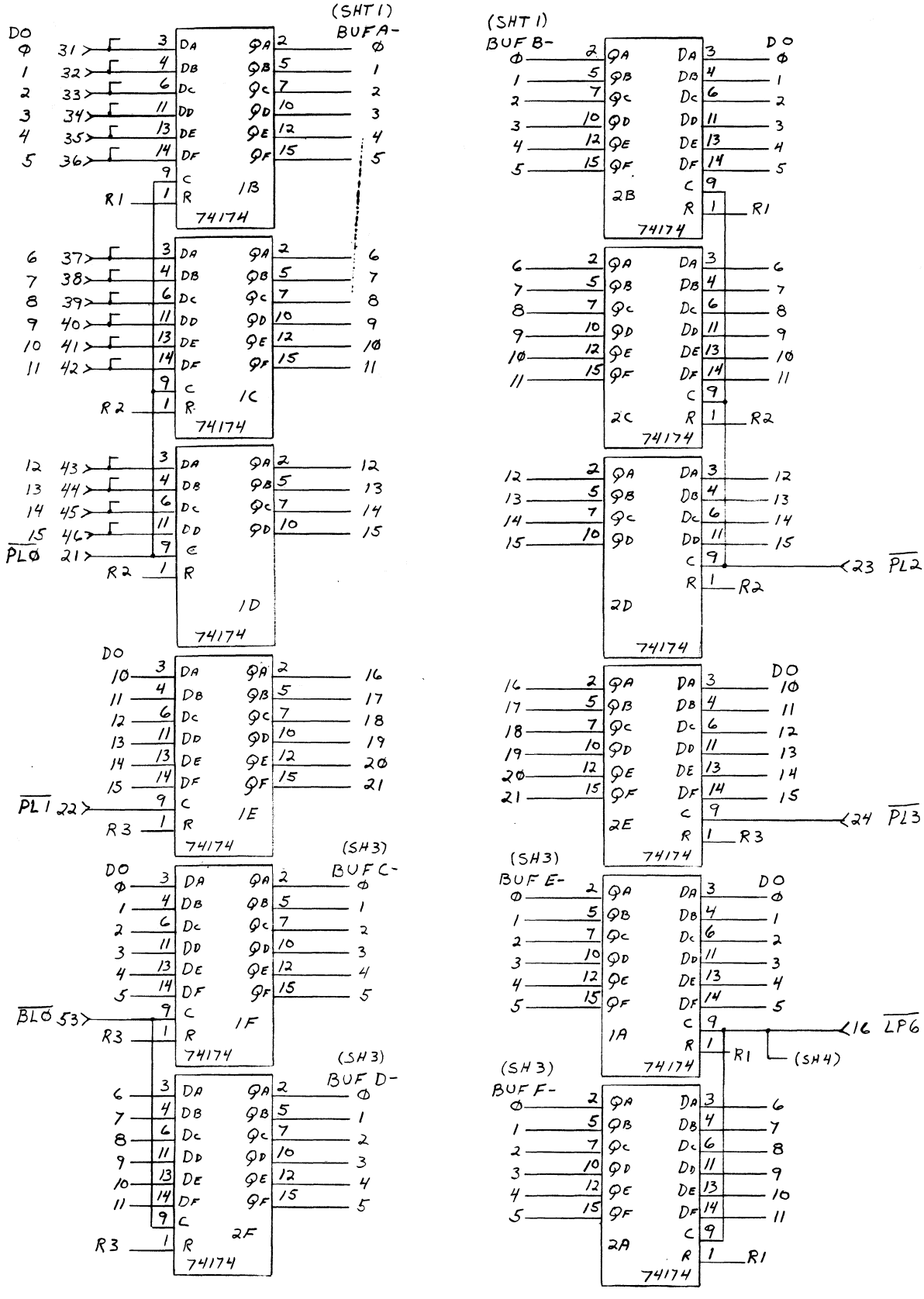
Memonic	Origin Slot	
I/O	Calculator	Input/Output from Calculator
$\overline{\text{LAST}}$	9	Indicates Calculator Read All Counter Data
$\overline{\text{LINTD}}$	8	Latch Integrator Data
$\overline{\text{LP5}}$	9	Data Strobe for Calibration
$\overline{\text{LP6}}$	9	Data Strobe for #Chs, #Phases, ADV.SIG.
$\overline{\text{PCTL}}$	Calculator	Peripheral Control Line
$\overline{\text{PFLG}}$	9	Completes Data Transfer with Calculator
PHASE X	3	One of a Possible of Four Rec. Phases
PILØ9 SET	9	Interrupt to Host Computer
$\overline{\text{PLX}}$	9	Loads Phase Period in Buffer
$\overline{\text{RCTR}}$	9	Reset Phase Period Counters
$\overline{\text{RESET}}$	Calculator	Peripheral Reset
RESET INT	9	Reset Integrator Counters
$\overline{\text{RESET OFSTAT}}$	9	Reset VCO Error Status
RFIFO	9	Reset Host Computer Fifo
$\overline{\text{SAMPLE IGNORED}}$	9	Calculator Missed a Sample
SCAN	Host Comp.	Start Scan from Host Computer
$\overline{\text{STIX}}$	9	Receiver Status to Calculator
VCO X	Receiver	VCO from Receiver



NOTE 1 14 PIN CHIP IN A 16 PIN LOCATION
( ) = 16 PIN #
FREQ = 8.214429 MHZ

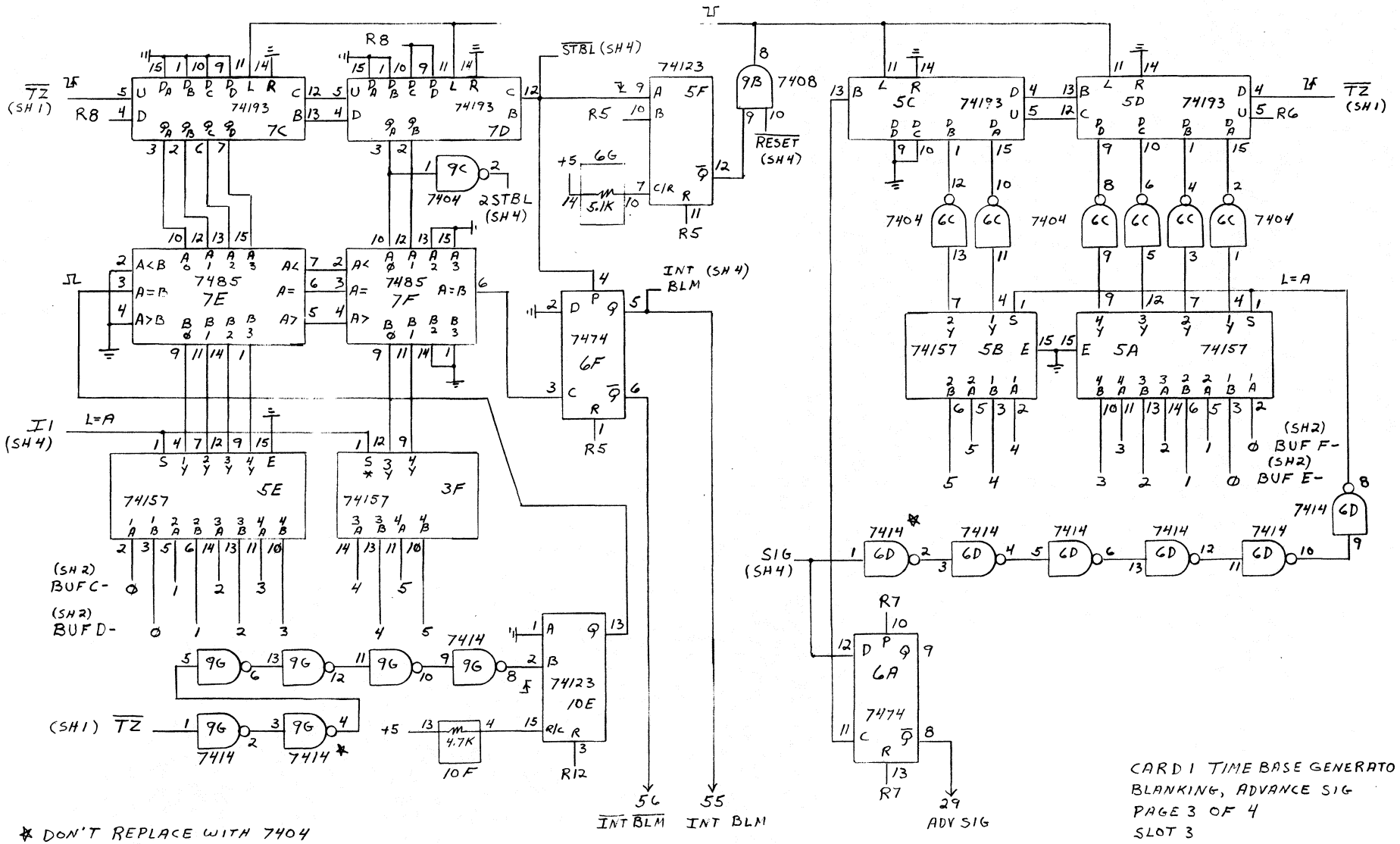
CARD 1 TIME BASE GENERATO

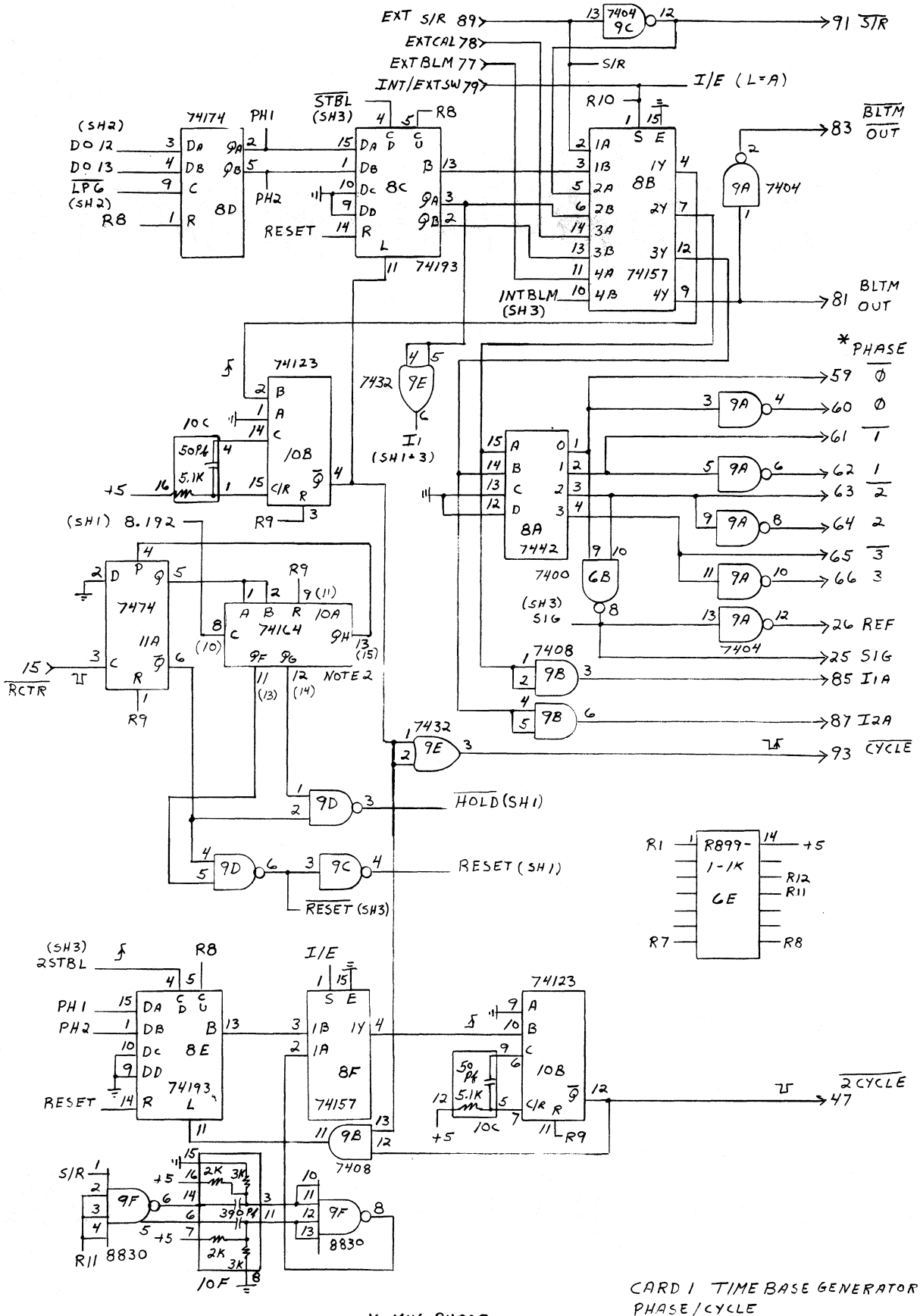
PHASE PERIOD
VARRIABLE DIVIDER
PAGE 1 OF 4
SLOT 3



BUF A = PHASE Ø + 2
BUF B = PHASE 1 + 3
BUF C = BLANKING PHASE Ø + 2
BUF D = BLANKING PHASE 1 + 3
BUF E = SIG ADVANCE
BUF F = REF ADV

CARD 1 TIME BASE GENERATOR
BUFFERS
PAGE 2 OF 4
SLOT 3

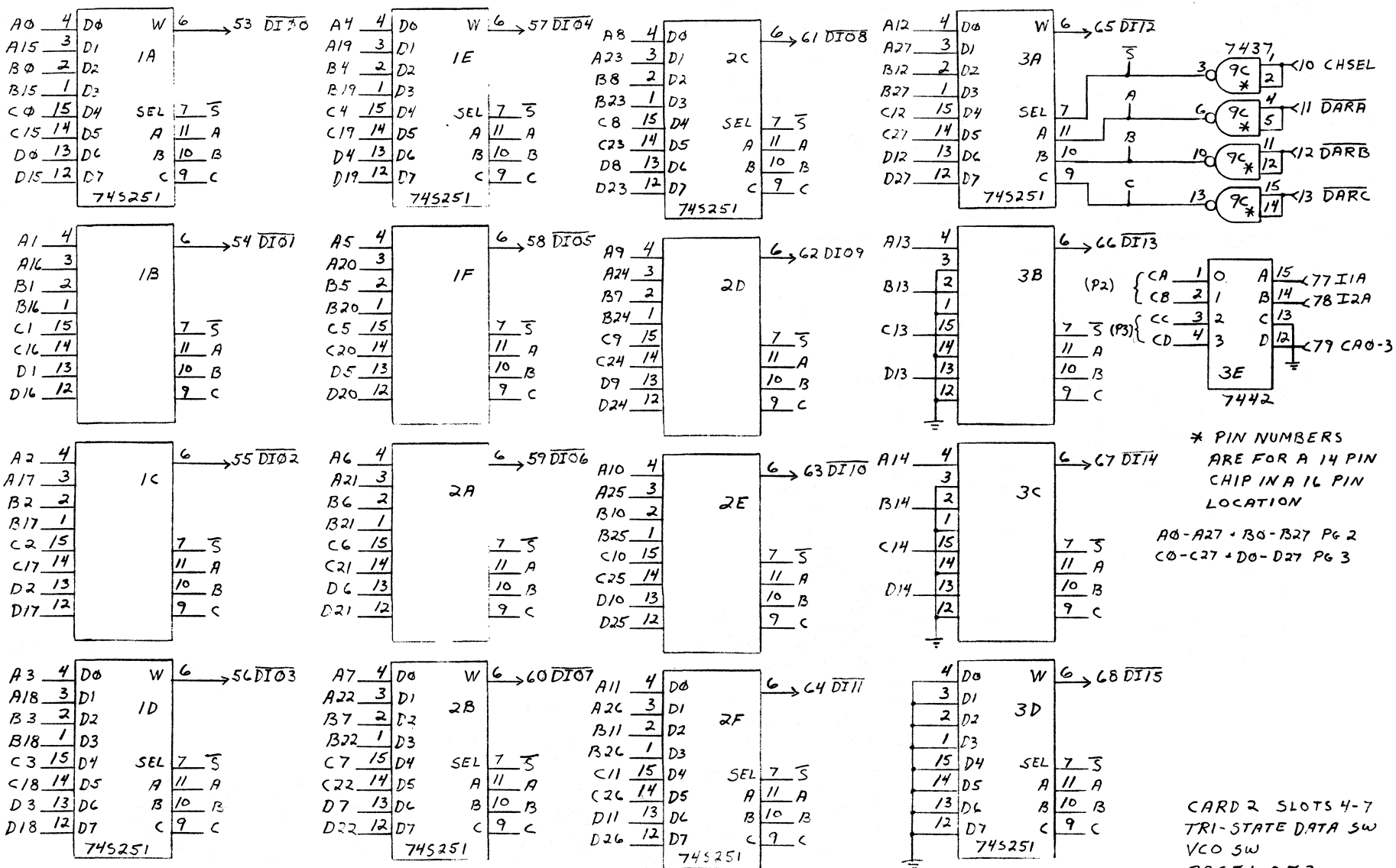

74193 7C
74193 7D
74193 5C
74193 5D
7485 7E
7485 7F
74123 5F
74123 10E
7408 9B
7404 9C
7404 6C
7404 6C
7414 9G
7414 6D
7474 6F
7474 6A
74157 5E
74157 3F
74157 5B
74157 5A
R8
R5
R12
R7
R6
10F
STBL (SH4)
2STBL (SH4)
RESET (SH4)
INT (SH4) BLM
TZ (SH1)
I1 (SH4)
L=A
SIG (SH4)
(SH2) BUF C-
(SH2) BUF D-
(SH2) BUF F-
(SH2) BUF E-
56 INT BLM
55 INT BLM
29 ADV SIG
★ DON'T REPLACE WITH 7404
★ REFERENCE ONLY, SEE PAGE 1 FOR OTHER HALF OF CHIP
CARD 1 TIME BASE GENERATO
BLANKING, ADVANCE SIG
PAGE 3 OF 4
SLOT 3

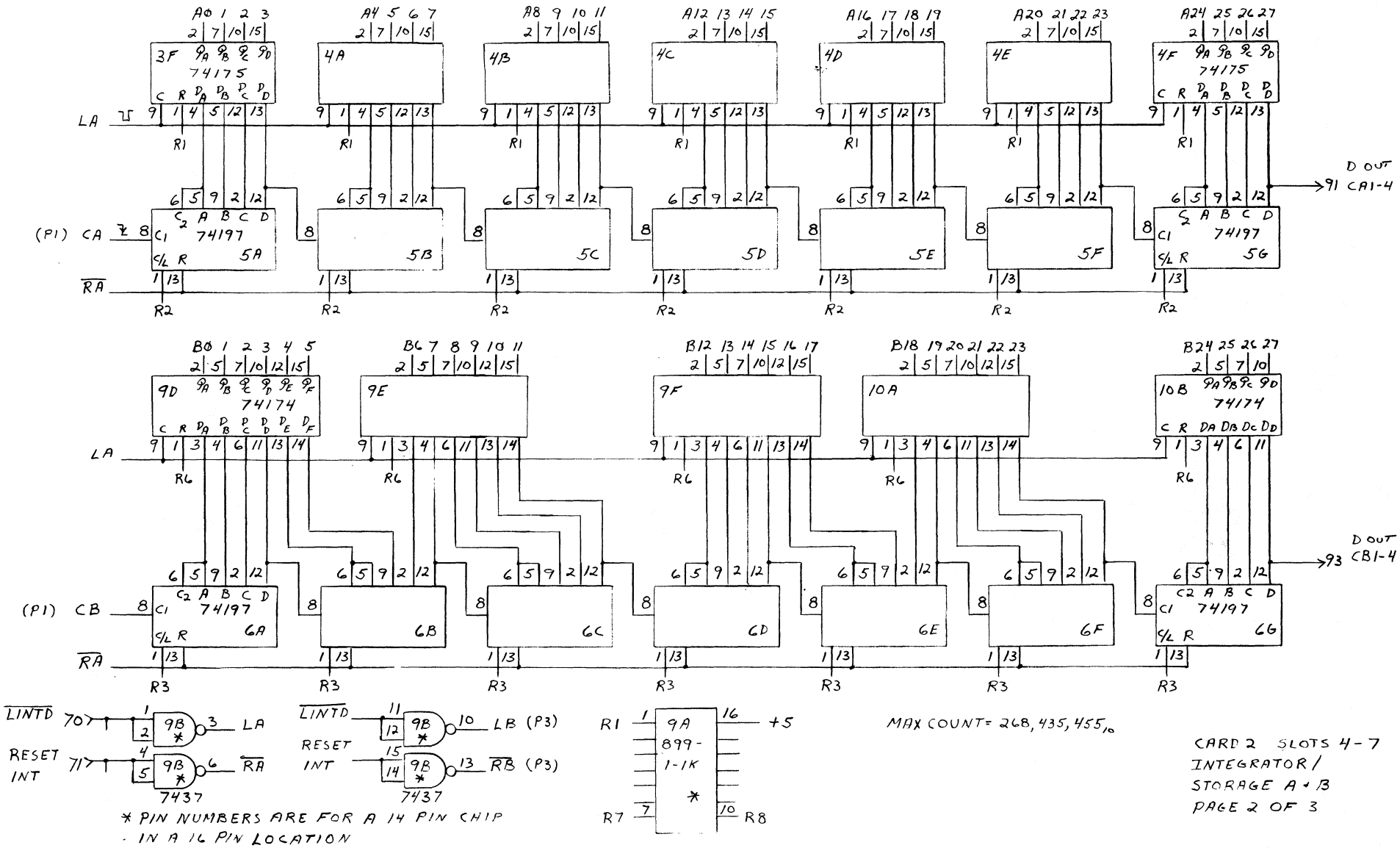


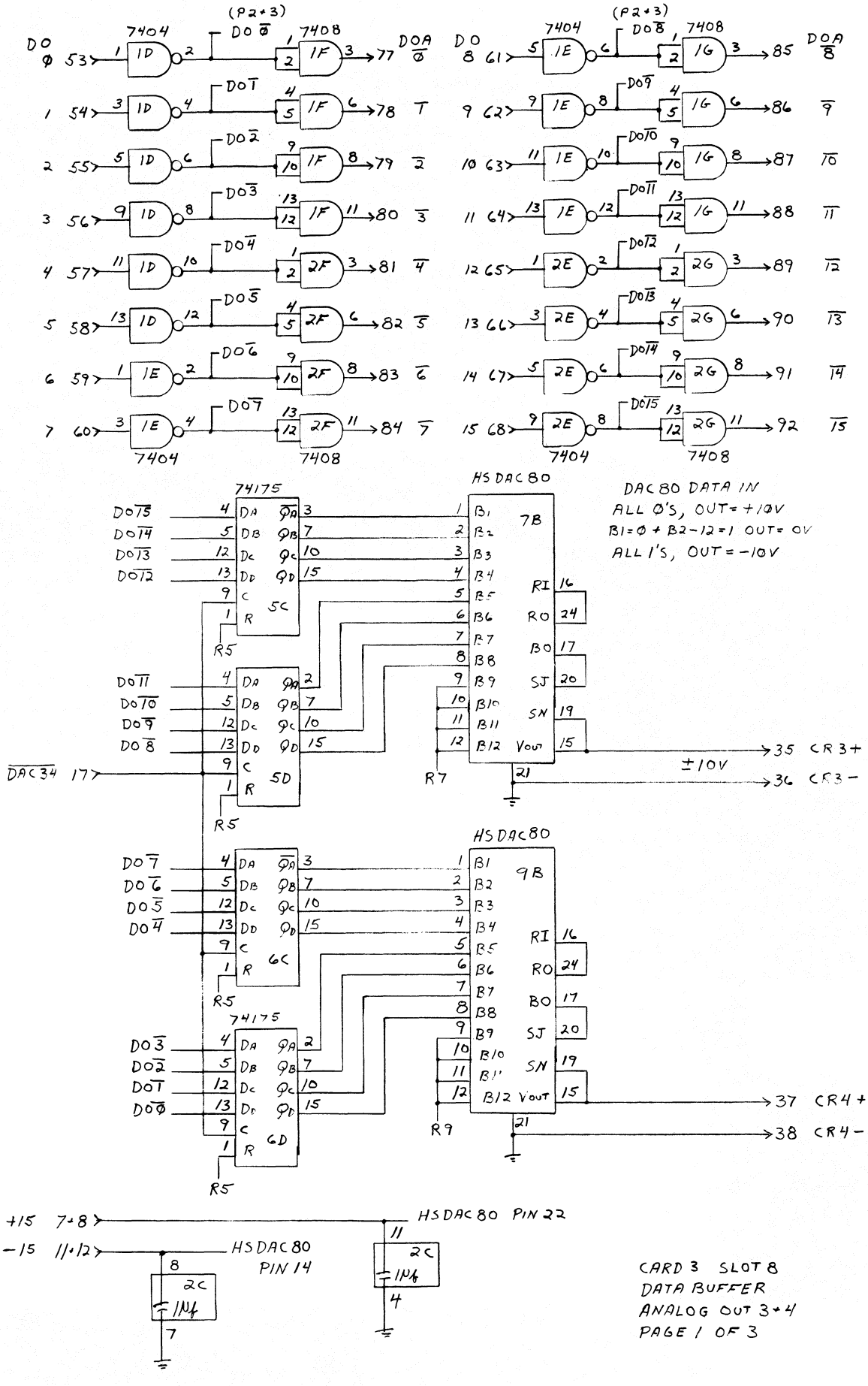
NOTE 2 14 PIN CHIP IN A 16 PIN LOCATION
( ) = 16 PIN NUMBER

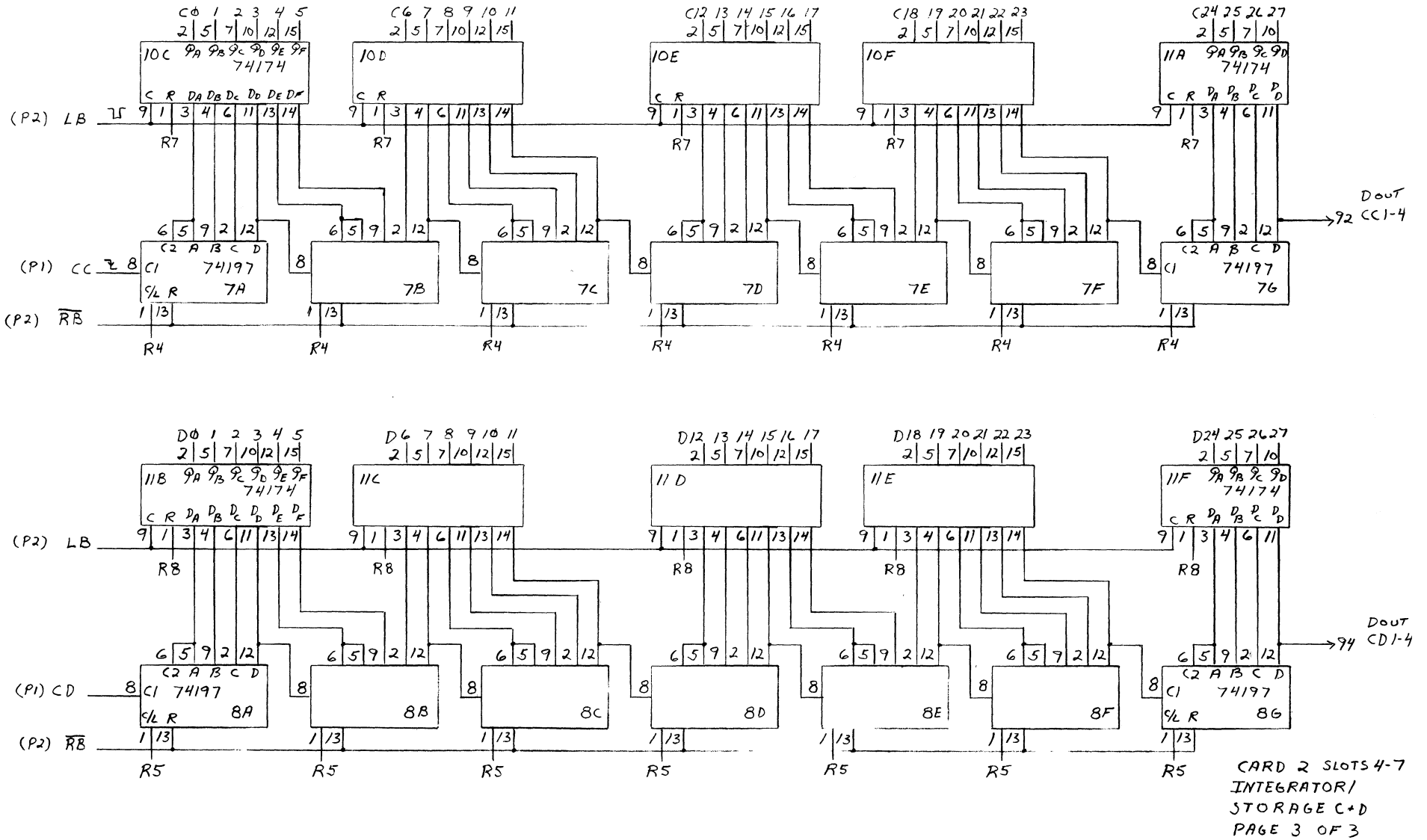
* MIN. PHASE PERIOD = 15.56 NS

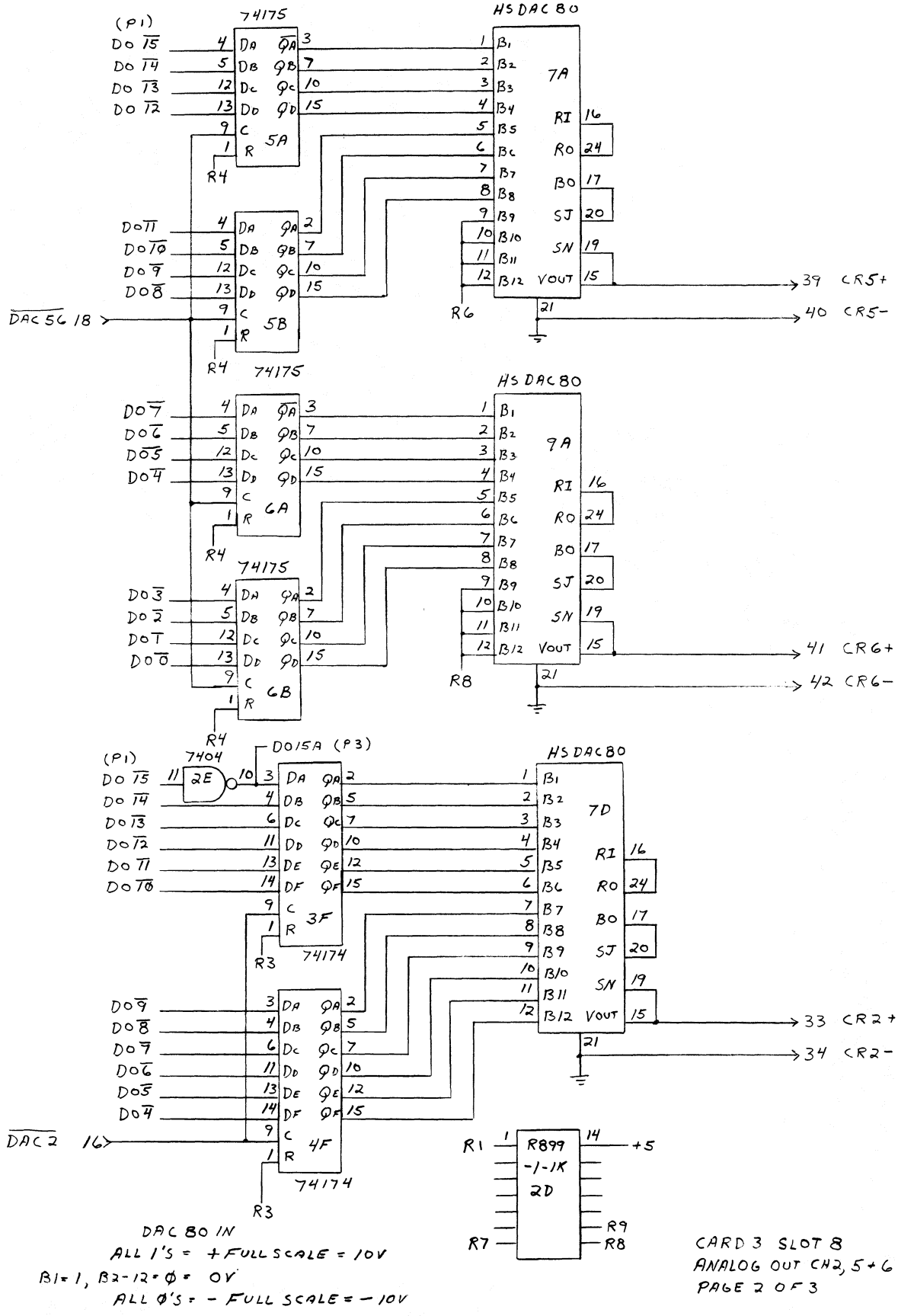
CARD 1 TIME BASE GENERATOR
PHASE/CYCLE
START SCAN RESET
CENTER INTEGRATION CLK
PAGE 4 OF 4
SLOT 3

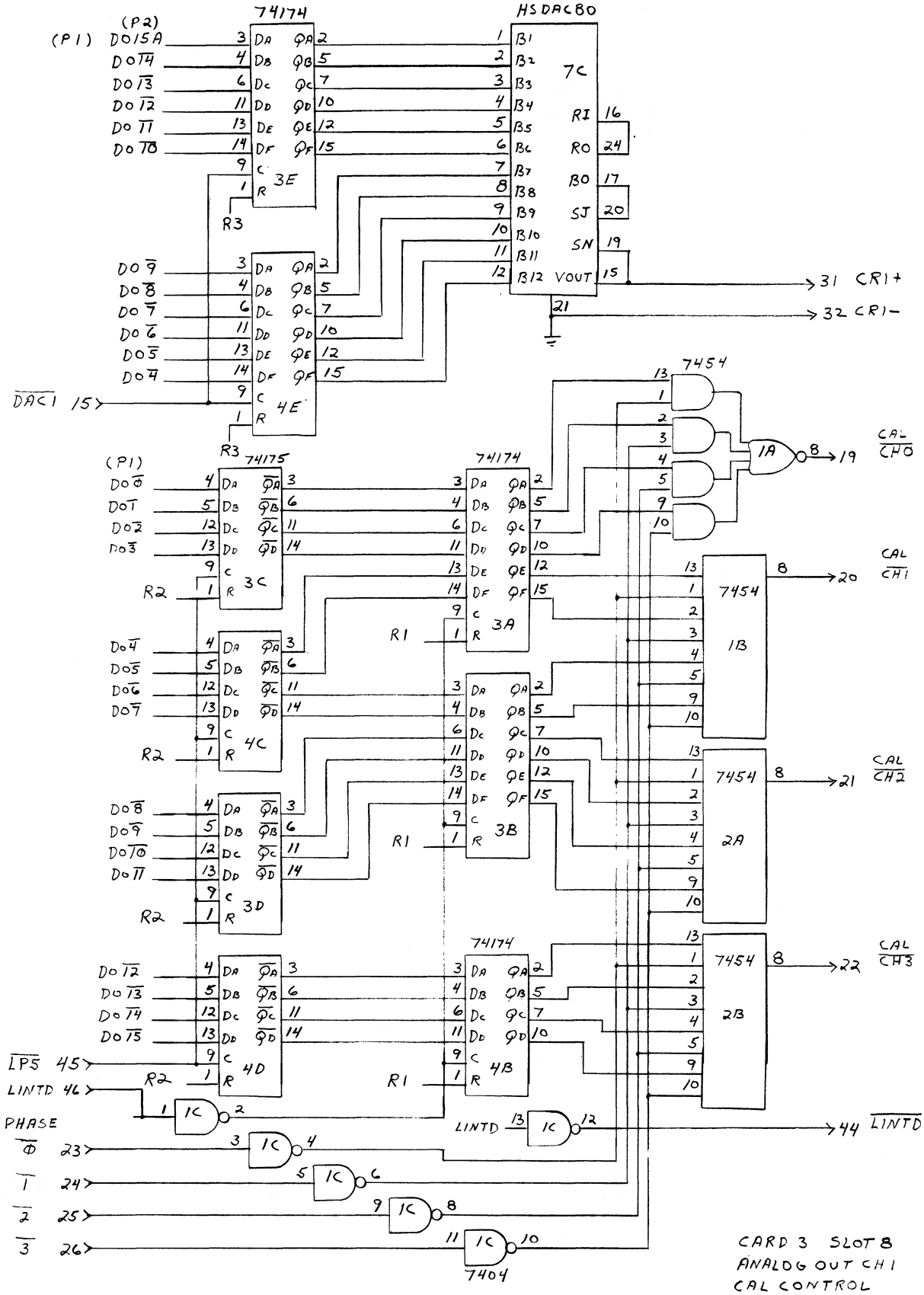

1A
1E
2C
3A
1B
1F
2D
3B
1C
2A
2E
3C
1D
2B
2F
3D
745251
7437
7442
3E
53 DI*0
57 DI04
61 DI08
65 DI12
54 DI01
58 DI05
62 DI09
66 DI13
55 DI02
59 DI06
63 DI10
67 DI14
56 DI03
60 DI07
64 DI11
68 DI15
10 CHSEL
11 DARA
12 DARB
13 DARC
(P2)
(P3)
77 I1A
78 I2A
79 CA0-3
* PIN NUMBERS ARE FOR A 14 PIN CHIP IN A 16 PIN LOCATION
A0-A27 • B0-B27 PG 2
C0-C27 • D0-D27 PG 3
CARD 2 SLOTS 4-7
TRI-STATE DATA SW
VCO SW
PAGE 1 OF 3

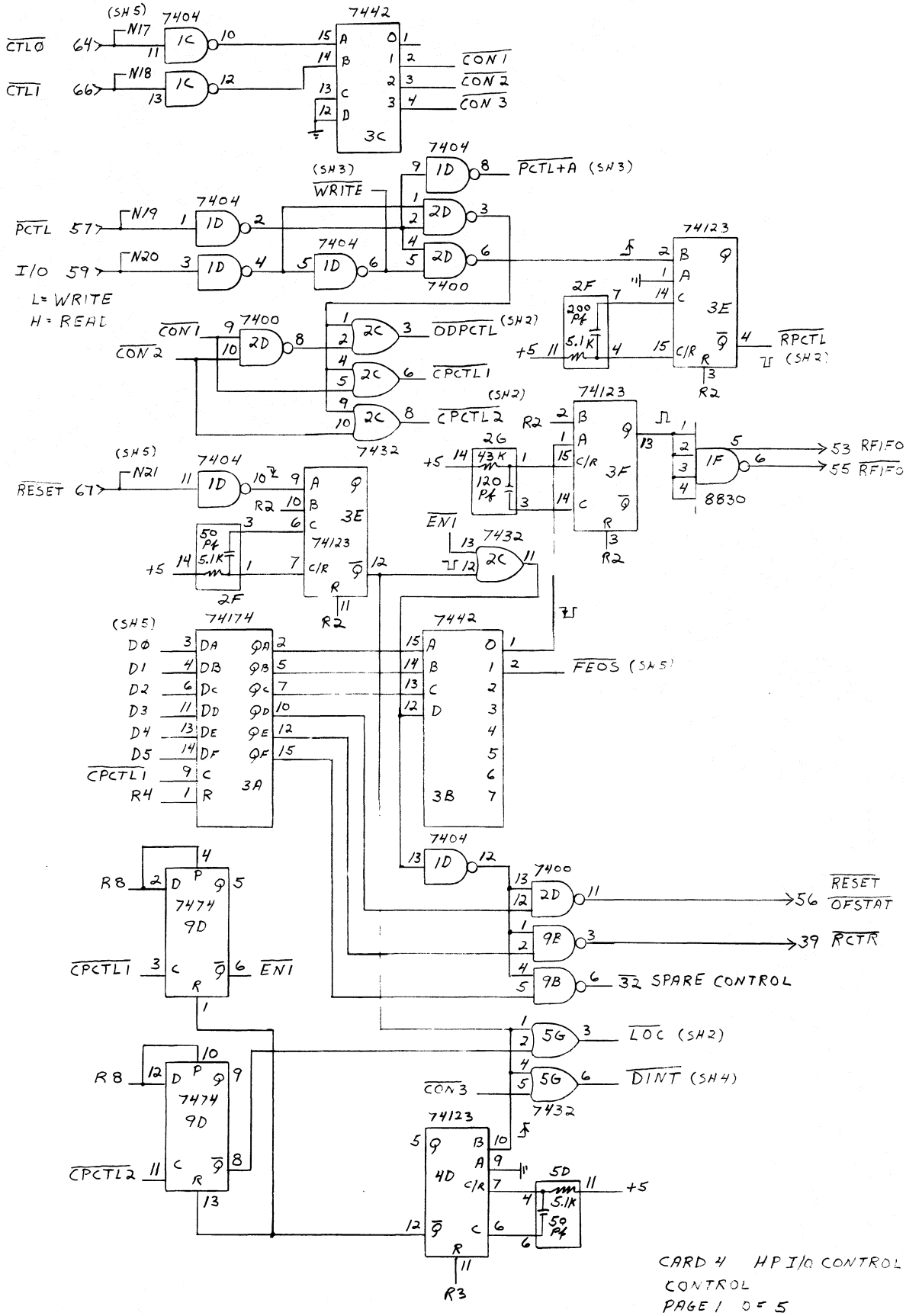

A0 1 2 3
A4 5 6 7
A8 9 10 11
A12 13 14 15
A16 17 18 19
A20 21 22 23
A24 25 26 27
3F 74175
4A
4B
4C
4D
4E
4F 74175
LA
R1
D OUT
91 CA1-4
(P1) CA
5A 74197
5B
5C
5D
5E
5F
5G 74197
RA
R2
B0 1 2 3 4 5
B6 7 8 9 10 11
B12 13 14 15 16 17
B18 19 20 21 22 23
B24 25 26 27
9D 74174
9E
9F
10A
10B 74174
R6
D OUT
93 CB1-4
(P1) CB
6A 74197
6B
6C
6D
6E
6F
6G 74197
R3
LINTD
RESET INT
7437
LA
RA
LB (P3)
RB (P3)
* PIN NUMBERS ARE FOR A 14 PIN CHIP
IN A 16 PIN LOCATION
R1
9A
899-1-1K
+5
R7
R8
MAX COUNT = 268,435,455₁₀
CARD 2 SLOTS 4-7
INTEGRATOR/
STORAGE A & B
PAGE 2 OF 3


(P2+3)
7404
7408
DO Ø
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DOA Ø
DO 8
DO 9
DO 10
DO 11
DO 12
DO 13
DO 14
DO 15
74175
HSDAC80
DAC80 DATA IN
ALL Ø'S, OUT=+10V
B1=Ø + B2-12=1 OUT=0V
ALL 1'S, OUT=-10V
DO 15
DO 14
DO 13
DO 12
DO 11
DO 10
DO 9
DO 8
DO 7
DO 6
DO 5
DO 4
DO 3
DO 2
DO 1
DO Ø
DAC 34
5C
5D
6C
6D
7B
9B
R5
R7
R9
±10V
+15
-15
HSDAC80 PIN 22
HSDAC80 PIN 14
2C
.1Mf
CARD 3 SLOT 8
DATA BUFFER
ANALOG OUT 3+4
PAGE 1 OF 3

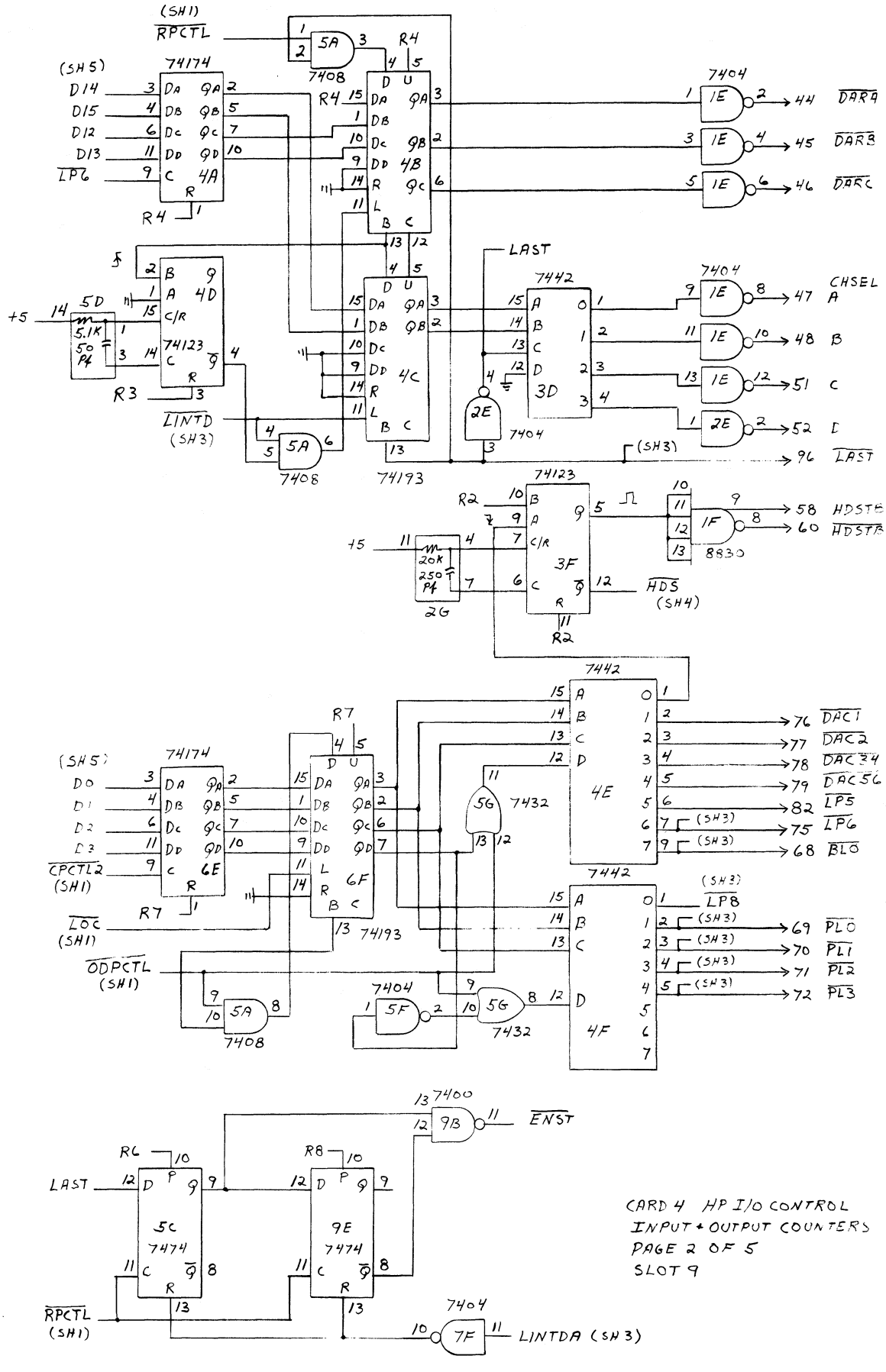

C0 1 2 3 4 5
C6 7 8 9 10 11
C12 13 14 15 16 17
C18 19 20 21 22 23
C24 25 26 27
10C 74174
10D
10E
10F
11A 74174
(P2) LB
R7
DOUT
92 CC1-4
(P1) CC
74197
7A
7B
7C
7D
7E
7F
7G
(P2) RB
R4
D0 1 2 3 4 5
D6 7 8 9 10 11
D12 13 14 15 16 17
D18 19 20 21 22 23
D24 25 26 27
11B 74174
11C
11D
11E
11F 74174
R8
94 CD1-4
(P1) CD
8A
8B
8C
8D
8E
8F
8G
R5
CARD 2 SLOTS 4-7
INTEGRATOR/
STORAGE C+D
PAGE 3 OF 3


(P1)
DO 15
DO 14
DO 13
DO 12
74175
5A
R4
HSDAC80
7A
RI
RO
BO
SJ
SN
VOUT
R6
39 CR5+
40 CR5-
DO 11
DO 10
DO 9
DO 8
5B
DAC 5C 18
74175
DO 7
DO 6
DO 5
DO 4
6A
74175
DO 3
DO 2
DO 1
DO 0
6B
HSDAC80
9A
R8
41 CR6+
42 CR6-
(P1)
DO 15
DO 14
DO 13
DO 12
DO 11
DO 10
7404
2E
DO15A (P3)
3F
74174
R3
HSDAC80
7D
33 CR2+
34 CR2-
DO 9
DO 8
DO 7
DO 6
DO 5
DO 4
4F
74174
DAC 2 16
R1
R899
-/-1K
2D
R7
R9
R8
+5
DAC 80 IN
ALL 1'S = +FULL SCALE = 10V
B1=1, B2-12=0 = 0V
ALL 0'S = -FULL SCALE = -10V
CARD 3 SLOT 8
ANALOG OUT CH2, 5+6
PAGE 2 OF 3

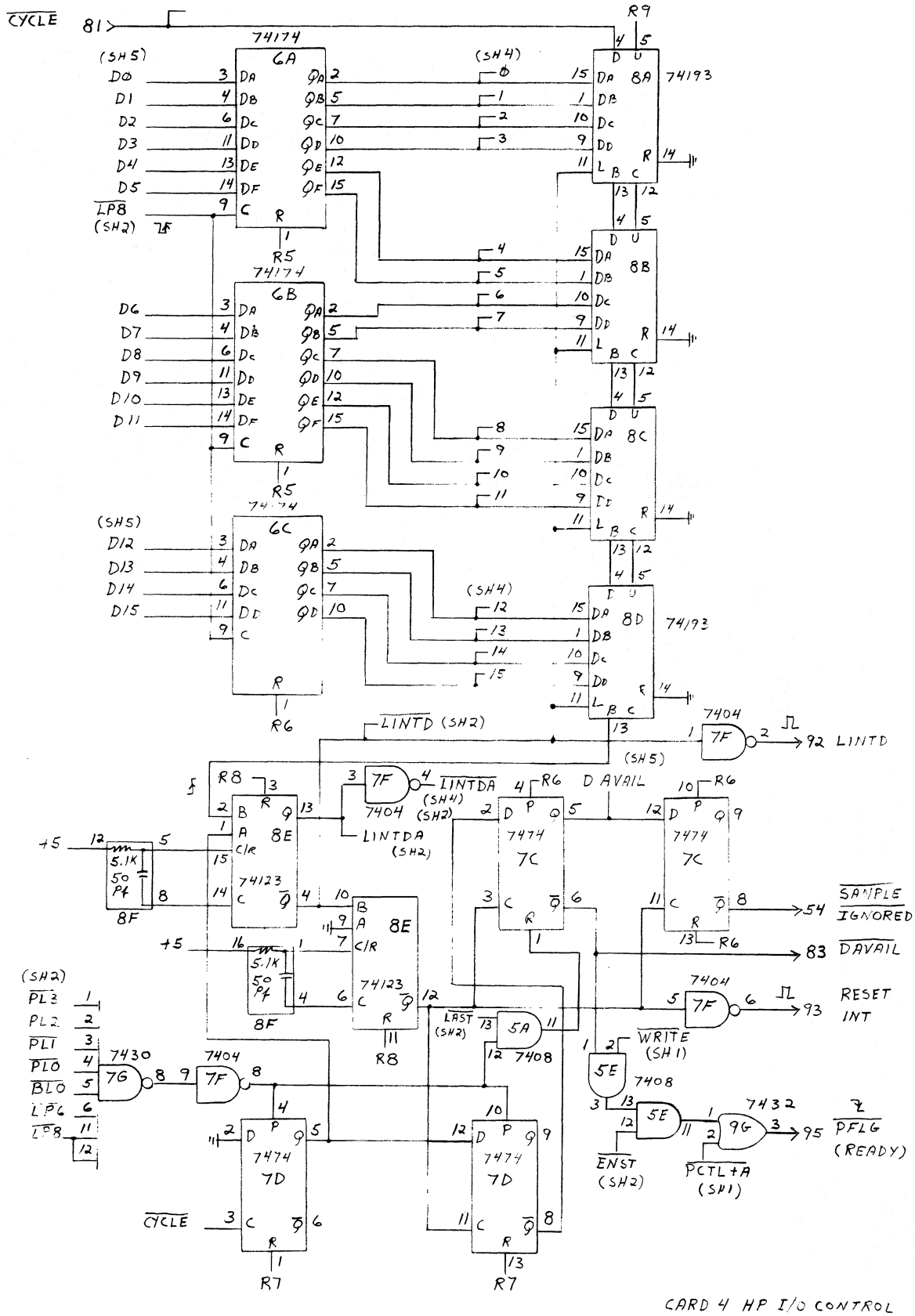

74174
HSDAC80
(P2)
(P1)
D015A
D014
D013
D012
D011
D010
3E
R3
D09
D08
D07
D06
D05
D04
4E
DAC1 15
7C
RI 16
RO 24
BO 17
SJ 20
SN 19
VOUT 15
31 CR1+
32 CR1−
21
7454
CAL CH0
CAL CH1
CAL CH2
CAL CH3
1A
1B
2A
2B
74175
3C
4C
3D
4D
3A
3B
4B
R1
R2
LP5 45
LINTD 46
PHASE
Φ 23
1 24
2 25
3 26
LINTD
44 LINTD
7404
CARD 3 SLOT 8
ANALOG OUT CH 1
CAL CONTROL
PAGE 3 OF 3


CTL0
CTL1
PCTL
I/O
L = WRITE
H = READ
RESET
CON1
CON2
CON3
WRITE
ODPCTL
CPCTL1
CPCTL2
RPCTL
ENI
FEOS
LOC
DINT
RESET OFSTAT
RCTR
SPARE CONTROL
53 RFIFO
55 RFIFO
56
39
7404
7442
7400
7432
74123
74174
7474
8830
CARD 4 HP I/O CONTROL
CONTROL
PAGE 1 OF 5
SLOT 9

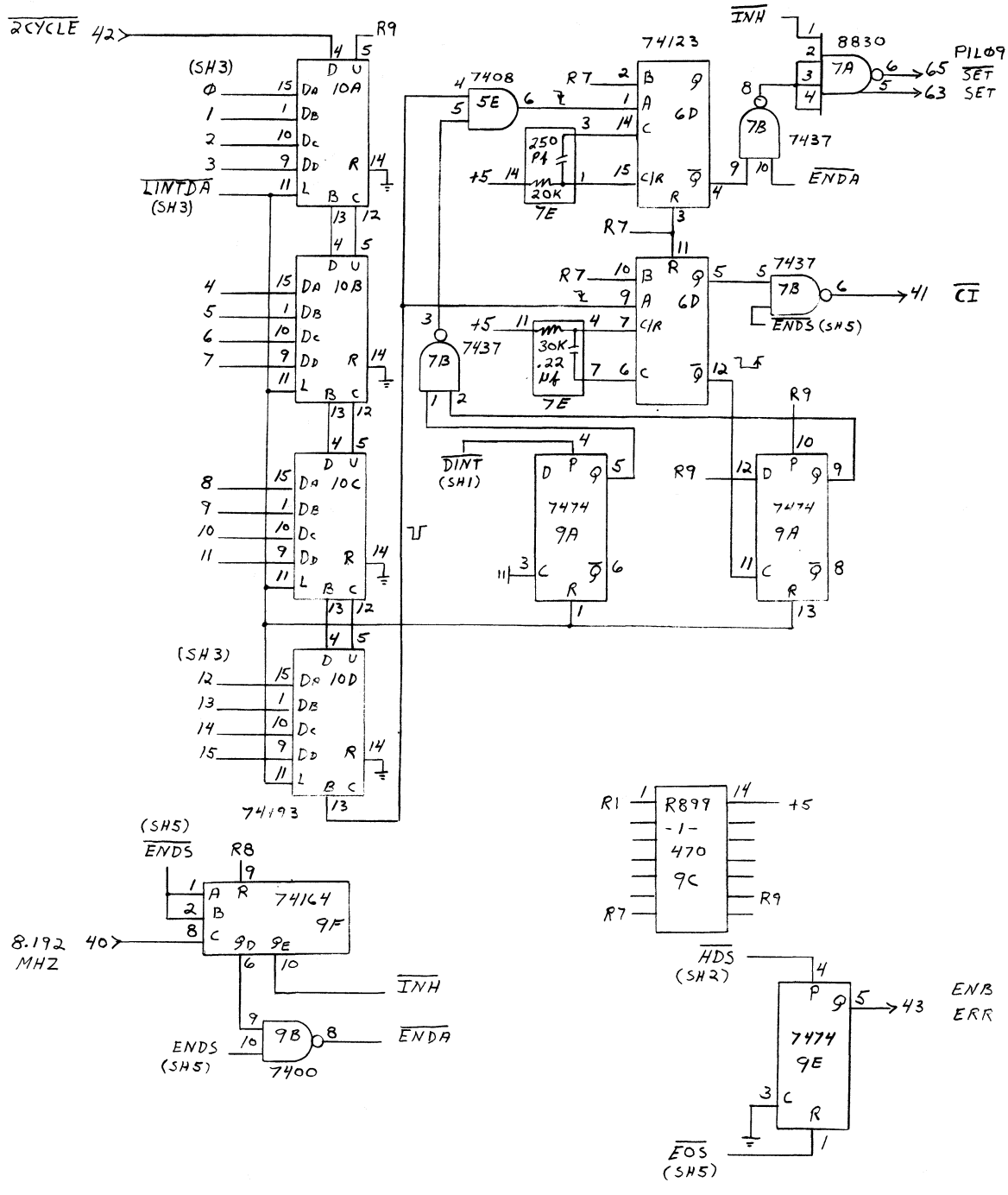
D14 + 15 = CH#
D12 + 13 = #PHASES



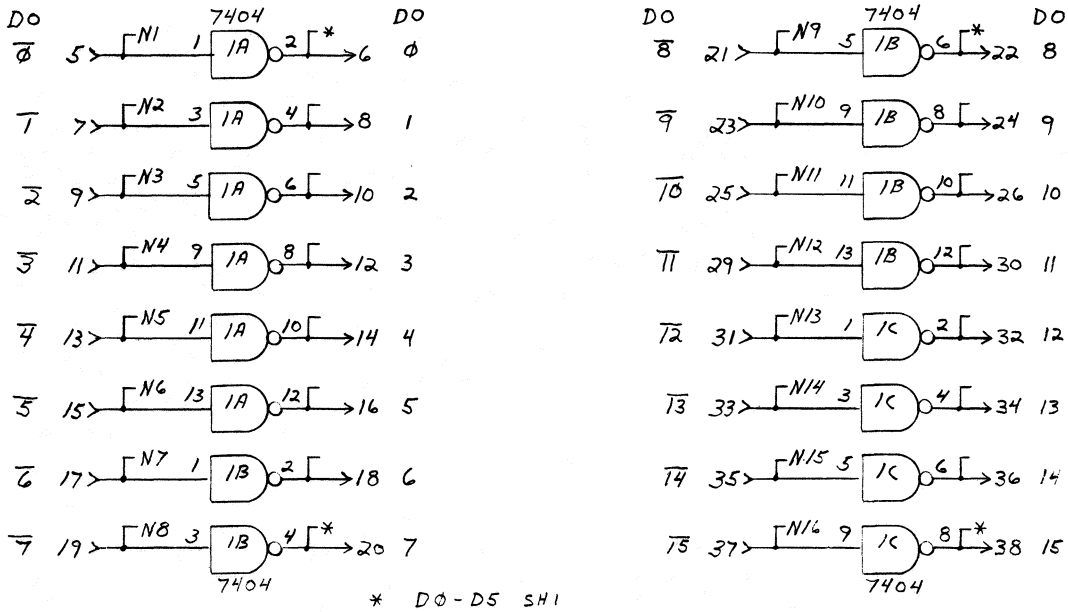
CARD 4 HP I/O CONTROL
INPUT + OUTPUT COUNTERS
PAGE 2 OF 5
SLOT 9

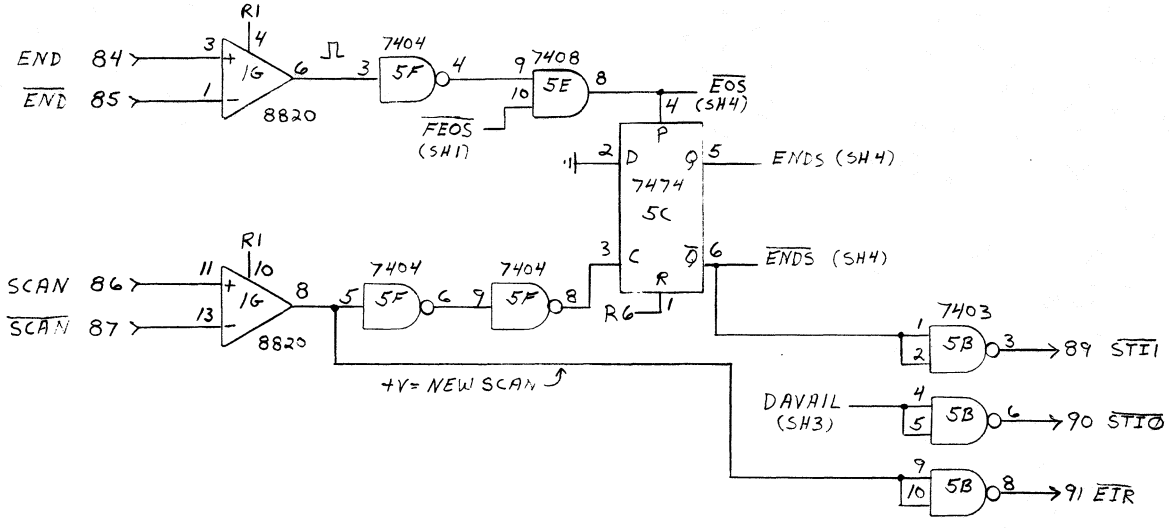


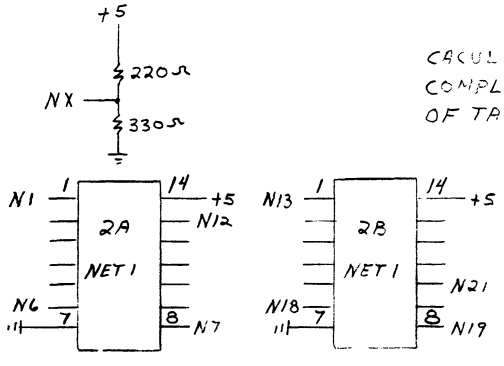
CARD 4 HP I/O CONTROL
CYCLE / DUMP COUNTER
SKIP A SAMPLE LOGIC
PAGE 3 OF 5
SLOT 9



CARD 4 HPI/O CONTROL
HOST COMPUTER
INTERRUPTS
PAGE 4 OF 5
SLOT 9



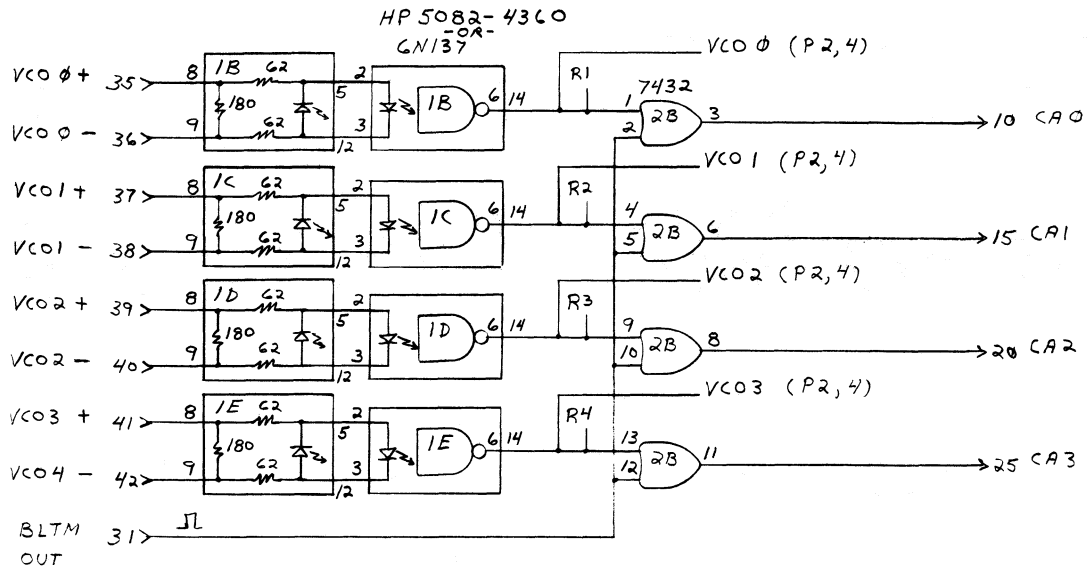


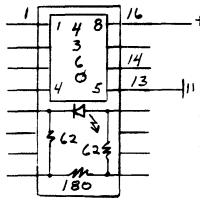


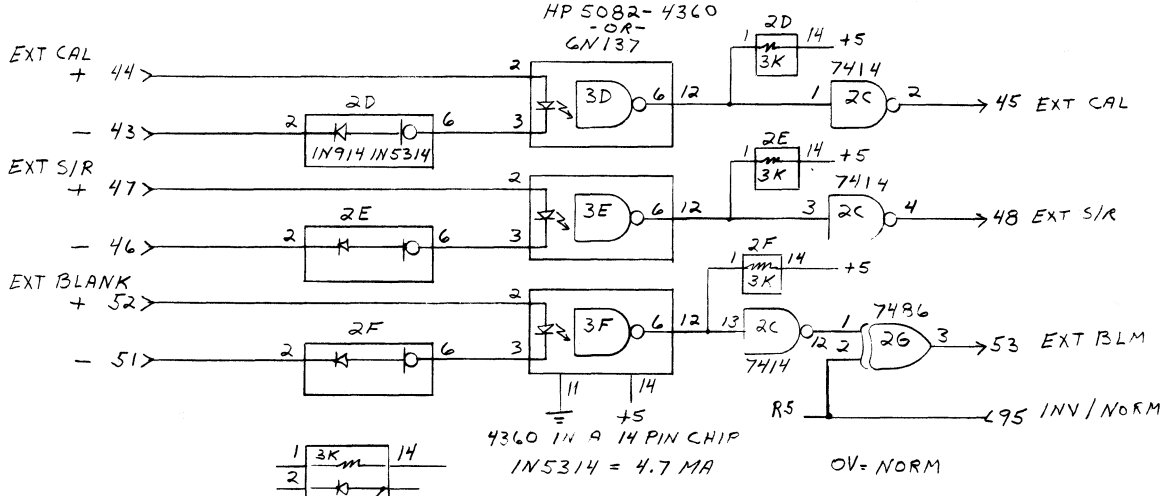
CALCULATES 6'S COMPLEMENT OF TABLE

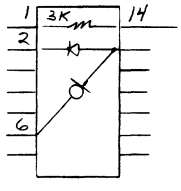
STI1	STI0	
1	1	END SCAN
1	0	END SCAN DATA RDY
0	1	START SCAN
0	0	START SCAN DATA RDY

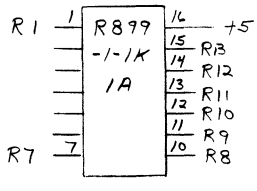
CARD 4 HP I/O CONTROL
OUTPUT DATA BUFFER
STATUS GENERATOR
PAGE 5 OF 5
SLOT 9

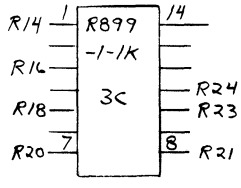


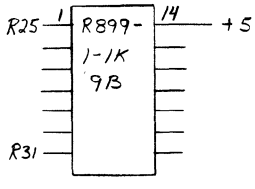




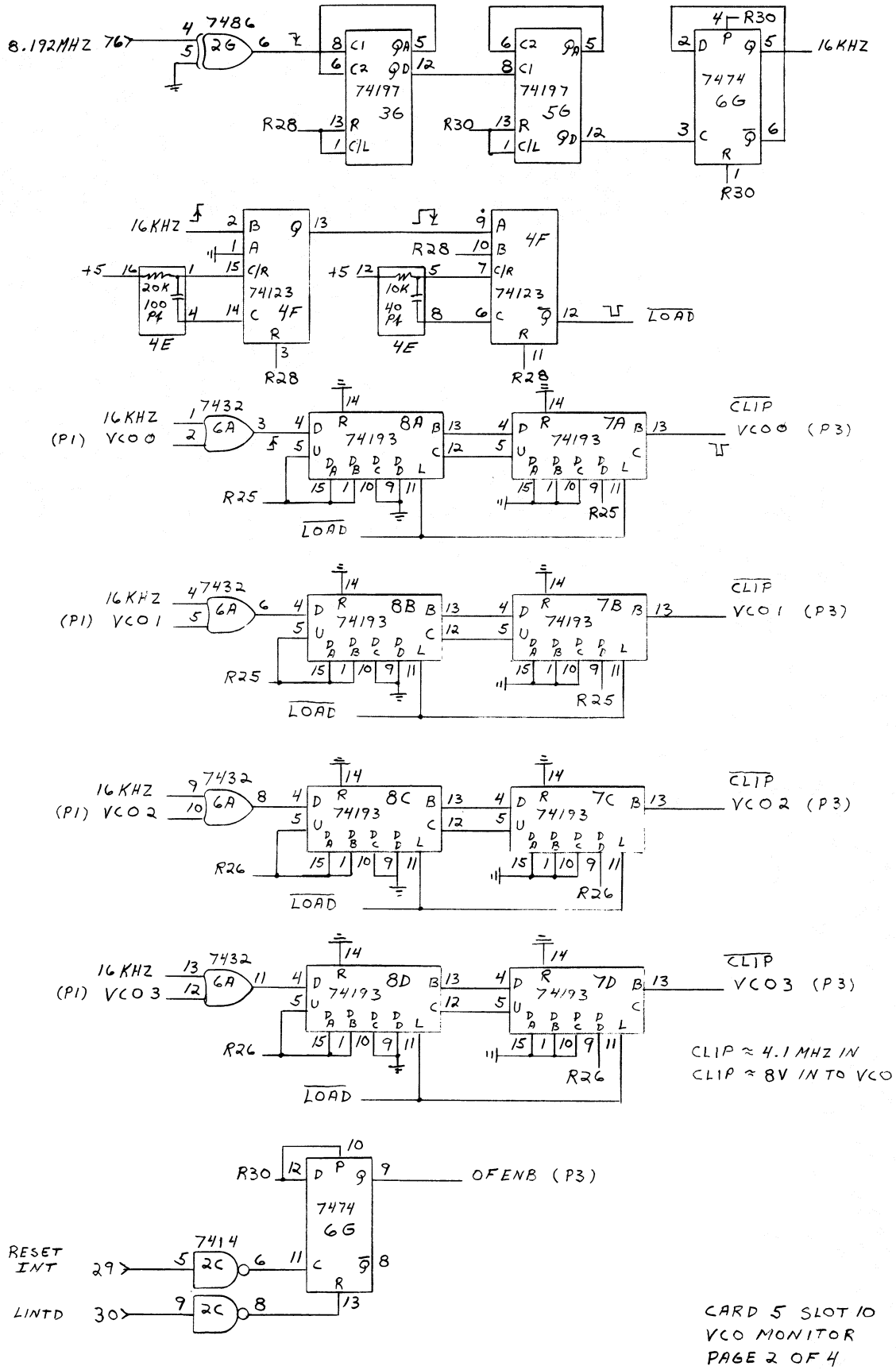


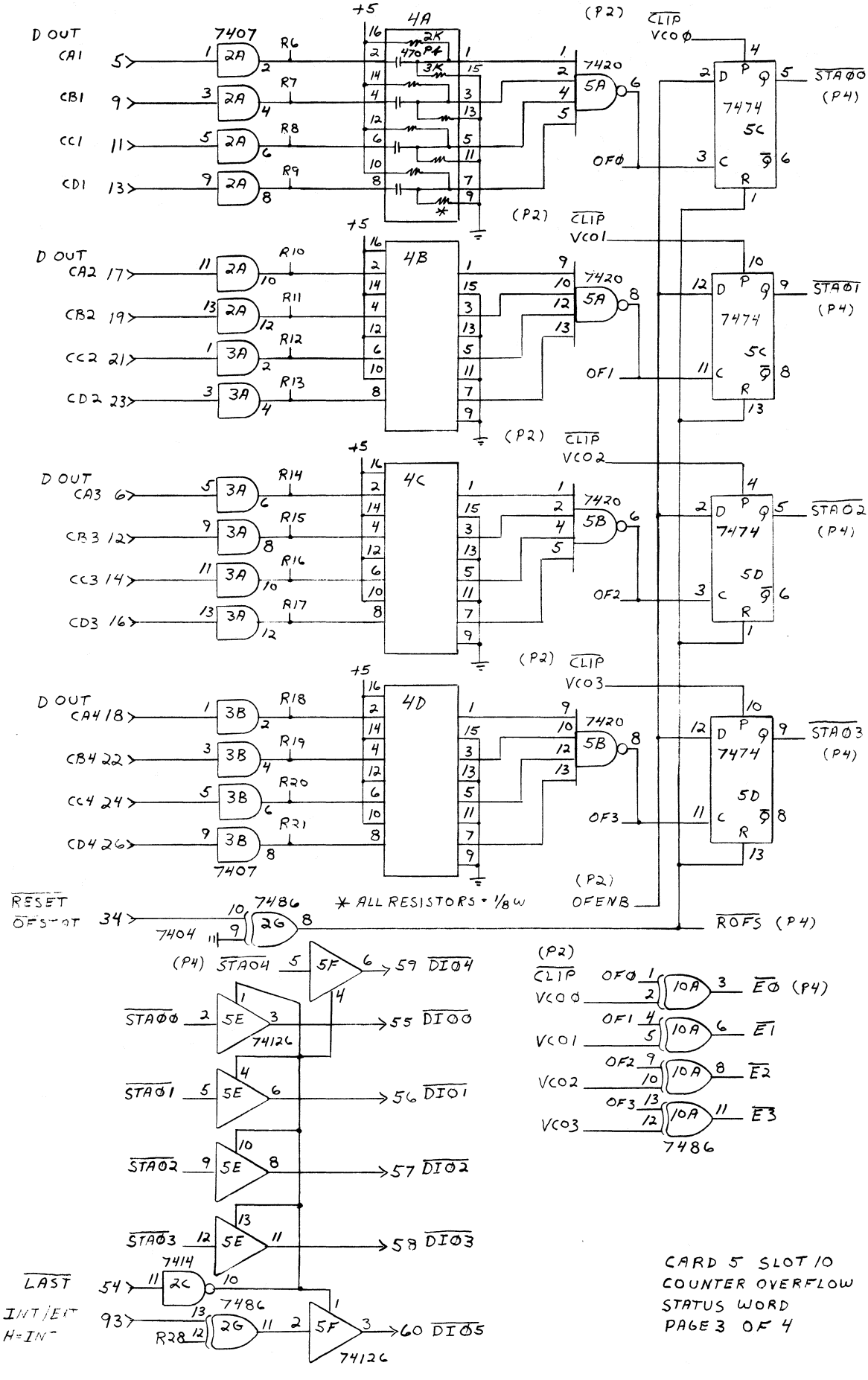




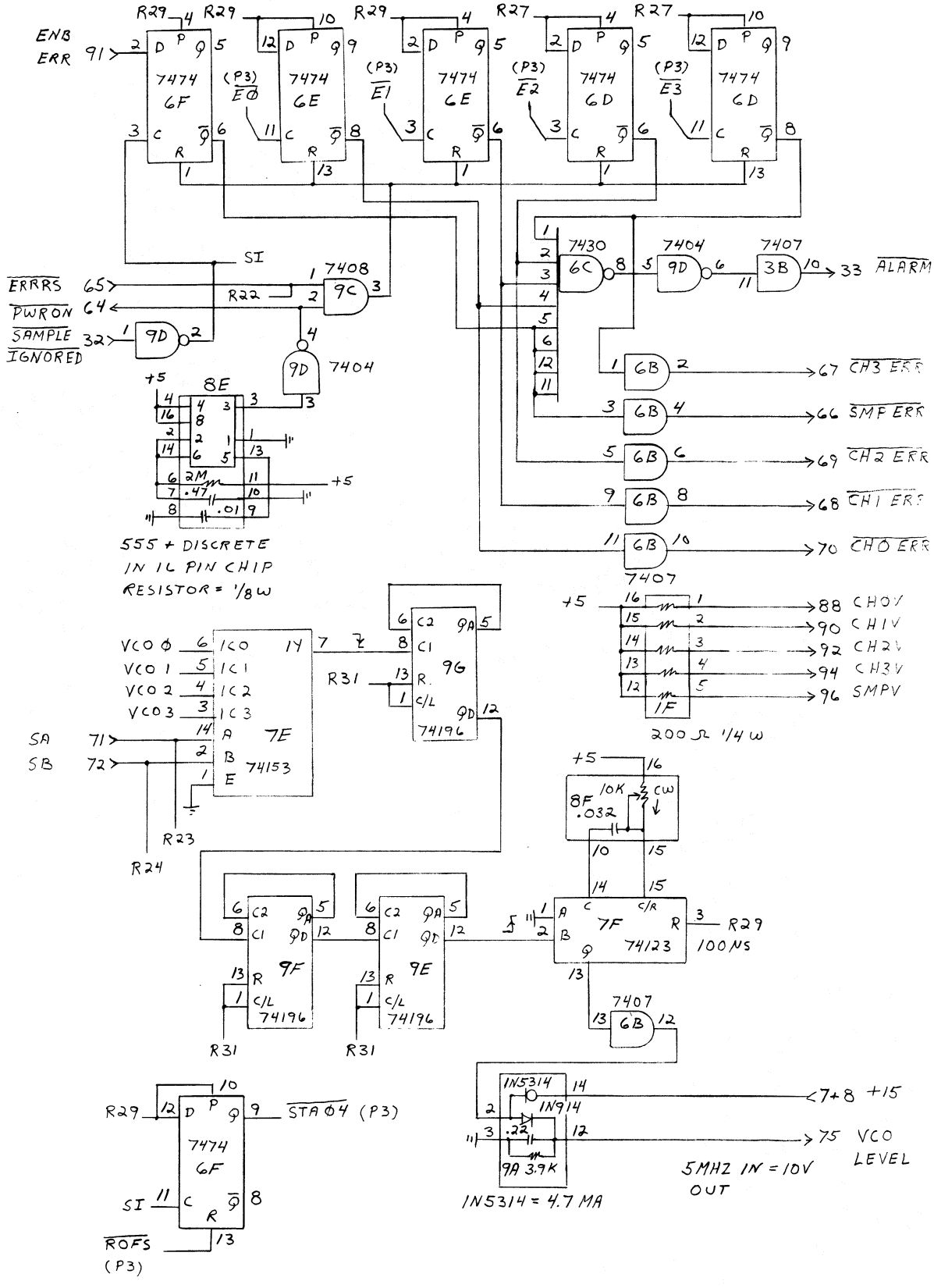


CARD 5 SLOT 10
VCO BLANKING, EXTERNAL
BUFFERS
PAGE 1 OF 4

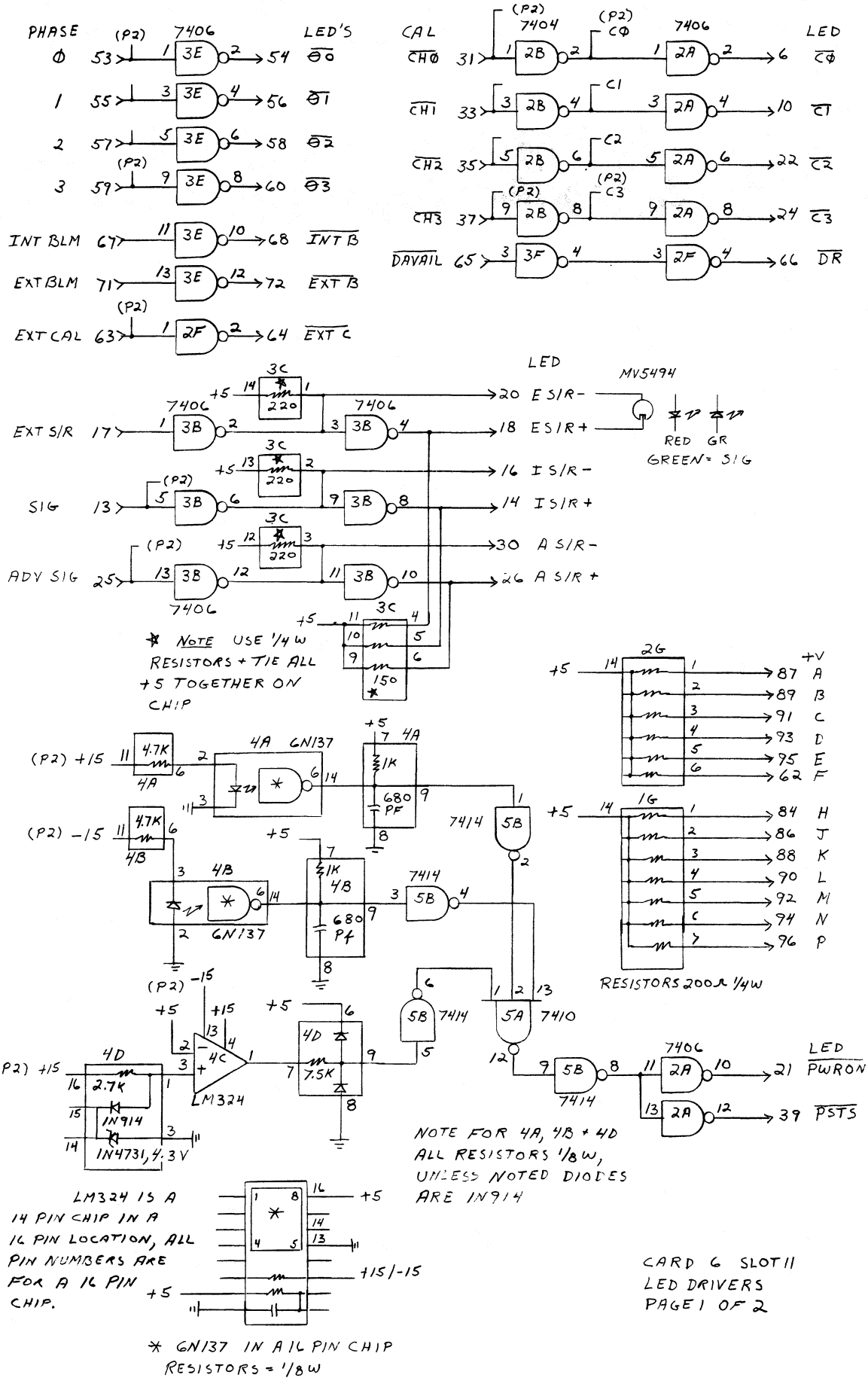

8.192MHZ
7486
74197
36
56
7474
66
R28
R30
16KHZ
74123
4F
4E
20K
100 PF
10K
40 PF
LOAD
7432
6A
74193
8A
7A
8B
7B
8C
7C
8D
7D
R25
R26
CLIP
VCO0 (P3)
VCO1 (P3)
VCO2 (P3)
VCO3 (P3)
(P1) VCO0
(P1) VCO1
(P1) VCO2
(P1) VCO3
OFENB (P3)
7414
RESET INT
LINTD
CLIP ≈ 4.1 MHZ IN
CLIP ≈ 8V IN TO VCO
CARD 5 SLOT 10
VCO MONITOR
PAGE 2 OF 4

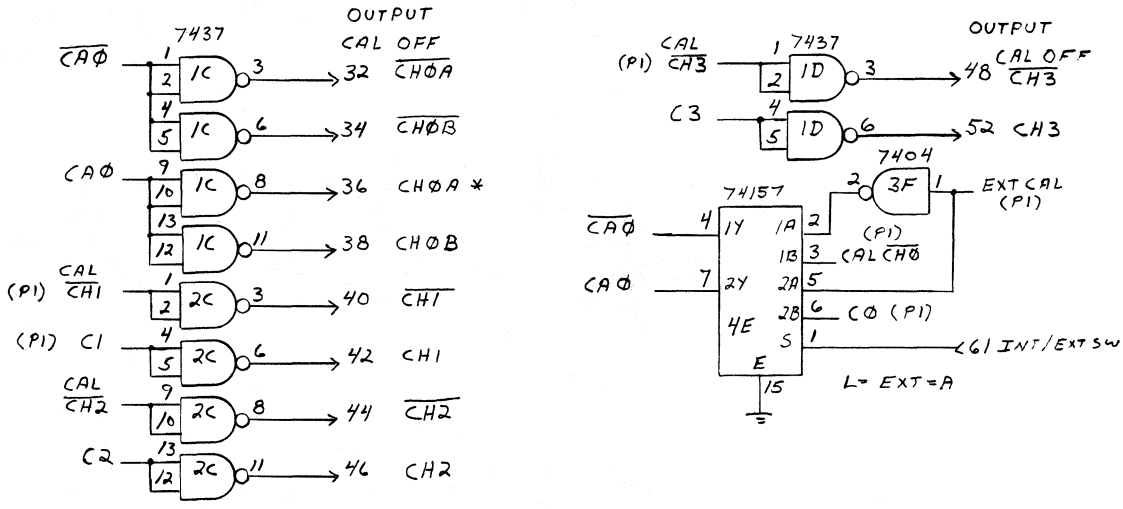


CARD 5 SLOT 10
COUNTER OVERFLOW
STATUS WORD
PAGE 3 OF 4

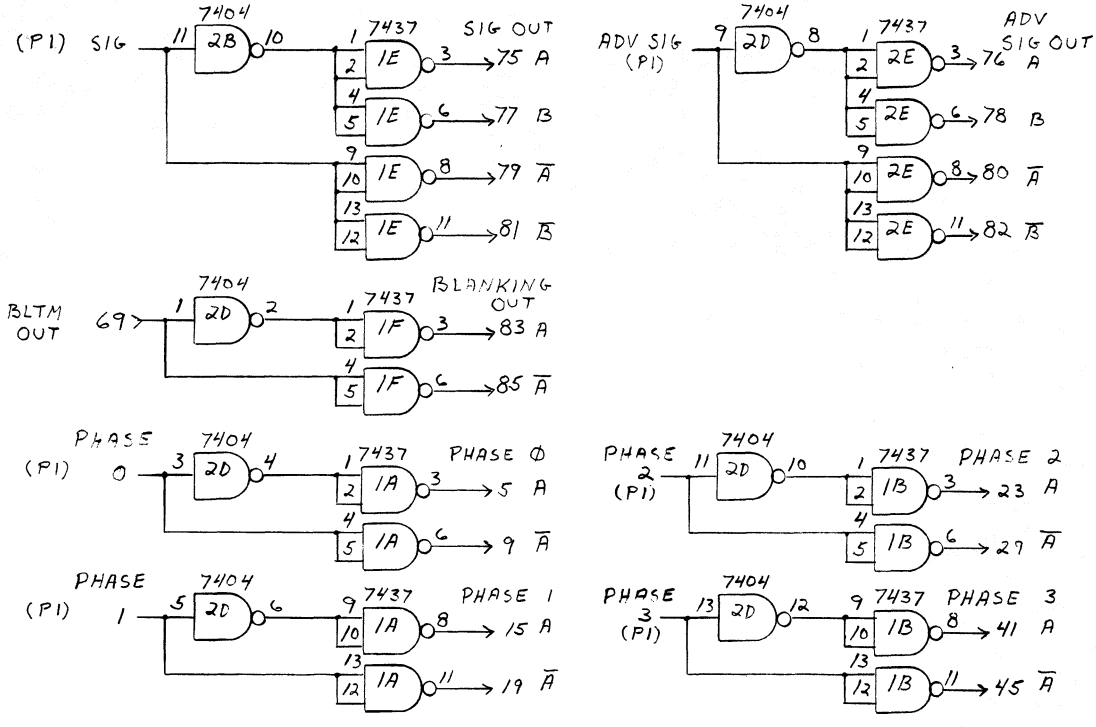


CARD 5 SLOT 10
ERROR INDICATOR
VCO LEVEL
PAGE 4 OF 4

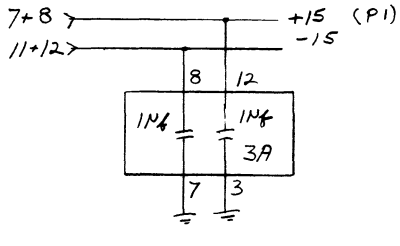

PHASE
7406
LED'S
Φ 53 54
1 55 56
2 57 58
3 59 60
INT BLM 67 68 INT B
EXT BLM 71 72 EXT B
EXT CAL 63 64 EXT C
CAL
7404
7406
LED
CHΦ 31 6 CΦ
CH1 33 10 C1
CH2 35 22 C2
CH3 37 24 C3
DAVAIL 65 66 DR
LED
MV5494
RED GR
GREEN = SIG
7406
EXT S/R 17 20 E S/R-
18 E S/R+
SIG 13 16 I S/R-
14 I S/R+
ADV SIG 25 30 A S/R-
26 A S/R+
220
150
NOTE USE 1/4 W RESISTORS + TIE ALL +5 TOGETHER ON CHIP
+V
87 A
89 B
91 C
93 D
95 E
62 F
84 H
86 J
88 K
90 L
92 M
94 N
96 P
RESISTORS 200Ω 1/4W
4.7K
4A GN137
1K
680 PF
7414
5B
4B
7410
5A
(P2) -15
(P2) +15
4C
LM324
4D
2.7K
1N914
1N4731, 4.3V
7.5K
LED
PWRON
21
PSTS
39
NOTE FOR 4A, 4B + 4D ALL RESISTORS 1/8 W, UNLESS NOTED DIODES ARE 1N914
LM324 IS A 14 PIN CHIP IN A 16 PIN LOCATION, ALL PIN NUMBERS ARE FOR A 16 PIN CHIP.
+15/-15
* GN137 IN A 16 PIN CHIP RESISTORS = 1/8 W
CARD 6 SLOT 11
LED DRIVERS
PAGE 1 OF 2



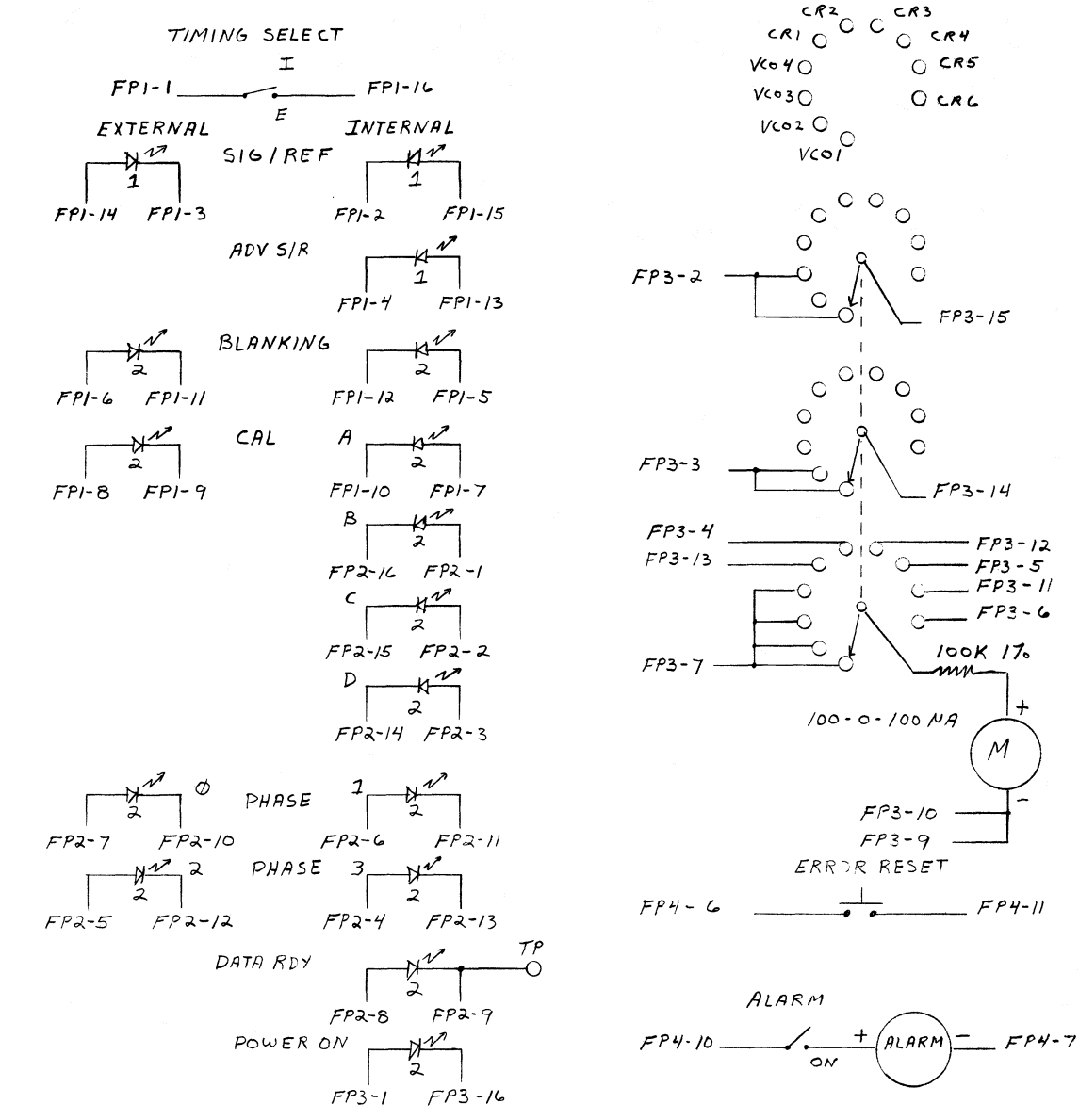
* NORMAL OUTPUT IS CHØ, A+B, CH1, CH2, CH3
CAL IS OFF AT A TTL HIGH



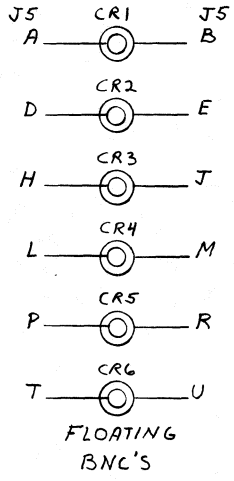
ALL Ā + B̄ SIGNALS ARE ACTIVE LOW

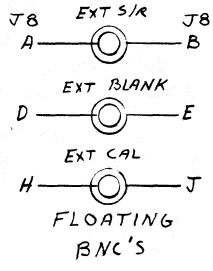


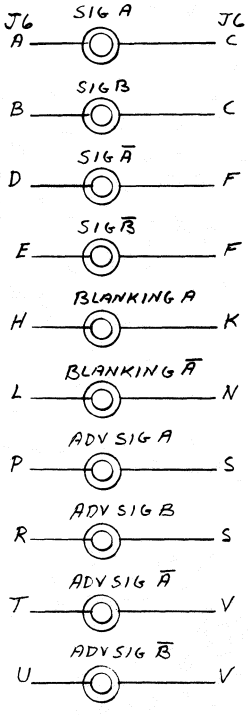
CARD 6 SLOT 11
OUTPUT DRIVERS
PAGE 2 OF 2

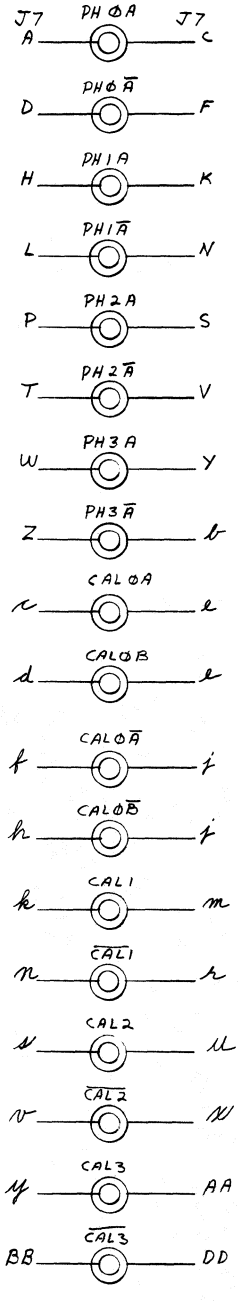


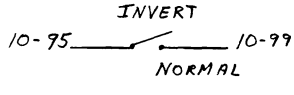
DIGITAL STD REC
FRONT PANEL
PAGE 1 OF 1











BACK OF CHASSIS

DIGITAL STD. REC.
BNC'S TOP OF RACK
PAGE 1 OF 1