NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 239

FRONT-END DATA LINK
(FEDAL)

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DECEMBER 1983

NUMBER OF COPIES: 150

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FRONT-END DATA LINK (FEDAL)

Richard J. Lacasse

1.0 Introduction

Monitor and control of a receiver front-end from the telescope control room has traditionally been done using several multiconductor cables. Limitations of such systems include reliability, since operation depends on many cable elements, and cost. This report describes a system which ameliorates the receiver monitor and control problem in terms of both cost and reliability. Consisting of two identical FRONT-END DATA LINK (FEDAL) subsystems, the system digitizes all monitor and control data and transmits it digitally over four doubly redundant, optically-isolated twisted pairs. Thus, four twisted pairs replace up to 128 cable elements to form a reliable, cost-effective monitor and control medium.

This report presents FEDAL block diagrams, specifications, theory of operation, schematics, and user interconnections. Another document, the FRONT-END DATA LINK USER'S MANUAL, provides the information required for customizing a FEDAL, giving documentation on the system firmware and on board and chassis testing.

2.0 System General Description

A partial, simplified system block diagram is shown in Figure 1. The system is composed of two identical devices, one in the receiver box and one in the control room. Each device is capable of digitizing 32 analog channels, limit checking each channel, reading 32 digital inputs, formatting, and transmitting all this information, as well as receiving and displaying similar information from the second device. The information is sent over redundant, optically-isolated twisted pairs. Several diagnostic tests are performed at

power-on and during operation, to monitor the condition of the hardware and the quality and quantity of received data. Delay through the system varies from 20 to 40 milliseconds.

3.0 Specifications

This section details the system specifications.

3.1 Mechanical

General ..... Figures 2, 3 and 4 show the FEDAL physical layout. Note that access to all boards and power supplies can be gained by lowering the front panel.

Width ..... 19 in (48.2 cm)

Depth ..... 12 in (30.4 cm) including front panel handles and rear panel connectors.

Height ..... 7 in (17.8 cm)

Weight ..... 24 lb (10.8 kg)

Connector Pin Assignments: See Tables 1 through 5.

3.2 Analog Input/Output

3.2.1 Analog Input

Number of inputs: 32

Quantization: 12 bits

Input voltage reference: One "pseudo-ground" is brought out of the chassis for connection to the common voltage reference of the 32 input signals. Internally, it is connected to the inverting input of an instrumentation amplifier.

Max input or pseudo-ground voltage for linear operation: $\pm$ 10 V.

Max input differential voltage: $\pm$ 10 V.

Input and pseudo-ground overvoltage protection: $\pm$ 22 V.

Input common mode rejection with 1 KΩ source imbalance: $\geq$ 75 dB from DC to 60 Hz.

3.2.1 Analog Input (continued):

Input sampling rate: 25 Hz, typical; 22 Hz, minimum.

Max input current: $\leq$ 100 na, $0 \leq T \leq 55°C$, $-10 \leq V \leq +10$ V.

Recommended source impedance: $\leq$ 1 KΩ
(Larger impedances degrade common mode rejection.)

3.2.2 Analog Output

Number of outputs: 32 dedicated to inputs, plus 4 monitors.

Quantization: 12 bits

Output voltage range: $\pm$ 10 V

Output current capability: $\pm$ 5 mA, minimum.

Short circuit duration: Indefinite to ground.

Output impedance: 0.05 Ω typical

3.2.3 Analog System

System error for DC inputs, analog input through link to analog output: $\leq$ 5 mV at 25°C, $\leq$ 35 ppm/°C tempco

Input to output delay through link: $\leq$ 45 ms

Monotonicity: Guaranteed.

Limit testing: Each analog input is tested against high and low voltage limits programmed in ROM 10A. Results of these tests are stored and transmitted as "Limit Bits". Default limits in V1.0-RJL ROM are -9.995 V and +9.991 V. These limits may be reprogrammed by the user as described in the Front-End Data Link User's Manual.

3.3 Digital Input/Output

3.3.1 Digital Input

Number of inputs: 32

Input source characteristics: Four diode multiplexed banks of eight switches as shown in Figure 5, or four groups of eight tri-state gates as shown in Figure 5, or any combination of diode multiplexed switches and tristate gates.

Input sampling rate: $\geq$ 22 Hz

3.3.2 Digital Output

Number of outputs: 32

Drive capability: High Output: $\geq$ 2.4 V @ $\geq$ 12 mA
Low Output: $\leq$ 0.4 V @ $\geq$ 24 mA

3.3.3 Digital System

System delay from digital input through link to digital output: $\leq$ 45 ms

Output bit mapping: Local digital outputs 0 through 15 are always obtained from remote digital inputs 0 through 15.

Local digital outputs 16 through 31 are obtained either from remote digital inputs 16 through 31 or from remote limit bits 0 through 15 (reference section 3.2.3). Selection of these two alternatives is accomplished as shown in Figure 7. Mapping of Limit Bits to Digital Outputs is shown in Table 3, sheet 2.

Limit bit polarity: Out of range is indicated by a high output.

3.4 Remote Analog Voltage Monitors

Number of monitors: 4

Output voltage range: $\pm$ 10 V

Location of monitors: Two are on the FEDAL front panel wired to meters and BNC connectors. Two are available to the user via rear panel connectors.

Connection of user monitors: See Figure 8.

Monitor channel selection: Digiswitches select channels 00 to 31. Channel 31 is the default for switch values greater than 31.

Out of range indication: The front panel digital voltmeter is blinked when an out of range condition exists in the selected channel.

3.5 Front Panel Status/Error Display and Display Select Switch

A front panel display enhances system reliability by giving the user a variety of information on the FEDAL's performance. Three switch positions give access to three types of information as described below. The information from the remote FEDAL unit is transmitted over the same communication link as the monitor and control data and is updated at the same 20 to 45 ms rate. The remote display is blanked until a good data frame is received from the remote unit.

3.5.1 Switch in STATUS Position

The FEDAL performs a self test at power-on. Error conditions detected during this self test or during routine operation are displayed with the select switch in status position. A status value of ØØ means no errors have been detected. Error conditions are described in Table 6.

3.5.2 Switch in COMMUNICATIONS ERRORS Position

The FEDAL keeps a running count of communications errors detected in the received data. The count is incremented each time a sync word is expected but not detected. A stable count indicates that the link is performing satisfactorily.

3.5.3 Switch in RESTART ERRORS Position

During normal operation the FEDAL controller pulses an "auto-reset circuit" every 40 ms. If the program is somehow disrupted, this circuit will probably time-out and reset the controller. A hardware counter increments each time the controller is reset, and its count is displayed with the select switch in this position. A stable count indicates normal operation.

3.6 RS232 Communication

Sufficient hardware is built into the FEDAL to enable simple RS232 communication. Drivers and receivers, for DATA OUT and DATA IN, respectively, and an Asynchronous Communications Interface Adapter (ACIA) are provided. Drivers and receivers for handshaking are not provided, but there is ample room on the board to add them as required. However, no RS232 communications firmware is provided in the V1.0-RJL ROMS. Instructions for adding such firmware are given in the FRONT-END DATA LINK USER'S MANUAL. Baud rate is selectable by changing jumpers on the MP board. (See Figure 20.)

4.0 Theory of Operation

This section supplements the general description given in Section 2 by detailing the theory of operation. First, analog and digital data are tracked through the system from input to output. Then several miscellaneous functions are discussed.

The system consists of two identical units. For descriptive purposes, one is dubbed remote and the other local. This section describes data acquisition by the local unit with transmission to the remote unit where it is displayed, as pictured in Figure 1. This system is completely symmetrical and the following description can be applied equally well to remote acquisition and local display simply by exchanging the words remote and local.

4.1 Analog Acquisition

Analog input signals are routed from the local rear panel connector to the local analog input board multiplexers shown in Figure 9. The local FEDAL controller sends signals through the LS377 on Figure 9 and the LS138 on Figure 10 to select one signal to be routed through the multiplexer to the instrumentation amplifier. PSEUDO-GND from the user goes to the inverting amplifier input through a 240 Ω resistor whose purpose is first to match the impedance of the multiplexers for improved common mode rejection and, second, to protect the low-leakage, over-voltage protection diodes. The amplifier drives the 12 bit ADC shown in Figure 10. Offset and gain adjustments are provided for the ADC. A convert signal, initiated by the FEDAL controller, through the LS138, starts the conversion process. When a conversion process is initiated, the ADC status output goes high. It returns low at the completion of the conversion process, regardless of whether or not the ± 15 V supply is on. The opto-isolator circuit in Figure 10 gives an indication of the state of the ± 15 V supply, and is used to gate the STATUS signal sent to the controller, giving it some indication of problems with the supply or ADC. The controller reads the digitized outputs by enabling the tri-state output buffers.

The controller usually operates the Analog Input Card as follows: First, it selects input zero on the multiplexer. Then it waits at least 170 μs to allow the input to the ADC to settle, and gives a start command. Having initiated the conversion process, it reads the status output until either a conversion complete is indicated or a programmed time-out occurs. Subsequently, it converts input channels 1 to 31 similarly. Each channel is tested against high and low limits programmed in EPROM.

4.2 Digital Acquisition

User digital inputs are multiplexed into the local controller in groups of eight. The inputs must be arranged as shown in Figures 5 and/or 6. The receiver, located in the local chassis, for these inputs is shown in Figure 22; it consists of eight comparators biased at 3 volts, and a tri-state buffer.

4.3 Formatting

The local controller formats the analog and digital data, the information on the analog limit checks, and the local status and control information into frames for transmission to the remote site. Details of the format are included in the FRONT-END DATA LINK USER'S MANUAL. The local Asynchronous Communication Interface Adapter, Figure 13, further encodes the data, adding start and stop bits for serial transmission.

Data is transmitted over redundant 50 Ω shielded twisted pairs. The local line drivers are shown in Figure 15. The resistors make the driver impedance roughly 50 Ω, limit the rise time on the cables, and provide short circuit protection.

4.5 Reception

The two remote link receivers are shown in Figure 14. Each receiver consists of a pair of 66.5 Ω resistors, a pair of 0.01 μF capacitors, an MV50 LED and a 6N137 opto-isolator. The resistors and capacitors optimize the receiver for about 400 feet of the 50 Ω twisted pair cables commonly used in Green Bank. Steady state current through the opto-isolator diode is provided by the resistors, and the capacitors critically damp the current. The MV50 provides reverse polarity protection for the opto-isolator's input diode. The two receivers are OR-tied and the 74LS74 flip-flop allows only one of the two to be active at any time.

Complete redundancy is provided by the transmitter/receiver so that only one of the two data channels needs to be operational for the link to function properly. The controller tests both channels during initialization and alternates between channels until good data is found. The user is notified, via the STATUS word, of a bad channel.

4.6 Decoding

The serial bit stream is routed to the remote ACIA, which does the serial to parallel conversion and interrupts the controller each time a byte is received. The controller decodes the byte stream by finding patterns of sync words in the byte stream and ensures the quality of the data by computing the frame's checksum and comparing it to the received checksum.

4.7 Output and Display

Locally acquired analog and digital data are output remotely in analog and digital forms, respectively. The output system consists of three identical cards, each residing in a separate address space of the controller. Each card contains 12 Digital-to-Analog Converters (DAC's) with associated latches (Figures 30 through 35) for analog output and 16 latches and associated drivers for digital output (Figure 29), as well as some decoding logic (Figure 29).

All of the outputs of the top two output boards in the chassis are dedicated to user outputs. However, the third, bottom-most card is required for only eight analog and no digital outputs to form the system complement of thirty-two of each. Two of the "extra" DAC's drive the FEDAL front-panel meters and the other two are available to the user as switch-selectable monitors. (See Section 3.4 and Figure 8.) A few "extra" digital outputs are used for internal FEDAL control purposes, and the rest are truly spare.

4.8 Miscellaneous Functions

4.8.1 Microprocessor

A Motorola 6809 CPU (Figure 11), a 1K RAM (Figure 17), and two 2K EPROMS (Figures 17 and 18) comprise the basic microprocessor control system. The 6809 non-maskable interrupt is dedicated to the link ACIA to ensure link reliability, while the IRQ interrupt is dedicated to the user ACIA. The system clock rate is 1 MHz.

4.8.2 Power-On Reset

The power-on reset circuit (Figure 11) consists of a one-shot, triggered by the rise of the 5 V supply, that resets the microprocessor about 0.1 sec after power-on.

4.8.3 Auto-Reset

Consisting of two one-shots, the auto-reset circuit (Figure 12) provides a hardware reset for the microprocessor if the program goes awry. The first one-shot is pulsed by the microprocessor each time it goes through the main program loop, approximately every 40 ms in normal operation, keeping it set. If the program goes awry and the one-shot is not pulsed within 200 ms, it goes to the reset state, triggering the second one-shot which gives a reset pulse to the 6809 processor.

4.8.4 Select Logic

The address lines of the 6809 processor are decoded by the 74LS-138 decoders and associated logic shown in Figures 25 and 26. Select pulse width is approximately 750 ns. A summary of select signals and corresponding high order address bits is included in Figure 24.

4.8.5 Restart Error Counter

In addition to resetting the microprocessor, the auto-reset circuit clocks an eight bit, tri-state output counter (Figure 27) to give the user some indication of how often the program runs awry. The counter is cleared by the power-on reset pulse. The counter is read by the microprocessor and transmitted along with all the other data on the link. It can also be displayed on the FEDAL front-panel display by selecting RESTART ERRORS with the 3-position rotary switch.

4.8.6 Logic Analyzer Interface

The address and data busses are brought out to the last (Z) row of the MP card (Figure 28). This provides easy access to these important signals for debugging and development purposes, using a logic analyzer.

5.0 Further Documentation

In addition to the schematics incorporated into the text of this report, other documentation is available. Appendix A of this report contains parts lists, board layouts, and ROM listings. Wirelists for all boards, and the chassis, are on the Pandora System, data set name ELECTR.GRNBNK.PANDORA, member names FEDALIN, FEDALMP, FEDALOUT, and FEDALWI. The FRONT-END DATA LINK USER'S MANUAL includes all the firmware listings and instructions for modifying it, and test procedures for all boards and the chassis.

6.0 For Future Development

Interconnecting two Front End Data Link Chassis using fiber optics would be a reasonably straightforward and useful project. Several TTL to fiber optic transmitter/receiver modules are presently on the market, and the link transmit and receive signals are available in TTL on the controller (MP) card. Picking suitable cables and connectors for a telescope environment is also a non-trivial part of this task.

One Front End Data Link Chassis can also be used as a data acquisition and output device for a computer with RS232 capabilities. Some of the FEDAL firmware would have to be reworked, and an appropriate driver written for the computer.

7.0 Acknowledgements

Many people have contributed to this project. John Payne got the project started; he and Graham Moorey provided some of the specifications. Dwayne Schiebel, Rick Fisher, Bill Brundage, Jim Coe and others provided many useful suggestions. The crew at the machine shop did their usual great job interpreting and supplementing my mechanical drawings, and constructing the chassis. Ira Jeffries and Bill Vrable did most of the construction and testing.

LIST OF TABLES

LIST OF FIGURES

Connector: 56 Pin, Panel Mount Elco, exposed pins:

Pin	Function	
A	Analog Input	31
B		30
C		29
D		28
E		27
F		26
H		25
J		24
K		23
L		22
M		21
N		20
P		19
R		18
S		17
T		16
U		15
V		14
W		13
X		12
Y		11
Z		10
a		9
b		8
c		7
d		6
e		5
f		4
h		3
j		2
k		1
ℓ	Analog Input	0
m	Pseudo Ground	

Table 1: Analog Input Connector Pin Designations.

Connector: 25 Pin, D-Type, Female

Pin	Function
1	Ground
2	RS232 Out
3	RS232 In
6	DSR
7	Ground

Table 2: RS232 Interface Connector Pin Designations.

Connector: 56 Pin, Panel Mount Elco, Protected Pins

Pin	Function
A	Link Receiver Channel Ø +
B	Link Receiver Channel Ø -
C	Link Transmitter, Channel Ø +
D	Link Transmitter, Channel Ø -
E	Link Receiver, Channel 1 +
F	Link Receiver, Channel 1 -
H	Digiswitch Input MSD 8
J	Link Transmitter, Channel 1 +
K	Link Transmitter, Channel 1 -
L	Digiswitch Input MSD 4
M	Digiswitch Input MSD 2
N	Digiswitch Input MSD 1
P	Digiswitch Input LSD 8
R	Digiswitch Input LSD 4
S	Digiswitch Input LSD 2
T	Digiswitch Input LSD 1
U	Digiswitch Select Line DWS2SEL-
V	Digiswitch Select Line DSW3SEL-
W	Digiswitch Select Line DSW4SEL-
X	Digiswitch Select Line DSW5SEL-
Y	Toggle Switch Select Line TSW3SEL-
Z	Toggle Switch Select Line TSW2SEL-
a	Toggle Switch Select Line TSW1SEL-
b	Toggle Switch Select Line TSWØSEL-

Table 3: Digital Input/Output Connector Pin Designations.
(Sheet 1 of 2.)

Connector: 56 Pin, Panel Mount Elco, Protected Pins continued:

Pin	Function
c	Digital Output 31/Limit Bit 8
d	Digital Output 30/Limit Bit 9
e	Digital Output 29/Limit Bit 10
f	Digital Output 28/Limit Bit 11
h	Digital Output 27/Limit Bit 12
j	Digital Output 26/Limit Bit 13
k	Digital Output 25/Limit Bit 14
ℓ	Digital Output 24/Limit Bit 15
m	Digital Output 23/Limit Bit Ø
n	Digital Output 22/Limit Bit 1
p	Digital Output 21/Limit Bit 2
r	Digital Output 20/Limit Bit 3
s	Digital Output 19/Limit Bit 4
t	Digital Output 18/Limit Bit 5
u	Digital Output 17/Limit Bit 6
v	Digital Output 16/Limit Bit 7
w	Digital Output 15
x	Digital Output 14
y	Digital Output 13
z	Digital Output 12
AA	Digital Output 11
BB	Digital Output 10
CC	Digital Output 9
DD	Digital Output 8
EE	Digital Output 7
FF	Digital Output 6
HH	Digital Output 5
JJ	Digital Output 4
KK	Digital Output 3
LL	Digital Output 2
MM	Digital Output 1
NN	Digital Output Ø

Note that pins c through f serve dual functions and are selected as shown in Figure 7.

Table 3: Digital Input/Output Conector Pin Designations.

(Sheet 2 of 2.)

Connector: 56 Pin, Panel Mount Elco, Protected Pins

Pin	Function
A	Analog Output Ø
B	Return
C	Analog Output 1
D	Return
E	Analog Output 2
F	Return
J	Analog Output 3
K	Return
L	Analog Output 4
M	Return
N	Analog Output 5
P	Return
R	Analog Output 6
S	Return
U	Analog Output 7
V	Return
W	Analog Output 8
X	Return
Y	Analog Output 9
Z	Return
a	Analog Output 10
b	Return
c	Analog Output 11
d	Return
k	Analog Output 12
ℓ	Return
m	Analog Output 13
n	Return
p	Analog Output 14
r	Return
s	Analog Output 15
t	Return
z	User Analog Monitor Ø
AA	Return
BB	User Analog Monitor 1
CC	Return

Table 4: Analog Outputs 0-15 Connector Pin Designation.

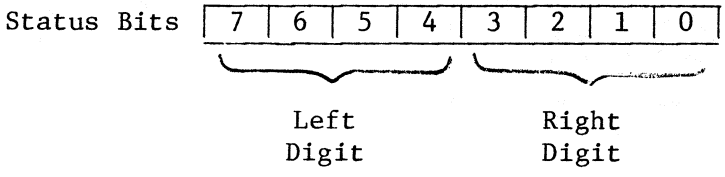
Connector: 56 Pin, Panel Mount Elco, Exposed Pins

Pin	Function
A	Analog Output 16
B	Return
C	Analog Output 17
D	Return
E	Analog Output 18
F	Return
J	Analog Output 19
K	Return
L	Analog Output 20
M	Return
N	Analog Output 21
P	Return
R	Analog Output 22
S	Return
U	Analog Output 23
V	Return
W	Analog Output 24
X	Return
Y	Analog Output 25
Z	Return
a	Analog Output 26
b	Return
c	Analog Output 27
d	Return
k	Analog Output 28
ℓ	Return
m	Analog Output 29
n	Return
p	Analog Output 30
r	Return
s	Analog Output 31
t	Return

Table 5: Analog Outputs 16-31 Connector Pin Designations.

Status Bit	Error Condition
Ø	No data being received.
1	Spare.
2	Analog Input Board problem (or ± 15 V supply).
3	Data Link ACIA problem (MP board).
4	Bad received channel (cable, local or remote MP board)
5	Bad RAM test (MP board).
6	Bad ROM test (MP board).
7	User ACIA problem (MP board or user device not ready).

Note: Status bits are encoded in hexadecimal for front panel display, and should be read as follows:



For example: Status = Ø1 means no data being received,
Status = 2Ø means bad RAM test, and
Status = 85 means user ACIA problem and Analog Input Board problem and no data being received.

Table 6: Status Bit Decoding.

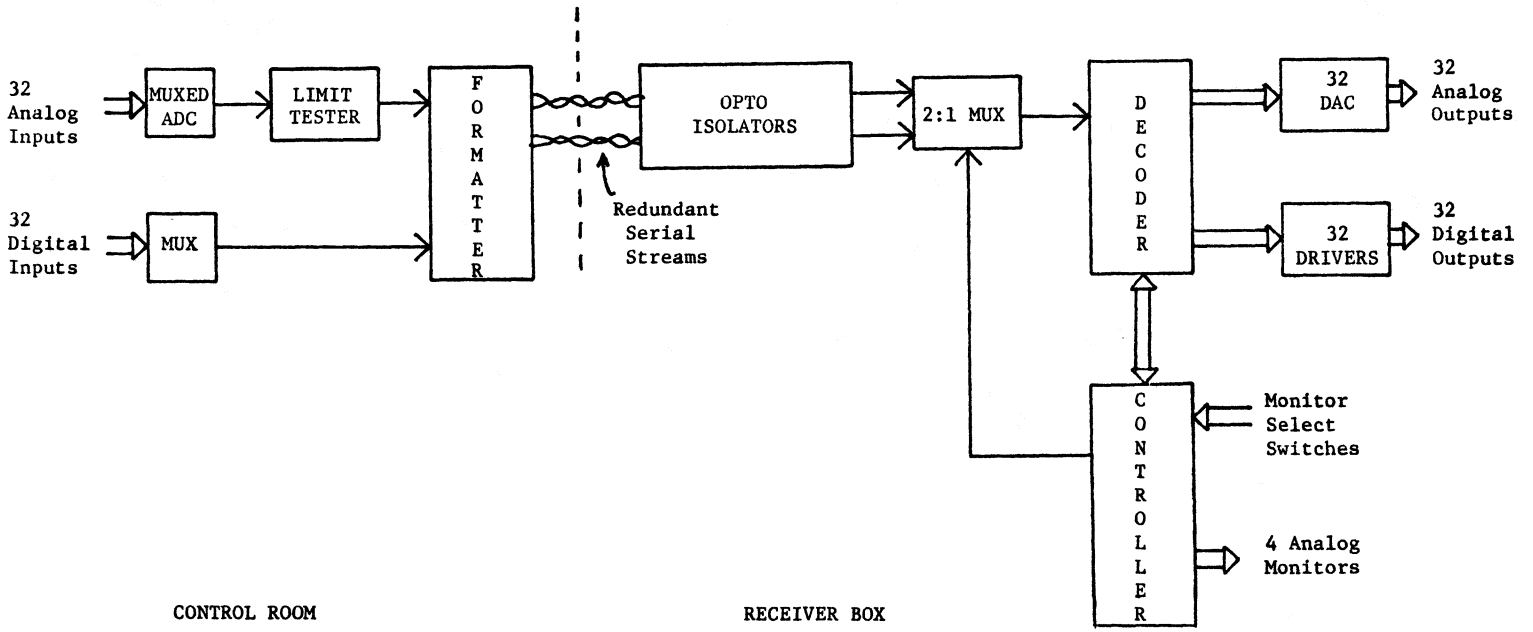


FIGURE 1

FRONT-END DATA LINK Simplified Block Diagram.

For clarity, only one-half of a complete system is shown: acquisition in the control room for display in the receiver box. An identical subsystem acquires data in the receiver box for display in the control room.

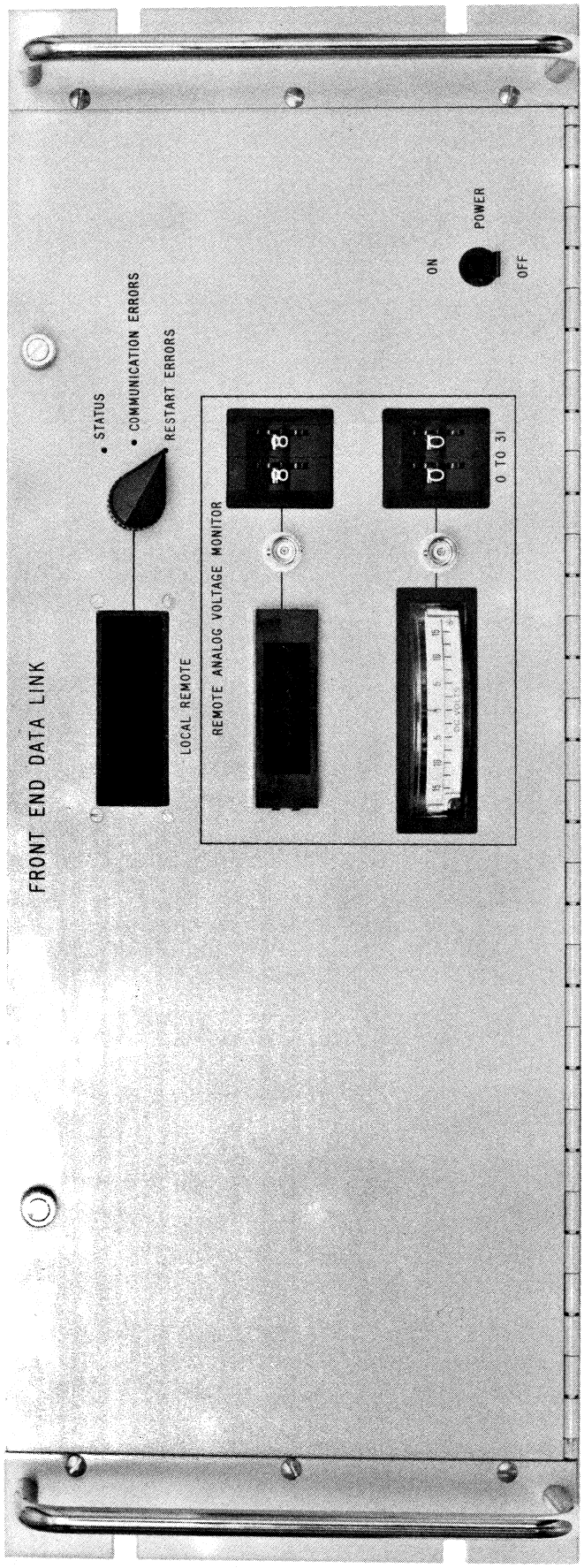


FIGURE 2

Front-End Data Link, Front View

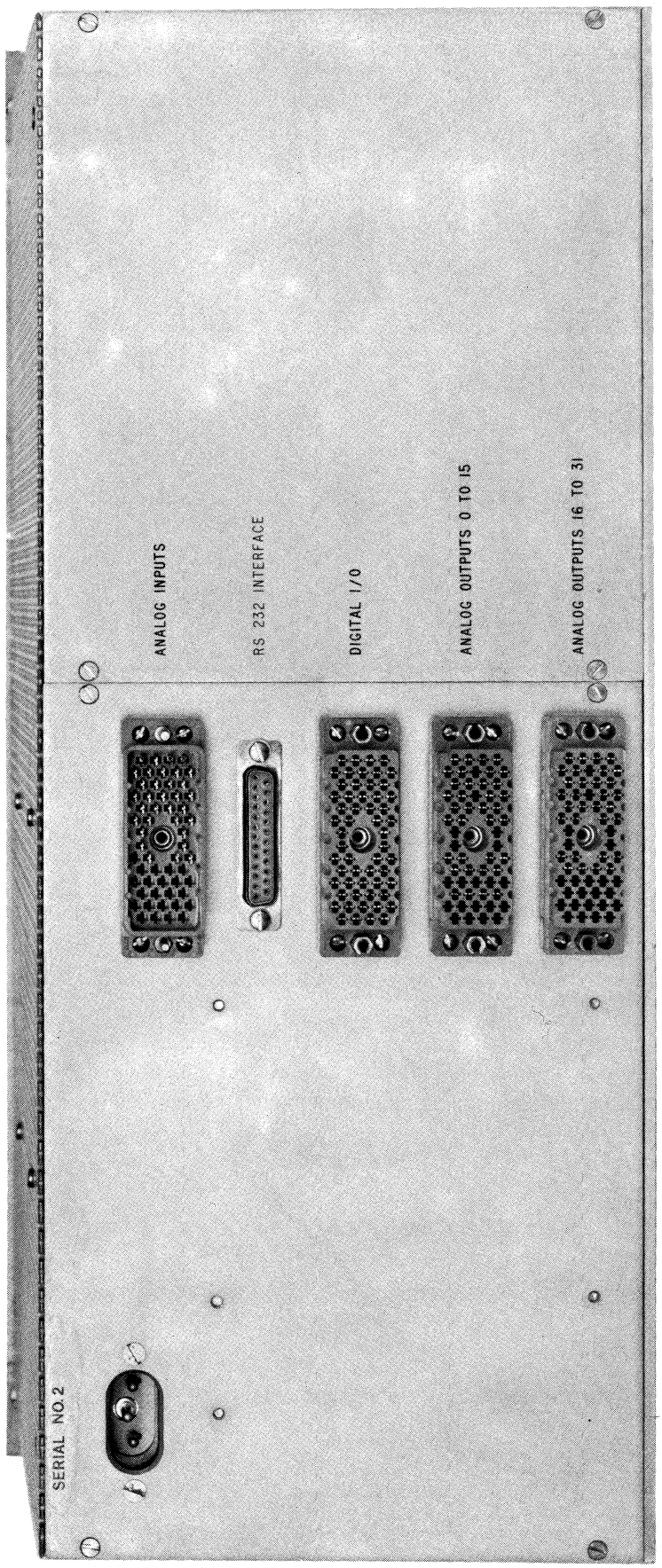


FIGURE 3

Front-End Data Link, Rear View

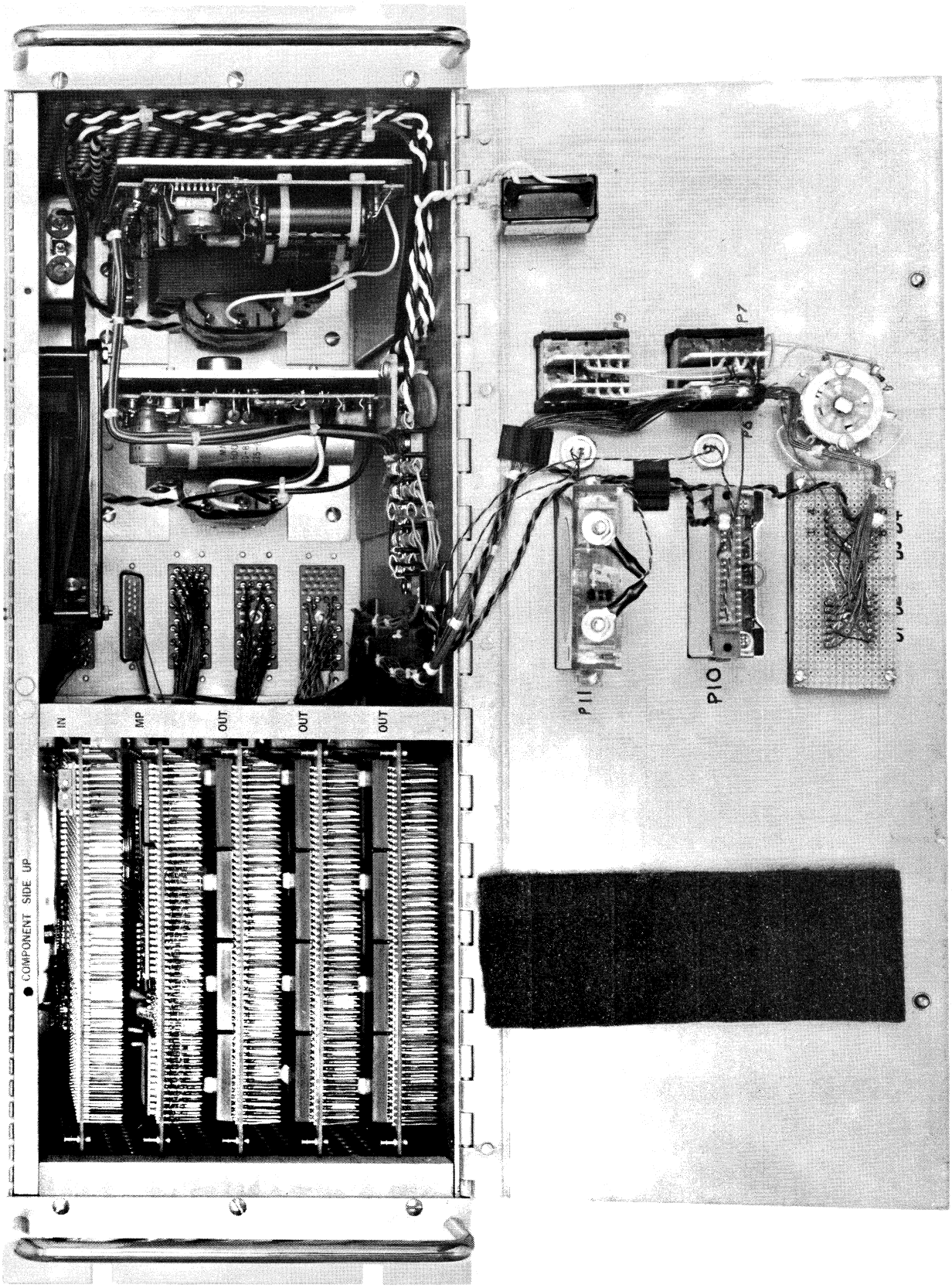


FIGURE 4

Front-End Data Link, Inside Front View

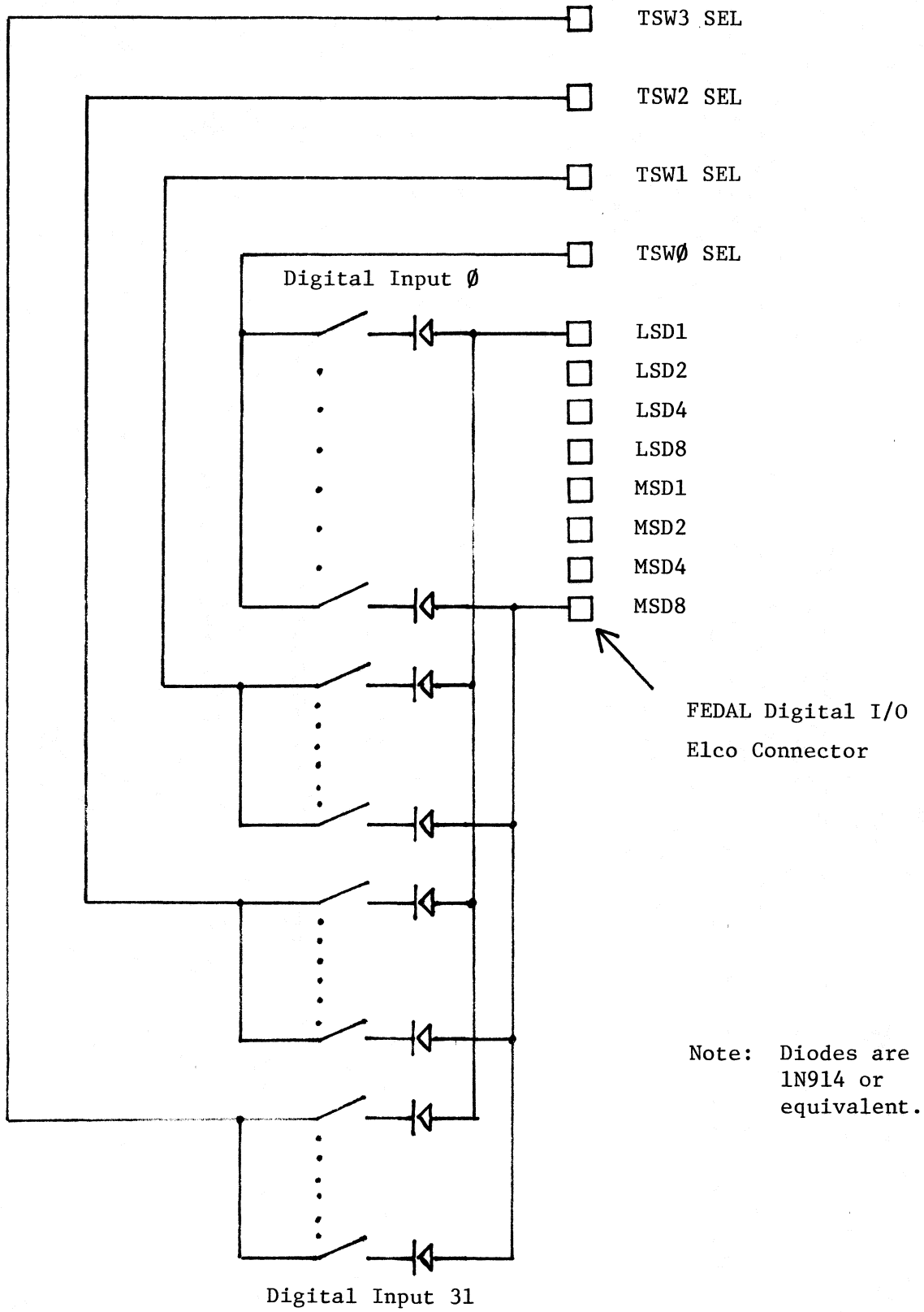


FIGURE 5

A possible digital input configuration using switches and diodes.

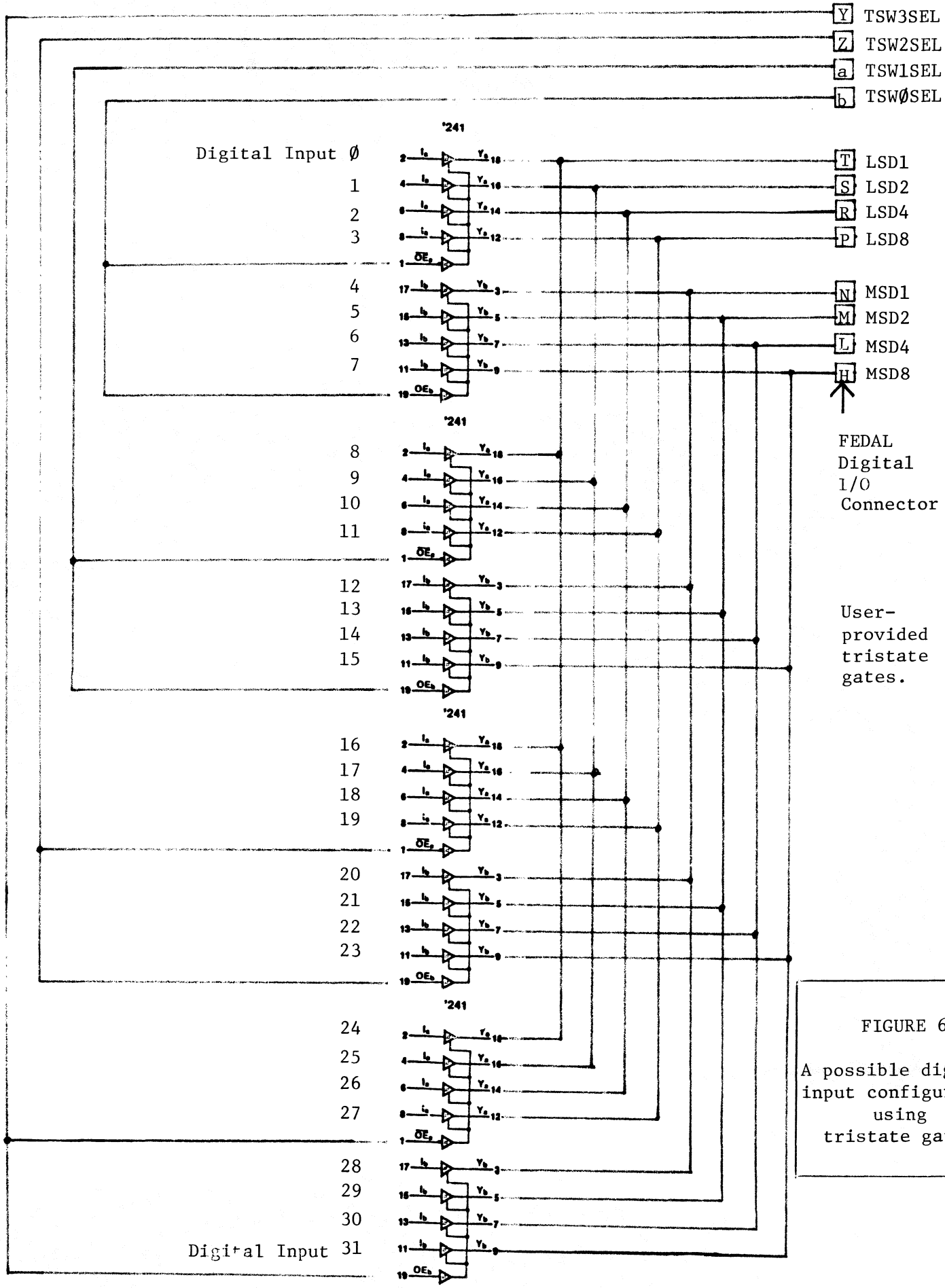
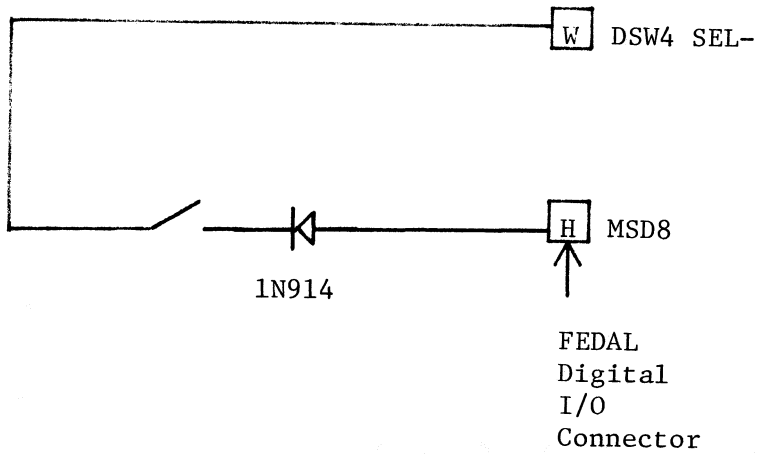


FIGURE 6

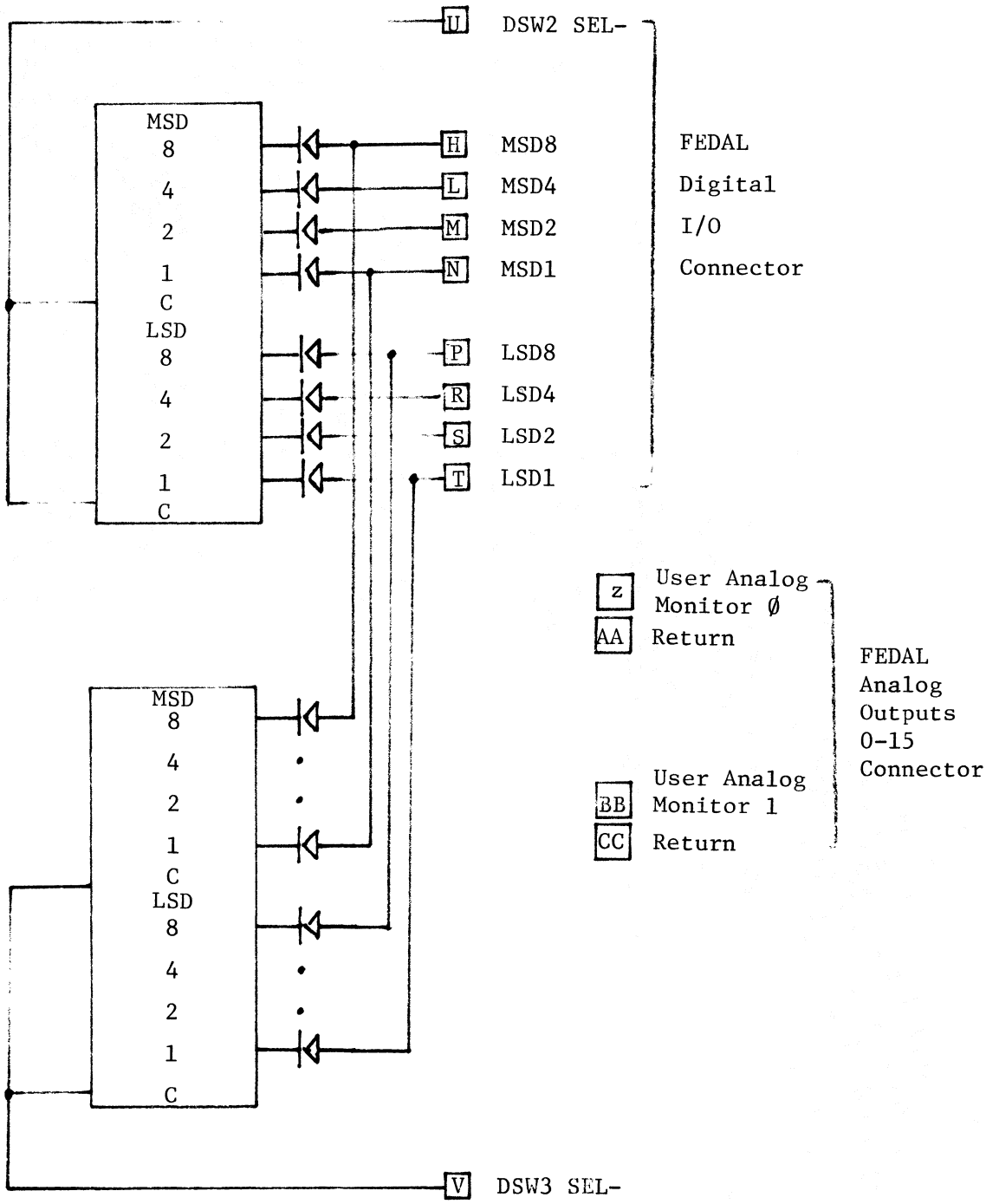
A possible digital input configuration using tristate gates.



Note: Digital Output select requires switch open, or not implemented. Limit Bit Output select requires switch closed.

FIGURE 7

Limit-bit/digital-output select switch.



User supplied digiswitches (Cherry T75-52M-2, or equivalent) and diodes (1N914, or equivalent).

FIGURE 8

Connection of user remote analog voltage monitors.

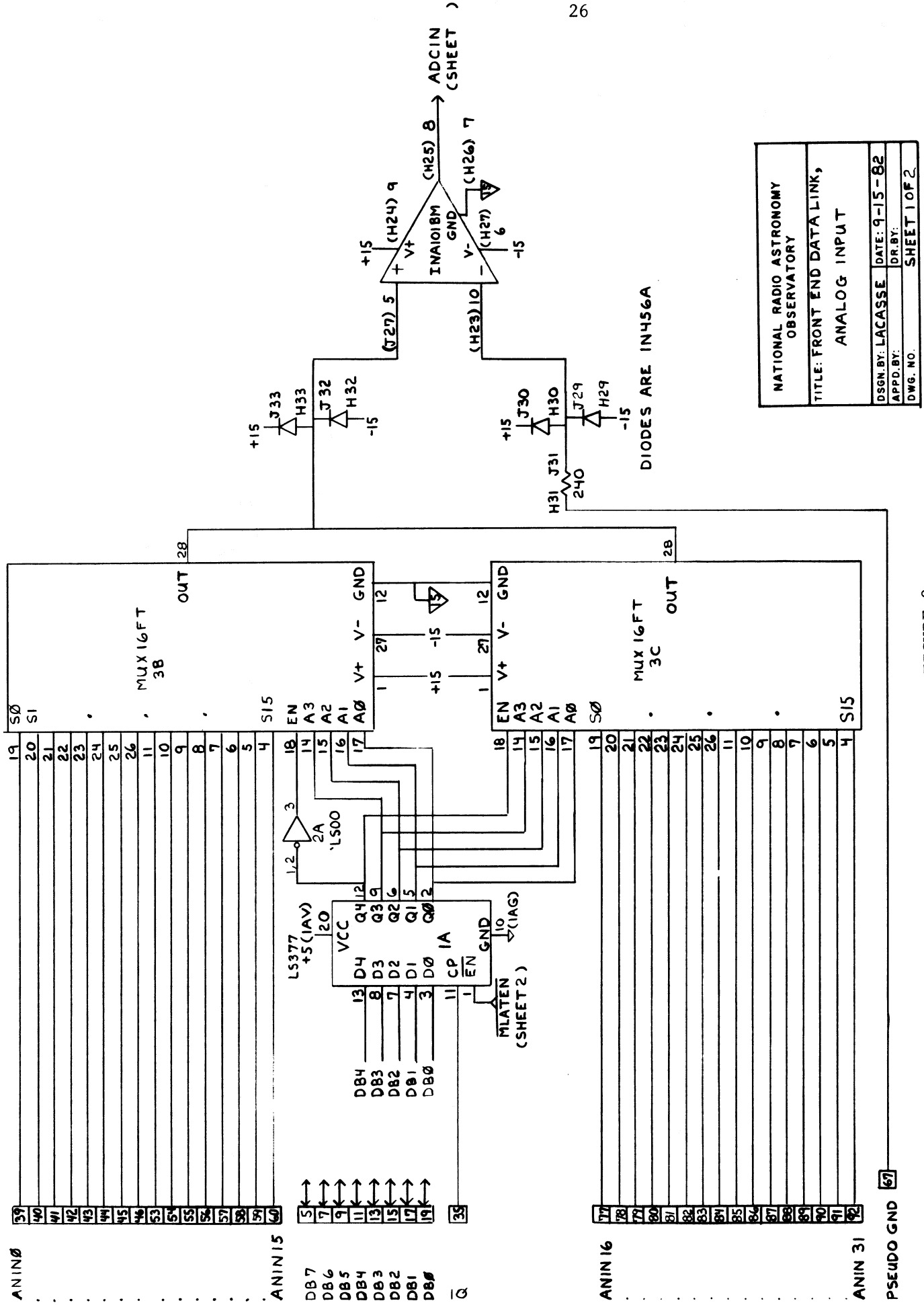
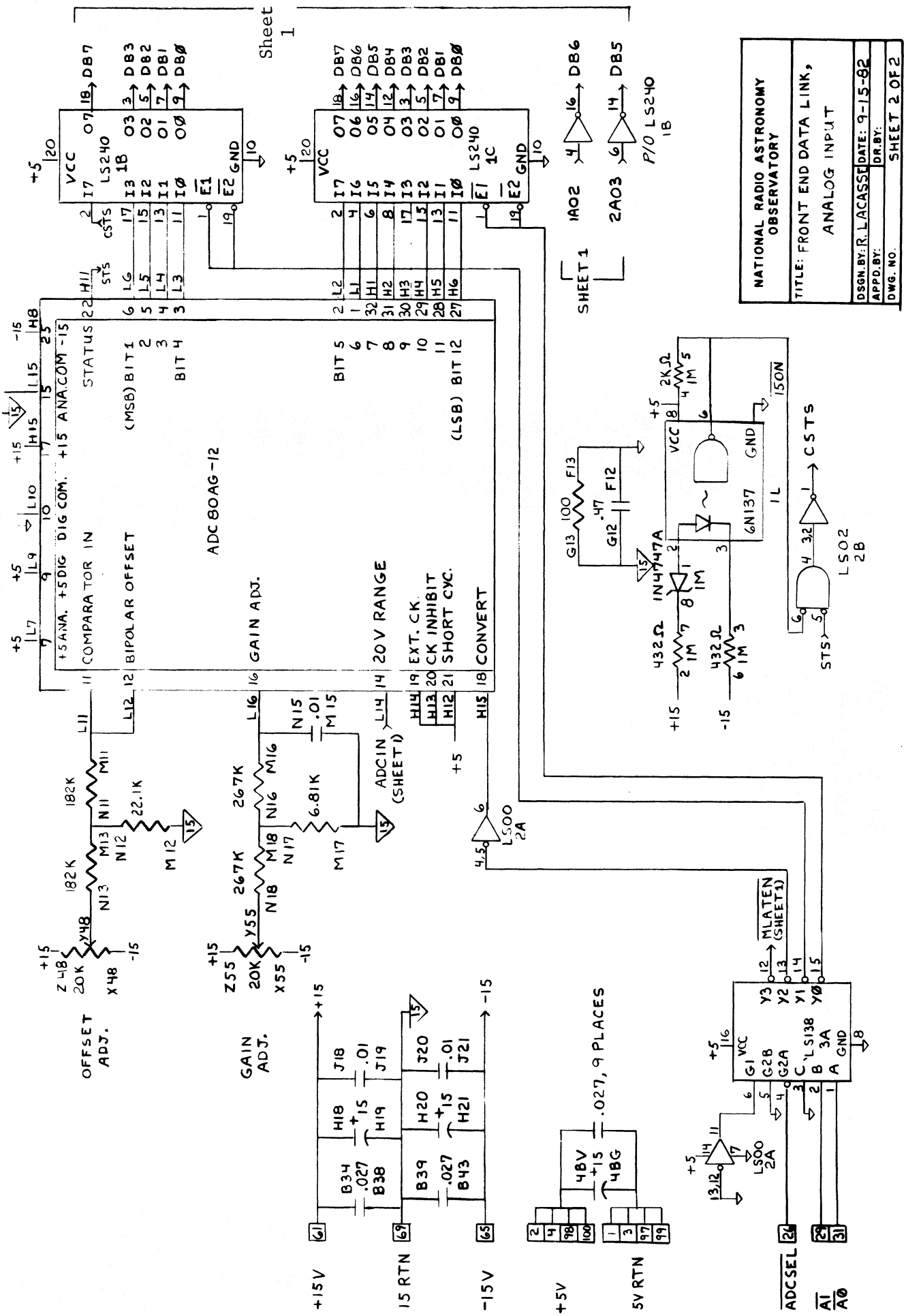

ADCIN (SHEET)
INA101BM
(H25) 8
(H26) 7
(H24) 9
(H27) 6
+15
-15
(J27) 5
(H23) 10
J33 H33
J32 H32
J30 H30
J29 H29
J31
H31 240
DIODES ARE IN456A
NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: FRONT END DATA LINK, ANALOG INPUT
DSGN. BY: LACASSE
DATE: 9-15-82
APPD. BY:
DR. BY:
DWG. NO.
SHEET 1 OF 2
MUX 16FT 3B
MUX 16FT 3C
OUT
GND
V-
V+
EN
A3
A2
A1
A0
S0
S1
S15
LS377 +5(IAV)
VCC
GND
(IAG)
CP
EN
D4
D3
D2
D1
D0
Q4
Q3
Q2
Q1
Q0
2A
LS00
MLATEN (SHEET 2)
DB4
DB3
DB2
DB1
DB0
ANIN0
ANIN15
ANIN 16
ANIN 31
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
PSEUDO GND

FIGURE 9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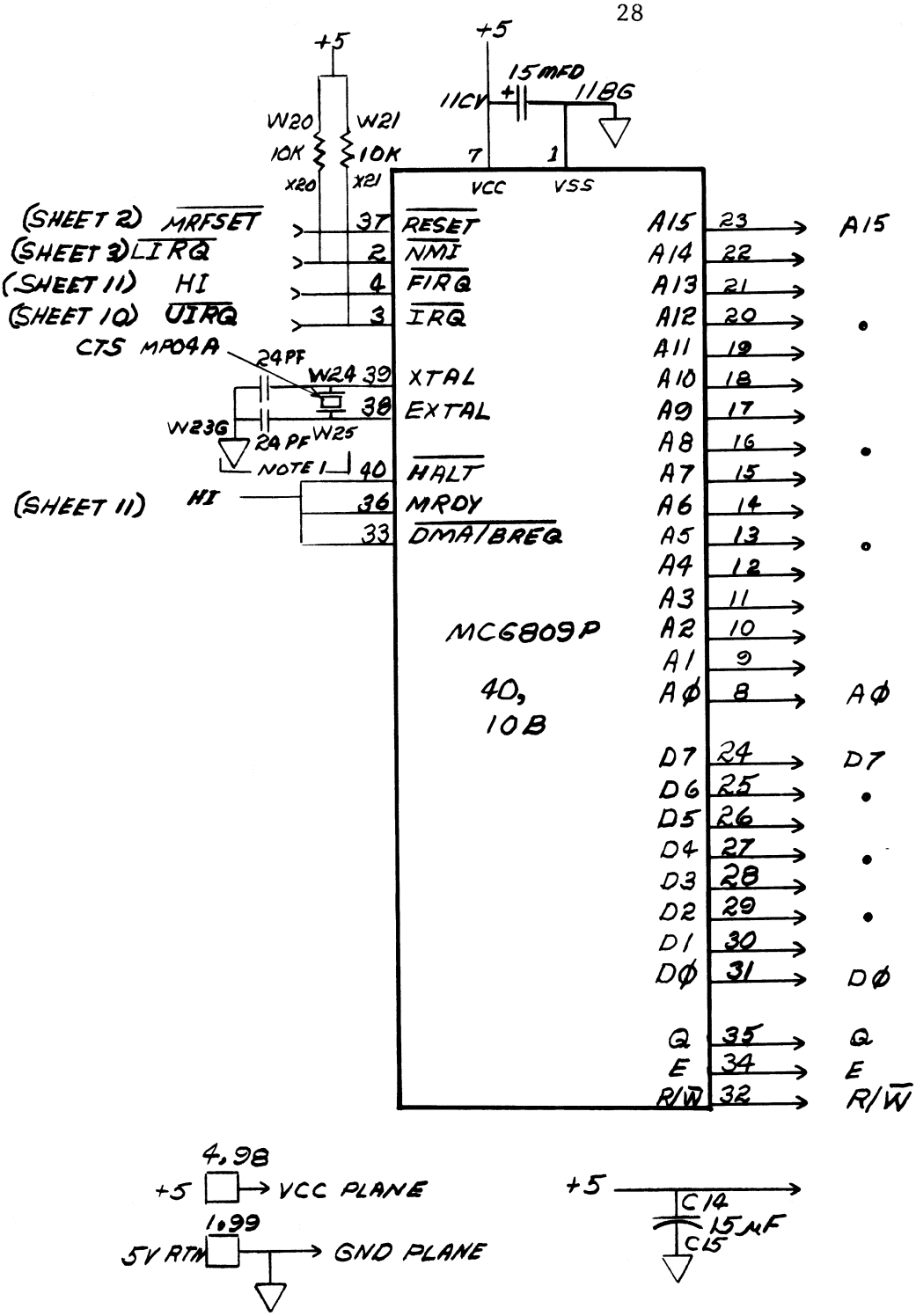
BIPOLAR OFFSET
GAIN ADJ.
20V RANGE
EXT. CK.
CK INHIBIT
SHORT CYC.
CONVERT
+5ANA. +5DIG
DIG COM.
+15 ANA.COM
-15
STATUS
(MSB) BIT 1
BIT 4
BIT 5
(LSB) BIT 12
LS240 1B
LS240 1C
P/O LS240 1B
SHEET 1
1A02
2A03
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
CSTS
STS
182K
22.1K
267K
6.81K
100
.47
2K Ω
432 Ω
1N4447A
6N137
LS02 2B
LS00 2A
LS138
MLATEN (SHEET 1)
ADCIN (SHEET 1)
OFFSET ADJ.
GAIN ADJ.
20K
.01
.027
4BV
4BG
.027, 9 PLACES
+15V
15 RTN
-15V
+5V
5V RTN
ADCSEL
AI
A0
NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: FRONT END DATA LINK, ANALOG INPUT
DSGN. BY: R. LACASSE
DATE: 9-15-82
APPD. BY:
DR. BY:
DWG. NO.
SHEET 2 OF 2

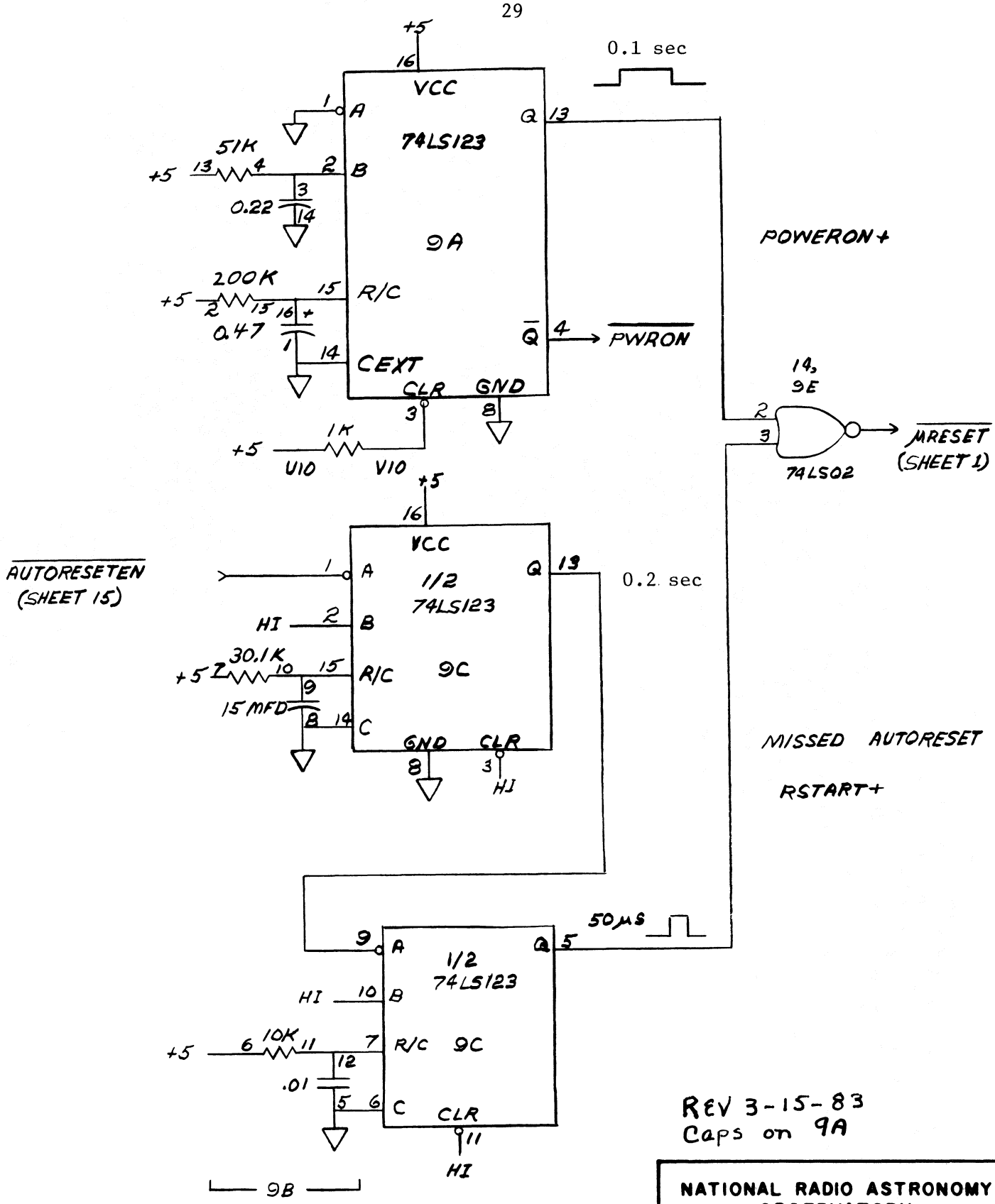
FIGURE 10



NOTE 1: THESE THREE COMPONENTS ARE WRAPPED ON THE WIRE SIDE OF THE BOARD

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK (FEDAL), MP BOARD, MICROPROCESSOR	
DSGN. BY: R. LACASSE	DATE: 6/83
APPD. BY:	DR. BY:
DWG. NO.	SHEET 1 OF 18

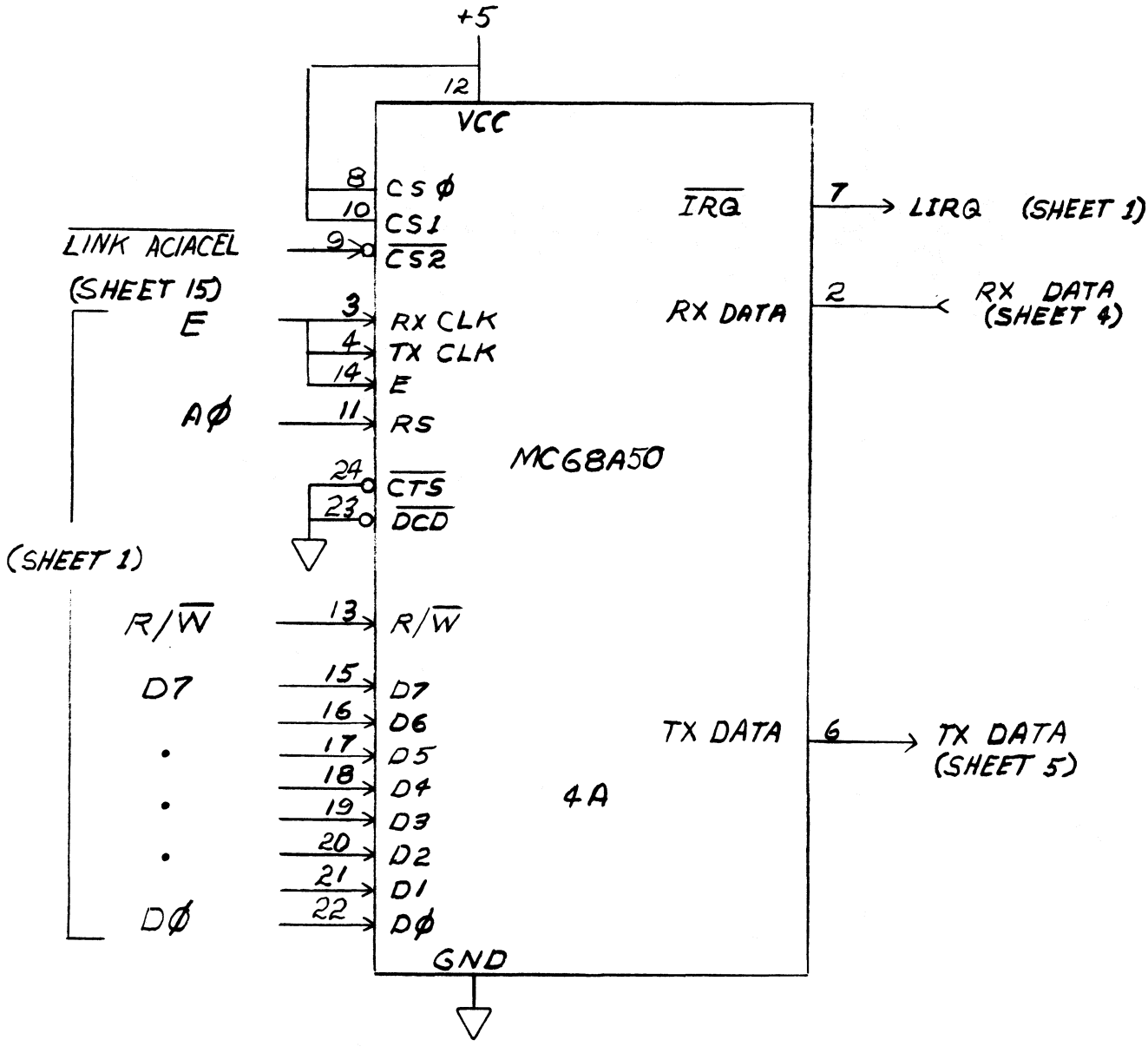
FIGURE 11



REV 3-15-83
Caps on 9A

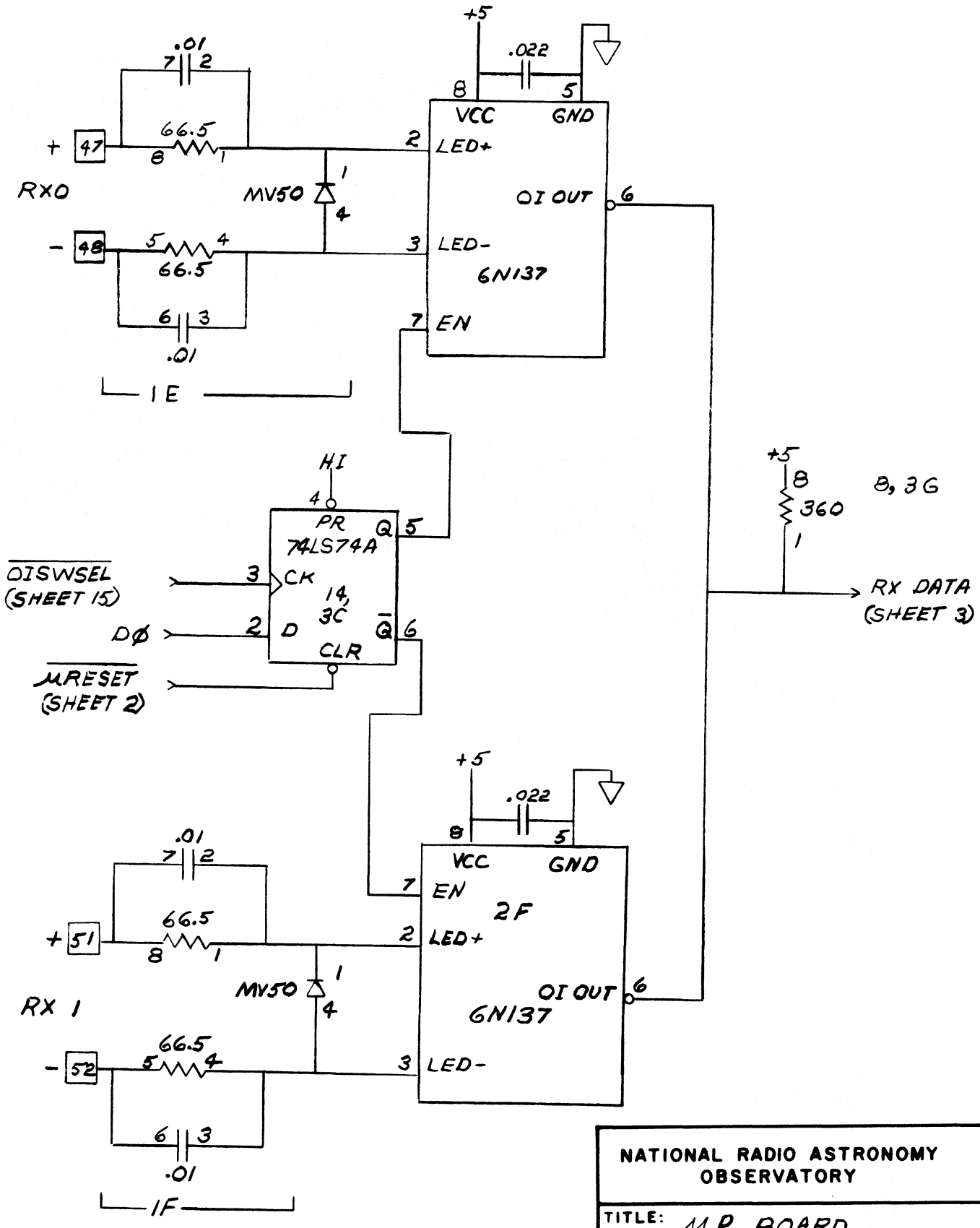
NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD RESET AND AUTO RESET	
DSGN. BY:	DATE:
APP'D. BY:	DR. BY:
DWG. NO.	SHEET 2 OF 18

FIGURE 12



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD LINK ACIA	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 3 OF 18

FIGURE 13



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD, LINK RECEIVERS	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 4 OF 18

FIGURE 14

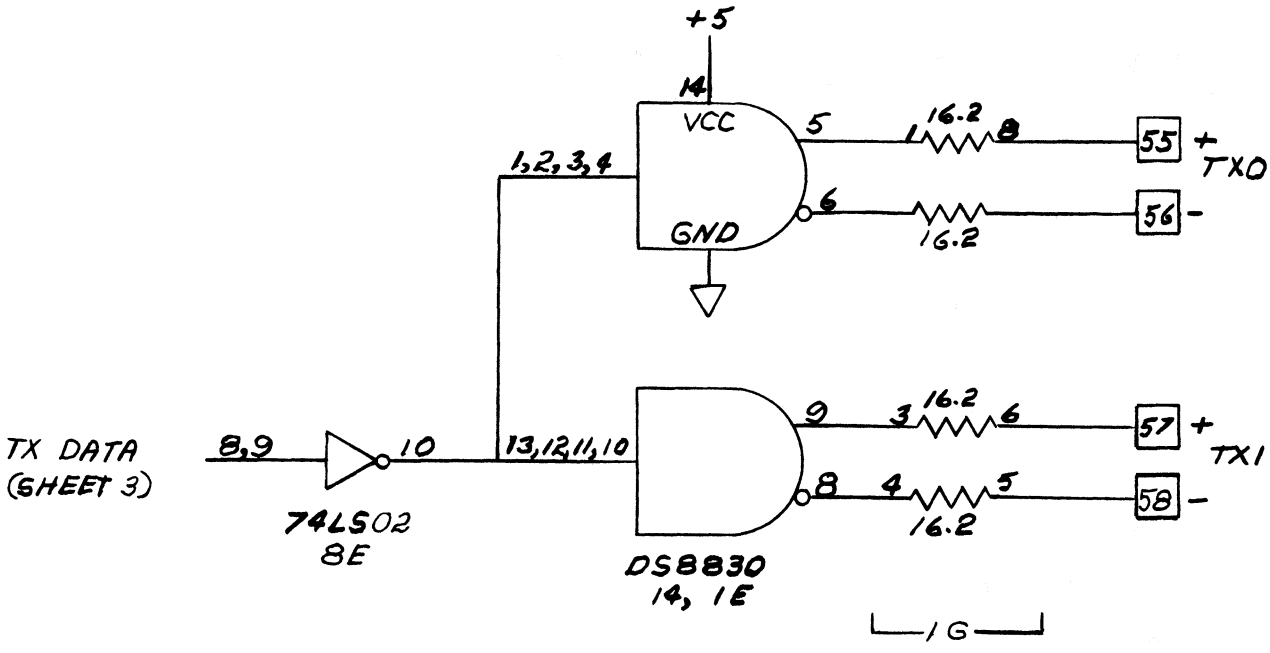
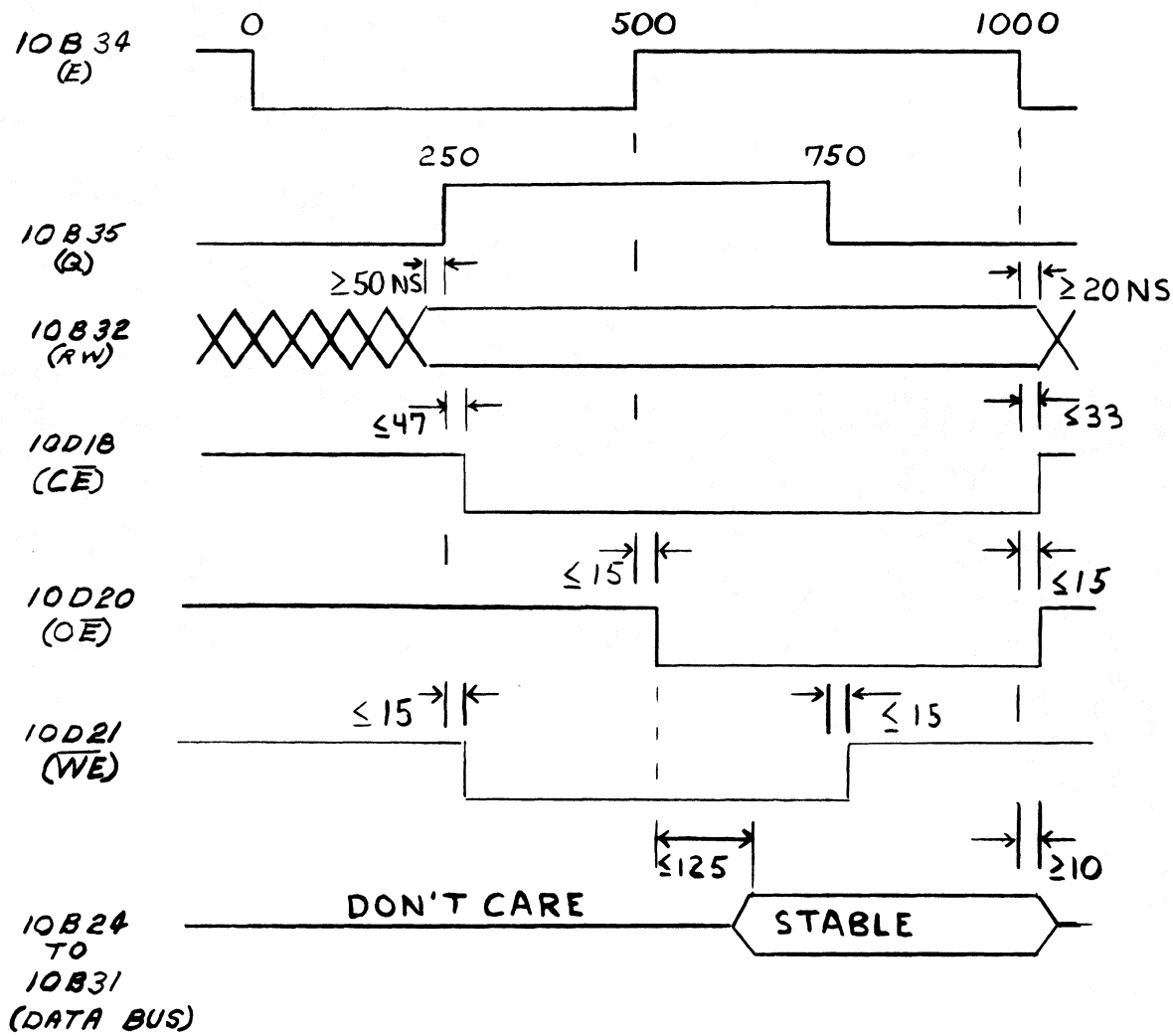


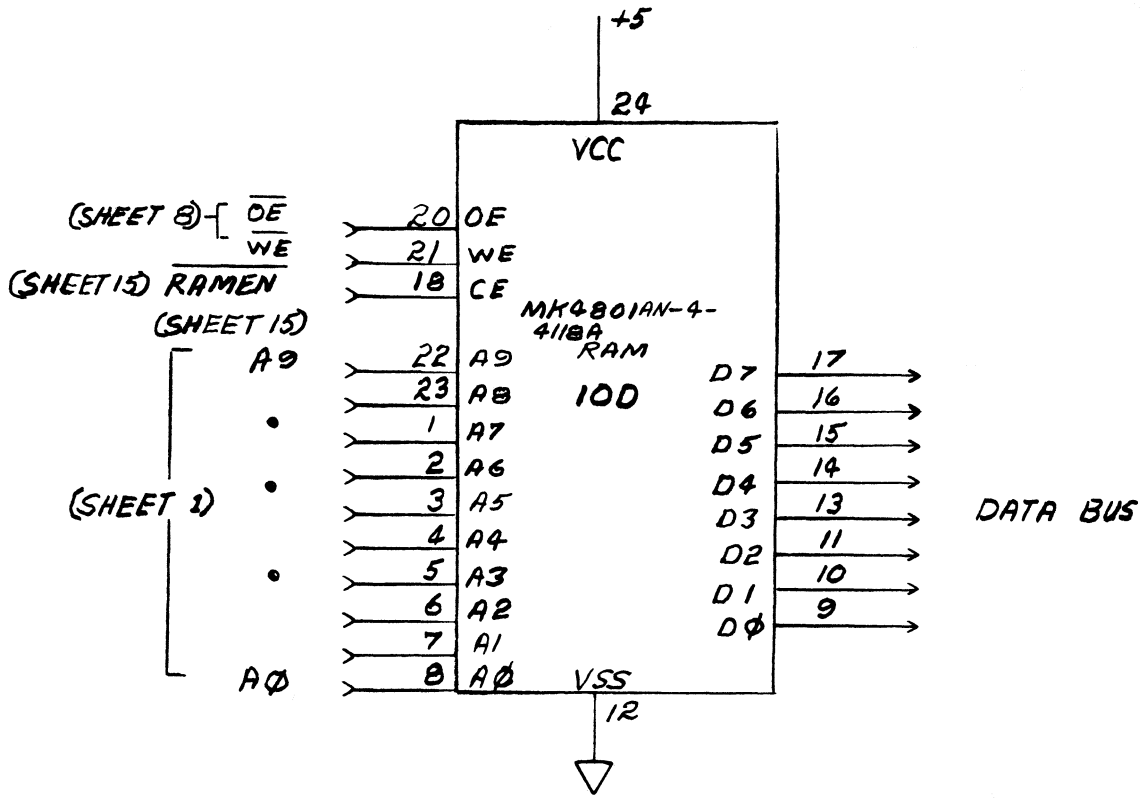
FIGURE 15

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD LINK DRIVERS	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 5 OF 18



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD SYSTEM TIMING	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 6 OF 18

FIGURE 16



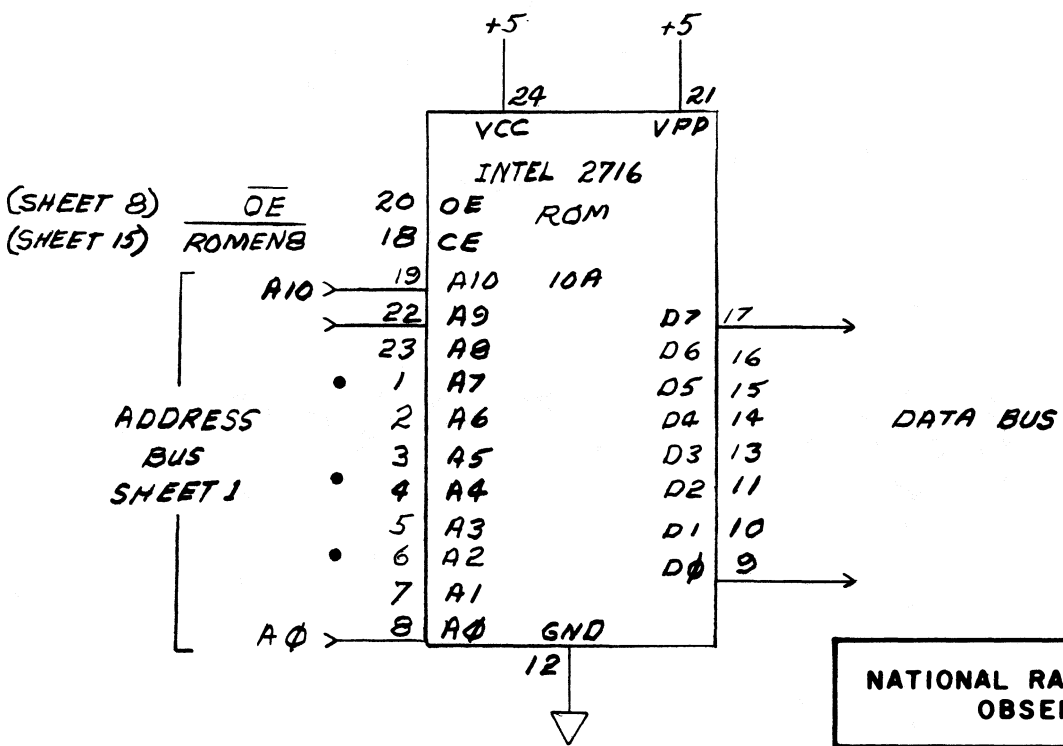


FIGURE 17

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: μP BOARD RAM, F800 ROM	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 7 OF 18

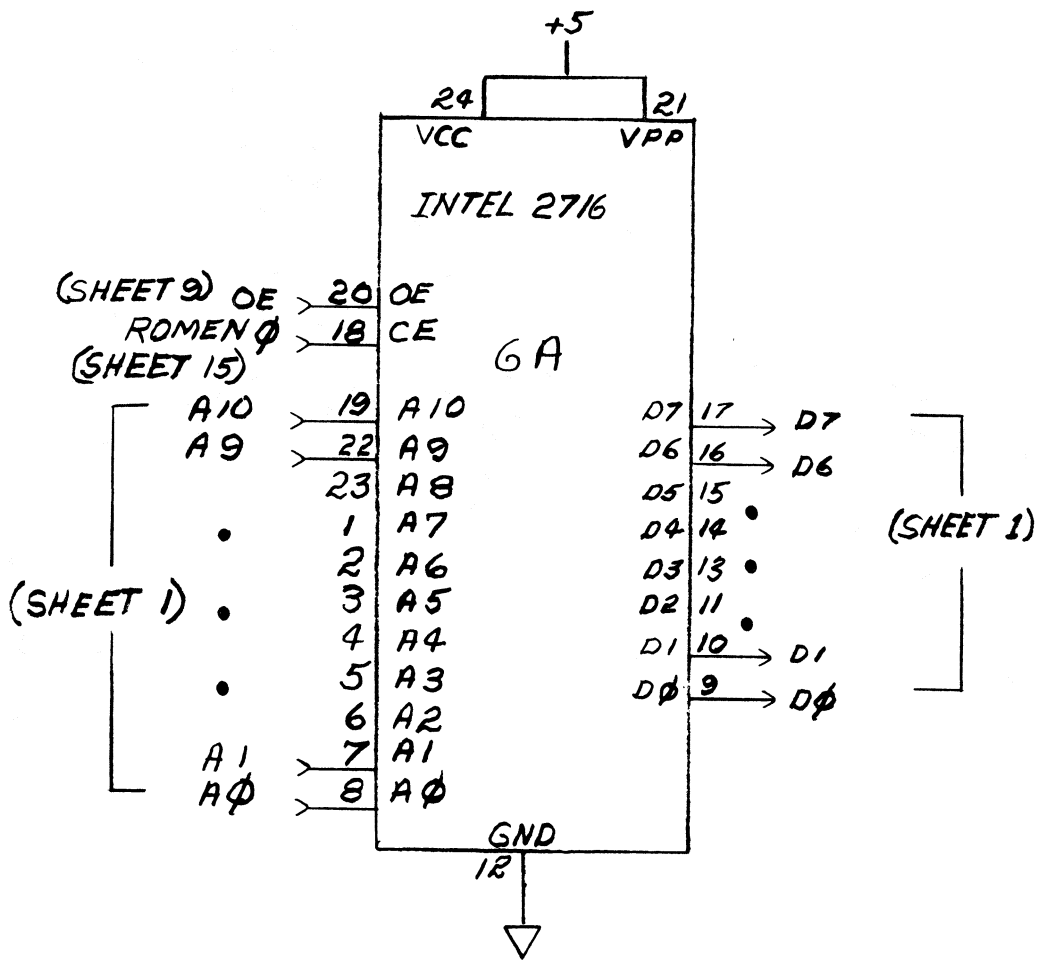


FIGURE 18

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD F000 ROM	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 8 OF 18

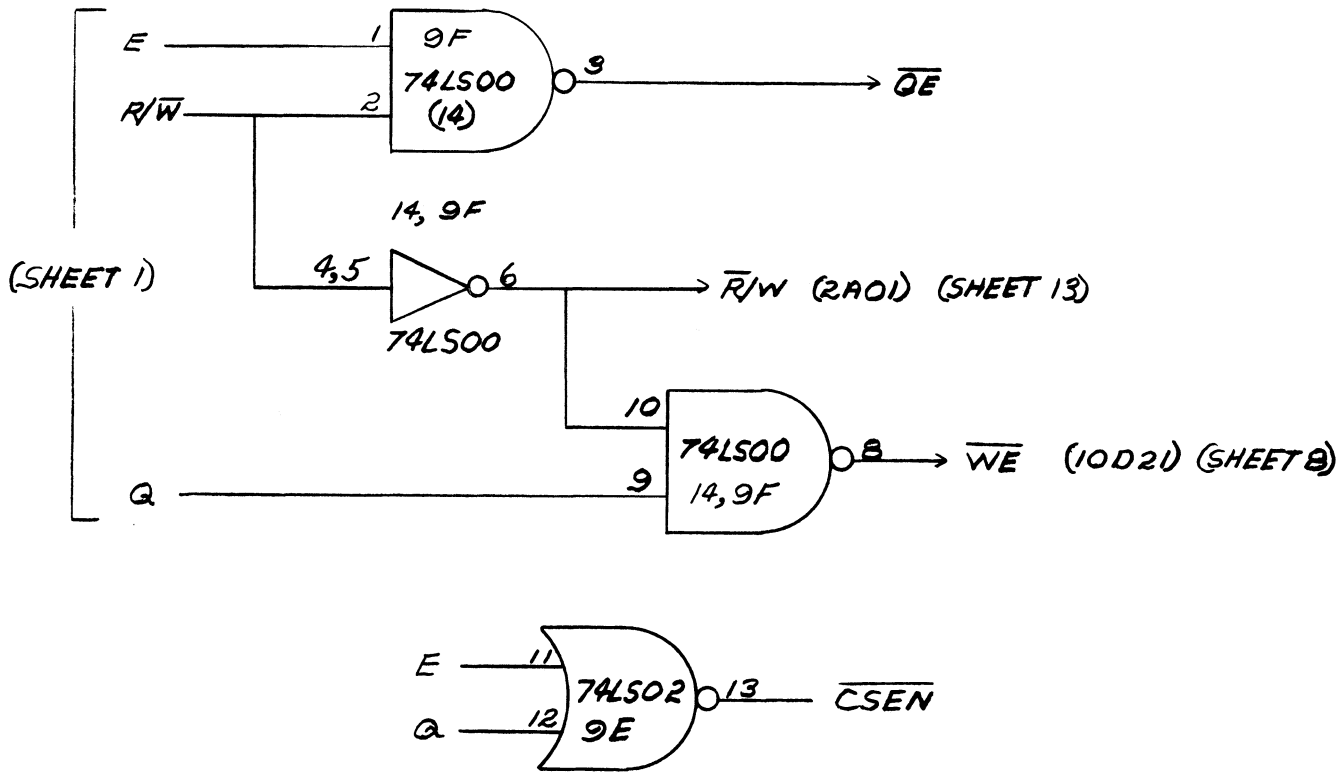
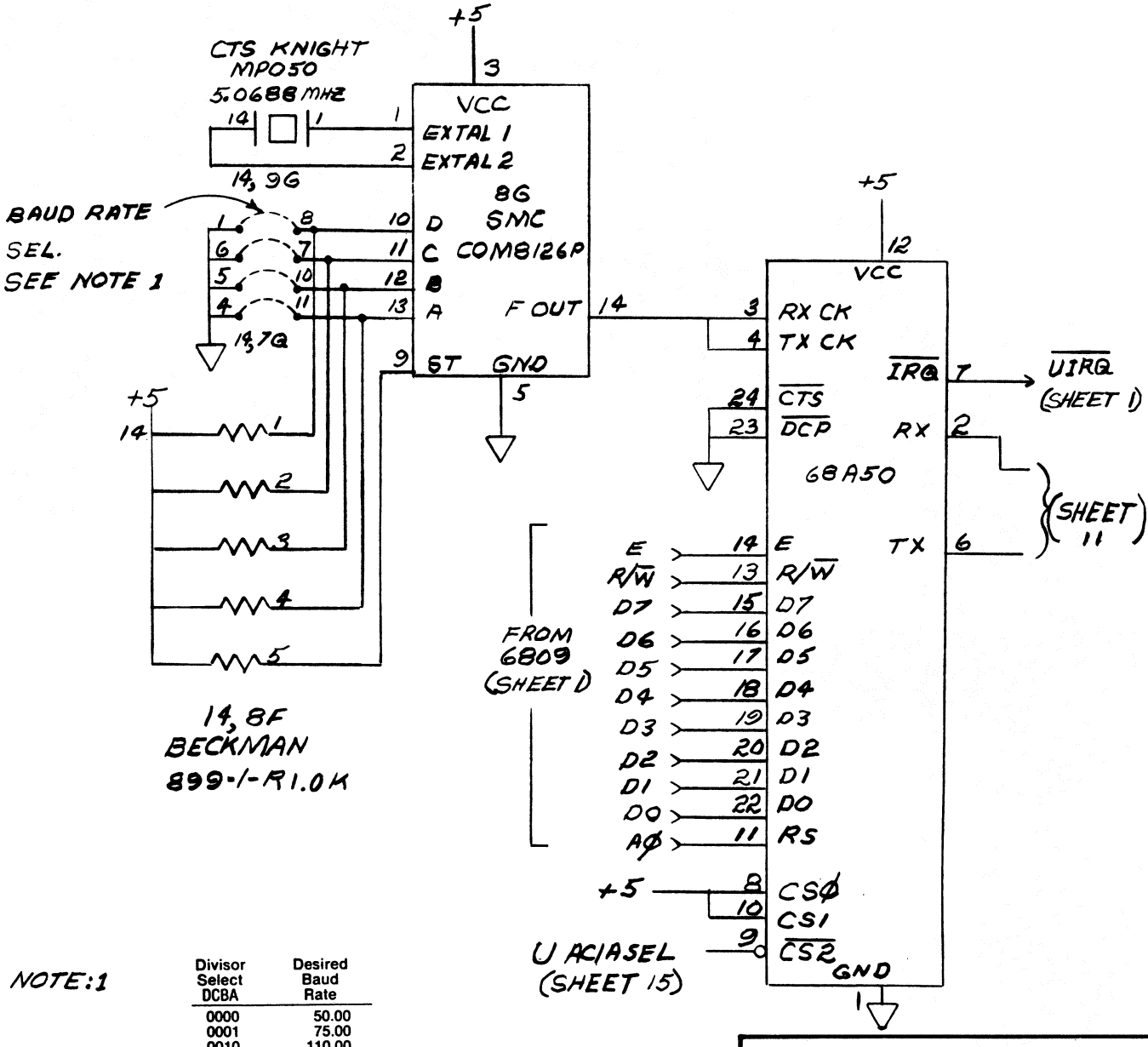


FIGURE 19

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD RAM CONTROL SIGNALS	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 9 OF 18

RS232 INTERFACE

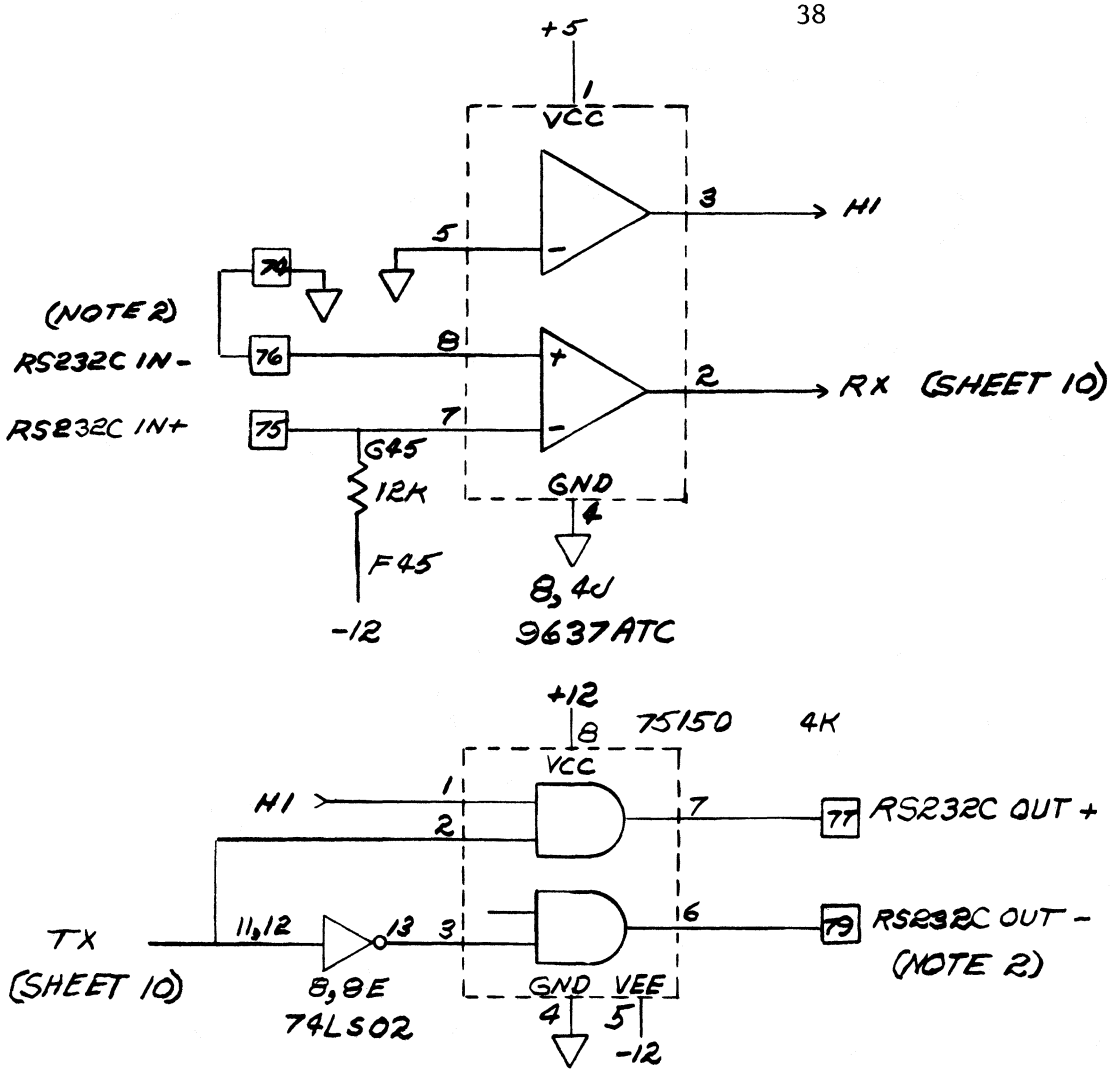


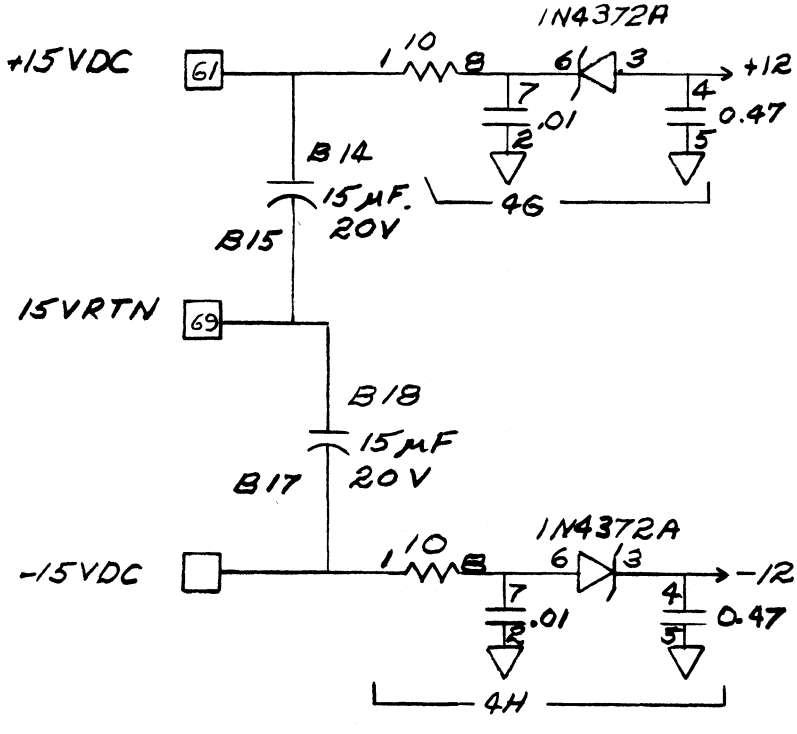
NOTE:1

Divisor Select DCBA	Desired Baud Rate	
0000	50.00	
0001	75.00	
0010	110.00	
0011	134.50	
0100	150.00	
0101	300.00	
0110	600.00	
0111	1200.00	DEFAULT
1000	1800.00	
1001	2000.00	
1010	2400.00	
1011	3600.00	
1100	4800.00	
1101	7200.00	
1110	9600.00	
1111	19200.00	

FIGURE 20

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD USER ACIA	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 10 OF 18

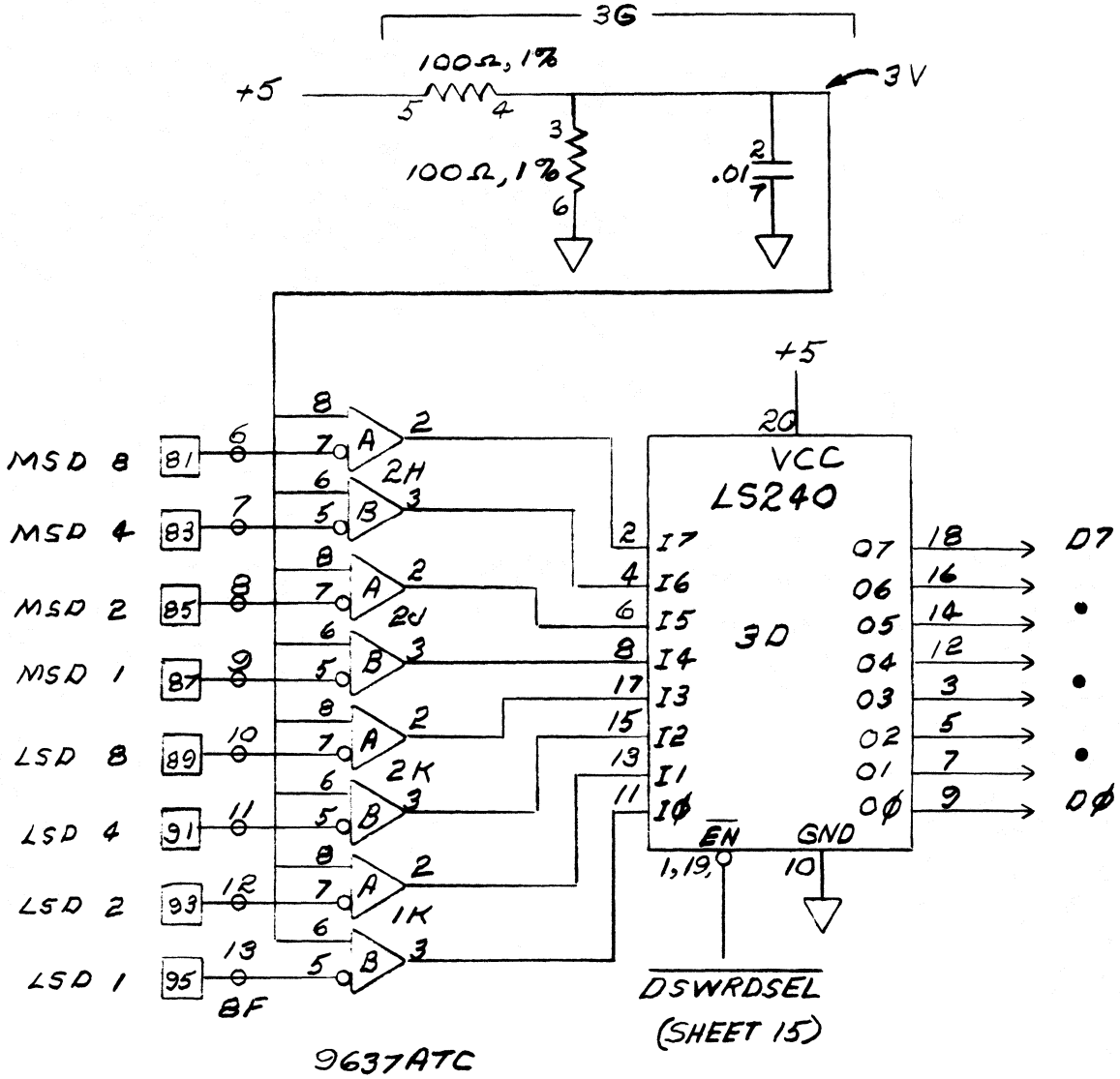




NOTE 2: THE MINUS INPUT IS NORMALLY GROUNDED ON THE CONNECTOR, AND THE MINUS OUTPUT IS UNUSED FOR RS232 COMMUNICATION. THEY ARE BROUGHT OUT FOR POSSIBLE COMPATIBILITY WITH DIFFERENTIAL STANDARDS.

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD USER RS232 RECEIVER AND TRANSMITTER	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 11 OF 18

FIGURE 21

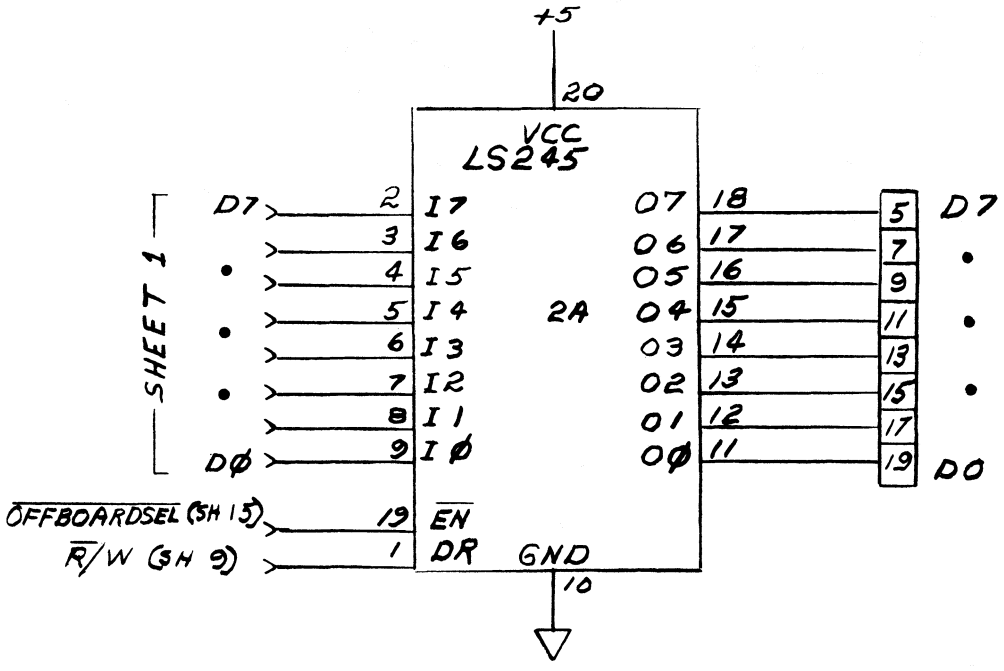


9637ATC
LINE RECEIVERS
VCC = 1
GND = 4
ON EACH OF 4 PACKAGES

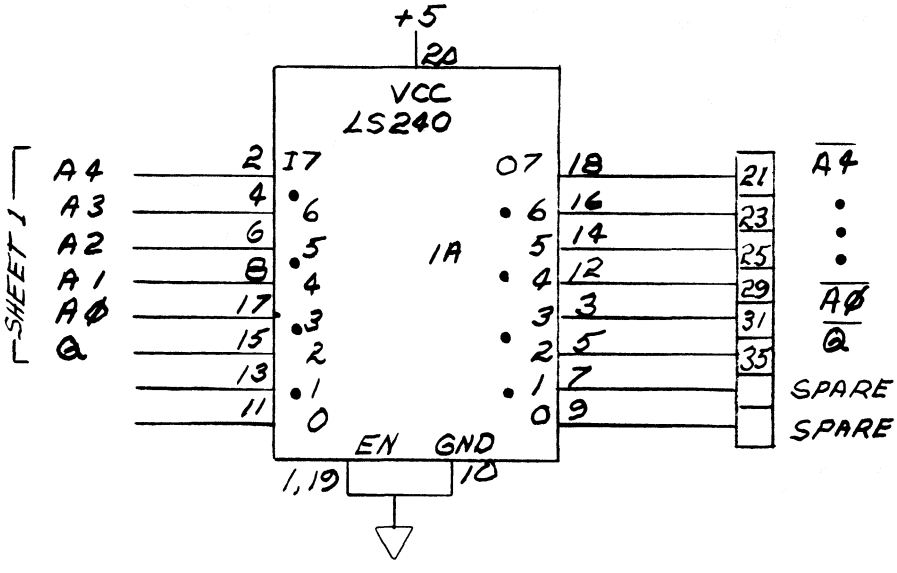
O = 4.7K PULL UP TO 5V

FIGURE 22

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD DIGI-SWITCH READ LOGIC	
DSGN. BY:	DATE:
APP'D. BY:	DR. BY:
DWG. NO.	SHEET 12 OF 18



OFF CARD DATA BUS DRIVER



MISC SIGNAL DRIVER

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD OFF BOARD DRIVERS, RECEIVERS	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 13 OF 18

FIGURE 23

A15	A14	A13	A12	A11	
1	1	1	1	1	ROMEN 8
1	1	1	1	0	ROMEN Ø
1	1	1	0	1	
1	1	1	0	0	
1	1	0	1	1	
1	1	0	1	0	
1	1	0	0	1	
1	1	0	0	0	
1	0	1	1	1	
1	0	1	1	0	
1	0	1	0	1	
1	0	1	0	0	
1	0	0	1	1	
1	0	0	1	0	
1	0	0	0	1	
1	0	0	0	0	
0	1	1	1	1	
0	1	1	1	0	
0	1	1	0	1	
0	1	1	0	0	
0	1	0	1	1	
0	1	0	1	0	
0	1	0	0	1	
0	1	0	0	0	
0	0	1	1	1	
0	0	1	1	0	RSTEN
0	0	1	0	1	UACIASEL
0	0	1	0	0	OISWSEL
0	0	0	1	1	LINKACIASEL
0	0	0	1	0	AUTORESETEN
0	0	0	0	1	POSSIBLE RAM EXPANSION
0	0	0	0	0	RAMEN

SELSWEN
TSWSEL — TSWSEL Ø, TSWSEL 1, TSWSEL 2, TSWSEL 3

A1	A0
0	0
0	1
1	0
1	1

DSW 5 SEL
DSW 4 SEL
DSW 3 SEL
DSW 2 SEL
DSW 1 SEL
DSW Ø SEL
} DSWRD SEL

RLATEN
LLATEN
ANOUTSEL 2
ANOUTSEL 1
ANOUTSEL Ø
ADCSEL
} OFF BOARD SEL

FIGURE 24

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD SELECT SIGNAL SUMMARY	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 14 OF 18

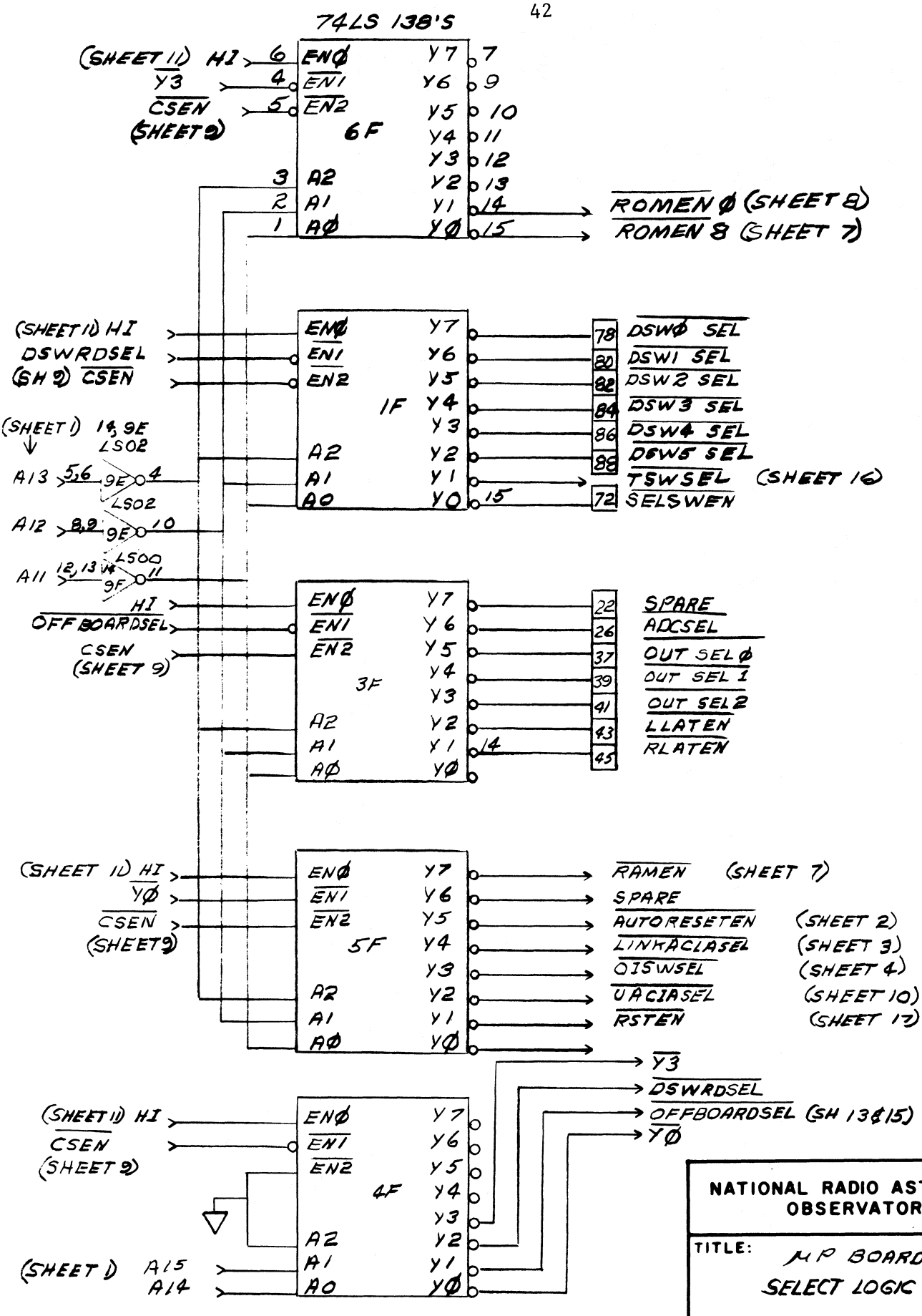
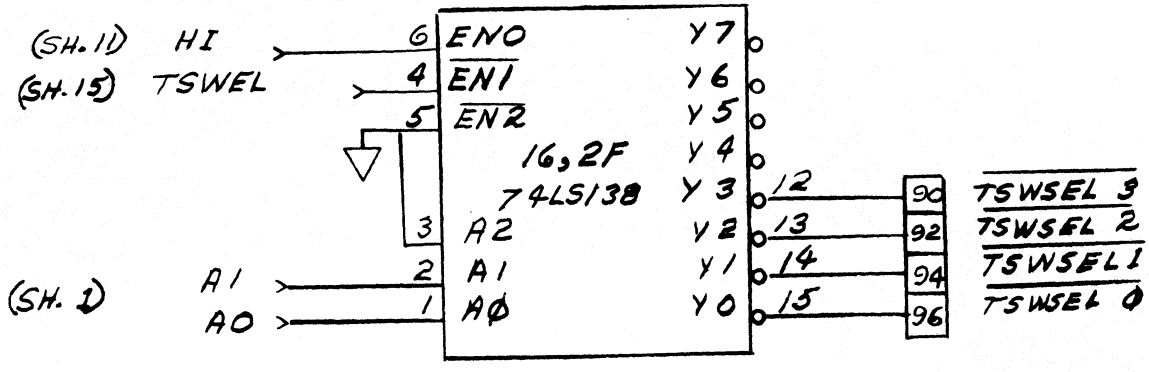


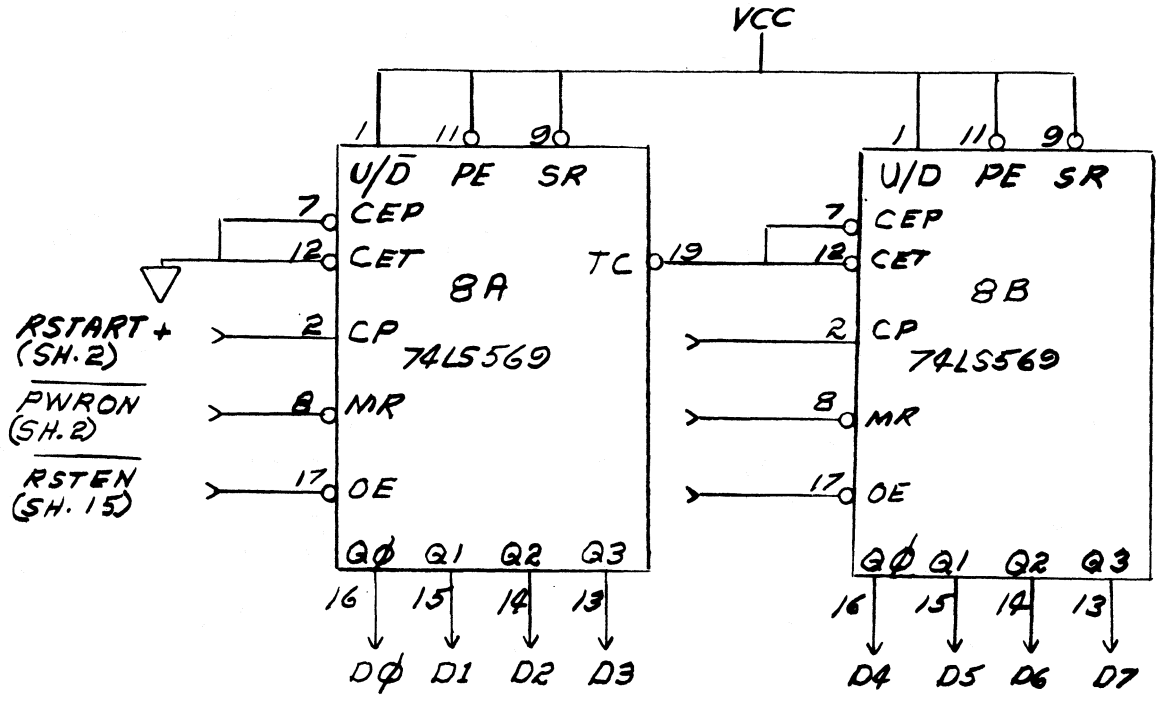
FIGURE 25

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: μP BOARD SELECT LOGIC	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 15 OF 18



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD SELECT LOGIC CONT'D	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 16 OF 18

FIGURE 26



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: MP BOARD RESTART ERROR COUNTER	
DSGN. BY:	DATE:
APPD. BY:	DR. BY:
DWG. NO.	SHEET 17 OF 18

FIGURE 27

SIGNAL	ANALYZER INPUT	BOARD PIN
	-POD A-	
A15	D15	Z16
A14	D14	Z15
A13	D13	Z14
A12	D12	Z13
A11	D11	Z12
A10	D10	Z11
A9	D9	Z10
A8	D8	Z9
A7	D7	Z8
A6	D6	Z7
A5	D5	Z6
A4	D4	Z5
A3	D3	Z4
A2	D2	Z3
A1	D1	Z2
AØ	DØ	Z1
Spare	QTRIG	Z17
R/$\overline{W}$	QCLK	Z18
E	CLK	Z19
GND	GND	Z20
	-POD B-	
D7	D15	Z36
D6	D14	Z35
D5	D13	Z34
D4	D12	Z33
D3	D11	Z32
D2	D10	Z31
D1	D9	Z3Ø
DØ	D8	Z29
$\overline{Y3}$	D7	Z28
$\overline{DSWRDSEL}$	D6	Z27
$\overline{OFFBOARDSEL}$	D5	Z26
$\overline{YØ}$	D4	Z25
$\overline{RAMEN}$	D3	Z24
$\overline{ROMEN}$	D2	Z23
$\overline{AUTORESETEN}$	D1	Z22
$\overline{LINKACIASEL}$	DØ	Z21
SPARE	QTRIG	Z37
R/$\overline{W}$	QCLK	Z38
E	CLK	Z39
GND	GND	Z40

FIGURE 28

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: LOGIC ANALYZER INTERFACE	
DSGN.BY:	DATE:
APPD.BY:	DR.BY:
DWG. NO.	SHEET 18 OF 18

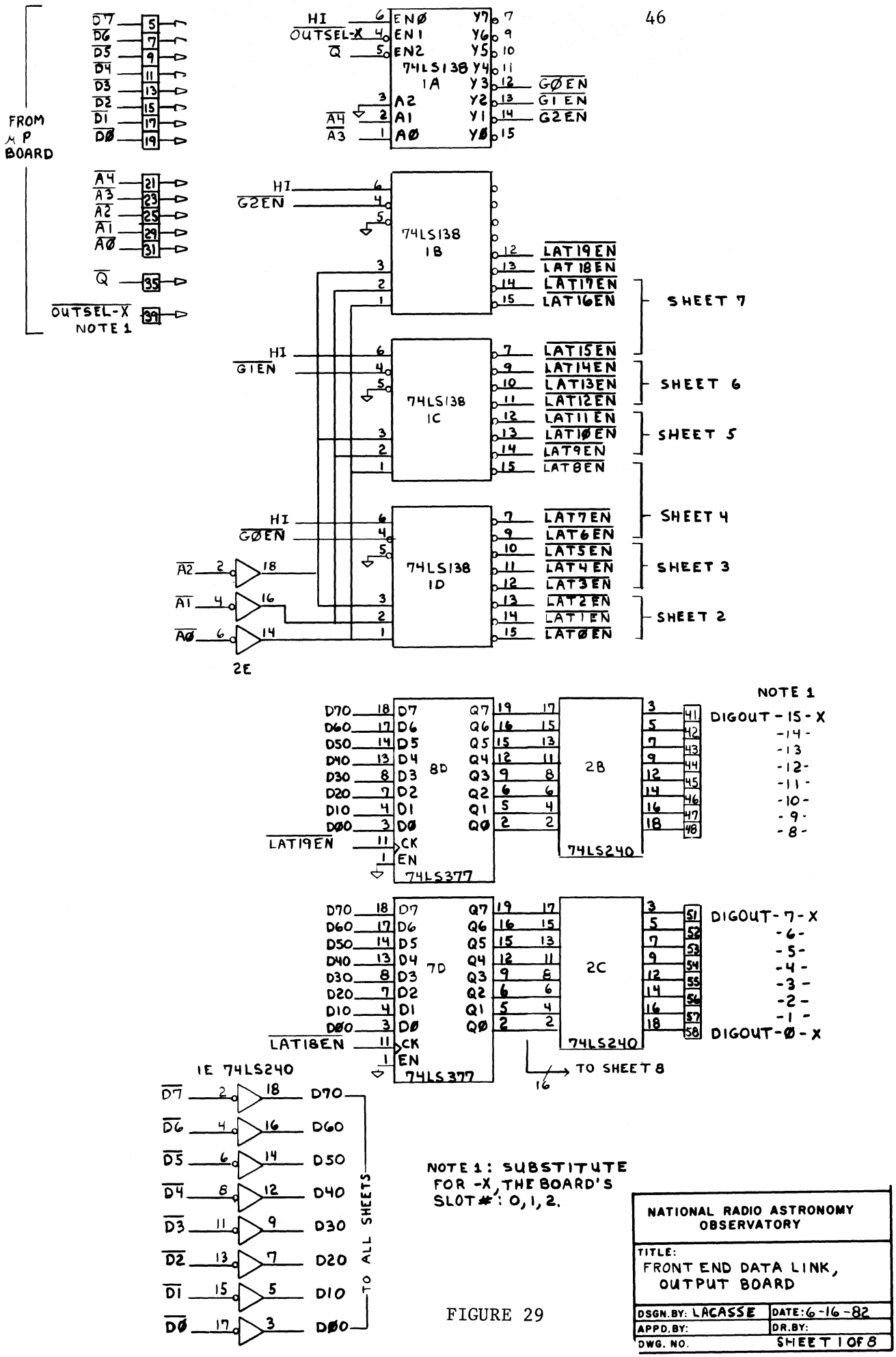
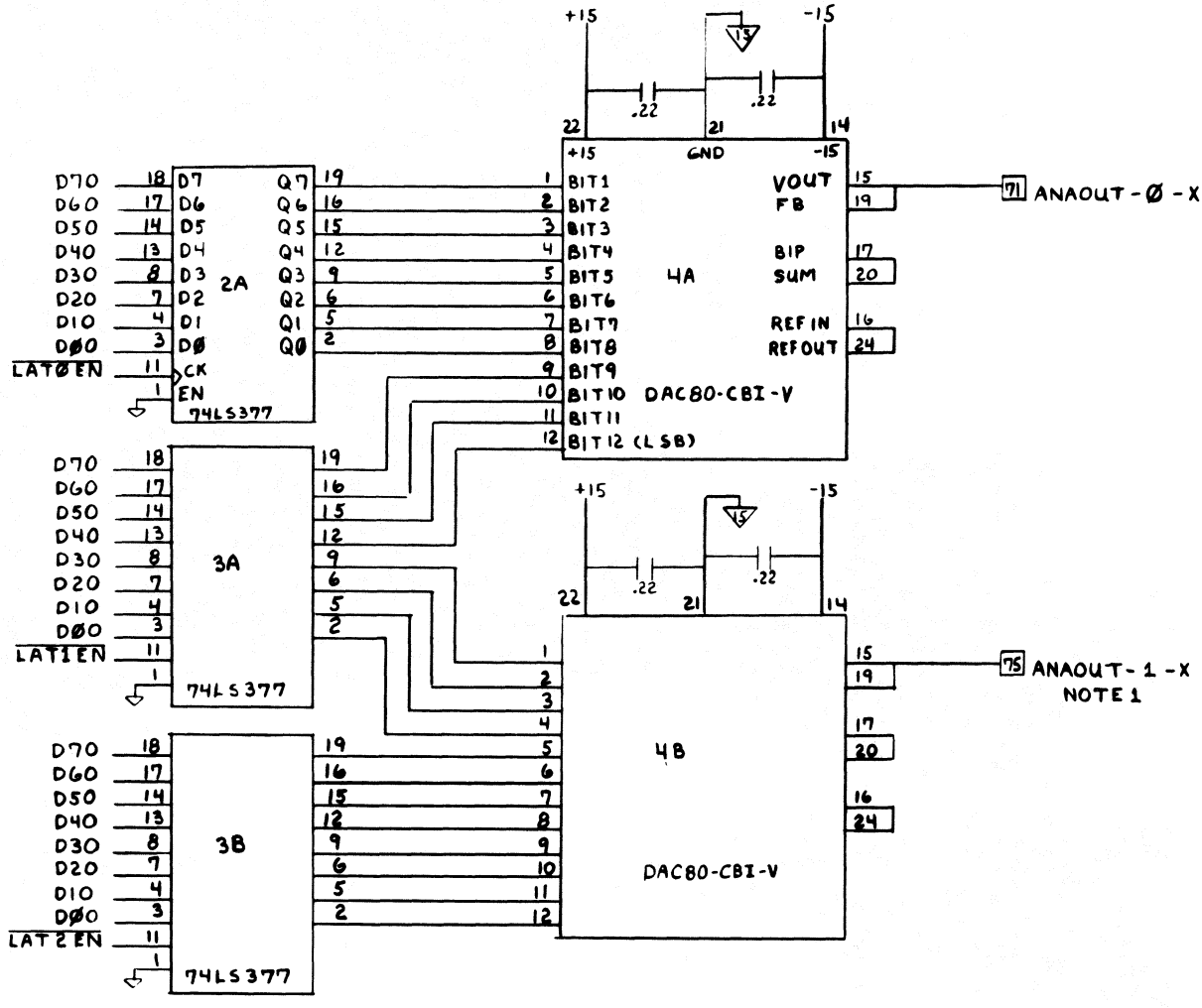


FIGURE 29

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN.BY: LACASSE	DATE: 6-16-82
APPD.BY:	DR.BY:
DWG. NO.	SHEET 1 OF 8



NOTE: THE 0.22μF, 15V DECOUPLING CAPACITORS ARE SOLDERED ON THE WIRE SIDE OF THE BOARD. SOME DACS SHARE DECOUPLING.

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 2 OF 8

FIGURE 30

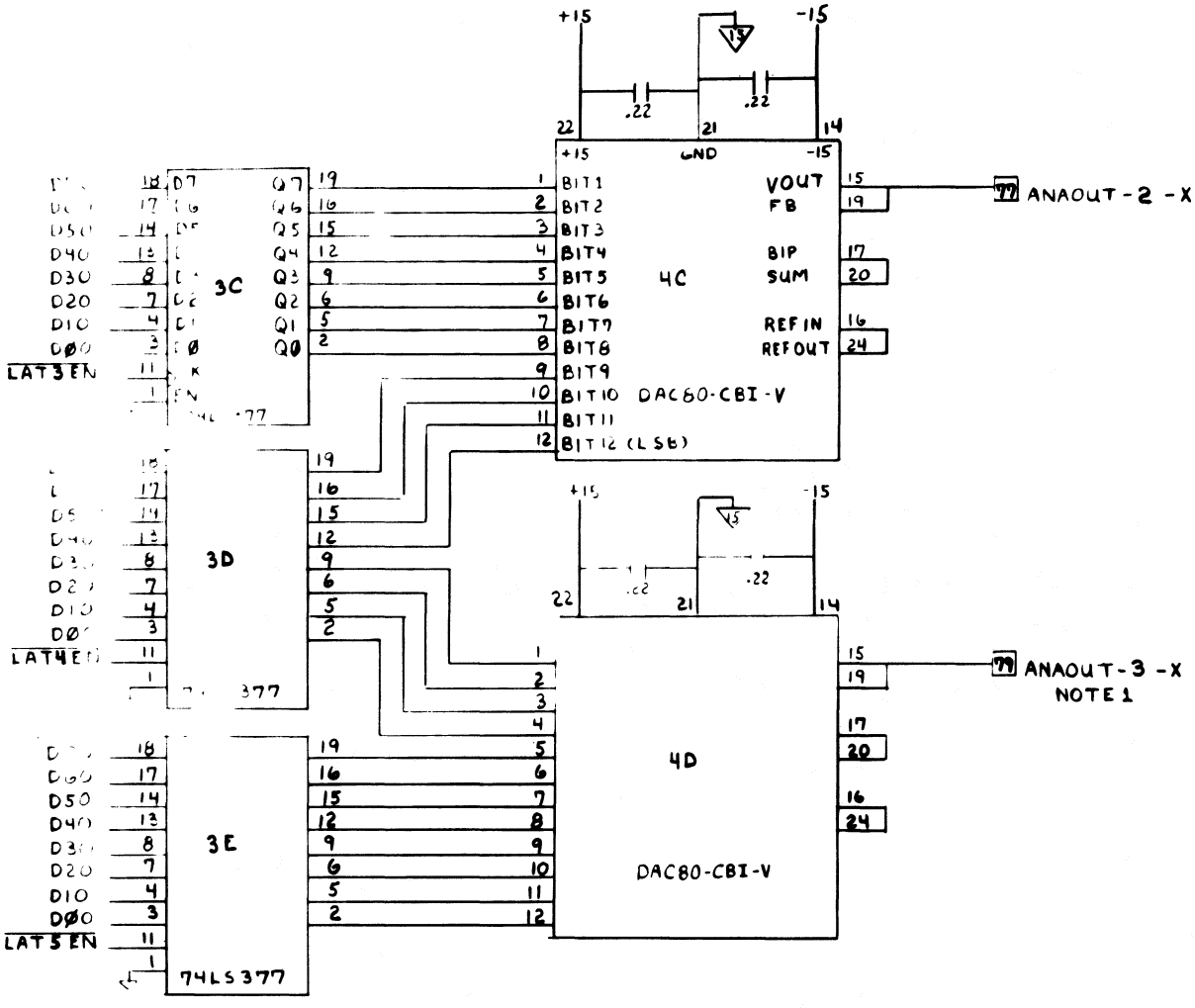


FIGURE 31

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DRAWN BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 3 OF 8

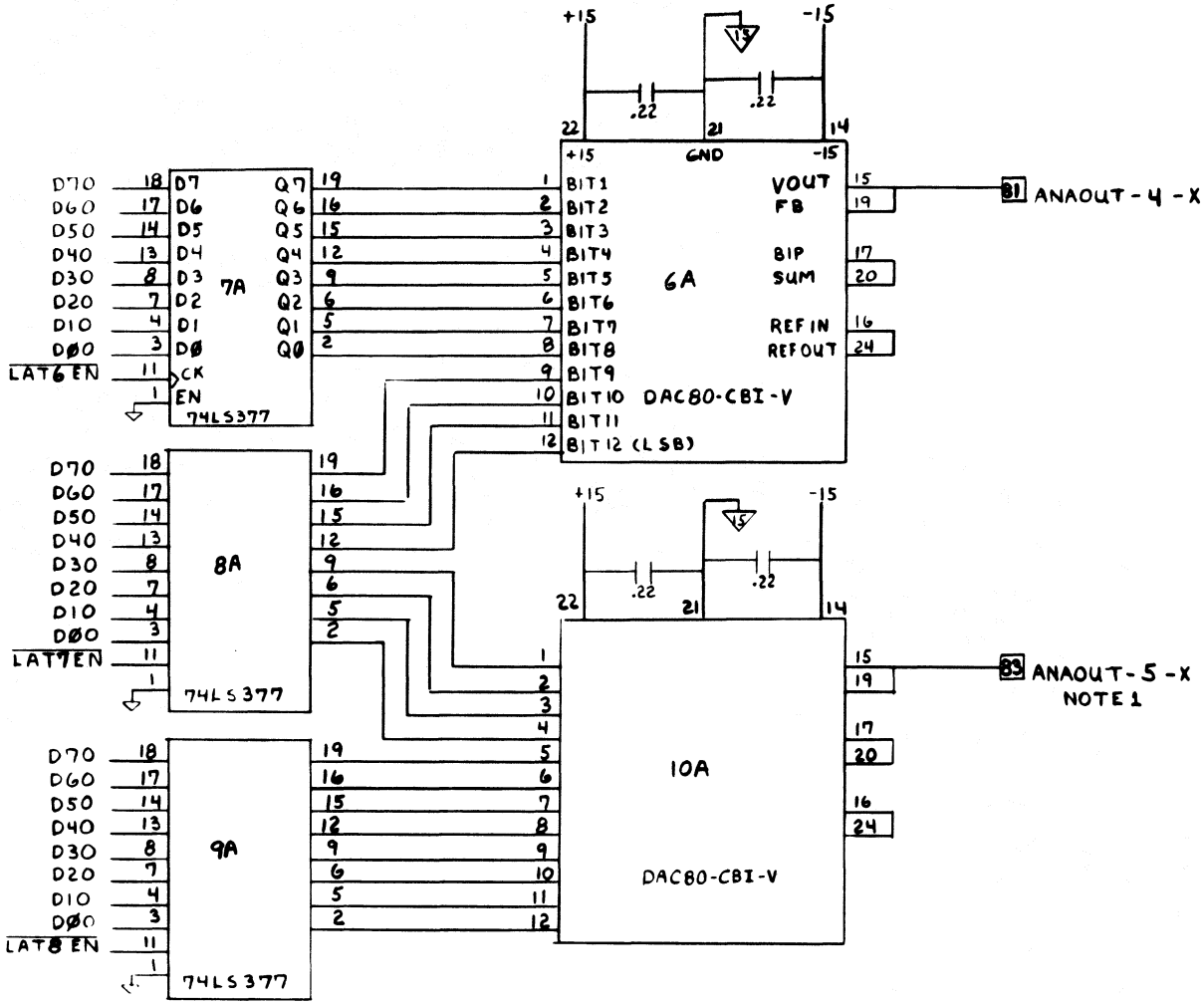


FIGURE 32

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 4 OF 8

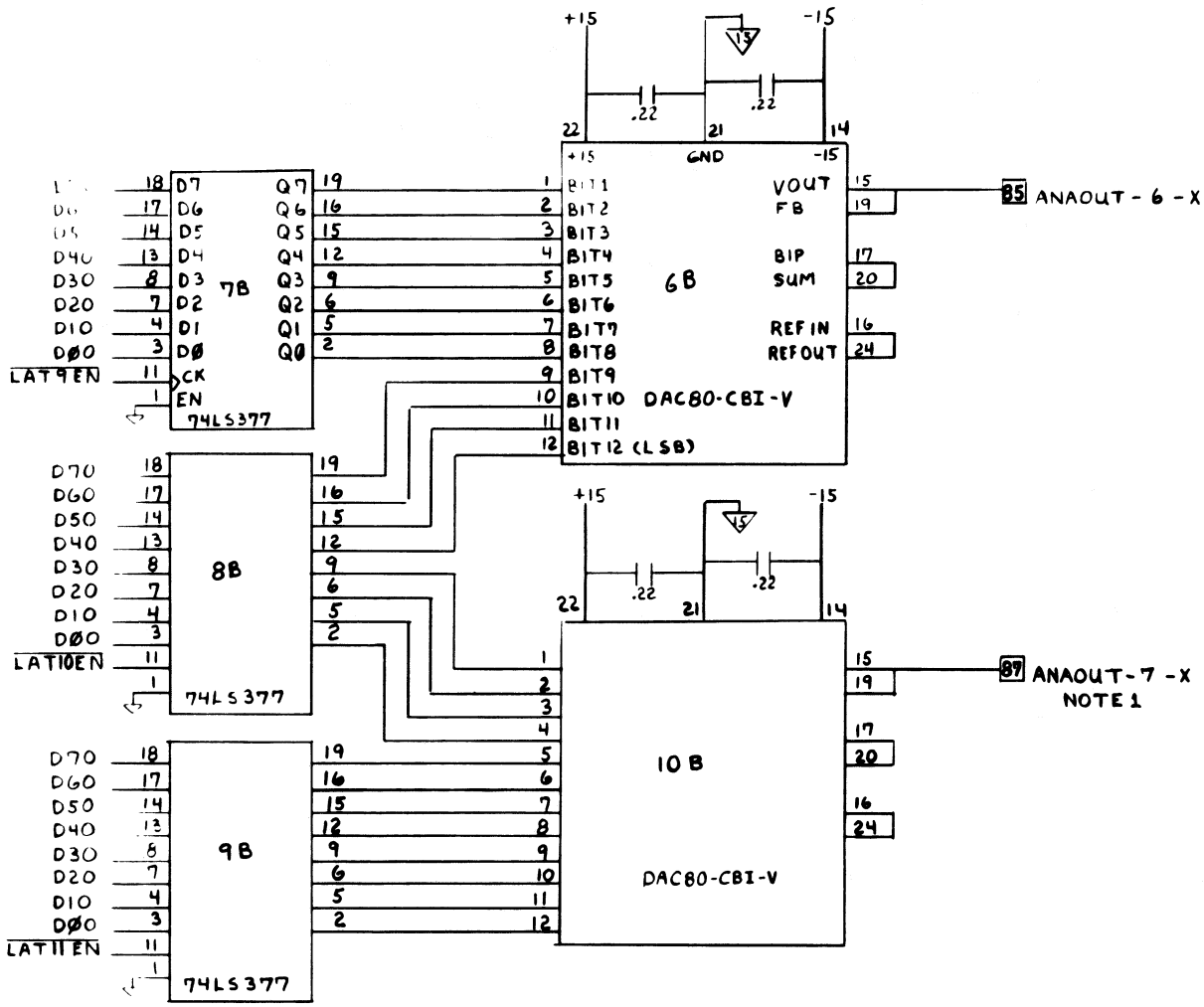


FIGURE 33

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 5 OF 8

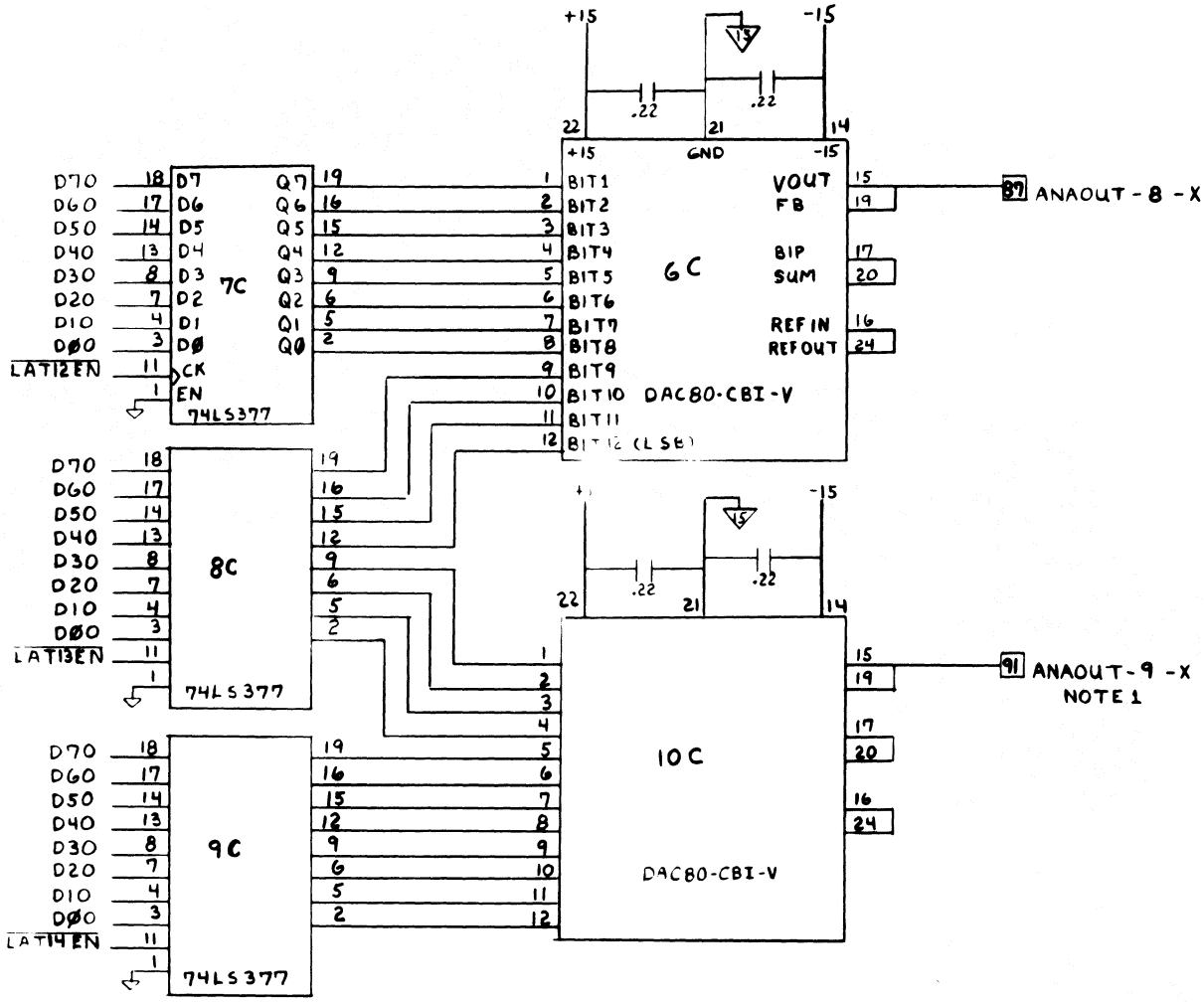


FIGURE 34

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 6 OF 8

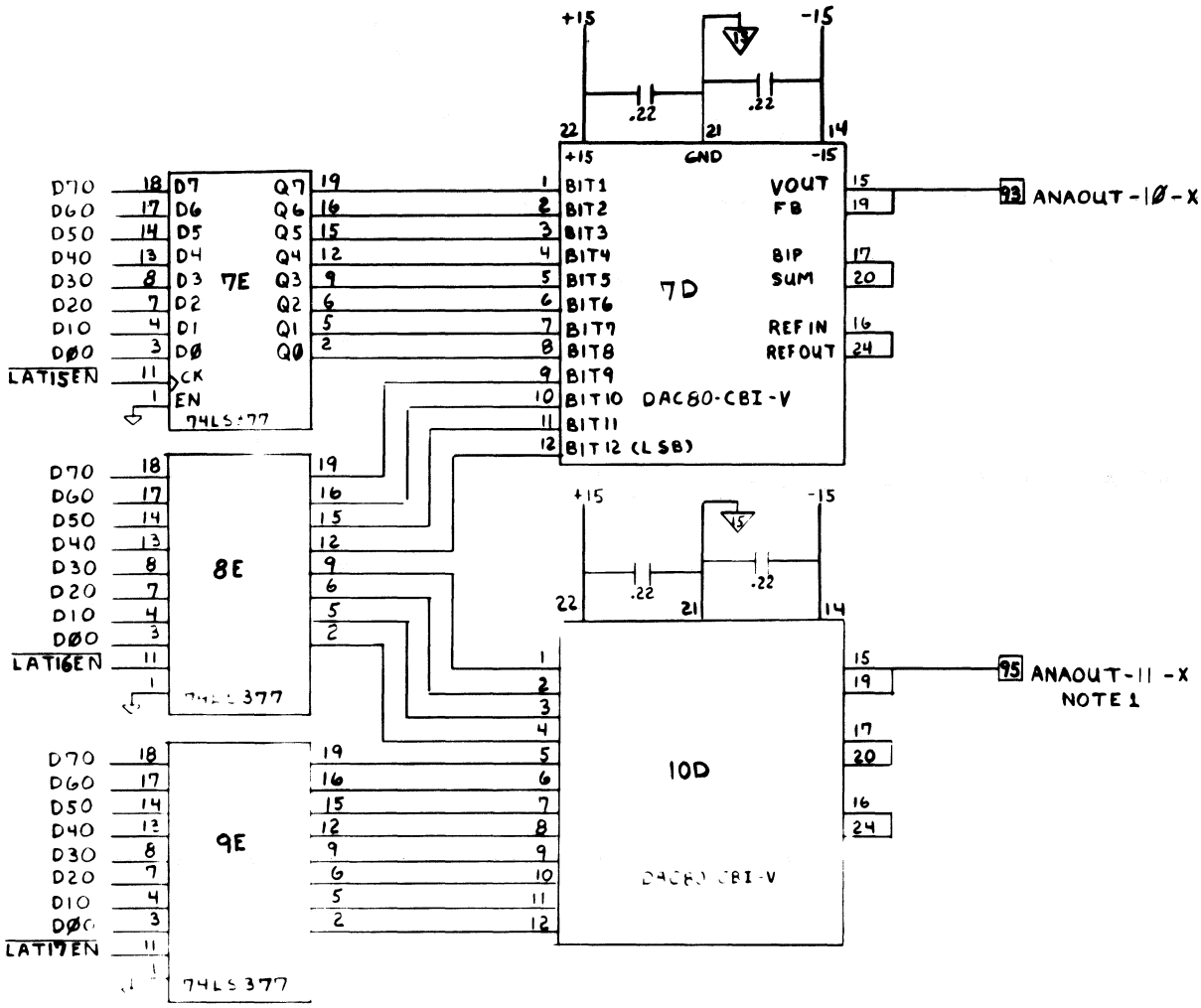


FIGURE 35

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-16-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 7 OF 8

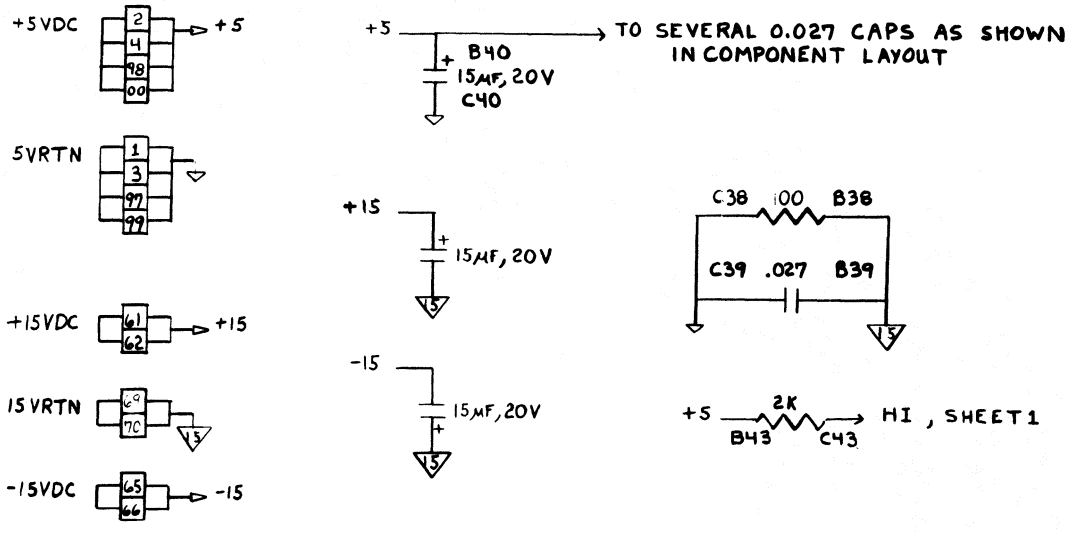


FIGURE 36

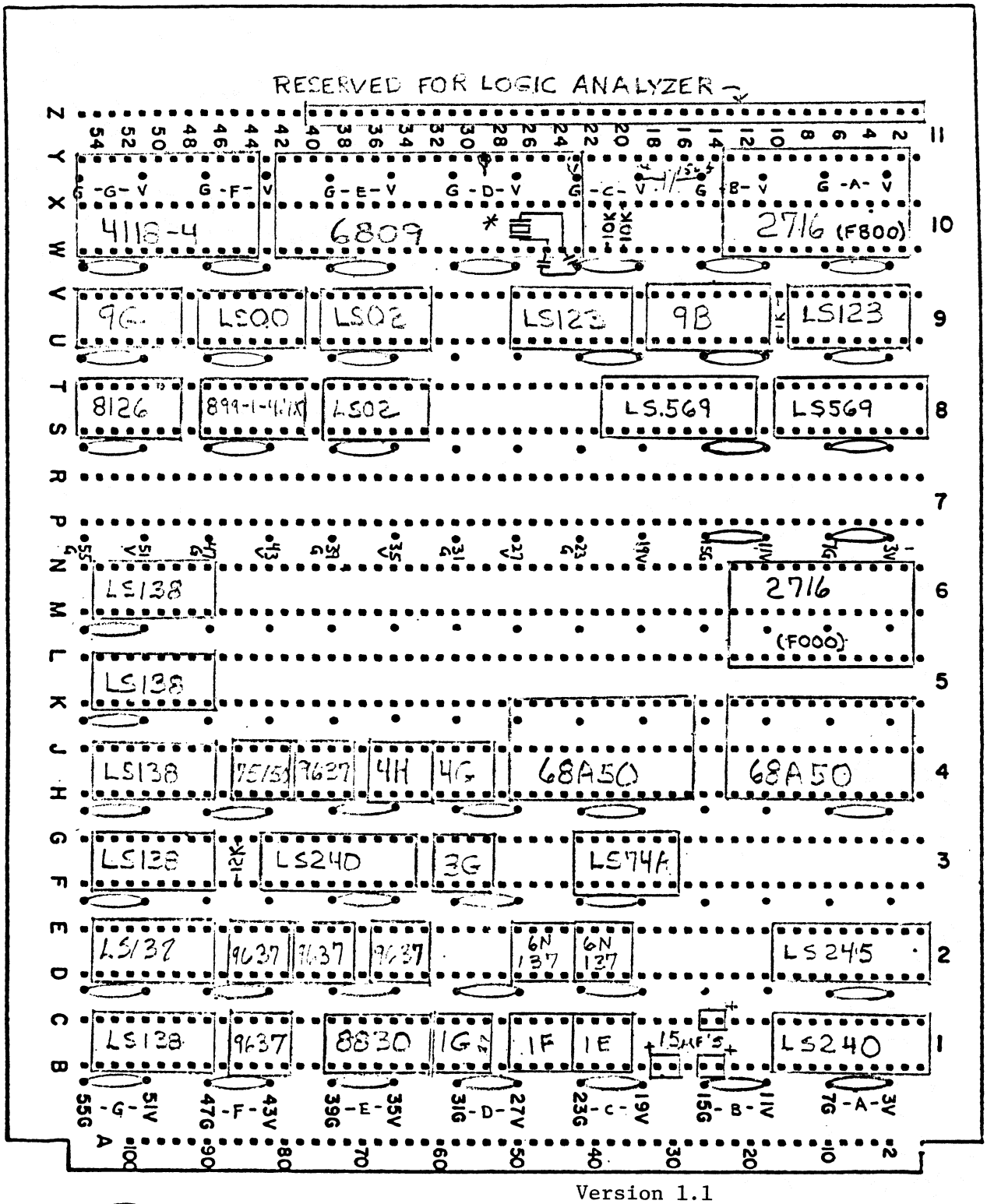
NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: FRONT END DATA LINK, OUTPUT BOARD	
DSGN. BY: LACASSE	DATE: 6-22-82
APPD. BY:	DR. BY:
DWG. NO.	SHEET 8 OF 8

APPENDIX A

Board Layouts

Parts Lists

ROM Listings



Version 1.1

Note: ⬭ = .027 µF Cap

SUPPLY REQ. (TYP.)

+5	690 mA
+15	8 mA
-15	7 mA

* 4 MHz crystal and 24 PF caps wrapped.
⬭ => solder clip to VCC plane; ⬭ => to gnd.

FRONT-END DATA LINK
MICROPROCESSOR BOARD
COMPONENT LAYOUT

Sheet 1 of 2 7-23-82

9B

15	µF +
30.1	KΩ
10	KΩ
0.1	µF
51	KΩ
0.22	µF
200	KΩ
0.47	µF

1E & 1F

66.5	Ω
.01	µF
.01	µF
66.5	Ω

1G

16.2	Ω
16.2	Ω
16.2	Ω
16.2	Ω

9G

(1200 Baud)

3G

100Ω,	1%
100Ω,	1%
.01	µF
360	Ω

4G

.47	µF
1N4372A	
.01	µF
10	Ω

4H

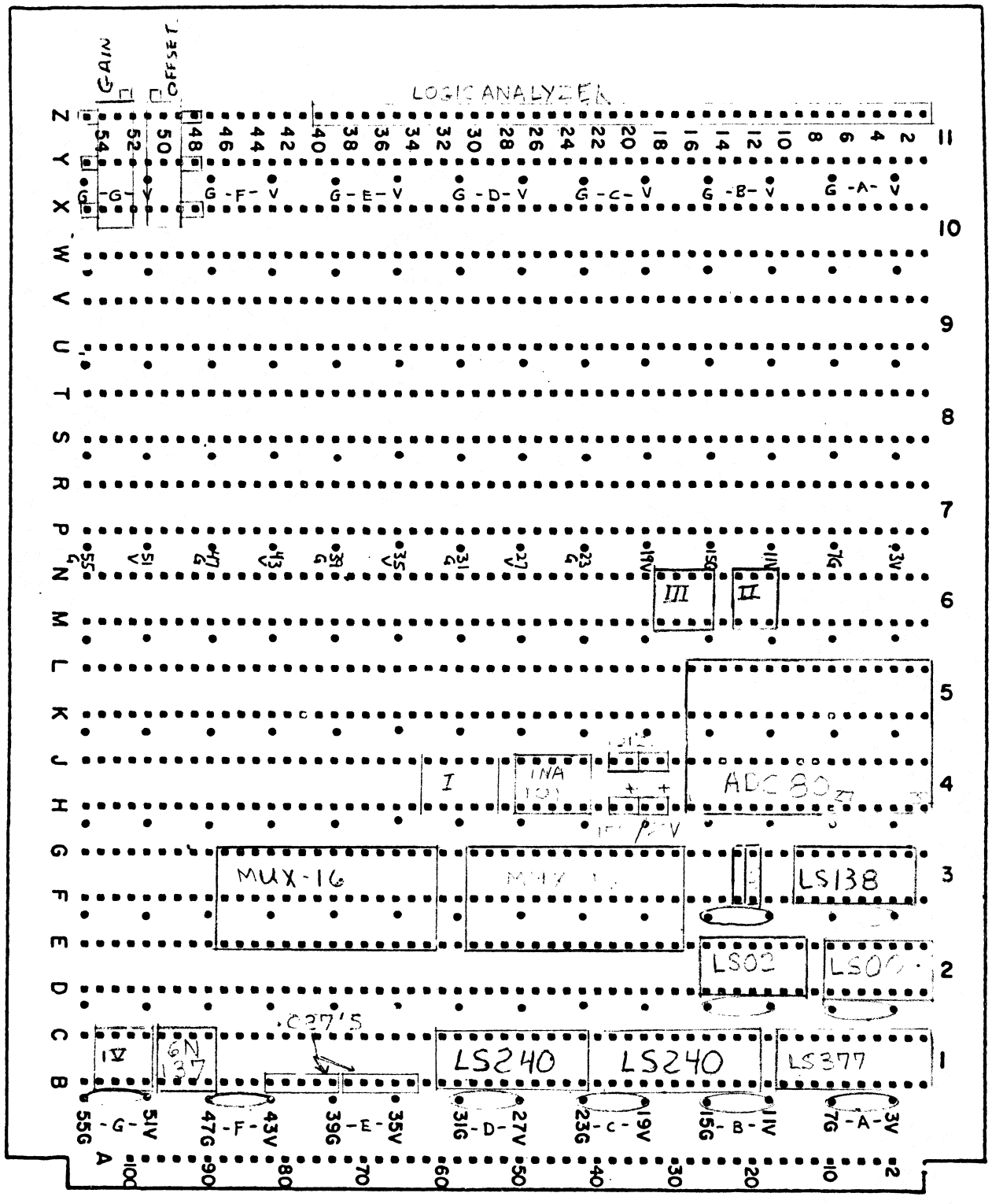
.47	µF
1N4372A	
.01	µF
10	Ω

NOTES:

1. Make up 1E and 1F on one 16-pin component carrier.
2. 1G, 4G, 4H, and 9B components can be plugged directly into the board, without component carriers.
3. 3G and 9G require component carriers.

FRONT-END DATA LINK
MICROPROCESSOR BOARD
COMPONENT LAYOUT

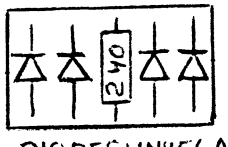
Sheet 2 of 2 7-23-82



V 2.0

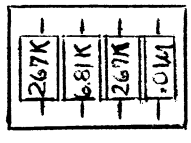
⬭ = .027μF

I =



DIODES: IN456A

III =



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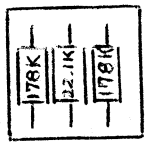

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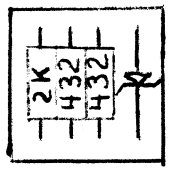
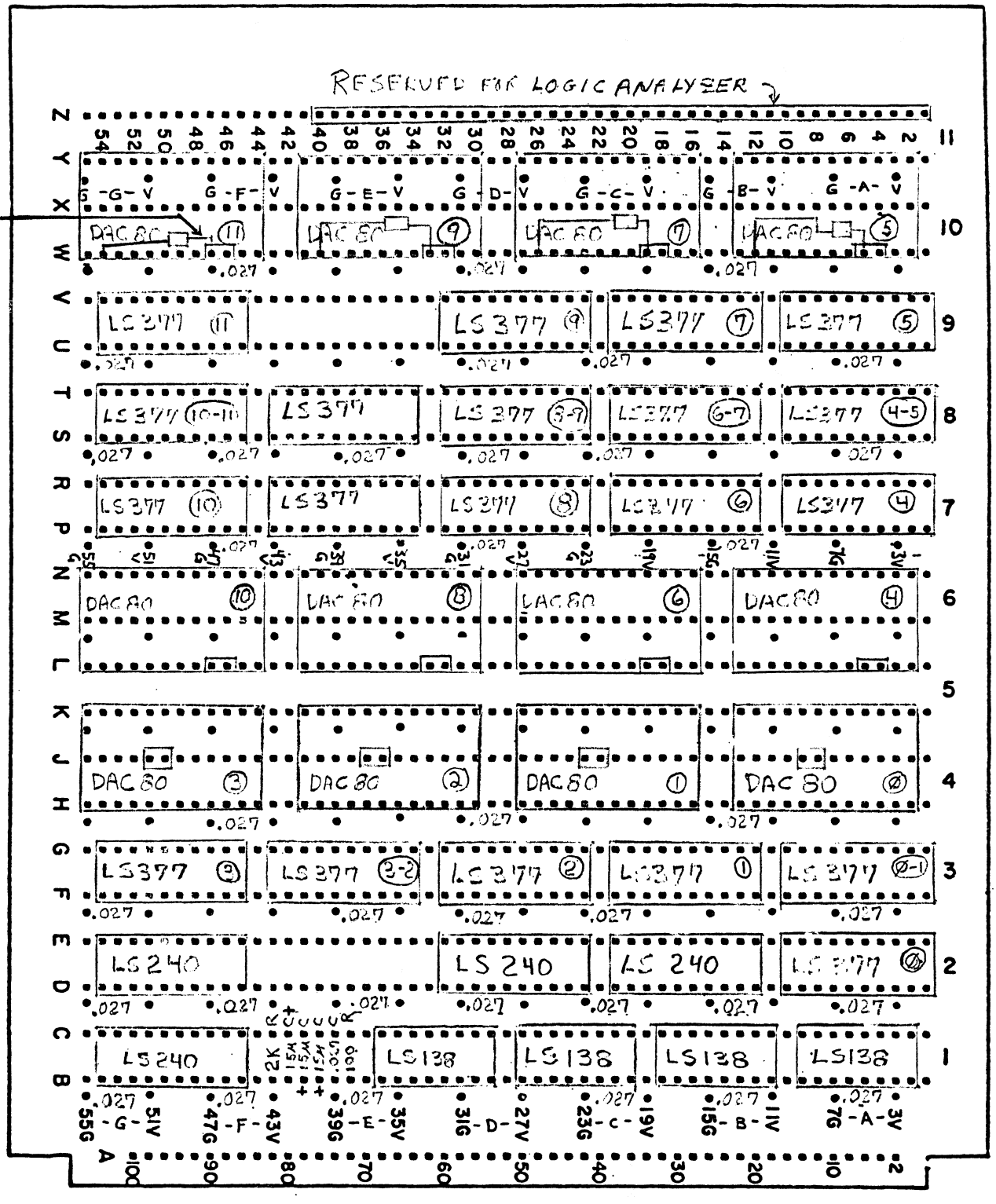


IN4747A

FEDAL ANALOG IN

9-15-82



ANALOG OUTPUT V 1.3

Note: Cut off pin 23 on all DAC's.

Note: The small circled numbers in the LS 377's and DAC80's indicate that latch x 's outputs feed DAC x 's inputs.

Current Consumption: +15, 258 mA; -15, 141 mA; +5, 448 mA.

FEDAL-MP PARTS LIST

Part No.	Manufacturer and Description	Qty.
196D156X9020KA1	Sprague capacitor, tantalum, 15 µF, 20 V	5
0.47 µF	Various, Decoupling capacitor	2
0.22 µF	Various, Capacitor, ceramic	2
0.027 µF	? (Runion), Decoupling Capacitor	45
0.01 µF	Various, Capacitor, ceramic	8
24 PF	Various, Capacitor, Ceramic	2
10 Ω, 1/8 W, 5%	Various, Resistor	2
16.2 Ω, RN55C	Various, Resistor	4
66.5 Ω, RN55C	Various, Resistor	4
100 Ω, RN55C	Various, Resistor	2
360 Ω, 1/4 W, 5%	Various, Resistor	1
1 KΩ, 1/8 W, 5%	Various, Resistor	1
10 KΩ, 1/8 W, 5%	Various, Resistor	3
12 KΩ, 1/8 W, 5%	Various, Resistor	1
51 KΩ, 1/8 W, 5%	Various, Resistor	1
30.1 K, RN55C	Various, Resistor	1
200 K, RN55C	Various, Resistor	1
MV50	Monsanto, LED	2
1N4372A	Various, 3V Zener	2
MP04A	CTS Knight, 4.00 MHz Crystal	1
MP050	CTS Knight, 5.0688 MHz Crystal	1
2716	Various, 2K x 8 ROM	2
MK 4801AN-4-4118A	Mostek, 1K x 8 RAM	1
6N137	Hewlett-Packard, Opto Isolator	2
MC6809P	Motorola, Microprocessor	1
MC68A50P	Motorola, A.C.I.A. (UART)	2
74LS00N	Various, 2-NAND	1
74LS02N	Various, 2-NOR	2
74LS74AN	Various, Flip-Flop	1
74LS123N	Various, 1-Shot	2
74LS138N	Various, Decoder	6
74LS240N	Various, Buffer	2
74LS245N	Various, Buffer	1
74LS569N	Various, Tri-State Counter	2
75150N	Various, RS232 Line Driver	1
COM8126	Standard Microsystems, Baud Rate Gen.	1
DS8830N	National, Line Driver	1
899-1-1.0K	Beckman, 13 Resistor D/P	1
9637ATC	Various, RS232 Receiver	5
X8136-UG268	Augat, Wire Wrap Card	1
FEDAL-MP	Contact Systems Wiring	1

FEDAL-IN PARTS LIST

Part No.	Manufacturer and Description	Qty/Card
X8136-UG268	Augat, Wire Wrap Card	1
FEDAL-IN	Wiring by Contact Systems	1
74LS377	Various, Latch	1
74LS240	Various, 3-State Buffers	2
6N137	HP, Opto Isolator	1
74LS00	Various, 2-NAND	1
74LS02	Various, 2-NOR	1
74LS138	Various, Decoder	1
MUX-16	PMI, 16 Input MUX	2
ADC-80	Burr Brown, 12-bit ADC	1
INA 101	Burr Brown, Instr. Amplifier	1
0.027 µF	? (Runion), Decoupling	12
1N 4747A	Various, 20 V Zener	1
432 Ω, RN55C	Various, Resistor	2
2 K , 5%, 1/8 W	Various, Resistor	1
0.47 µF	Various, Decoupling Capacitor	1
100 Ω, 5%, 1/8 W	Various, Resistor	1
15 µF, 20 V	Sprague, Capacitor 196D156X9020KA1	2
1N 456A	Various, Low Leakage Diodes	4
240 Ω, 5%, 1/8 W	Various, Resistor	1
0.01 µF, 50 V	Various, Cap, 0.1" Spacing	3
	Assorted Component Carriers	
178 KΩ, RN55C	Various, Resistor	2
22.1 KΩ "	" "	1
267 KΩ "	" "	2
6.81 KΩ "	" "	1
20 KΩ Pot	Amphenol 6034P-203-75N or equivalent	2

FEDAL-OUT PARTS LIST*

Part No.	Manufacturer and Description	Qty.
X8136-UG268	Augat, Wire Wrap Card	1
100 Ω, 5%, 1/8 W	Various, Resistor	1
2 KΩ, 5%, 1/8 W	Various, Resistor	1
0.027 µF, 50 V	Various, Ceramic Decoupling Capacitor	35
0.22 µF, 50 V	Various, Ceramic Decoupling Capacitors	16
15 µF, 25 V	Sprague, 196D156X902KA1	3
74LS138N	Various, Decoder IC	4
74LS240N	Various, Driver IC	4
74LS377N	Various, Latch IC	20
HS DAC-80-CBI-V	Hybrid Systems, 12 Bit DAC	12
FEDAL-OUT	Contact Systems, Wiring	1

* Note: This list is for one card; a complete chassis requires three cards.

FEDAL CHASSIS PARTS LIST

Part No.	Manufacturer and Description	Qty.
00-8016-56-000-701	Elco, 56 Pin, Exposed Pin Connector	1
00-8016-56-000-707	Elco, 56 Pin, Protected Pin Connector	4
31-10	Amphenol, Insulated BNC Connector	2
36A-3	Velonex, Digital Panel Meter	1
4800X	Pamotor, 9W Fan	1
50-12A-30	TRW, Edge Connector	4
50-30C-10	TRW, Edge Connector	1
50-282012NAND	General Electric, Analog Panel Meter	1
5082-7340	HP, LED Display IC	4
5B4	Corcom, AC Line Filter	1
BB15-1.5	Condor, ± 15 V Supply	1
C5-6/OVP	Condor, +5 V Supply	1
DB-25S	TRW, 25 Pin Female Connector	1
OVP-12	Condor, OVP for ± 15 V Supply	1
T11-1-5.00A	Airpax, Circuit Breaker	1
T3	CTS, 3-Pole, 3-Position, Rotary Switch Wafer	1
T75-52M-2	Cherry, Digi-Switches	2
V130LA20A	General Electric, Surge Protection	1
---	NRAO, FEDAL Chassis	1
---	Various, NRAO Standard Digital Chassis' components, including card guides, five 100-pin wirewrap connectors and bus materials.	

```
0000 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0010 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0020 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0030 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0040 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0050 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0060 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0070 0F FE 00 01 0F FE 00 01 0F FE 00 01 0F FE 00 01
0080 8A A5 D1 3F 3F 3F 3F 3F FF FF FF FF FF FF 3F 3F
0090 10 8E 00 10 4F D6 15 58 58 C3 F8 00 1F 01 96 15
00A0 84 07 4C 5F 1A 01 56 4A 26 FC 43 A1 84 27 0A 11
00B0 A3 81 2E 10 11 A3 84 2D 0B 96 15 44 44 44 53 E4
00C0 A6 E7 A6 39 96 15 44 44 44 EA A6 E7 A6 39 3F 3F
00D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
00E0 B7 48 01 86 FB 94 17 97 17 CE 00 03 33 5F 11 83
00F0 00 00 2F 0A FC 48 02 2C F3 84 0F 1F 03 39 86 04
0100 9A 17 97 17 8A 80 39 3F 3F 3F 3F 3F 3F 3F 3F 3F
0110 F9 2C F9 34 F9 49 F9 55 F9 5A F9 C8 F9 DA F9 E5
0120 FA 10 1A 50 96 1B 48 8E F9 10 6E 96 8E F9 18 96
0130 1D 48 6E 96 B6 18 01 81 7E 26 09 0A 1B 86 02 97
0140 1D 7E FA 37 0C 1B 7E FA 37 B6 18 01 81 7E 26 02
0150 0A 1B 7E FA 37 0A 1B 7E FA 37 B6 18 01 0D 1F 27
0160 19 D6 DF 8E 00 20 0D C1 27 03 8E 00 70 A7 85 0C
0170 DF 0A 1F 9B C3 97 C3 7E FA 37 91 C3 27 1C 86 02
0180 91 C5 2E 0D 86 03 97 1B 86 01 9A 17 97 17 7E FA
0190 37 0C C5 86 04 97 1D 7E FA 37 86 04 97 1D 0F C5
01A0 96 17 84 FE 97 17 0D C1 27 0F 0F C1 0D CD 26 06
01B0 8E 00 70 BD FD F0 7E FA 37 0C C1 0D CD 26 06 8E
01C0 00 20 BD FD F0 7E FA 37 B6 18 01 4A 97 1F 4C 9B
01D0 C3 97 C3 0A 1D 0F DF 7E FA 37 B6 18 01 97 C9 0A
01E0 1D 97 C3 20 52 B6 18 01 81 7E 26 0A 0A 1D 0D CD
01F0 26 02 0F CD 20 41 0C D3 86 02 91 CD 2F 06 0C CD
0200 0A 1D 20 33 86 02 97 1B 86 01 9A 17 97 17 20 27
0210 B6 18 01 81 7E 26 06 0F CD 0A 1D 20 1A 0C CD 0C
0220 D3 86 02 91 CD 2F 06 0C CD 0A 1D 20 0A 86 02 97
0230 1B 86 01 9A 17 97 17 1C AF 3B 3F 3F 3F 3F 3F 3F
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02C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
02D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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02F0 15 44 44 44 EA 86 E7 86 39 3F 3F 3F 3F 3F 3F 3F
0300 8E 00 0A C6 02 F5 18 00 26 0B 30 1F 26 F7 C6 08
0310 DA 17 D7 17 39 B7 18 01 C6 F7 D4 17 D7 17 39 3F
0320 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0330 86 7E BD FB 00 BD FB 00 39 3F 3F 3F 3F 3F 3F 3F
0340 10 8E B0 00 A6 A0 BD FB 00 9B D1 97 D1 10 8C B0
0350 03 2F F1 39 3F 3F 3F 3F 10 8E 00 10 A6 A0 BD FB
0360 00 9B D1 97 D1 10 8C 00 13 2F F1 96 D3 BD FB 00
0370 9B D1 97 D1 B6 30 00 BD FB 00 9B D1 BD FB 00 39
0380 3F 3F 3F 3F 3F 3F 3F 3F BD F1 70 C6 03 46 84 0F
0390 24 0E 3D 5C EC AB 58 49 58 49 58 49 58 49 20 05
03A0 3D EC AB C4 F0 DD CF 30 89 08 00 BD F1 70 C6 03
03B0 46 84 0F 24 08 3D 5C EC AB 84 0F 20 0B 3D EC AB
03C0 44 56 44 56 44 56 44 56 9A D0 39 3F 3F 3F 3F 3F
03D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03F0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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04B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
04C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
04D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
04E0 86 03 B4 B8 00 27 38 44 27 1B B6 30 00 B7 68 00
04F0 0D D7 27 3B 8E 00 59 0D C1 26 03 8E 00 A9 A6 84
0500 B7 70 00 20 34 96 D3 B7 68 00 0D D7 27 21 8E 00
0510 58 0D C1 26 03 8E 00 A8 A6 84 B7 70 00 20 1A 96
0520 17 B7 68 00 0D D7 27 07 96 C9 B7 70 00 20 0A 86
0530 03 9A D5 97 D5 B7 60 12 39 86 FD 94 D5 97 D5 B7
0540 60 12 10 8E 00 20 0D C1 26 04 10 8E 00 70 10 9F
0550 CF 8E 80 00 BD F1 70 1F 89 44 44 44 8B 34 31 A6
0560 C4 07 5C 4F 1A 01 46 5A 26 FC A5 A4 27 06 86 FE
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0620 58 12 0F D9 39 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0630 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0640 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0650 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0660 B7 10 00 0D D9 27 05 2D 48 0C D9 39 0D DB 27 29
0670 4F 4C 97 E3 97 E4 0D E2 26 09 4F 97 DB B7 20 00
0680 0C D9 39 0D E1 26 09 86 10 9A 17 97 17 0C D9 39
0690 86 EF 94 17 97 17 0C D9 39 4F 4C 97 E1 97 E2 0D
06A0 E4 26 08 B7 20 00 97 DB 0C D9 39 0D E3 26 E1 20
06B0 D6 0D DB 27 3A 0D E2 26 0A 4F 97 DB B7 20 00 4C
06C0 97 D9 39 0D E1 26 19 4F 97 DB B7 20 00 97 E1 97
06D0 E2 97 E3 97 E4 86 01 97 D9 86 11 9A 17 97 17 39
06E0 4F 97 DB B7 20 00 97 D9 97 E3 4C 97 E4 20 98 0D
06F0 E4 26 0A 4F 4C 97 DB B7 20 00 97 D9 39 0D E3 26
0700 0A 4F 4C 97 DB B7 20 00 4F 20 C2 4F 97 D9 97 E1
0710 4C 97 E2 97 DB B7 20 00 16 FF 6C 3F 3F 3F 3F 3F
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07C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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```

Table A-1: 10A, V1.0-RJL ROM Listing

```
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0010 FF AE A4 27 15 86 06 EF 81 E7 80 4A 26 F9 31 22
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0030 22 EE A4 27 09 EC 81 ED C8 12 31 22 20 F3 CC AA
0040 AA 8E 00 00 10 8E 04 00 ED 84 10 A3 81 26 0E 31
0050 3E 26 F5 10 83 55 55 27 0A 44 54 20 E4 86 20 97
0060 17 20 03 4F 97 17 FC F7 FE F3 F8 81 DD CF 10 8E
0070 10 00 8E F0 00 4F 5F EB 80 24 01 4C 31 3F 26 F7
0080 10 93 CF 27 06 86 40 9A 17 97 17 4F B7 48 00 86
0090 60 B4 48 02 81 40 26 0E 4F 43 B7 48 00 86 60 B4
00A0 48 02 81 20 27 06 86 04 9A 17 97 17 8E 06 00 86
00B0 15 B7 28 00 B7 18 00 C6 02 86 3E B7 28 01 F5 28
00C0 00 26 09 F5 28 00 26 0A 30 1F 26 F7 86 80 9A 17
00D0 97 17 8E 00 03 86 3E B7 18 01 F5 18 00 26 09 F5
00E0 18 00 26 0A 30 1F 26 F7 86 08 9A 17 97 17 96 17
00F0 1F 03 4F 5F 8E 00 00 10 8E 04 00 ED 81 31 3E 26
0100 FA 86 01 97 D9 86 02 97 1B 1F 30 97 17 4F B7 20
0110 00 86 17 B7 18 00 B7 28 00 86 01 9A 17 97 17 86
0120 95 B7 18 00 86 95 B7 28 00 1C AF 10 CE 03 FF 7E
0130 F1 40 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0140 BD FE 60 BD FB 30 BD F5 00 BD FB 40 BD FB 58 BD
0150 FC E0 20 EC 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0160 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0170 A6 84 43 81 31 22 11 1F 89 84 0F 54 54 54 54 26
0180 01 39 8B 0A 5A 26 FB 39 86 1F 39 3F 3F 3F 3F 3F
0190 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01A0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
01F0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0200 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0210 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0220 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0230 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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0250 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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0280 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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02A0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
02B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
02C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
02D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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0310 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0320 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0330 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0340 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0350 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0360 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0370 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0380 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
0390 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03A0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
03F0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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0520 2D 0C 4F 4C B7 48 00 BD F8 90 0C 15 20 11 4F 4C
0530 B7 48 00 BD FA E0 0C 15 8E 00 02 30 1F 26 FC 1F
0540 30 58 49 58 49 58 49 58 49 D7 CF BD FB 00 9B D1
0550 97 D1 BD F8 E0 2D 0D 96 15 4C B7 48 00 BD F8 90
0560 0C 15 20 0B 96 15 4C B7 48 00 BD FA E0 0C 15 1F
0570 30 9A CF BD FB 00 9B D1 97 D1 1F 30 1F 98 BD FB
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0590 81 1F 2F 01 39 BD F8 90 0C 15 7E F5 3F 96 15 4C
05A0 B7 48 00 81 1F 2F 01 39 BD FA E0 0C 15 7E F5 3B
05B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
05C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
05D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
05E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
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07B0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07C0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07D0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07E0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F
07F0 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 3F 98 47 21
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Table A-2: 6A, V1.0-RJL ROM Listing

APPENDIX B

Typical User Configuration

1.0 Analog Input

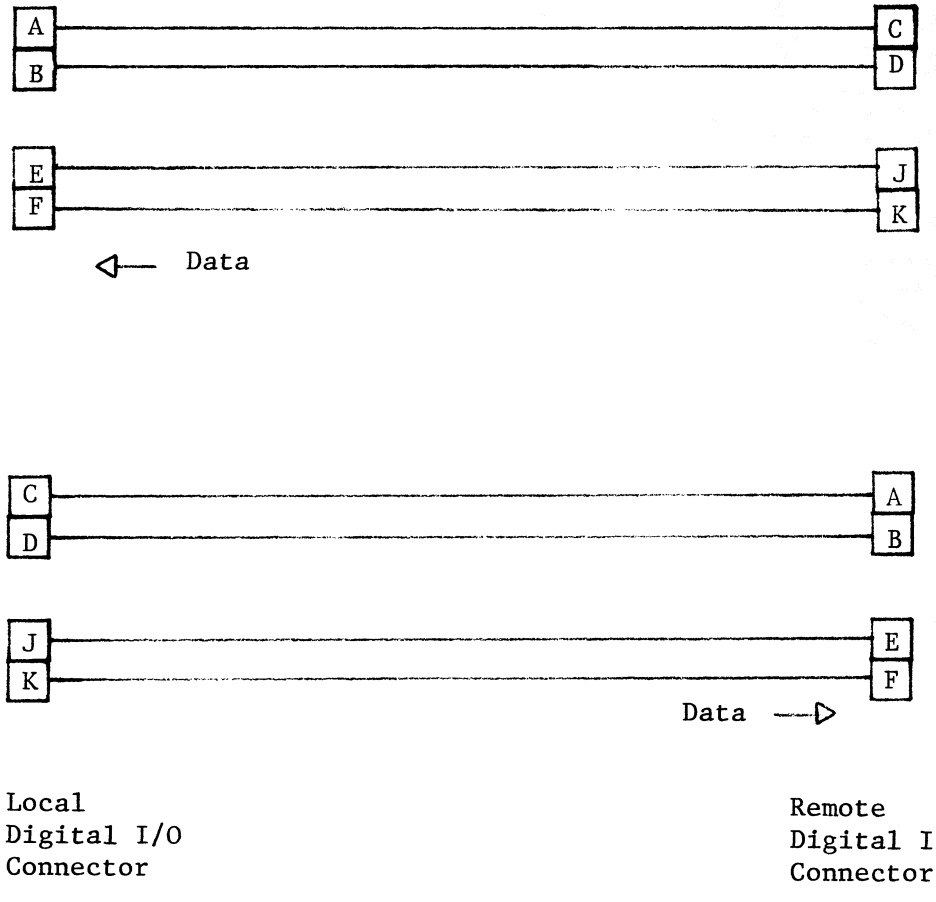
The user supplies 32 analog inputs to the ANALOG INPUT CONNECTOR. PSEUDO-GROUND should be connected to the analog signals' reference point. Pin-outs are shown in Table 1. Maximum input range is ± 10 V with respect to pseudo-ground.

2.0 Digital Input

Digital inputs are multiplexed into the controller and so must be configured as some combination of Figures 5 and 6.

3.0 Data Link

For maximum reliability, use redundant twisted pairs connected as shown below.



APPENDIX B (continued):

4.0 Analog Output

Analog outputs can conveniently be brought out from the two ANALOG OUTPUT CONNECTORS as twisted pairs. See Tables 4 and 5. Signals that must be clean should be filtered at the user end of the twisted pairs; the emitted signals contain about 15 mV of digital hash. Signals requiring less accuracy can be brought out single ended and referenced to chassis ground.

5.0 Digital Outputs

Digital outputs are available on the Digital I/O connector as shown in Table 3. The emitted signals have a 12 mA capability at logic high ($\geq$ 2.4 V) and a 24 mA capability at logic low ($\leq$ 0.4 V). The digital outputs are referenced to the chassis.

6.0 Miscellaneous Connections

6.1 Chassis ground.

The FEDAL chassis is grounded to AC ground via the AC cord. However, in some cases it may be helpful to attach a ground strap to the chassis, providing a better return path for the digital currents.

6.2 Analog monitors.

See Figure 8.

6.3 Digital output/limit bit select.

See Figure 7.