

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VIRGINIA

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LOW NOISE, 15 GHz, COOLED, GaAsFET AMPLIFIER

S. WEINREB

R. HARRIS

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LOW NOISE, 15 GHz, COOLED, GaAsFET AMPLIFIER

S. Weinreb and R. Harris

I. Introduction

This report describes the testing and construction of 60 amplifiers for the VLA with the following specifications at a physical temperature of 15K:

<u>FREQUENCY GHz</u>	<u>NOISE (including isolator)</u>	<u>GAIN (including 5 to 10 dB pad)</u>
15.1	< 57K	19 <u>+</u> 1 dB
15.4	< 66K	19 <u>+</u> 3 dB
14.4	< 106K	19 <u>+</u> 3 dB

The amplifier is incorporated with an input isolator, output attenuator (for matching), and a SMA to waveguide adaptor as shown in Figure 1. This configuration is designed to easily fit the existing VLA dewar and improve the system noise temperature from 300K to 100K.

Background information on the amplifier design is given in a paper [1] by Tomassetti, Weinreb and Wellington describing a similar 10.7 GHz amplifier and in a report [2] by Sierra describing noise parameter measurements and computer programs used for the amplifier design. The major characteristics of the design are as follows:

- 1) GaAs FET's in the 1.75 mm square package are used. Early experiments with chips gave similar results and it was believed that better reliability would be achieved with packaged devices.

- 2) A coaxial geometry with a round center conductor in a square groove as suggested by Tomassetti is used. The characteristic impedance of this

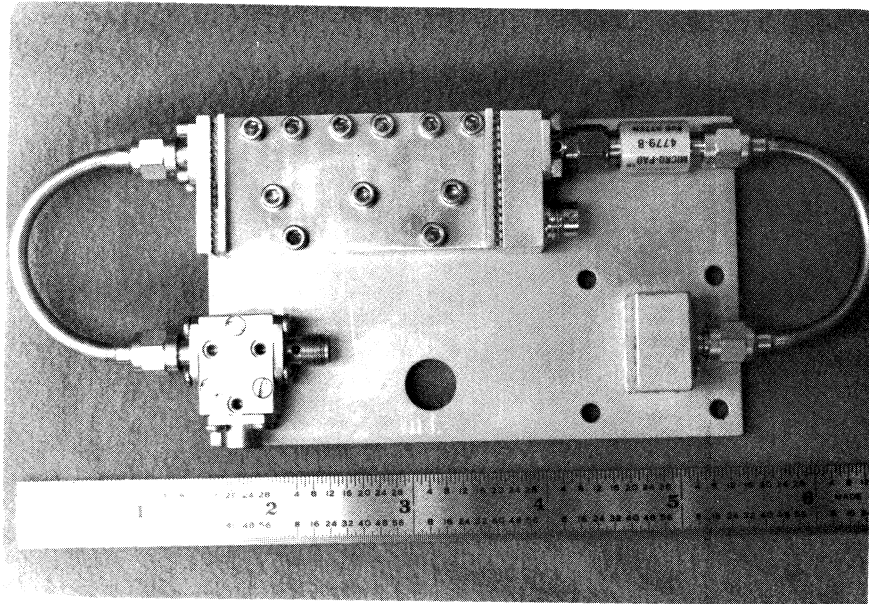


Fig. 1. Input isolator (lower left), amplifier, output 8 dB pad, and output coax-to-waveguide transition mounting plate. The isolator input connects via a short .141 coaxial cable to an input coax-to-waveguide transition which is part of a gapped waveguide thermal transition to 300K.

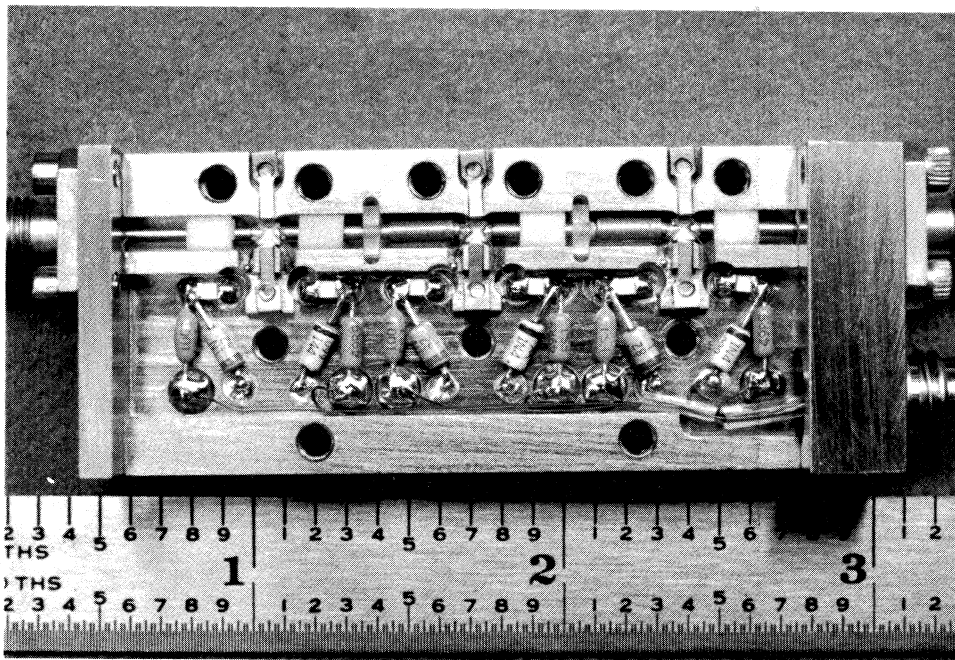


Fig. 2. Three-stage amplifier with cover removed. Input is at left and output and DC bias connector are at right.

geometry is given by Wheeler [3]. Tuning is accomplished by moving small $\lambda/4$ slugs on the center conductor and DC blocks are formed by enclosing the FET leads, cut to specified length, in Teflon tubing within a hollow center conductor. DC bias is provided by small wires, $\lambda/4$ long, soldered directly to the FET package. This configuration has been found to be reliable, mechanically stable, repeatable, and amenable to theoretical analysis.

3) The amplifier input and output return loss is reasonable (~ 10 dB) but an input isolator and output attenuator are used to provide > 20 dB return loss. The FET source lead inductance is kept to a minimum.

II. Construction

The chassis is milled from copper stock and plated with $1.2 \mu\text{m}$ of gold. A $7/64$ " carbide mill is useful for the rectangular slot. A thermostatically controlled hot plate, low power microscope, and a 60W, 700°F soldering iron with ~ 1 mm tip are needed for construction. The assembly procedure is as follows:

- 1) With chassis heated on a hot plate to 175 - 200°C , solder the input end plate to the chassis, all chip capacitors except the ATC111 0.8 pF gate bias bypass, and the ground wire posts utilizing Ersin SN62-.028 rosin filled, 2% silver solder. Clean chassis with flux remover and check all chip capacitor values with a capacitance meter.
- 2) Using the small soldering iron, solder chip resistors, bias resistors, and protection diodes with SN62 solder.
- 3) Using the hot plate again, but at a temperature of 100° - 120°C , solder the ATC111 0.8 pF gate bias bypass capacitors using Alpha 20E2 solder and Superior #30 flux.

4) Glue the rexolite support on interstage center conductors as shown in Figure 5 using Eastman 910 adhesive.

5) Trim the leads on the MGF1412-09 second-stage FET to 1.8 mm on both source leads and to the values given in Figure 3 for gate and drain leads. Solder #40 enameled-copper bias leads to the FET.

6) Install #22 Teflon tubing (OD = 0.94 mm, ID = 0.43 mm) in the center conductors cutting off the tubing 0.25 mm beyond the end of the center conductor. Install tuning slugs on center conductors checking for a firm, sliding fit.

7) Install second-stage FET together with both interstage networks into the chassis and fasten source lead champs.

8) Prepare MGF1412-10 third-stage FET as in paragraph 5), above, and install in chassis by bending the gate lead.

9) Using the hot plate at 200°C, solder the DC bias connector into the output end plate with SN62 solder. Solder #32 enameled copper bias wires to the connector pins using the small soldering iron and SN62 solder. Bolt the output end plate to the chassis and solder bias wires to chip capacitors.

10) Prepare and install the NE67383 first-stage FET as in paragraph 5), above.

11) Solder all FET bias wires using SN62 solder except the tie connection to the ATC111 gate bias bypass capacitor is made with 20E2 solder.

12) Install input and output SMA connectors complete with Teflon tubing and tuning slugs.

13) Apply a small amount of polystyrene cement to the FET lead to Teflon tubing interface points.

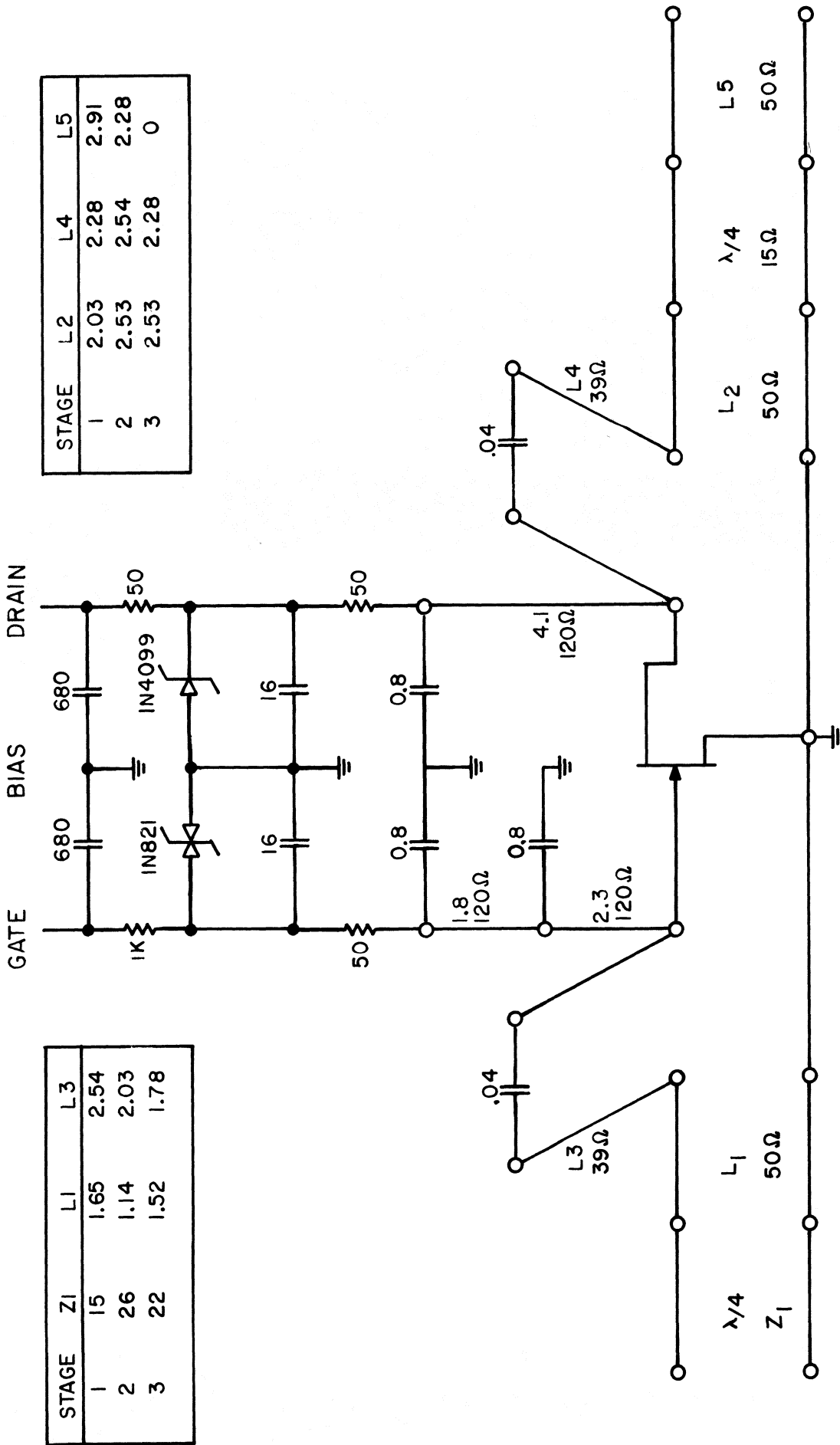


Fig. 3. Schematic of single amplifier stage with units of pF, ohms, and millimeters. All transmission lines are designated by their length (top) and characteristic impedance; propagation velocity is c except for .72c in 39Ω lines. The FET's are NE67383 in first stage, MGF1412-09 in second stage, and MGF1412-10 in third stage. Lengths L1 and L2 tune the amplifier center frequency and are changed by moving λ/4 transformer slugs.

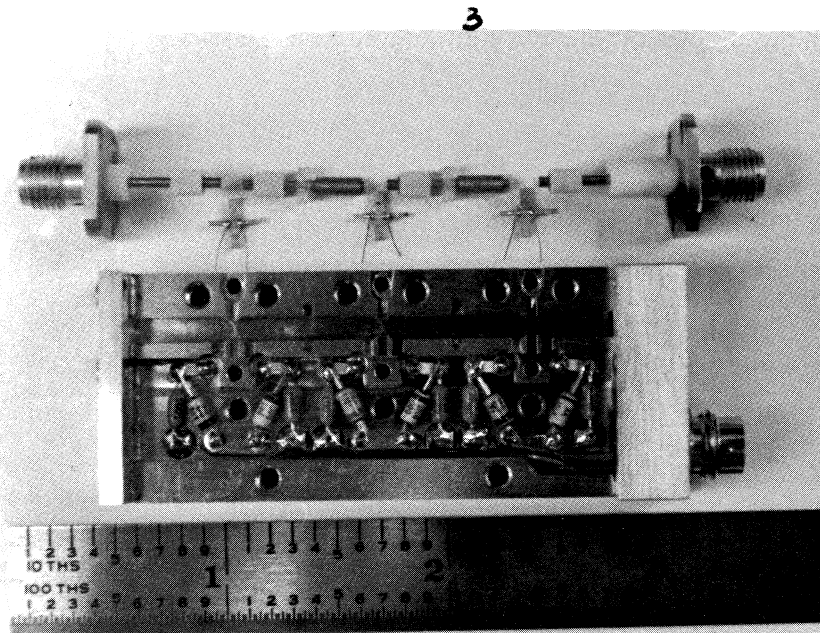


Fig. 4. Amplifier with coaxial components removed.

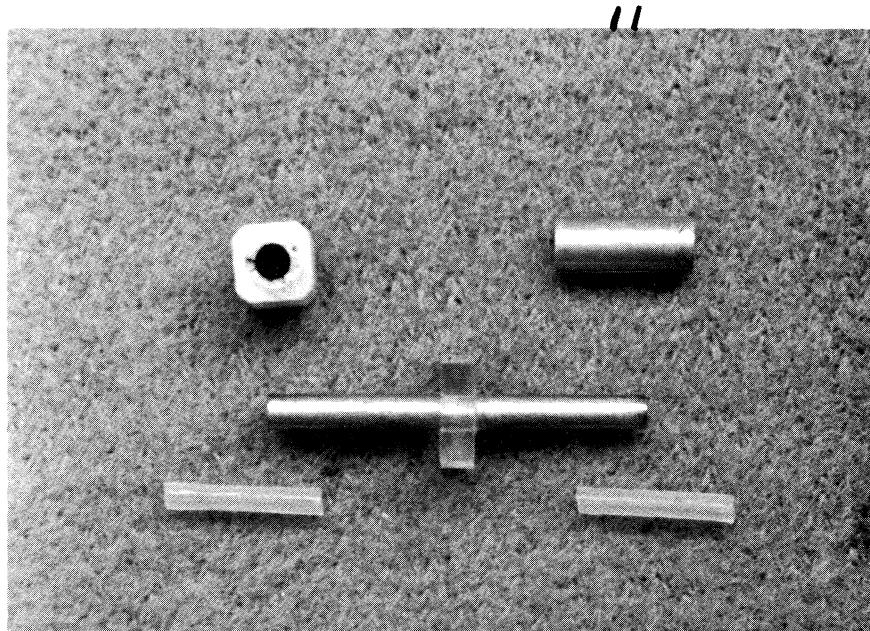


Fig. 5. Close-up view of sliding transformers (top), center conductor, and Teflon-tubing DC blocks.

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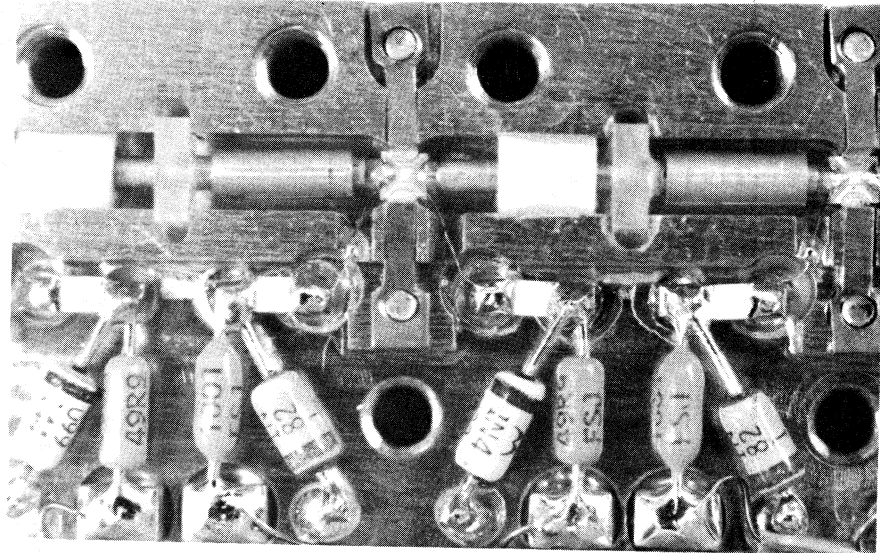


Fig. 6. Middle-stage view of amplifier.

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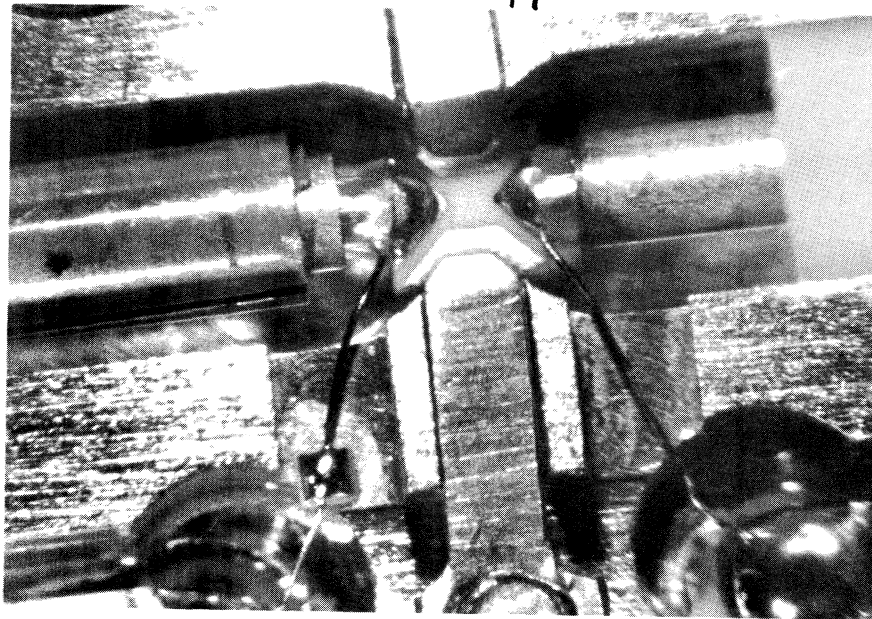


Fig. 7. Close-up view of FET, bias leads (#40 enameled copper wire), and 0.8 pF gate bypass capacitor. Note the Teflon tubing protruding from within center conductor and pressing against FET for mechanical stability.

III. Adjustment and Test

The test configuration for the amplifier is shown in Figures 8 and 9; this equipment is used in conjunction with an Apple computer, ADIOS A/D interface [4], and NOISE1 program to give data output as shown in Figure 10.

The accuracy of the low-noise temperature measurements is increased by utilizing a cooled 20 dB Narda Model 4779 attenuator at the amplifier input. By cooling this attenuator from 300K to 15K, the temperature added to the amplifier noise temperature of $\sim 40\text{K}$ is decreased from 300K to 18K. The error due to noise source or detector-law inaccuracy is then reduced by a factor of $(300 + 40)/(18 + 40) = 5.9$.

The noise source, input coaxial line, attenuator cascade was calibrated at the isolator input connector by comparison with a NRAO liquid nitrogen and room temperature noise standard. This was performed with the test dewar open at 300K. The change in the attenuation value due to cooling from 300K to 15K was measured at DC and was an increase of $0.18 \pm .01$ dB for two Narda attenuators. This is approximately compensated by a decrease in the loss of the coaxial lines as determined from measurements described in a previous report [5]. An error of 0.1 dB in the noise source excess noise temperature ratio would produce an amplifier noise temperature error of 1.3K. The temperature of the cooled attenuator is monitored with a Lake Shore Cryotronics DG-400 sensor.

The amplifier is tuned at 300K for minimum noise at 15.1 GHz and for gain flatness. An initial bias of 5V, 5 mA; 5.5V, 10 mA; and 4V, 10 mA is used for the first, second and third stages respectively at 300K. These values were then optimized at 15K for minimum noise and gain within specifications;

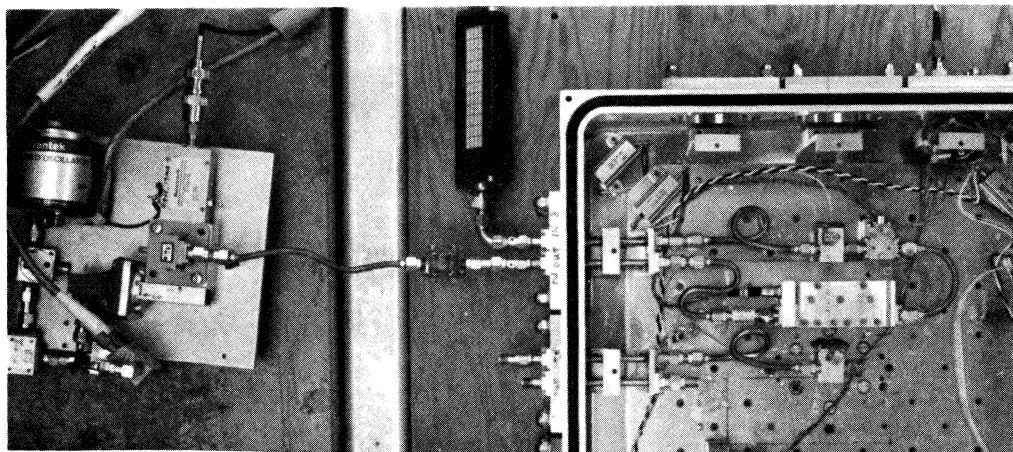


Fig. 8. Test configuration showing HP346B noise source (top, middle), low-loss coaxial thermal transition into dewar, Narda 20 dB attenuator with temperature sensor, Pamtech input isolator, amplifier under test, Narda 7 or 8 dB output attenuator, output transition, isolator, and test receiver.

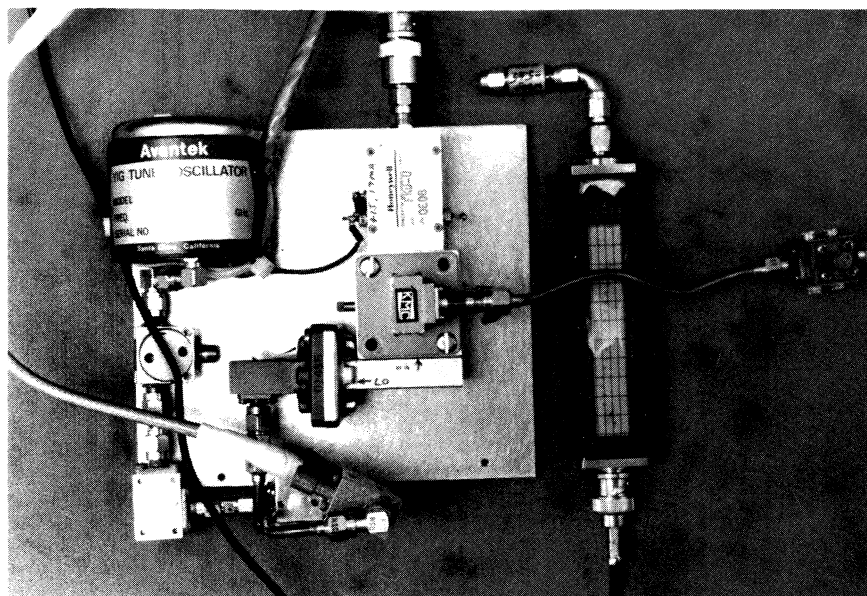
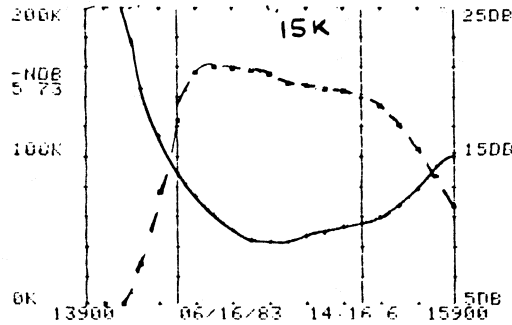


Fig. 9. Test receiver consisting of an Avantek 2-8 GHz YIG-tuned oscillator, Aertech RX16000 frequency doubler, isolator, directional coupler to provide reflectometer source, and mixer-preamp for noise temperature measurements.

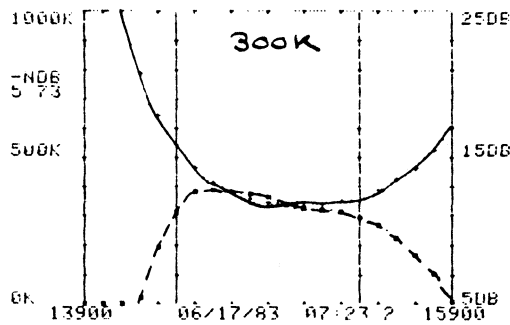
1) 360, PAN-123, OPT BIAS, 7 DB PAD
 14:16.6 06/16/83 TAU=54.7 TLO=42.9 @ 14950 GI=17.3 GH=21 T=11.5K
 3.93,6.1,-.735 5.52,14.8,-1.07 4.9,7,-1.011



14:27.4 06/16/83 ZERO=7.8 AOB=6 TF=15.4 -NDR=5.73

F,GHZ	NOISE	GAIN,DB	F,GHZ	NOISE	GAIN,DB
14.4	89.8	17.3	14.5	73	20.5
14.6	61	21	14.7	51.1	20.8
14.8	44.5	20.7	14.9	43.3	20.5
15	43.5	19.8	15.1	47.4	19.6
15.2	49.6	19.4	15.3	53.6	19.3
15.4	55.6	19	15.5	59.6	18.3

1) 360 @ 300K WITH OPT COLD BIAS
 07:23.2 06/17/83 TAU=376.4 TLO=332 @ 15000 GI=10.8 GH=12.8 T=297.1K
 7.98,6.1,-.43 5.52,14.8,-.821 4.9,7,-.804



07:26.1 06/17/83 ZERO=7.8 AOB=6 TF=300 -NDR=5.73

F,GHZ	NOISE	GAIN,DB	F,GHZ	NOISE	GAIN,DB
14.4	541.7	11.2	14.5	458.2	12.6
14.6	408.3	12.7	14.7	375.7	12.6
14.8	352	12.5	14.9	341.3	12.2
15	332	11.6	15.1	341.4	11.5
15.2	333.5	11.3	15.3	345	11.1
15.4	356	10.8	15.5	386.5	10.3

Fig. 10. Typical gain and noise temperature for an amplifier including input isolator and output 7 dB attenuator at physical temperatures of 15K (top) and 300K.

typical final values were 4V, 5 mA; 5.5V, 15 mA; and 4V, 8 mA. The amplifier gain including a 7 dB pad is typically 12 dB at 300K and 19 dB at 15K as shown in Figure 10. The typical improvement in noise temperature is a factor of ~ 8 .

A large variation of cold noise temperature with the NE67383 transistor batch was observed. An initial batch of 20 averaged 35K at optimum frequency; a second batch 40K; and the third batch 47K. The lowest noise temperature was 31K and $\sim 15\%$ of the transistors gave noise temperatures $> 50K$ and were rejected. Early tests with the NE13783 produced noise temperatures above 60K.

REFERENCES

- [1] G. Tomassetti, S. Weinreb, and K. Wellington, "Low-Noise 10.7 GHz Cooled GaAs FET Amplifier," Electronics Letters, vol. 17, no. 25/26, December 10, 1981, pp. 949-951.
- [2] M. Sierra, "15 GHz Cooled GaAsFET Amplifier-Design Background Information," NRAO Electronics Division Internal Report No. 229, June 1982.
- [3] H. A. Wheeler, "Transmission-Line Impedance Curves," Proc. IRE, vol. 38, no. 12, December 1950, pp. 1400-1403.
- [4] G. Weinreb and S. Weinreb, "ADIOS - Analog-Digital Input Output System for Apple Computer," NRAO Electronics Division Internal Report No. 212, April 1981.
- [5] S. Weinreb, "Cryogenic Performance of Microwave Terminations, Attenuators, Absorbers, and Coaxial Cable," NRAO Electronics Division Internal Report No. 223, January 1982.

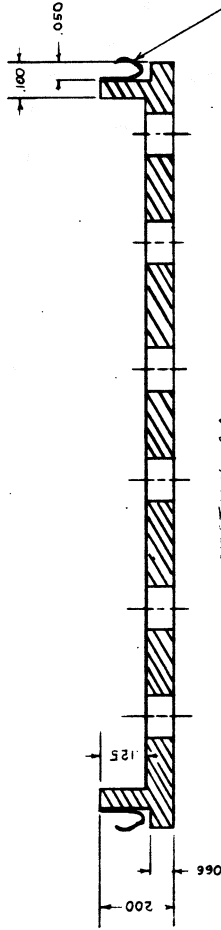
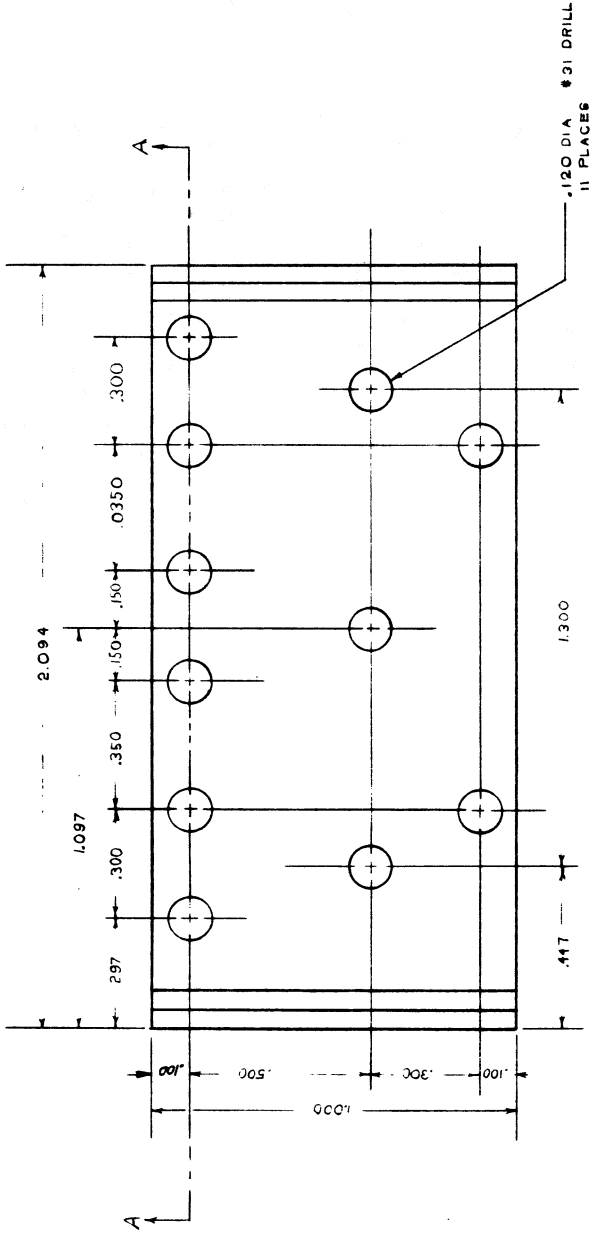
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1	1		15 GHz FET amplifier schematic	NRAO	A2.613S-01
2	1		Chassis	NRAO	D2.613M-73, sht. 1
3			Chassis details	NRAO	C2.613M-73, sht. 2
4	1		Amplifier cover	NRAO	C2.613M-70
5	6		Transistor strap	NRAO	B2.613M-71
6	1		Output end plate	NRAO	B2.613M-77
7	1		Input end plate	NRAO	B2.613M-78
8	4		Transformer slug (15 ohm)	NRAO	B2.613M-72
9	1		Transformer slug (26 ohm)	NRAO	B2.613M-72
10	1		Transformer slug (22 ohm)	NRAO	B2.613M-72
11	2		Interstage support	NRAO	B2.613M-75
12	2		Interstage inner conductor	NRAO	B2.613M-76
13	1		Mounting plate with output transition	NRAO	C2.613M-81
14	1		Input SMA modification	Omni-Spectra (modified)	204CC/NRAO B2.613M79
15	1		Output SMA modification	Omni-Spectra (modified)	204CC/NRAO B2.613M80

ITEM	QUANTITY	REF. DESIG.	DESCRIPTION	MFG.	PART NUMBER
16	4		SMA connector	Omni-Spectra	201-1A
17	1		Power connector	Micro-Tech	ER-7S-6
18	6		$\lambda/4$ transformer dielectric, Teflon	Alpha	AWG-24-LW
19	1		FET, first stage	NEC	NE67383
20	1		FET, second stage	Mitsubishi	MGF-1412-09
21	1		FET, third stage	Mitsubishi	MGF-1412-10
22	6		FET bias leads, 40 AWG T2 Beldure	Belden	8046
23	6		Bias wires, 30 AWG SGL-Beldsol	Belden	8055
24	2		Finger stock	Instrument Specialties	97-221-A
25	6		0-80 x 3/16 Filister HD screws (goldplated)		
26	8		4-40 x 3/16 socket HD SS screws	All-Metal	
27	3		4-40 x 5/16 socket HD SS screws	All-Metal	
28	2		2-56 x 1/2 socket HD SS screws	All-Metal	
29	4		2-56 x 1/4 socket HD SS screws	All-Metal	
30	2		2-56 x 3/16 socket HD SS screws	All-Metal	

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31	3		.8 pf chip capacitor	ATC	111TBAOR8B100AP
32	6		.8 pf chip capacitor	ATC	100AOR8CP50
33	6		16 pf chip capacitor	ATC	100A160CP50
34	6		680 pf chip capacitor	ATC	100B681KP50X
35	6		50 ohm chip resistor	Mini-Systems, Inc.	WA13PG-500J-S
36	3		49.9 ohm 1/8W metal film resistor	Corning	RLR05C-49R9-FR
37	3		1000 ohm 1/8W metal film resistor	Corning	RLR05C-1001-FR
38	3		Diode zener	Motorola	1N4099
39	3		Diode zener	Motorola	1N821
40	1		7 dB attenuator DC-18 GHz	Narda	4779-7
41	1		Cooled isolator	PamTech	PTC-2021M
42			.141 semi-rigid coax, 50 ohm	Uniform Tubes	UT-141A
43			Polystyrene Q-dope	GC Electronics	#37-2
44			910 adhesive	Permabond International	910
45			Solder B20E2, .032 dia.	Alpha Metals	B20E2-.032

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47			Flux, Super-Safe	Superior Flux & Mfg.	#30
48			Flux, rosin liquid	Kester	#1544

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CONTACT STRIPS: CAT. NO. 97-221-A
 BY INSTRUMENT SPECIALTIES CO.
 DELAWARE WATER GAP, PA.
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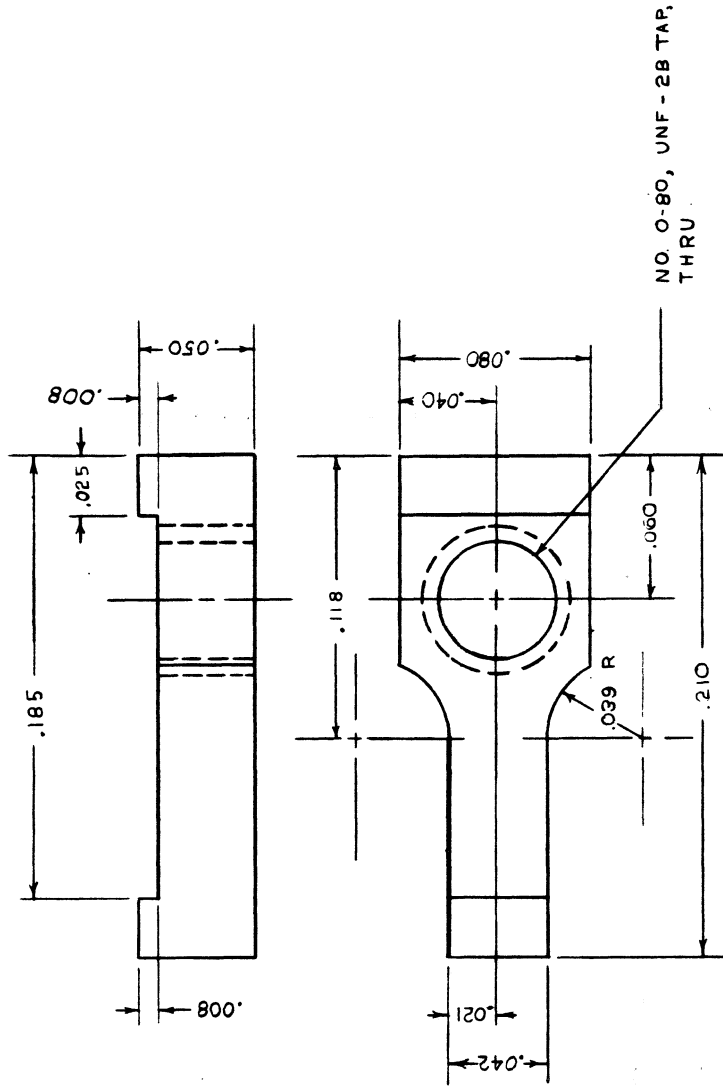
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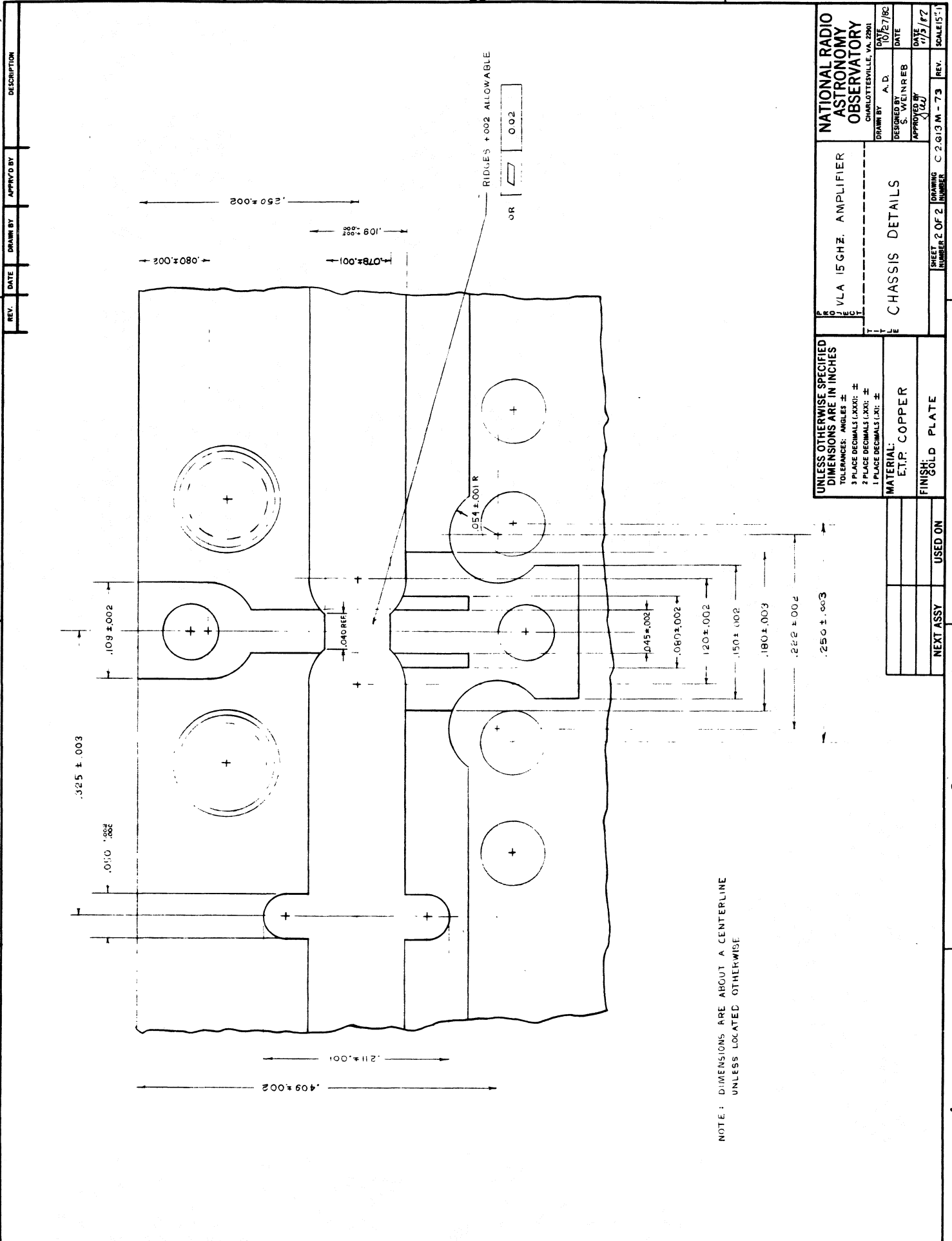
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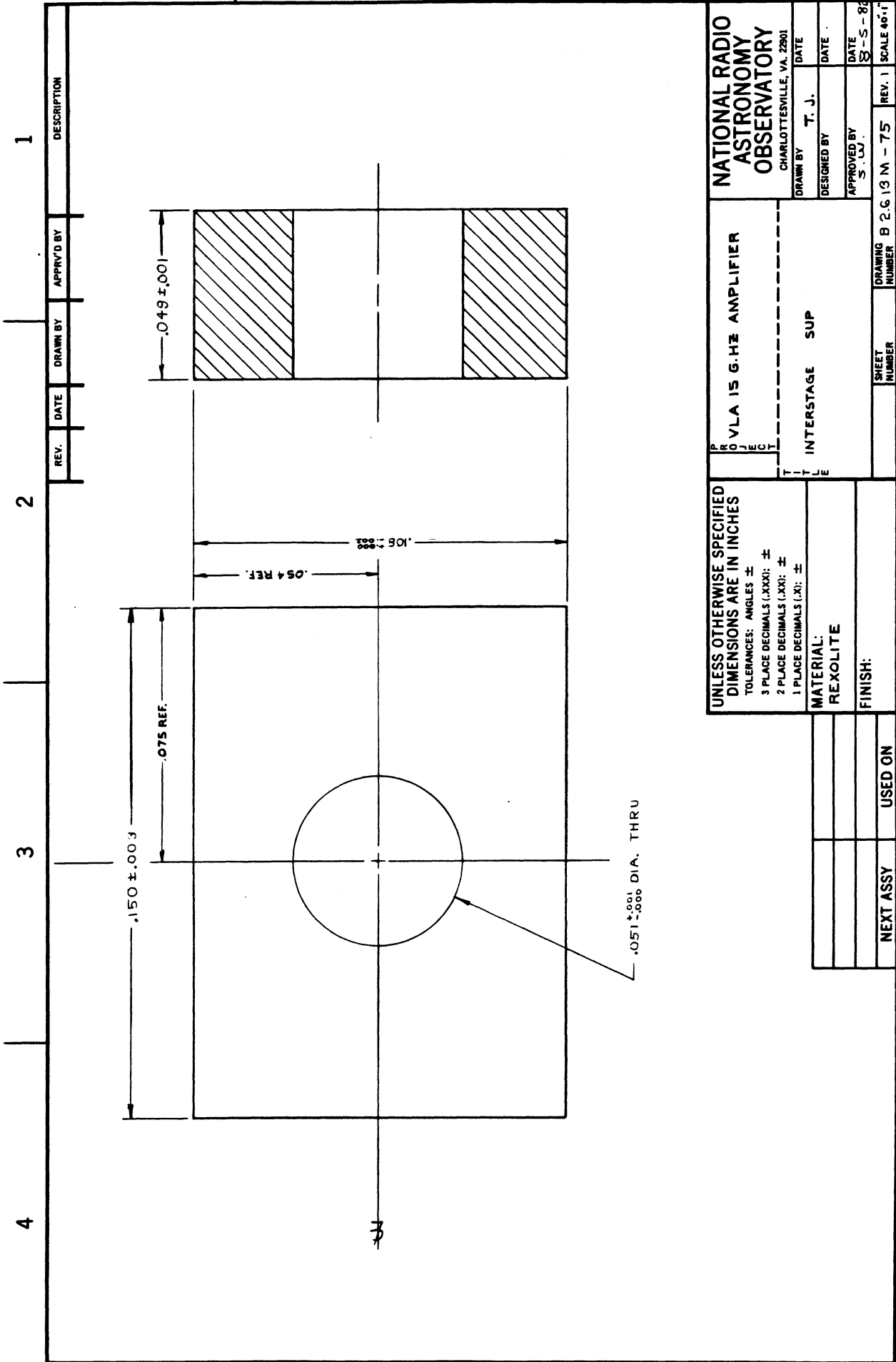
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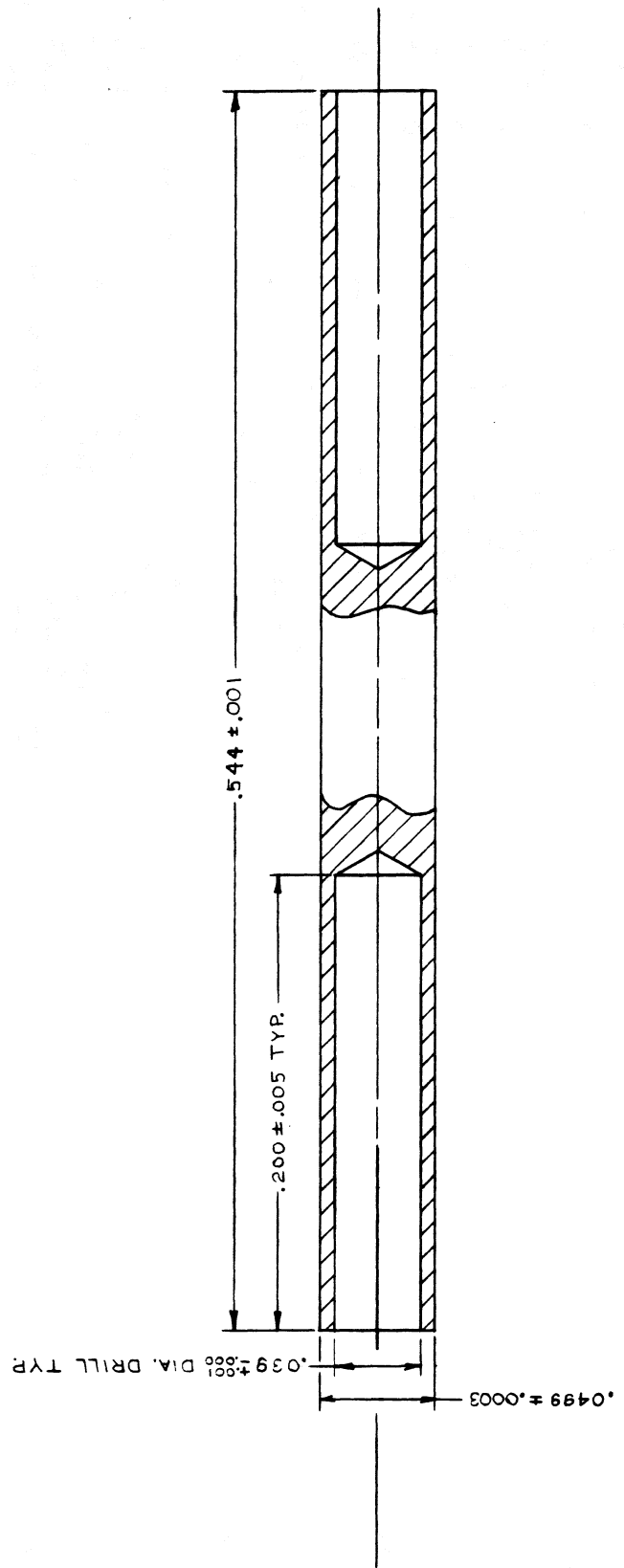
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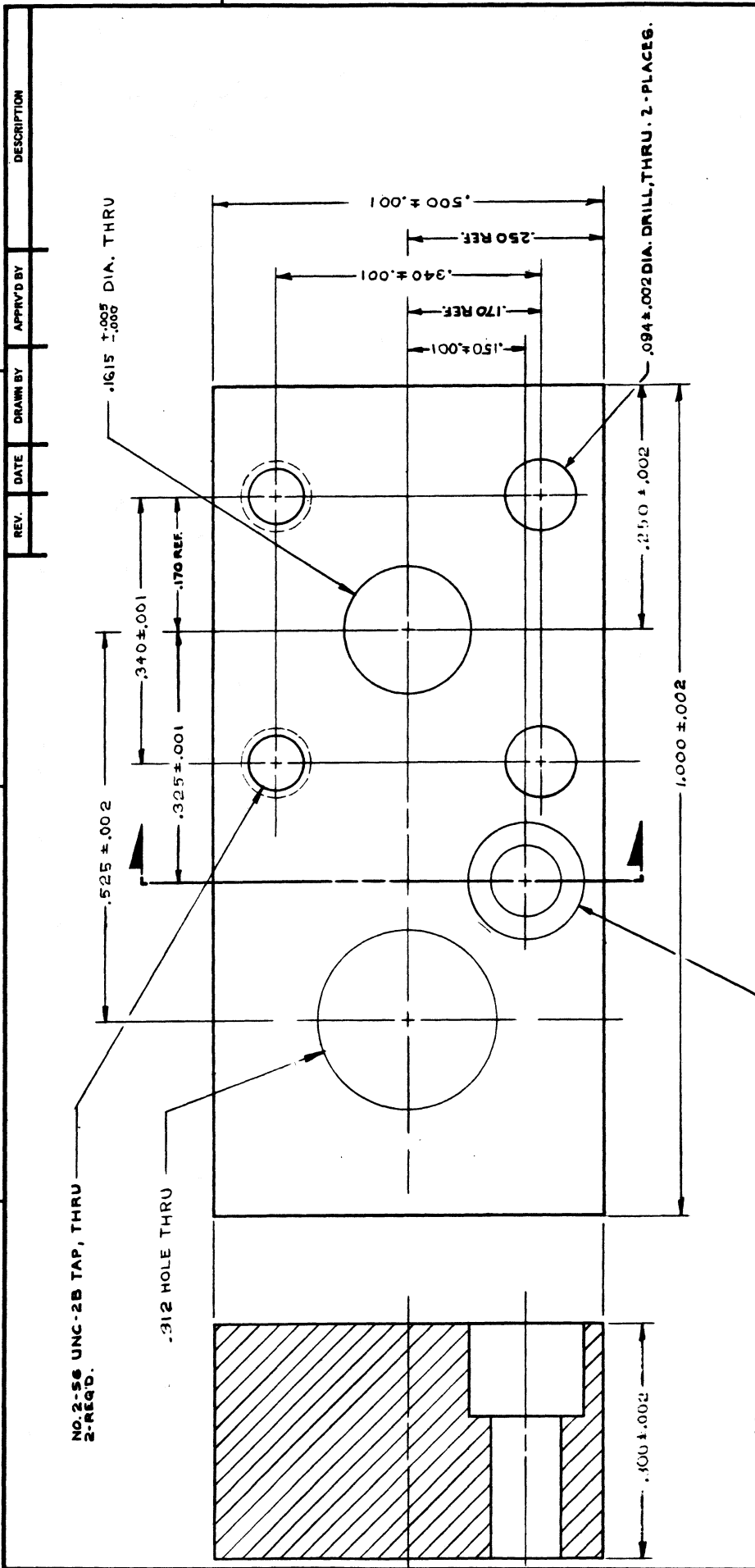
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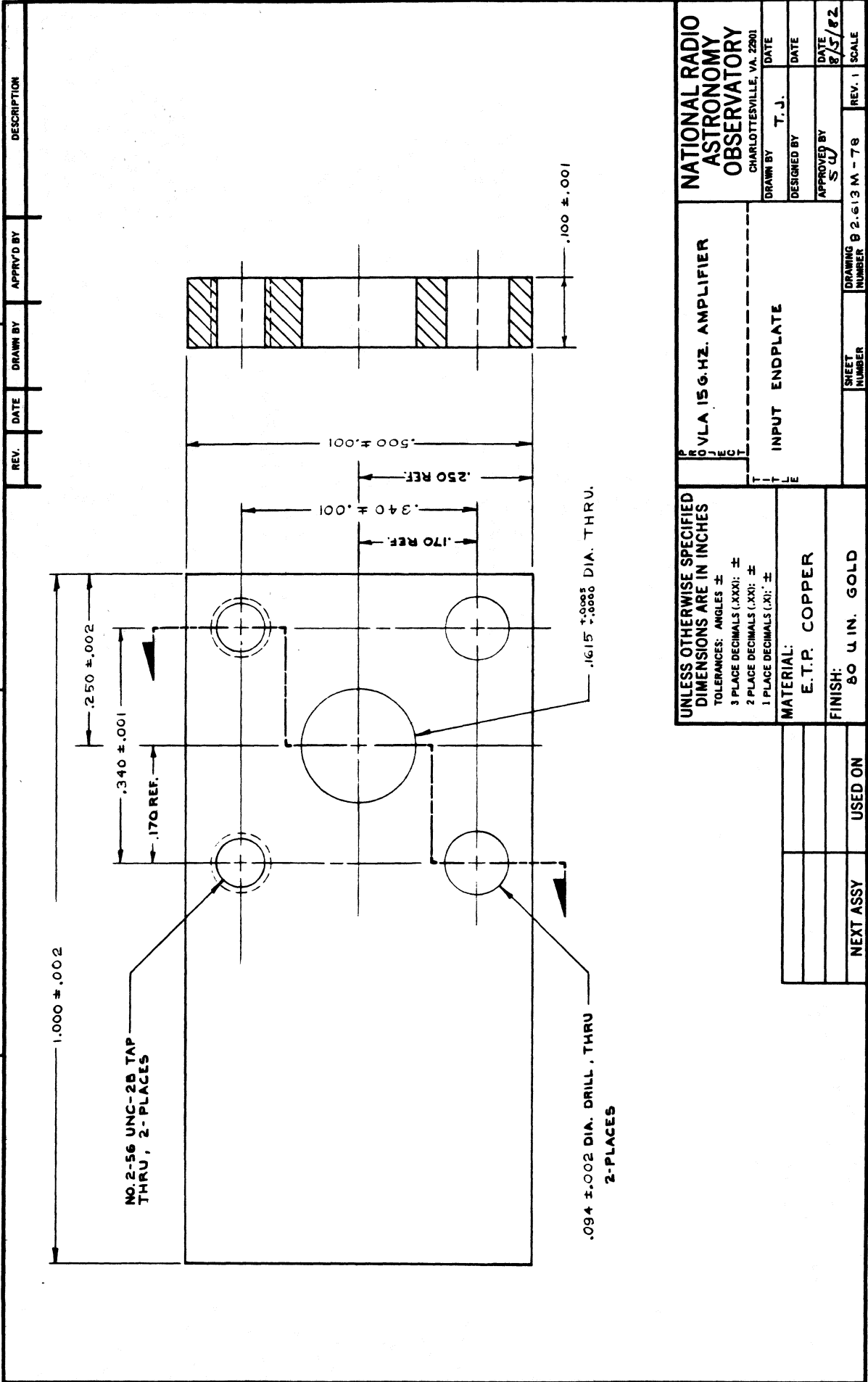
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NO. 2-56 UNC-2B TAP, THRU 2-REQD.					
.312 HOLE THRU					
.095 ± .001 DIA. DRILL, THRU .500 ± .001 DIA. C BORE, .119 ± .001 DEEP					
.094 ± .002 DIA. DRILL, THRU, 2 PLACES.					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±		NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTEVILLE, VA. 22901			
MATERIAL: E.T.P. COPPER		DRAWN BY T. J. DESIGNED BY APPROVED BY S J			
FINISH: 80 U. IN. GOLD		DATE 8/5/72 DATE DATE			
NEXT ASSY USED ON		SHEET NUMBER DRAWING NUMBER B 2-613 M - 77		REV. 1 SCALE	
		OUTPUT ENDPLATE		1	
		VLA 15 G. HZ. AMPLIFIER		1	

4 3 2 1

4 3 2 1



DESCRIPTION

APPR'D BY

DRAWN BY

DATE

REV.

NATIONAL RADIO ASTRONOMY OBSERVATORY
 CHARLOTTEVILLE, VA. 22901
 DRAWN BY T. J. DATE
 DESIGNED BY DATE
 APPROVED BY S W DATE 8/5/82
 REV. 1 SCALE

VLA 156 HZ. AMPLIFIER
 INPUT ENDPLATE
 DRAWING NUMBER 2.613 M - 78
 SHEET NUMBER

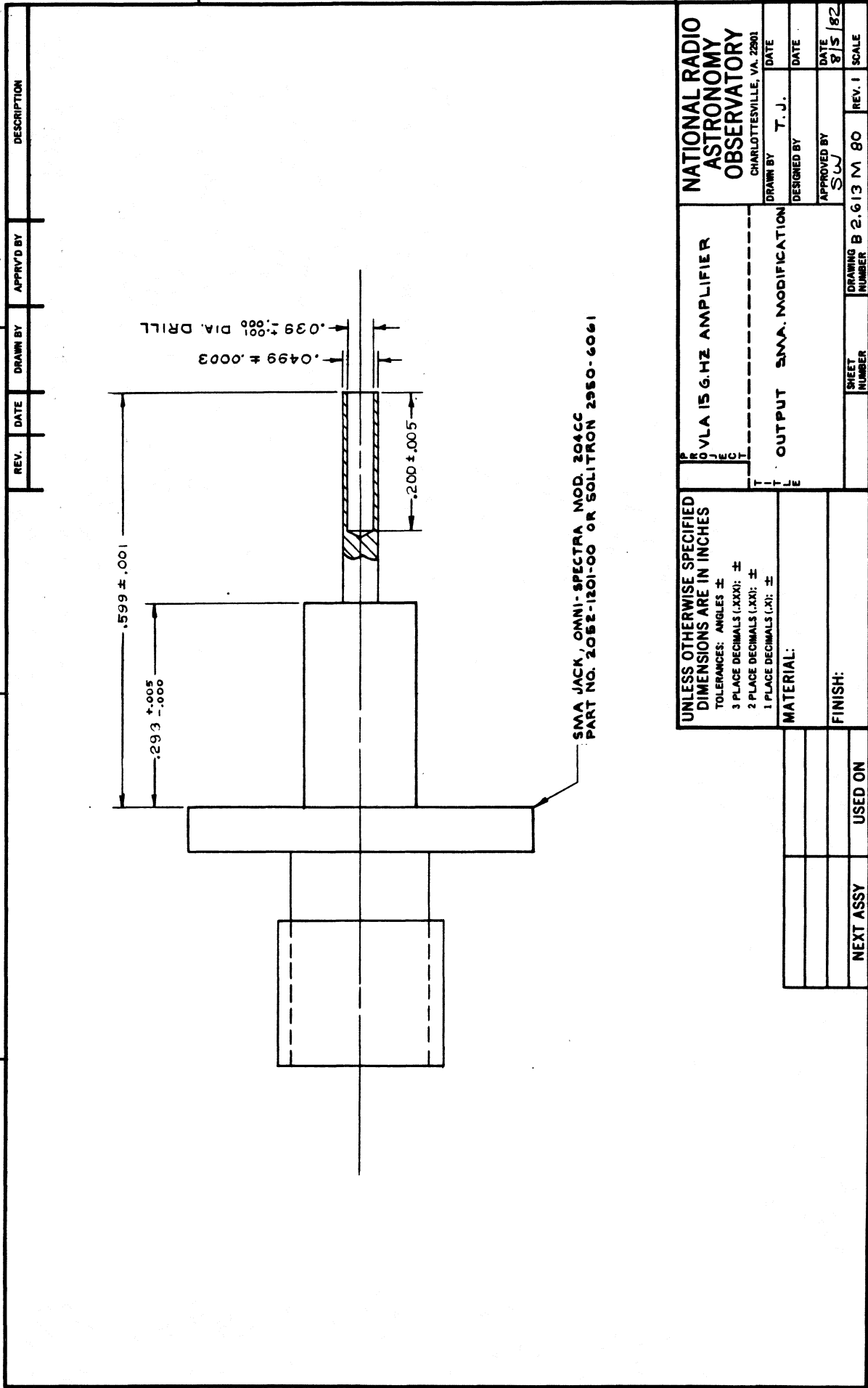
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
 TOLERANCES: ANGLES ±
 3 PLACE DECIMALS (.XXX): ±
 2 PLACE DECIMALS (.XX): ±
 1 PLACE DECIMALS (.X): ±
 MATERIAL: E.T.P. COPPER
 FINISH: 80 U.I.N. GOLD

USED ON

1 2 3 4

4	3	2	1
			DESCRIPTION 1
		REV. DATE DRAWN BY APPR'D BY 2	NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTEVILLE, VA. 22601 DRAWN BY T. J. DESIGNED BY APPROVED BY SW DATE 8/5/82 SCALE
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ± MATERIAL: FINISH: NEXT ASSY USED ON 3	PROJECT VLA 15-G.HZ. AMPLIFIER INPUT S.M.A. MODIFICATION SHEET NUMBER DRAWING NUMBER B 2.613M-79 REV. 1 1

4 3 2 1



REV.	DATE	DRAWN BY	APPR'D BY	DESCRIPTION

SMA JACK, OMNI-SPECTRA MOD. 204CC
PART NO. 2052-1201-00 OR SOLITRON 2950-6061

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: ANGLES ± 3 PLACE DECIMALS (.XXX): ± 2 PLACE DECIMALS (.XX): ± 1 PLACE DECIMALS (.X): ±		VLA 15 G. HZ AMPLIFIER		NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, VA. 22901	
MATERIAL:		OUTPUT SMA. MODIFICATION		DRAWN BY T. J.	
FINISH:		DRAWING NUMBER B 2.613 M 80		DESIGNED BY	
NEXT ASSY		SHEET NUMBER		APPROVED BY SW	
USED ON		DRAWING NUMBER		DATE 8/5/82	
				REV. 1 SCALE	

4 3 2 1

