NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 227

MODEL IV CORRELATOR IF SYSTEM

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MARCH 1982

NUMBER OF COPIES: 150

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Introduction

The Model IV Correlator IF System design represents a significant change from earlier NRAO correlators. Previous systems used bandpass filters to set the bandwidth. Cascaded mixers and filters allowed the center frequencies of the filters to be lowered along with bandwidth for better filter performance. Five mixer stages were used for the nine bandwidths provided. Input center frequency could be either 30 or 150 MHz. Important functions were set or monitored on the front panel.

The new system is simpler in block diagram form but requires more sophisticated units. It is a single sideband system having 11 bandwidths in octave steps from 78 kHz to 80 MHz that are determined by low pass filters. These filters are more economical than the bandpass type and provide a greater percentage of usable bandwidth. The disadvantage is providing the baseband signal with adequate image suppression over a large bandwidth, 4 kHz to 80 MHz, more than four decades. In addition, it was desirable to provide a variable IF so that the four inputs could be offset in frequency. These requirements were met by developing a SSB converter covering a LO input range of 100 to 500 MHz. The LO frequency determines one edge of the band and the width extends above or below this frequency by the bandwidth and sideband chosen. All functions are set or monitored remotely from the digital system.

Input Circuits

A block diagram showing one of the four IF systems is given in Figure 1. The input level must be equivalent to greater than -50 dBm/500 MHz. After amplification to -8 dBm an overload detector, Figure 2, monitors the total power to prevent mixer overload. The step attenuator is automatically adjusted

during the "balance" procedure at the beginning of a scan for the proper level for that part of the spectrum chosen. If the out-of-band noise from the front end should average more than about 6 dB above the in-band level, the conversion will become non-linear. The nominal mixer level is set high to overcome losses in the baseband networks and to keep the signal-to-noise ratio high.

The wide open front end in this system allows input signals at three times the desired input frequency to be converted to baseband with only about 12 dB additional conversion loss. This is a typical value for double balanced mixers and must be overcome by filtering. The IF input is limited to less than 600 MHz in a previous unit. When the desired LO is below 230 MHz a 320 MHz low pass filter is switched in automatically. Below 135 MHz the system may again have 3rd harmonic problems depending upon the bandwidth and sideband chosen. The interfering sideband is on the opposite side of the 3rd harmonic from the one selected. If a problem seems likely, a temporary filter should be added.

Single Sideband Converter

The SSB unit contains a commercial amplifier and quadrature hybrid for the LO signal, a switched transformer for sideband selection, two mixers, baseband quadrature networks, a resistive summing network, and a baseband amplifier. The circuit details are shown in Figure 3. The LO quadrature network is a custom-designed commercial unit used in the VLBI Mk III system. The 3°, 1 dB tolerance on these units was not adequate for this application so a better unit was sought. After the supplier showed no interest in a tolerance better than 2°, we tried improving the existing units. This effort paid off well in that the accuracy was improved to less than 1°. A variety of flat pack mixers were then tested for accuracy. Most of these

were disappointing in match. The best performance was obtained from a miniature Mini-Circuits unit. Even with padding on all terminals the mixers contribute more error than the hybrid or baseband network.

The baseband quadrature networks were designed to give more than 39 dB rejection from 4 kHz to 80 MHz. To have the network and output referenced to ground the input had to be floating. This was accomplished with the network arrangement shown in Figure 3. One inductor in each leg is tied to ground and is in series with two isolated inductors. This topography permits the input signals to be injected through the coils to the driving point by using coax for the windings. The generator is thereby floating. The network outputs are combined in a resistive summing network that feeds a low impedance amplifier. This passive method of combining eliminates the errors and drifts in an active circuit but introduces its own type of error due to interaction between outputs. A compromise was made between signal loss and error from crosstalk. Figure 4 shows the theoretical network error with complete output isolation and the error compromised by -43 dB of crosstalk in the summing network. The design for these networks and the associated curves were provided by J. Granlund. The output amplifier has a very low input impedance which is part of the network design. A rise in gain with frequency is required to compensate for losses in the very small coax in the network coils. Several extra components have been added between the emitter follower and the output jack to shape the response. The inductors in the summing network were added to compensate for high dc resistance in the coax.

The overall performance was measured at 50 MHz increments from 100 to 500 MHz and over the full baseband at each frequency. Image rejection is typically 34 dB on the peaks with the worst points being 29 to 30 dB. The networks were adjusted for a near uniform rejection across the band. As a result, the

crosstalk error does not produce the uneven peaks shown but does degrade performance.

Baseband Processing

Following the SSB unit the signal is amplified, limited to 80 MHz and fed to amplifier-switching units. These schematics are shown in Figures 5 and 6. The amplifiers are of a common IC type and the bandwidth determining filters are selected by diode switches driven from the IF Logic card. Fixed attenuators compensate for bandwidth changes to keep a constant output power. The square law detector is a back diode design used in many NRAO filter receivers and VLBI converters. One detector output feeds a V/F converter, Figure 7, for total power counting in the digital system. The X1 and X10 analog outputs are provided at the back of the rack for remote monitoring. The output amplifier is shown in Figure 2.

Clipper

The clipper is a new design for this system but is basically the circuit used in previous correlators. The redesign was done to provide offset slicing and to extend the bandwidth. Before developing this unit a high speed digital line receiver was tested for this application. A bandwidth of over 400 MHz was expected but measured less than 150 MHz. This was not adequate, so an updated design was developed.

In our older correlators the analog-to-digital conversion was done by a hard limiter detecting zero crossovers of the baseband signal thus providing one bit output data after sampling. This is a simple conversion system but does not include any amplitude information. With the two-bit 3-level conversion used here the loss of data is reduced from 36% to 19%. The slicing

levels are at ± 61.2% of the rms level of the noise. This is done by running two clippers in parallel with dc offsets at their inputs. See Figure 8. The offset magnitudes are set by determining the error in the percentage of ones beyond the samplers and feeding back an offset correction. The report on the digital system will provide additional information on this loop. The control range was made ± 6 dB, half of this allowed for circuit errors and half for total power changes due to noise tube, signal-reference unbalance and gain drift. Bias changes with temperature on the first two stages have been reduced by a diode compensating network. The zener diodes compensate the following stages. The original goal was to obtain 1.6 GHz bandwidth per stage. This was not obtained because of the tendency to oscillate. Four 1 pF capacitors and high frequency beads were added to obtain good stability and the resulting bandwidth is about 800 MHz. It has since been determined that the bandwidth is generously adequate and may well take care of future clipper requirements.

The units are adjusted by first removing the offset bias and control voltage and grounding these inputs. A DIP switch on the bias lines does this conveniently. Adjust both regulators for 7.5 V output. Insert a -10 dBm CW signal into the input amplifier. Adjust the second regulator for ECL levels symmetrical about -1.3 V. With the input signal removed, adjust the first regulator and the 5 K bias pot for maximum gain as indicated by maximum noise out. A jumper can be removed on the output line to insert a coupling capacitor when monitoring with a spectrum analyzer.

Synthesizer

The LO for the SSB converter is generated by a synthesizer system locked to an external reference. It consists of a digital divider, oscillator and amplifier. The system was developed for the VLBI Mark III system by Alan Rogers of the Haystack Observatory. The divider shown in Figure 9 contains

a prescaler, 5 ECL dividers and a detector. The 5 MHz reference is divided to 10 kHz, the minimum increment and frequency/phase compared with the divided oscillator frequency. The detector output is amplified, loop filtered and fed to the oscillator tuning diodes.

The oscillator range of 100 to 500 MHz is covered in two bands by varactor tuned tunnel diode oscillators. See Figure 10. The range change at 230 MHz is controlled from the IF Logic card. The lock detector output is fed to the logic card but is not presently used. The frequency is checked through the Frequency Monitor unit (Figure 7) by counters in the digital system. The amplifier, Figure 11, raises the -30 dBm oscillator level to drive the divider, mixer amplifier and monitor circuits.

IF Logic Card

The IF Logic card, Figure 12, receives serial commands from the digital system to set the attenuator, sideband, frequency, bandwidth and select the proper oscillator. The 320 MHz low pass filter is switched on the oscillator range command. The card also contains the drivers for most of these functions. The IF overload and LO lock circuits are monitored for transmitting to the digital system. A more detailed discussion of the operation and interfacing with other parts of the system will be given in the digital system report.

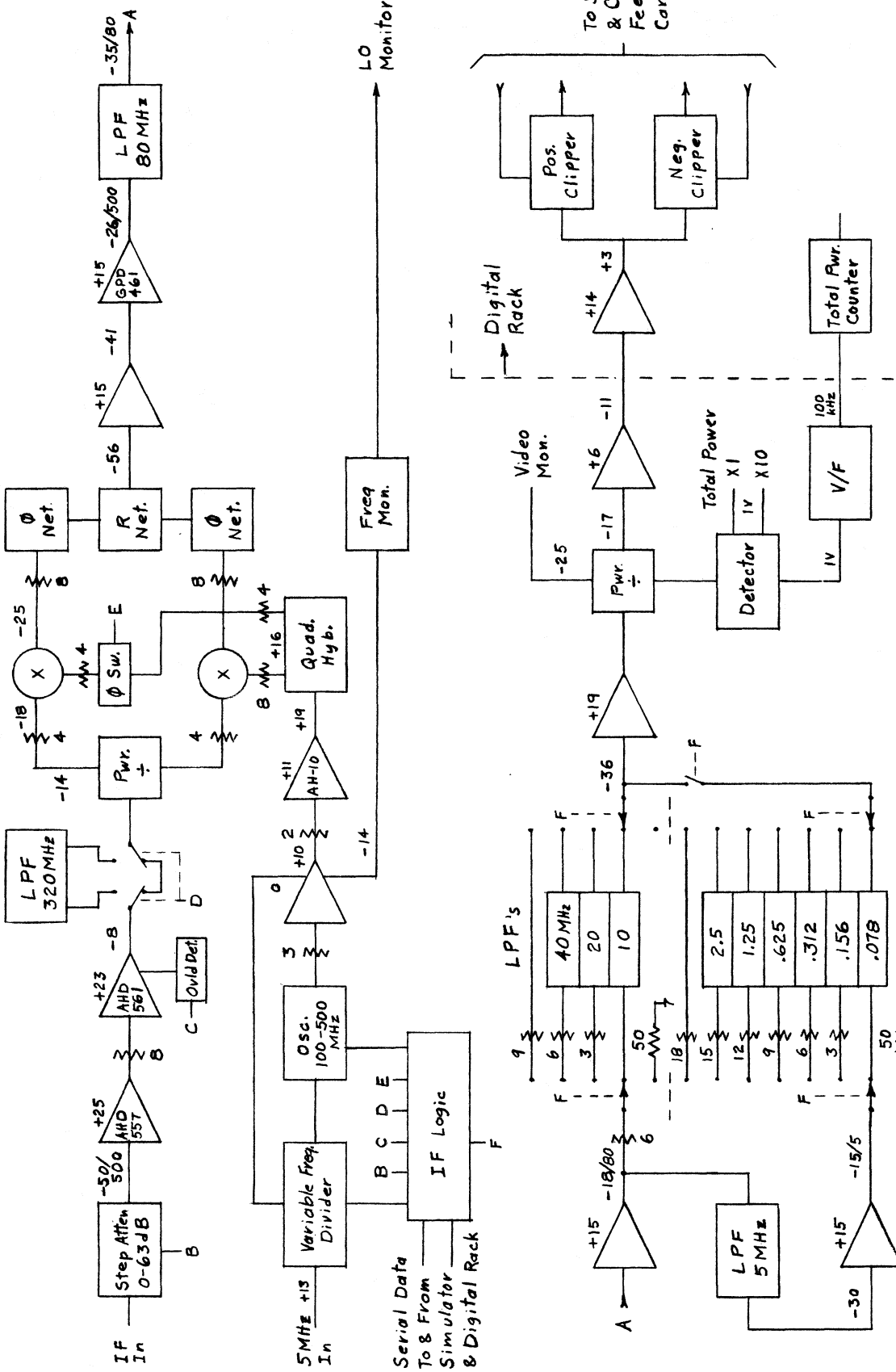
Acknowledgements

The writer wishes to acknowledge the major contributions made by John Granlund who did a very thorough and sometimes frustrating job of developing the SSB baseband and summing network designs. The results of his efforts deserve wider applications.

The wide range, compact, economical synthesizer developed by Alan E. E. Rogers for the VLBI Mark III IF Converter also added versatility to the input frequency of this system with the convenience of computer control.

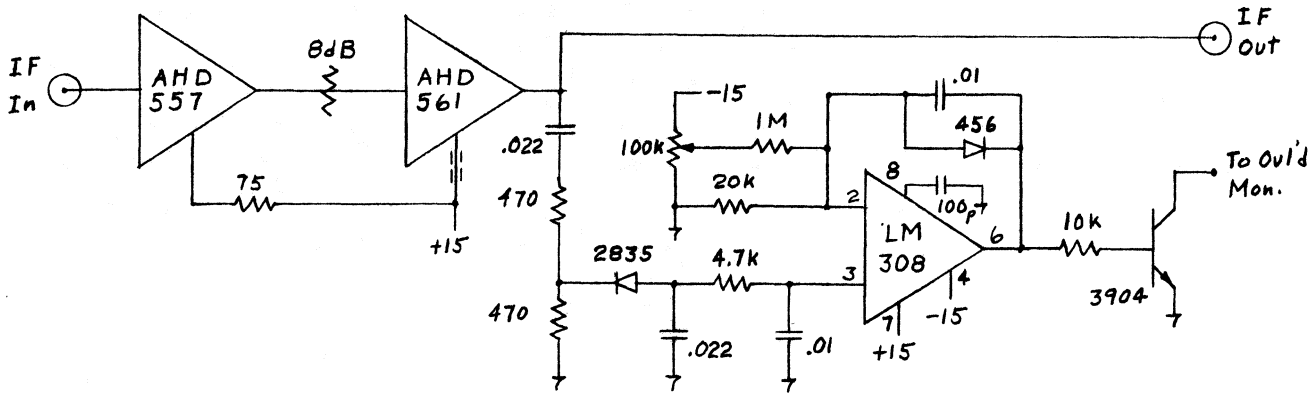
Acknowledgements (continued):

Lewis Beale constructed and tested five of these systems, arranged the layout of the components in the drawer, and helped with other packaging problems.

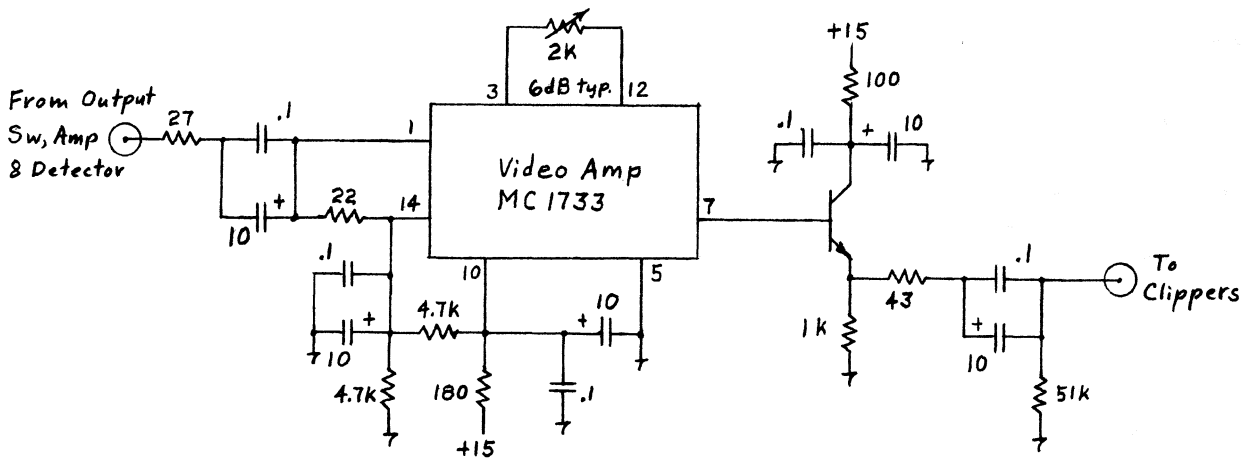


IF SYSTEM

FIGURE 1

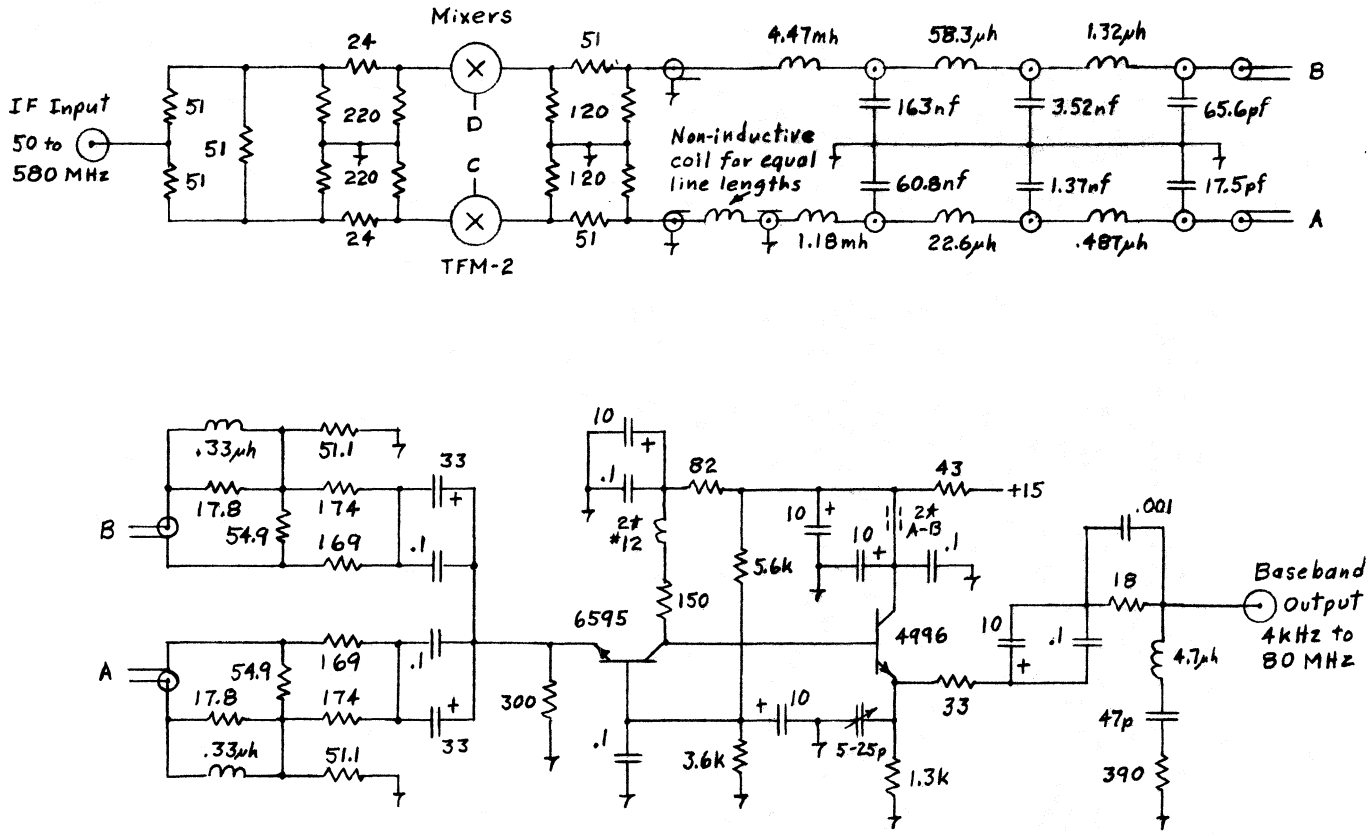


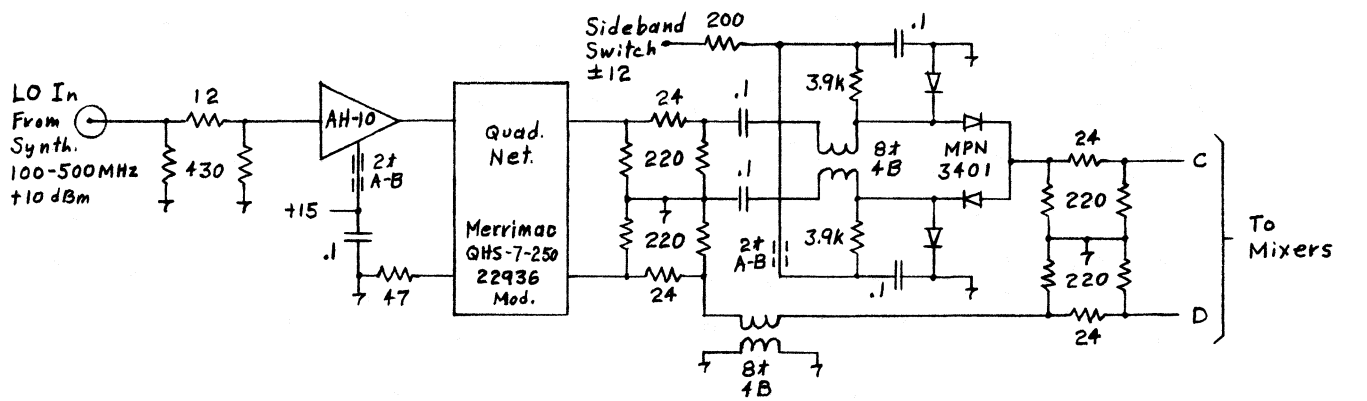
IF AMPLIFIER & OVERLOAD DETECTOR



OUTPUT AMPLIFIER

FIGURE 2





SINGLE SIDEBAND CONVERTER

FIGURE 3

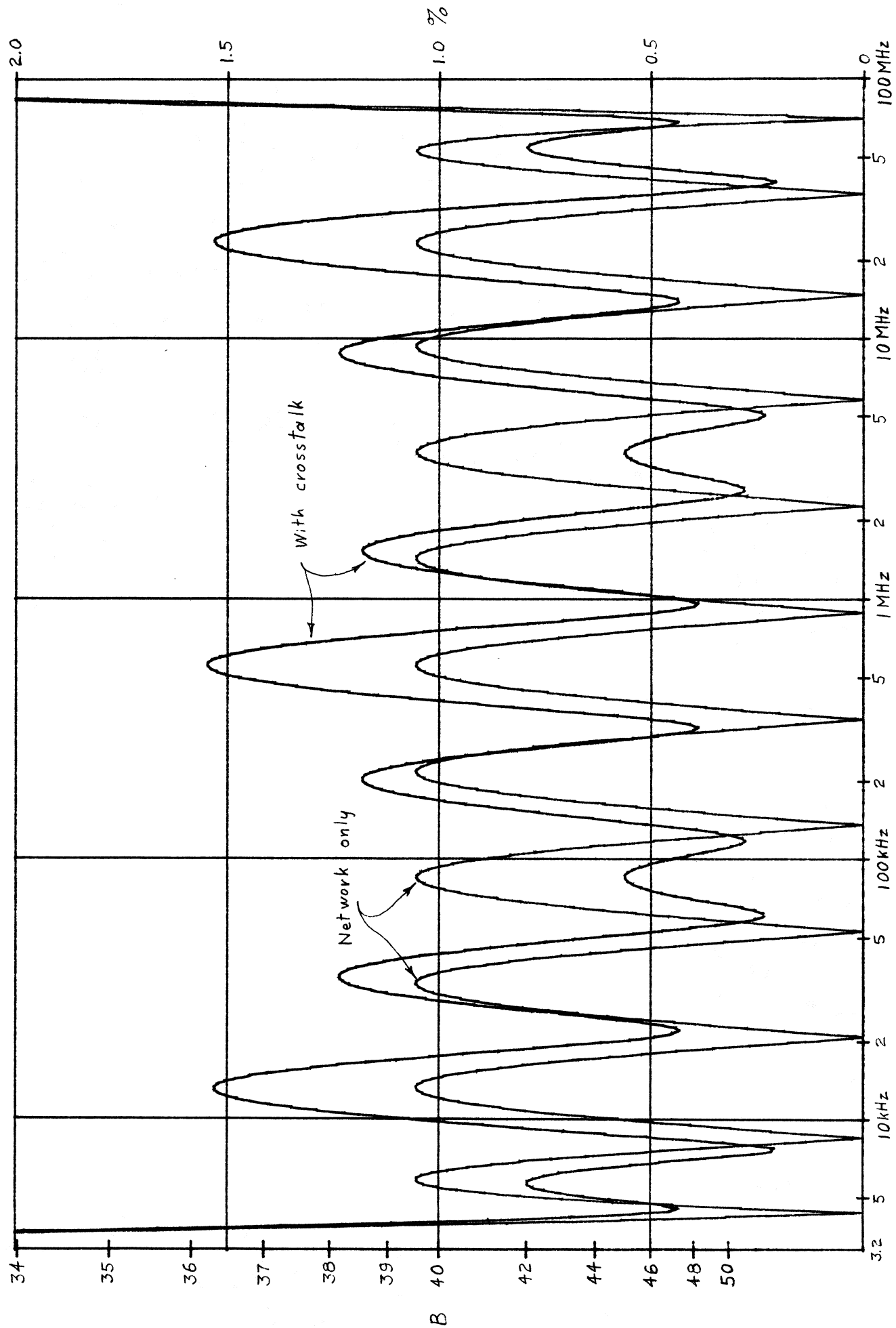


FIGURE 4

IMAGE REJECTION

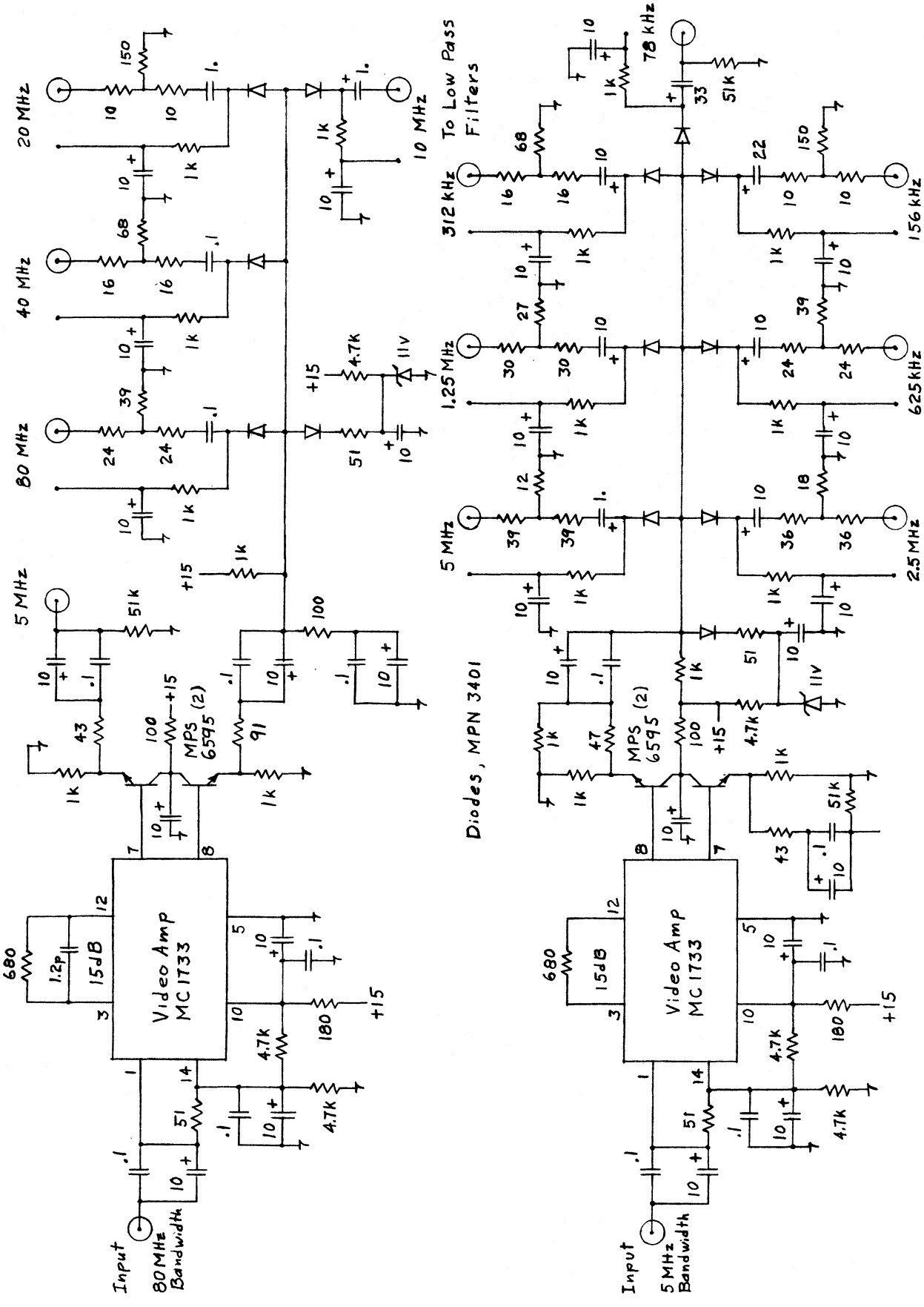


FIGURE 5

AMP, INPUT SWITCH

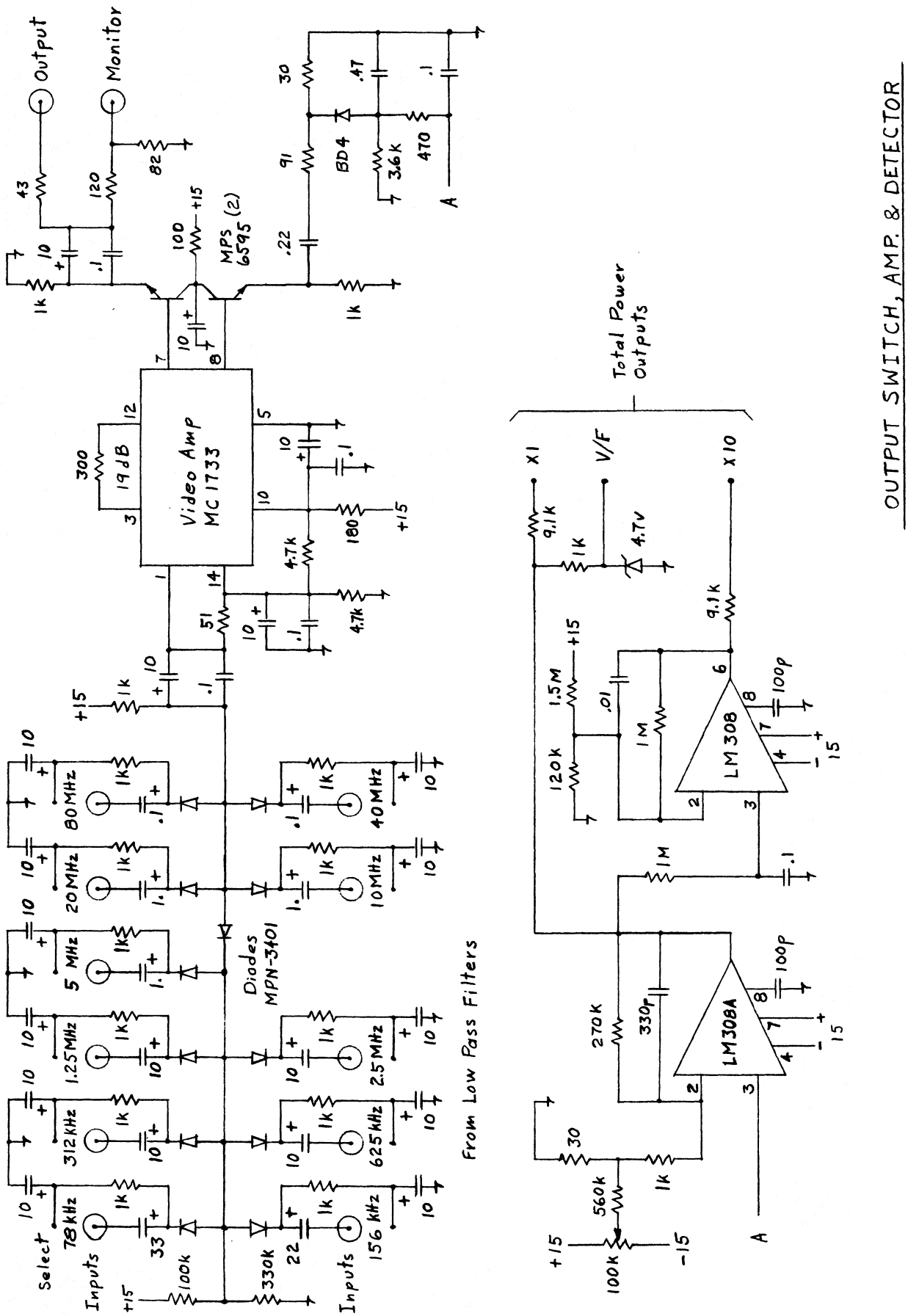
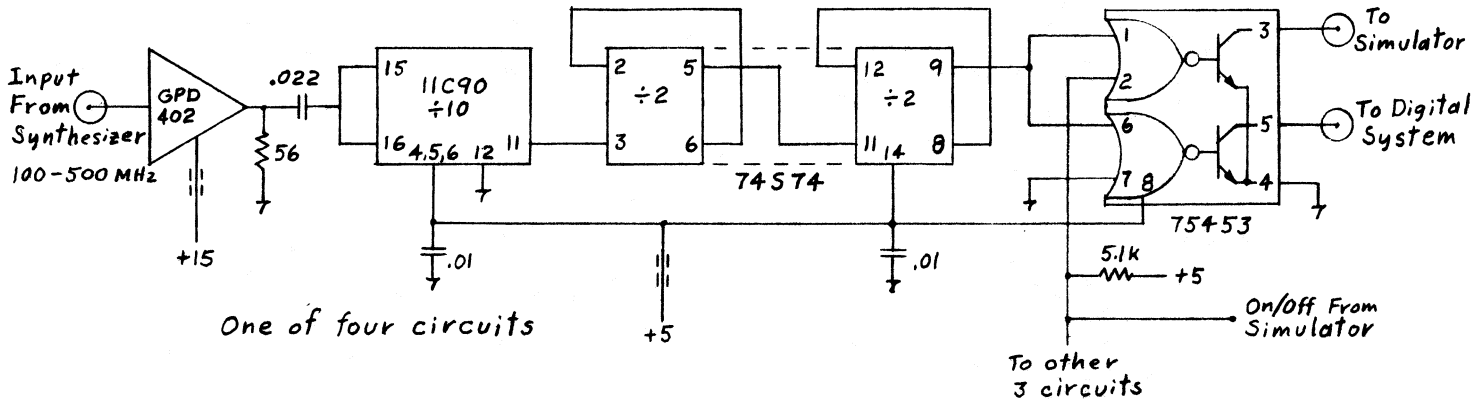
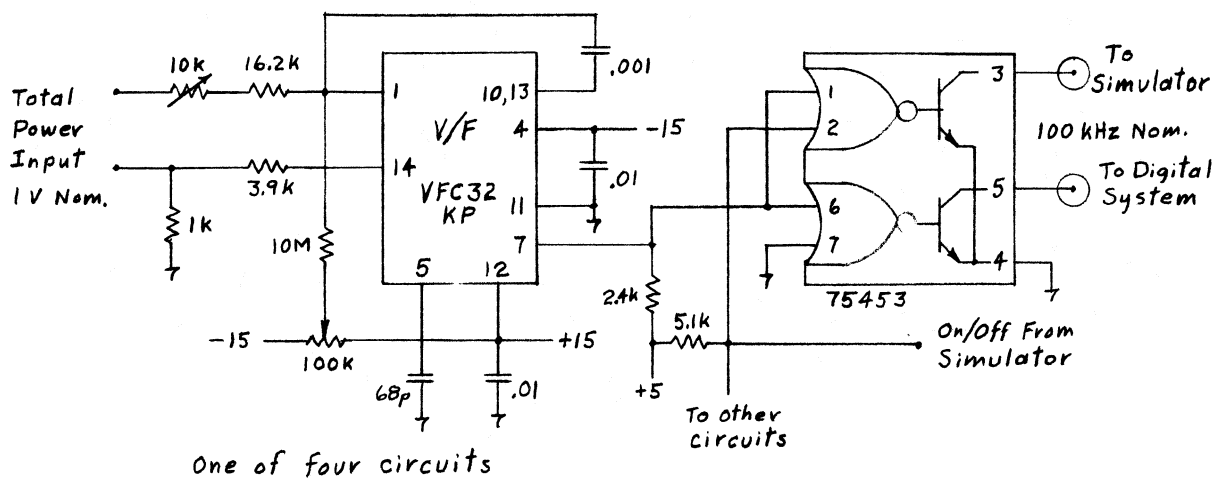


FIGURE 6

OUTPUT SWITCH, AMP. & DETECTOR

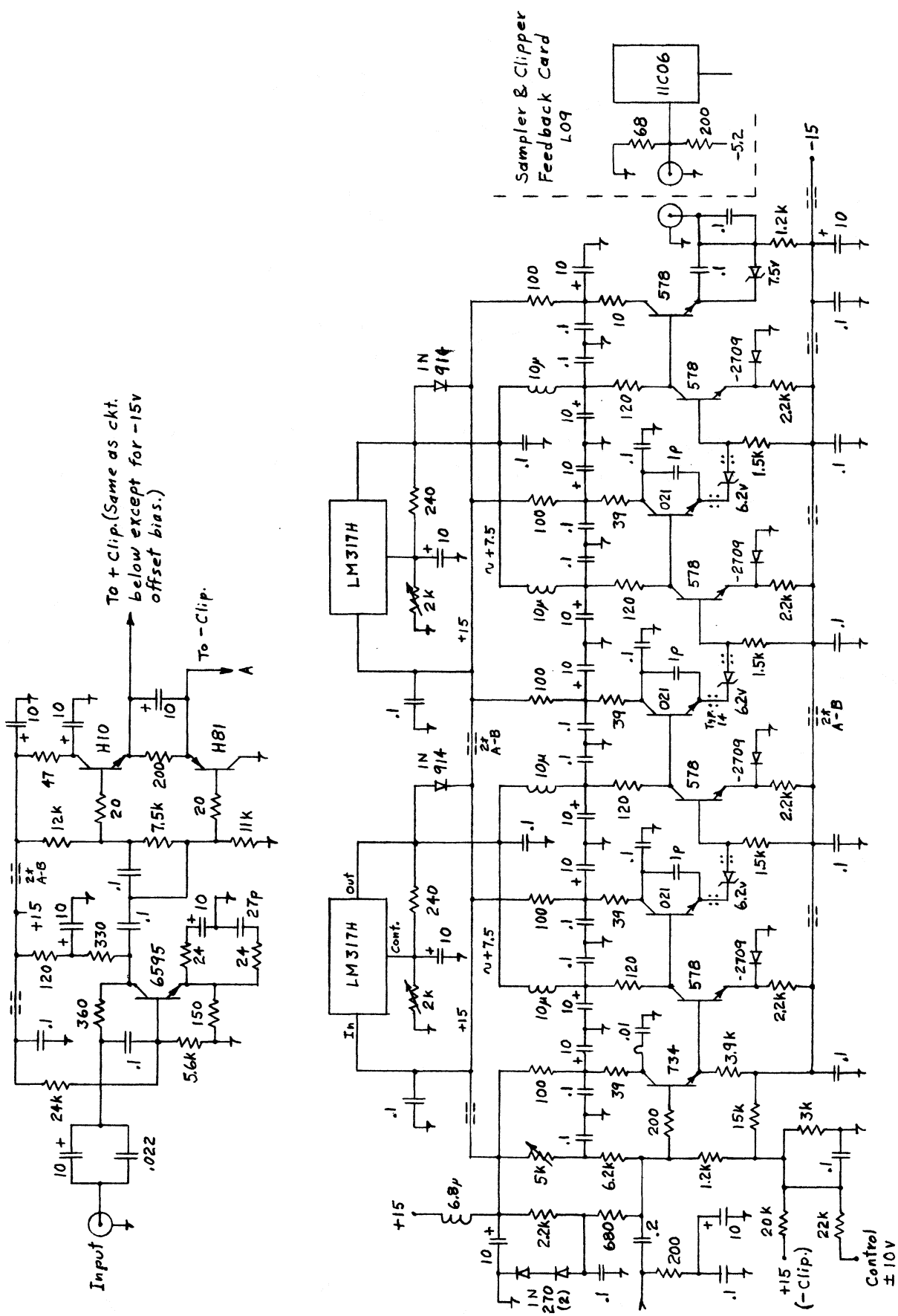


FREQUENCY MONITOR



TOTAL POWER V/F CONVERTER

FIGURE 7



TWO LEVEL CLIPPER

FIGURE 8

10-10-77
1-17-78

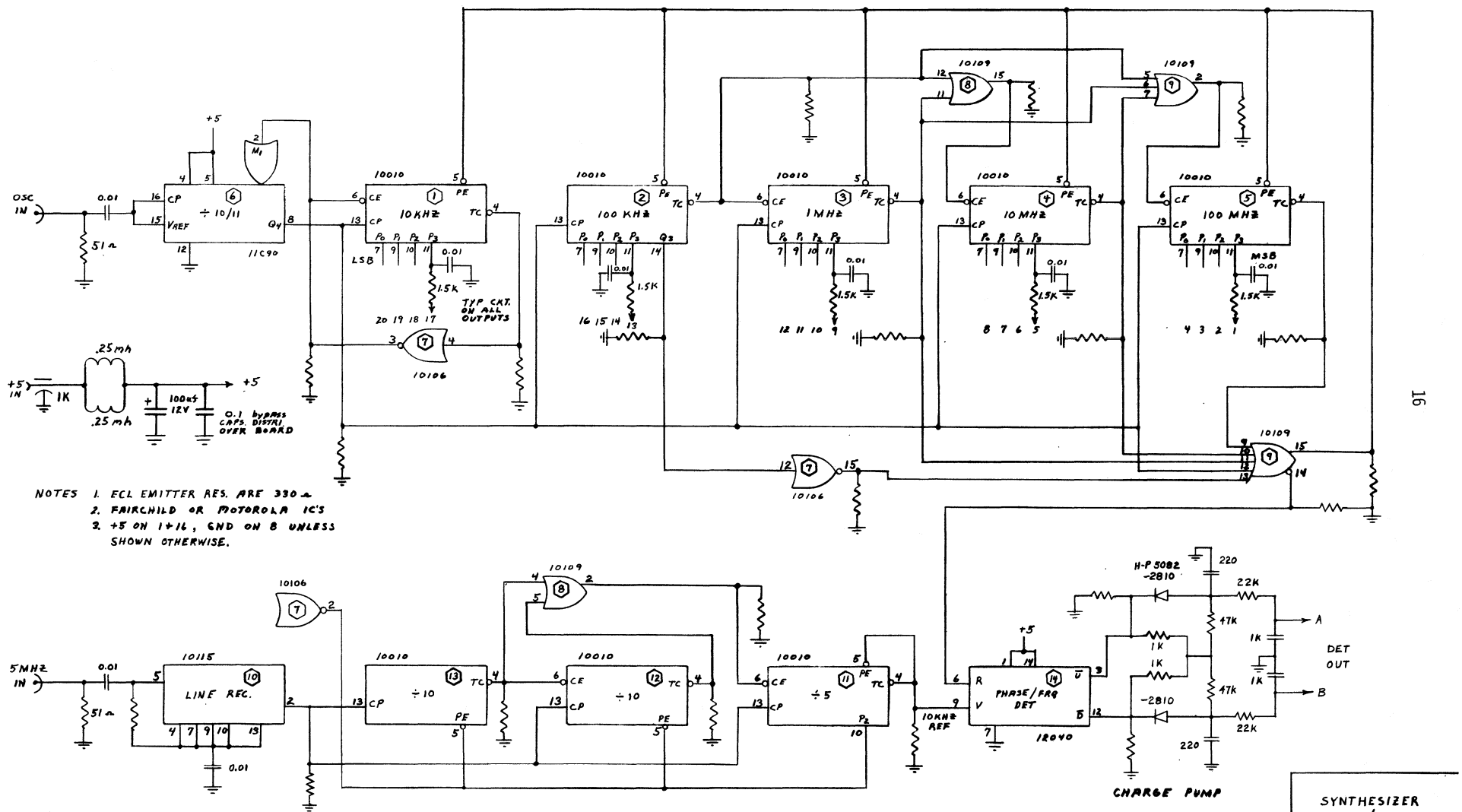


FIGURE 9

SYNTHESIZER COUNTER/DIVIDER

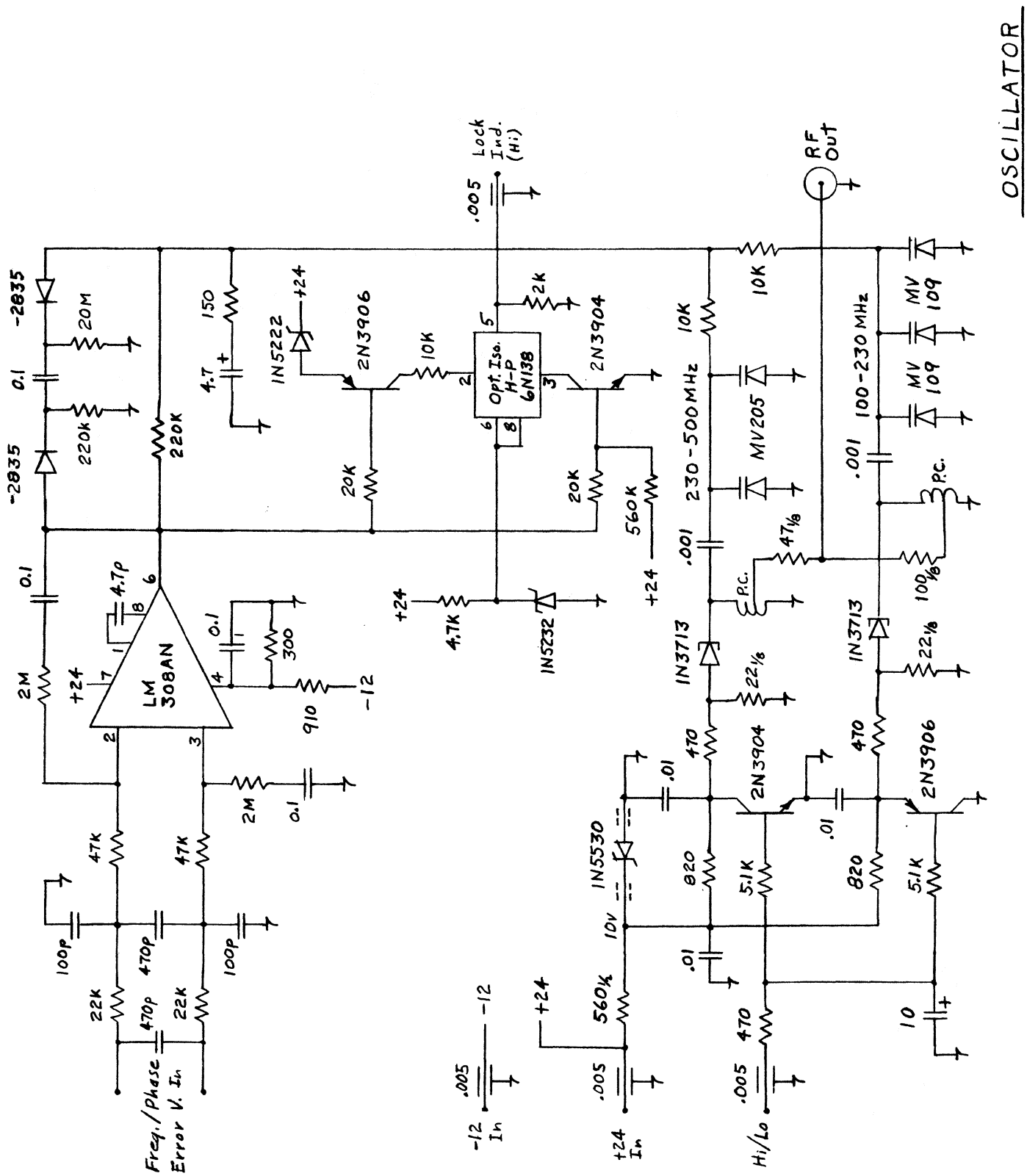
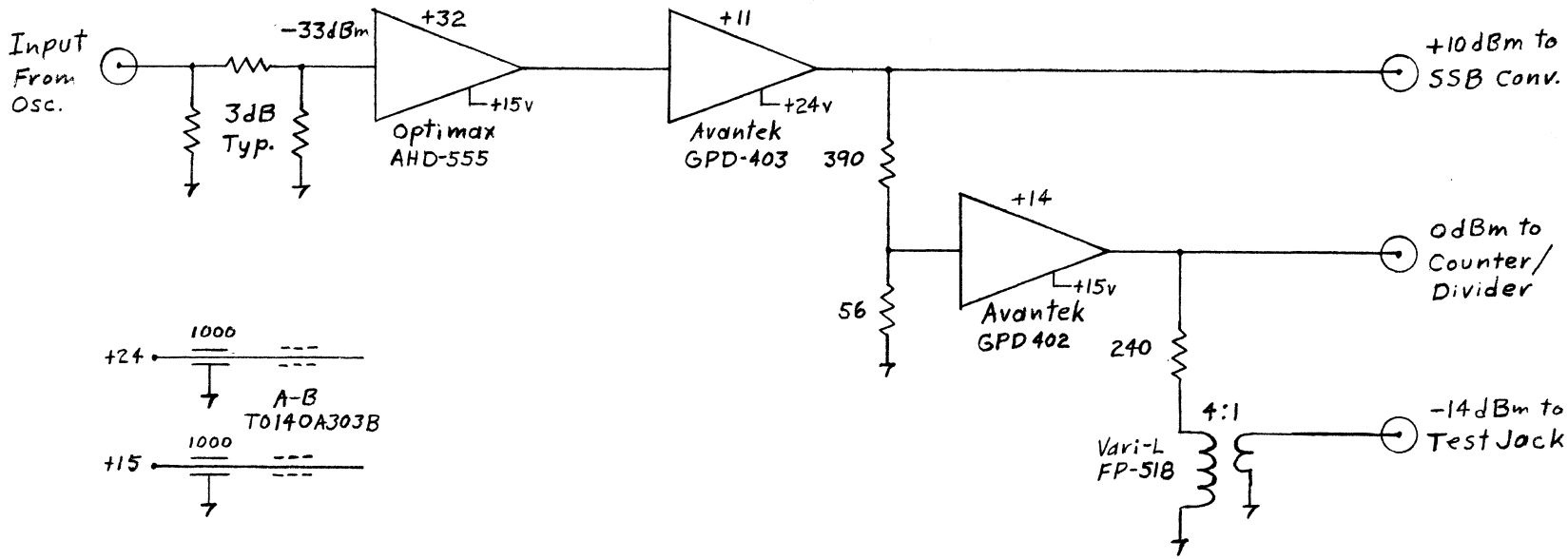

OSCILLATOR
RF OUT
Lock Ind. (Hi)
LM 308AN
Opt. Iso. H-P 6N138
2N3906
2N3904
IN5222
IN5232
IN5530
IN3713
MV205
MV 109
230-500 MHz
100-230 MHz
Freq./Phase Error V. In
-12 In
+24 In
Hi/Lo
P.C.

FIGURE 10



SYNTHESIZER BUFFER AMPLIFIER

FIGURE 11

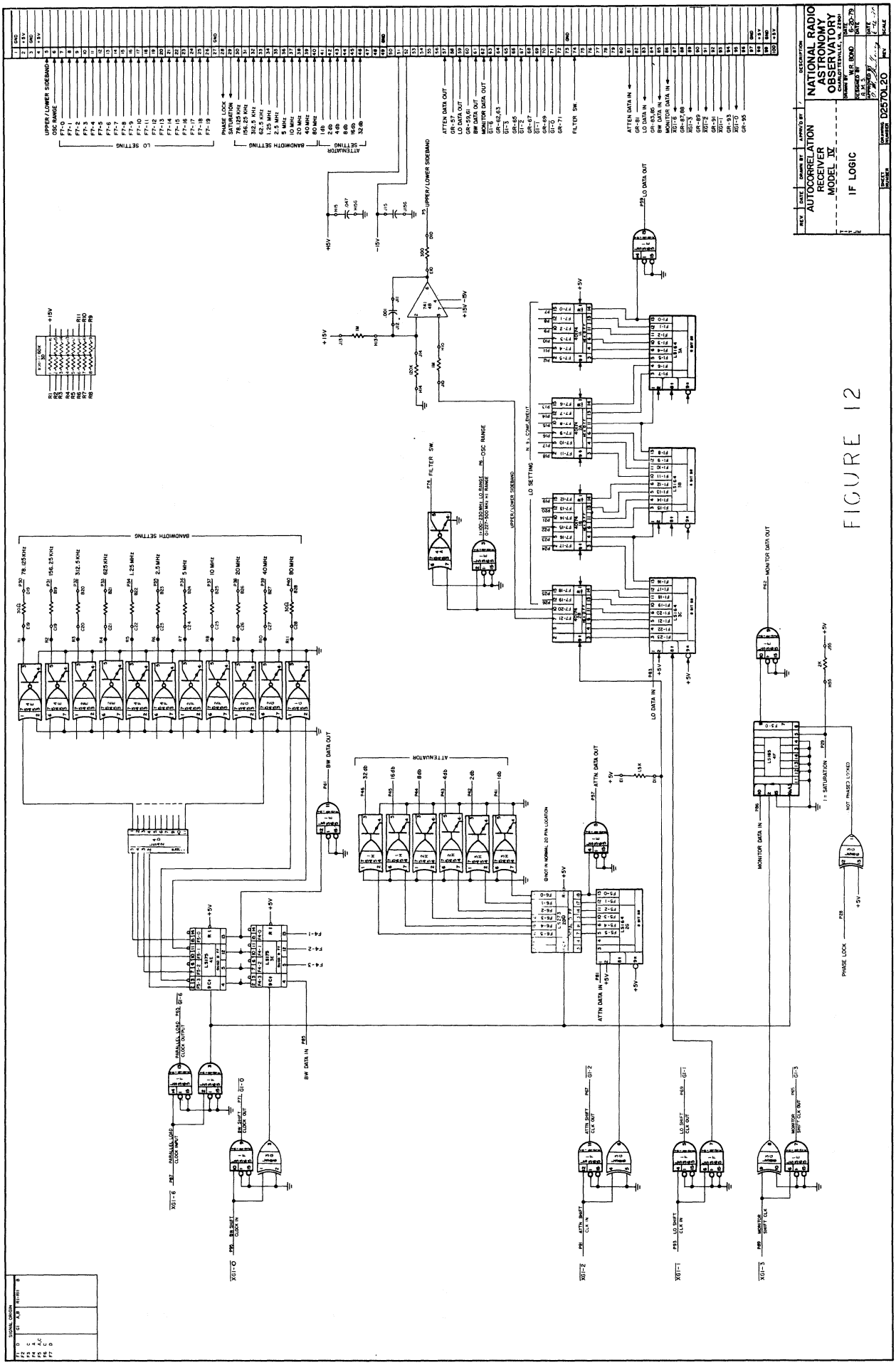

NATIONAL RADIO ASTRONOMY OBSERVATORY
AUTOCORRELATION RECEIVER MODEL III
IF LOGIC
02570L20
LO SETTING
BANDWIDTH SETTING
ATTENUATOR
PHASE LOCK SATURATION
ATTEN DATA OUT
LO DATA OUT
BW DATA OUT
MONITOR DATA OUT
FILTER SW
ATTEN DATA IN
LO DATA IN
BW DATA IN
MONITOR DATA IN
UPPER/LOWER SIDEBAND
OSC RANGE
LO DATA IN
MONITOR DATA OUT
ATTN DATA OUT
BW DATA OUT
ATTN DATA IN
BW DATA IN
MONITOR DATA IN
PARALLEL LOAD CLOCK INPUT
BW SHIFT CLOCK OUT
BW SHIFT CLOCK IN
ATTN SHIFT CLK OUT
ATTN SHIFT CLK IN
LO SHIFT CLK OUT
LO SHIFT CLK IN
MONITOR SHIFT CLK OUT
MONITOR SHIFT CLK
1= SATURATION
NOT PHASE LOCKED
PHASE LOCK
SIGNAL ORIGIN

FIGURE 12