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ADIOS –
ANALOG-DIGITAL INPUT OUTPUT SYSTEM
FOR APPLE COMPUTER

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ADIOS - Analog-Digital Input Output System for Apple Computer

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I. INTRODUCTION

ADIOS is a general purpose analog and digital input and output system for use with the Apple II Plus computer; a block diagram of the system is shown in Figure 1 and photographs of the ADIOS hardware and a complete Apple laboratory computer system are shown in Figures 2 and 3.

The system provides two .01% accuracy analog inputs denoted as AIN and BIN, two 16-bit accuracy analog outputs denoted as COUT and DOUT, six 1-bit TTL logic level digital inputs, and a 16-bit digital output which can be routed through an 8-bit bus driver, a 4-bit relay driver, or two solid-state relays. Three of the digital output bits can be used to control an 8-channel multiplexer on the BIN analog input. The hardware and software aspects of these functions are discussed together for each analog and digital input and output in subsequent sections of this report.

The A/D conversion is a slow integration method rather than a fast sampling type of conversion; the intention is to achieve high precision by averaging of noisy inputs. The integration is performed by counting of voltage-to-frequency (V/F) pulses for a duration denoted as COUNT time which is software controllable. After each integration the V/F pulses are not counted for a duration denoted as BLANK time which is also software controllable. In normal operation the ADIOS output analog and digital variables change near the beginning of BLANK time and transients caused by the change of these variables should decay before the

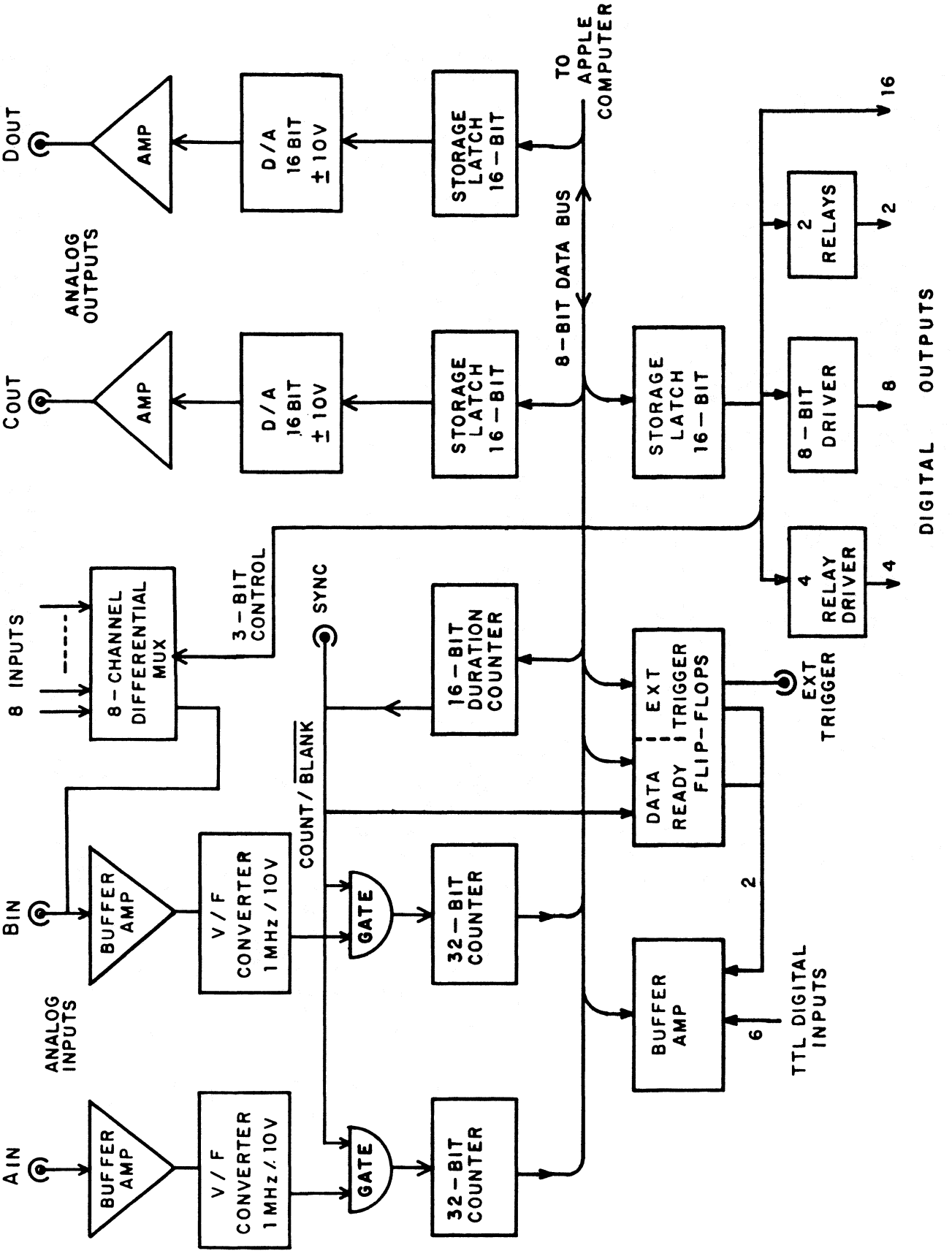


Fig. 1. ADIOS Block Diagram

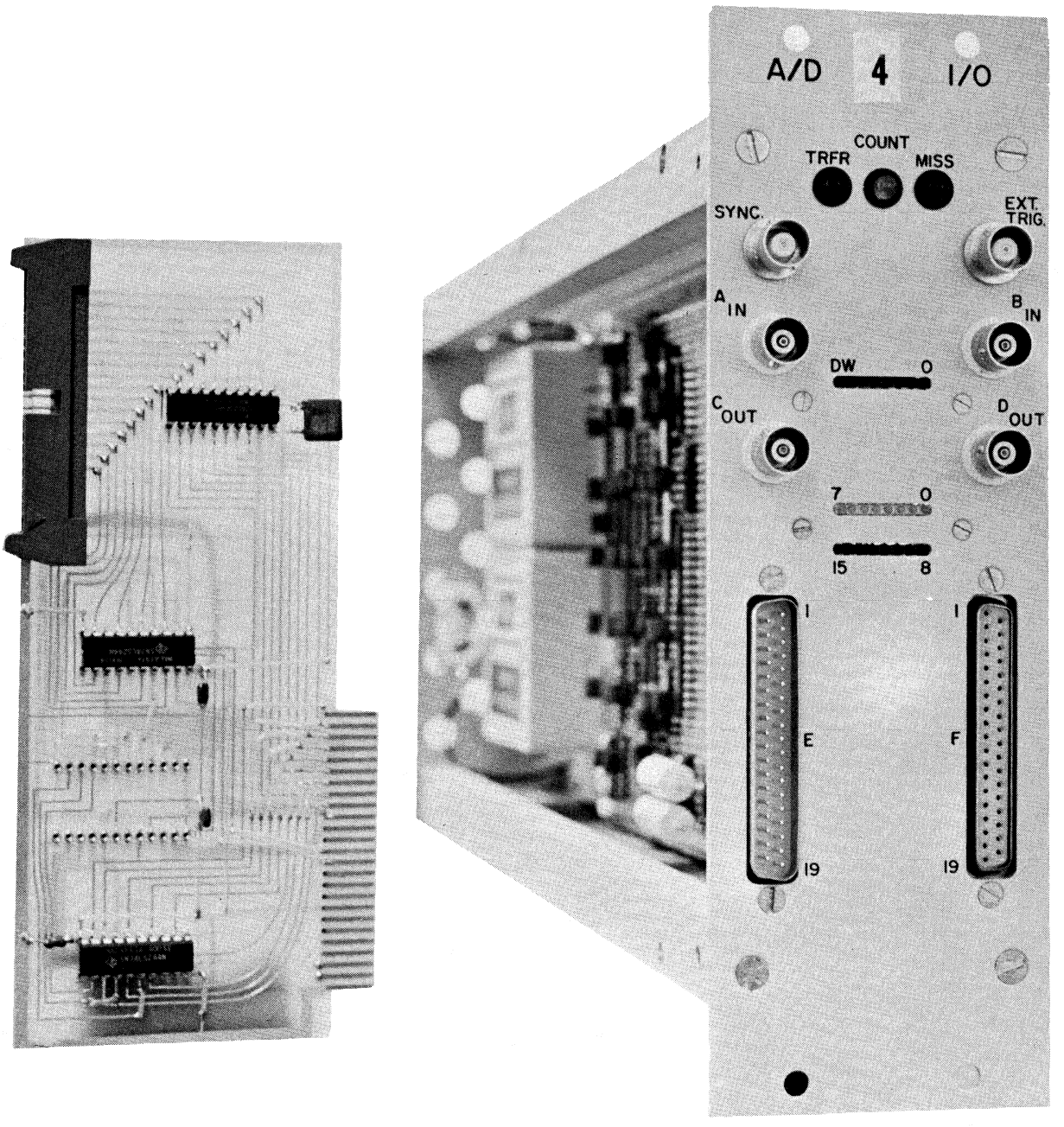


Fig. 2. ADIOS components - Apple I/O card and main module. The I/O card contains signal isolation drivers and a socket for a ROM containing future utility programs. Within the module are power supplies, V/F converters, counters, D/A converters, digital output drivers, and control logic.

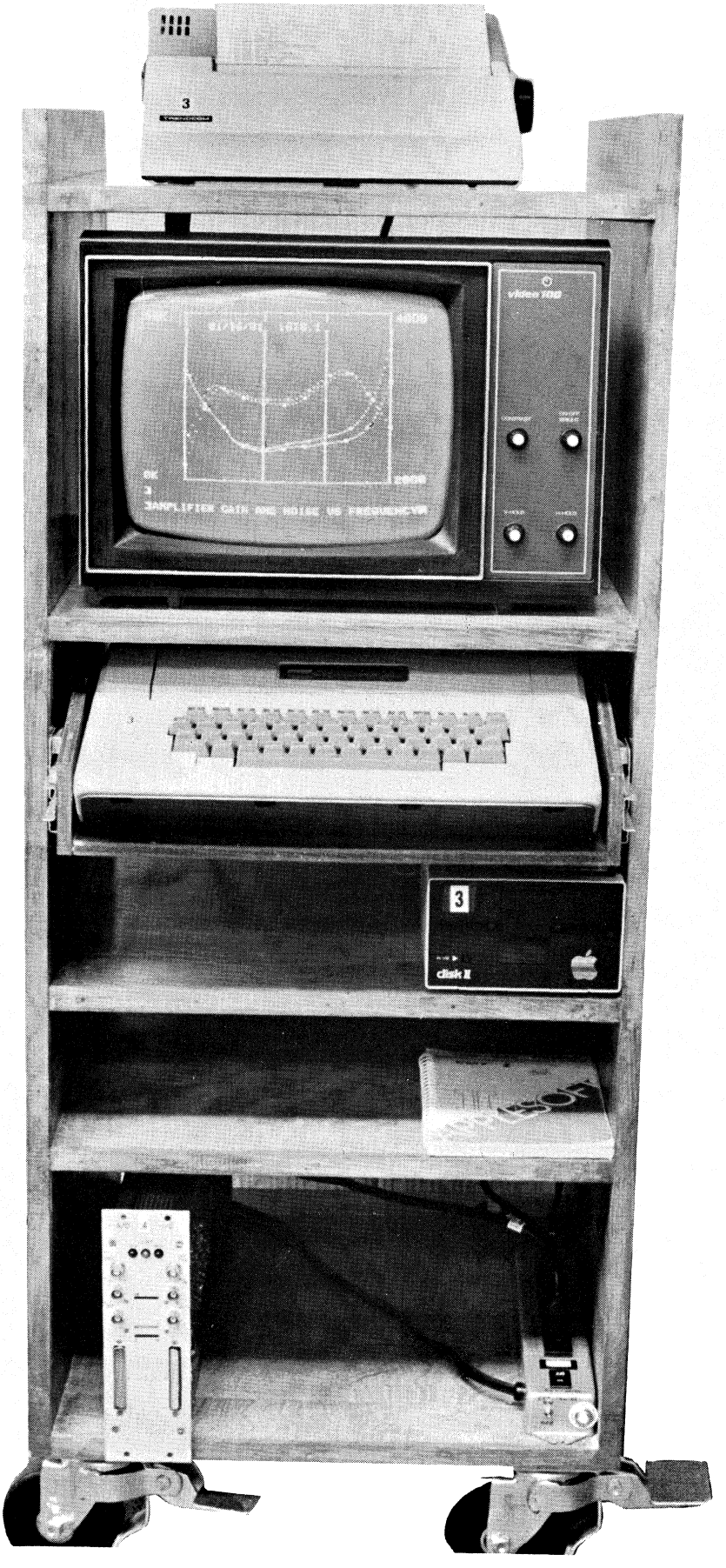


Fig. 3. Apple system on laboratory cart with ADIOS module on bottom shelf. A typical measurement of noise and gain of a microwave amplifier is displayed on the screen.

next COUNT time starts. The lower limits for COUNT and BLANK times are software dependent; practical limits are of the order of 100 milliseconds for a BASIC program. The maximum duration is approximately 65 seconds.

Before ADIOS can be used it must be initialized by a subroutine such as the machine language program, ADIOS INITB, described in Appendix 1. The initialization subroutine sets the values of COUNT and BLANK and also directs a programmable integrated circuit, the AM9513, which performs all counting, to the desired mode of operation. The subroutine is loaded from disk and executed with the following calling program:

```
310  REM  NEXT INITILIZES A/D INTERFACE  AND SETS UP INTEGRATION CYCLE
320  GOSUB 7000: REM  POKE COPY OF ADIOS-INITB
330  REM   BLOADED 85 = $55 BYTES IN 7986 = $1F32
340 COUNT = 400:BLANK = 80
350 CS = 10 / COUNT
360 COUNT = COUNT / 10:BLANK = BLANK / 10
370 CH% = COUNT / 256:BL% = BLANK / 256
380  REM  NEXT LOADS COUNT AND BLANK TIMES INTO ADIOS
390  POKE 7988,COUNT - 256 * CH%: POKE 7989,CH%
400  POKE 7990,BLANK - 256 * BL%: POKE 7991,BL%
410  CALL 8018: REM  STARTS ADIOS
```

To change COUNT or BLANK, change line 340 and then execute lines 340 thru 410; to restart after removal of ADIOS power, execute CALL 8018.

All of the Apple address locations associated with ADIOS are summarized in Table I. It is assumed in this Table that ADIOS is plugged into peripheral slot 3 of the Apple; if slot N is used, substitute N+8 for the third character of the hex address (=B for N=3) or add 16(N-3) to the decimal address. These addresses may be accessed by machine language programs (i.e., ADIOS INITB) or by BASIC programs using PEEK and POKE. Analog and digital output are accomplished by POKE'ing bytes into the appropriate registers; the details for doing this are discussed in IV and VI of this report. Digital input is also accomplished in a straightforward manner by PEEK'ing at address 49335. Analog input is slightly more

```
4325  REM NEXT PROGRAM LINES READ ANALOG INPUT COUNTERS
 .
 .    (See III for details)
 .
 .
4400  RETURN: REM COMPUTER MAY NOW DO OTHER TASKS BUT MUST RETURN TO
      4250 BY END OF COUNT TIME
```

Five indicator LED's on the ADIOS front panel indicate the status of initialization and synchronization. The large, green COUNT/BLANK LED is on during COUNT time after ADIOS has been initialized. Four other indicators, TRANSFER, MISS, DEAD, and WAIT, will function only if the program contains the following lines involving the CALL and MISSED DATA bits which are internal AMD9513 flip-flops accessible through the AMD9513 data register:

```
4205  REM NEXT 4 LINES SET UP CALL BIT TO OPERATE STATUS INDICATORS
4210  POKE 49342,20: REM ADDRESSES 9513 HD4
4220  ZZ = PEEK (49334): REM DUMMY PEEK TO ADVANCE 9513 DATA POINTER
4230  POKE 49334,174: REM SETS CALL BIT HIGH
4240  IF PEEK (49335) < 128 THEN 4500: REM IF DATA READY BIT IS ZERO
      PREVIOUS DATA WAS MISSED
      (Followed by WAIT statement and I/O lines previously described)
 .
 .
 .
4370  POKE 49342,19: REM ADDRESS 9513 HD4
4380  ZZ = PEEK (49334): REM DUMMY PEEK TO ADVANCE 9513 DATA POINTER
4390  POKE 49334,168: REM CLEAR CALL BIT
 .
 .
 .
4500  REM TURN ON MISSED DATA LIGHT
4510  POKE 49342,18: REM ADDRESS 9513 HD1
4520  ZZ = PEEK (49334): REM DUMMY PEEK TO ADVANCE 9513 DATA POINTER
4530  POKE 49334,172: REM CLOCKS MISSED-DATA ONE-SHOT
4540  POKE 49342,18: REM ADDRESS 9513 HD1
4550  ZZ = PEEK (49334): REM DUMMY PEEK TO ADVANCE 9513 DATA POINTER
4560  POKE 49334,168:  REM CLEARS MISSED-DATA CLOCK
4570  POKE 49335,0:  REM SET DATA READY BIT
4580  GOTO 4250
```

Lines 4210, 4220, 4510, 4520, 4540, and 4550 are obscure code necessary because of a quirk of the Apple POKE statement and also the 9513 addressing system. The Apple POKE command causes a PEEK followed by a POKE to be executed; the PEEK

causes the 9513 to advance its data pointer register. Thus a lower 9513 register must first be addressed to POKE into the desired address.

With the inclusion of the above lines TRANSFER lights for 0.5 seconds after each data transfer, MISSED DATA lights for 0.5 seconds if an integration is not read by the Apple, and WAIT is on while the Apple is waiting for the DATA READY bit.

III. ANALOG INPUT

A block diagram of the analog input system was given in Figure 1; detailed schematics and data sheets are included at the end of this report.

Inputs AIN and BIN are through front-panel BNC jacks or connector pins E30-33 as described in Table II. Inputs to BIN may also be through an 8-channel differential multiplexer with pins E1-16 as described in Table II. The multiplexer is addressed by bits 5(LSB), 6, and 7(MSB) of the digital output byte, address 49333. Input resistance is 1000 megohms differential and common mode for inputs in the range $\pm$ 14 volts. Common mode rejection is > 75 db for common mode voltage within $\pm$ 10 volts. The inputs are protected against overvoltage.

The full scale range of the analog inputs are controlled by two internal switches (see location drawing) for each input as follows:

SWITCH S1 or S3	SWITCH S2 or S4	V/F LOWER LIMIT 0 HZ	V/F UPPER LIMIT 1 MHz
OPEN	CLOSED	OV	+ 10.000 V
CLOSED	OPEN	- 10.000 V	+ 10.000 V

(The switch lever should be pushed towards the red dot for positive-only operation.) Thus each mode requires a different scaling in the program to convert counts to volts. The zero drift for the bipolar modes is typically 0.6 mV/°C and is much greater than the 0.01 mV/°C typical zero stability of the 0 to +10V range.

TABLE II - Pin Assignments for Front-Panel Connectors

E is Male - Cinch DC-37P

PIN	FUNCTION
E1	B0H
E2	B0L
E3	B1H
E4	B1L
E5	B2H
E6	B2L
E7	B3H
E8	B3L
E9	B4H
E10	B4L
E11	B5H
E12	B5L
E13	B6H
E14	B6L
E15	B7H
E16	B7L
	ANALOG INPUTS TO MUX
E17	AIN GAIN PROGRAMMING
E18	
E19	MUX ENABLE
E20	BIN GAIN PROGRAMMING
E21	
E22	+15 VOLTS
E23	GROUND
E24	-15 VOLTS
E25	DI1
E26	DI2
E27	DI3
E28	DI4
E29	DI5
	DIGITAL INPUTS
E30	AIN H
E31	AIN L
E32	BIN H
E33	BIN L
E34	COUT H
E35	COUT L
E36	DOUT H
E37	DOUT L

F is Female - Cinch DC-37S

PIN	FUNCTION
F1	DO0
F2	DO1
F3	DO2
F4	DO3
F5	DO4
F6	DO5
F7	DO6
F8	DO7
F9	DO8
F10	DO9
F11	DO10
F12	DO11
F13	DO12
F14	DO13
F15	DO14
F16	DO15
	DIGITAL OUTPUTS
F17	DO12 RELAY -
F18	DO12 RELAY +
F19	+5 VOLTS
F20	DI0 DIGITAL INPUT
F21	DO0
F22	DO1
F23	DO2
F24	DO3
F25	DO4
F26	DO5
F27	DO6
F28	DO7
	DRIVER OUTPUTS
F29	DRIVER ENABLE
F30	RELAY B+
F31	DO8
F32	DO9
F33	DO10
F34	DO11
	RELAY DRIVER
F35	GROUND
F36	DO11 RELAY -
F37	DO11 RELAY +

The full scale sensitivity of the analog inputs can also be increased by adding resistors between pins E17 and E18 for AIN and E20 and E21 for BIN. This increases the gain of the AD522 input amplifier by a factor of 1 + 200K/R where R is the value of the added resistor. In later versions of ADIOS, the internal bipolar/unipolar switches and also switches to give 1 volt full scale will be added to the front panel.

The 1 MHz V/F converter outputs are counted by 32-bit counters within the AM9513. At the end of COUNT time the contents of these counters are automatically transferred into 16-bit HOLD registers within the AM9513. This assumes that the initialization program of Appendix 1 (appropriate for Free Run mode) is used. The AM9513 can also be programmed to allow transfer to the HOLD registers under software control. AIN is stored in HOLD 2 (LSW) and HOLD 3 (MSW); BIN is stored in HOLD 4 (LSW) and HOLD 5 (MSW). The HOLD registers are read out by POKE'ing appropriate addresses into the AM9513 command register at address 49342 (see Table I). One byte at a time is then read by PEEK(49334) commands. The least-significant byte is read first and the AM9513 data pointer automatically advances to the most significant byte for the next PEEK(49334). (However, it does not automatically advance to the most significant word; this must be done with another POKE to 49342.) BASIC program lines to perform these tasks are given below:

```
510   MK = 256: MM = 65536: CS = 10/COUNT: CZ = 0: REM THESE ARE FOR 0
      TO +10V MODE
520   REM FOR -10V TO +10V MODE USE CS = 2*CS AND CZ = 10000

 .
 .
 .
 .
      (After DATA READY WAIT and output POKES)
4330  POKE 49342,18: REM ADDRESS 9513 FOR LSW OF AIN
4335  REM FOR BIN USE POKE 49342,20
4340  AIN = PEEK (49334) + MK*PEEK (49334)
4350  POKE 49342,19: REM ADDRESS 9513 FOR MSW OF AIN
4355  REM FOR BIN USE POKE 49342,21
4360  AIN = AIN + MM*PEEK (49334)
4365  REM MSB OF MSW NOT NEED FOR COUNT TIME < 16.77 SECONDS
4368  MV = CS*AIN - CZ: REM MV IS AIN IN MILLIVOLTS
```

IV. ANALOG OUTPUT

The interface contains two Datel/Intersil DAC-HP16BGC D/A converters (see data sheet) which directly provide ± 5 volt output with 16 bit resolution. These outputs are buffered and amplified X2 by an OP10-EY dual op-amp which has zero and gain trim adjustments. The two resulting ± 10 volt outputs are designated COUT and DOUT and are available on front-panel BNC jacks and also on pins E34 (COUT H), E35 (COUT L), E36 (DOUT H), and E37 (DOUT L) of the 37-pin E front-panel connector. The outputs can sense ground at the desired load but 100 ohms is presented by the output return lead to chassis ground.

COUT and DOUT are each accessed by two bytes within the Apple address space. If the interface card is plugged into slot 3, the addresses are given in Table I. The output voltage vs bit configuration is given in Table III.

The analog outputs are controlled by the computer POKE'ing bytes into the appropriate registers of Table I; two bytes must be POKE'ed for each output. A BASIC subroutine which converts a BASIC floating point variable, MV, equal to the desired output of COUT in millivolts, to the required bytes, ML% and MH%, is illustrated below:

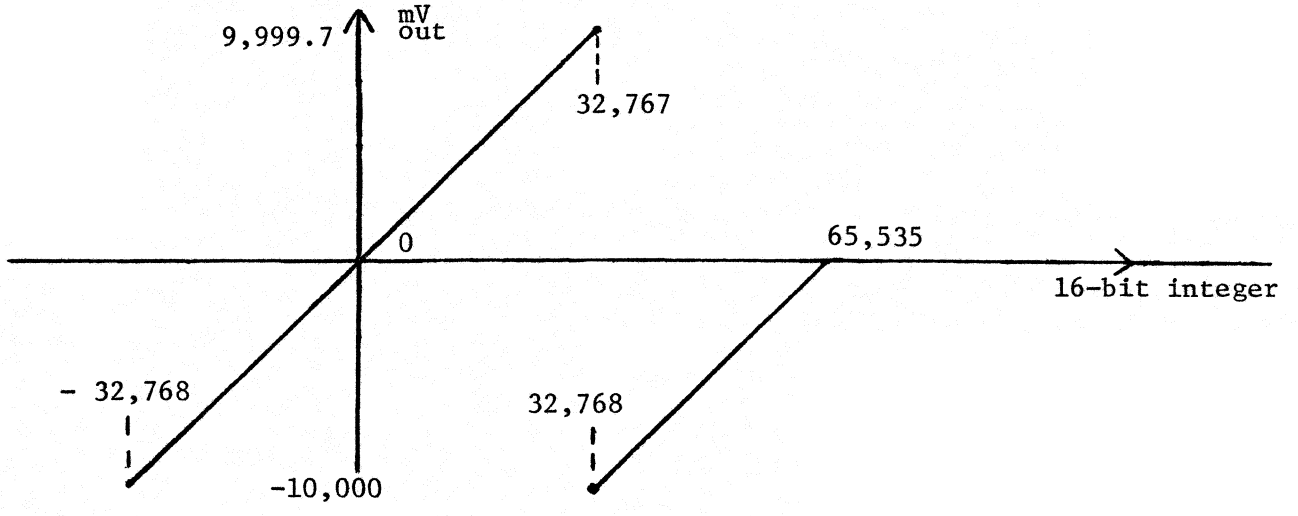
```
20000  REM D/A SERVICE ROUTINE
20010  IF MV > 9999.7 THEN MV = 9999.7
20020  IF MV < -10000.  THEN MV = -10000
20040  MT% = 3.2768*MV
20050  MH% = MT%/256:  ML% = MT% - 256*MH%
20060  POKE 49328,ML%: REM POKE 49330 FOR DOUT
20070  POKE 49329,MH%: REM POKE 49331 FOR DOUT
20080  RETURN
```

V. DIGITAL INPUT

The six digital input lines are available on pins F20 (LSB, DI0) and E25 (DI1) thru pin E29 (MSB, DI5) of the 37-pin front-panel connectors. Input is standard TTL

TABLE III. D/A Converter Bit Configuration

Output Voltage, mV	Hex LSB	MSB	Decimal
9,999.7	FF	7F	32,767
5,000.0	00	40	16,384
0.00	00	00	0
- 0.30	FF	FF	65,535 or -1
- 5,000.0	00	C0	49,152 or -16,384
- 9,999.7	01	80	32,769 or -32,767
- 10,000.0	00	80	32,768 or -32,768



logic levels; a "1" is > +2.0 volts (drawing < 40 μA at 2.4V) and "0" is < 0.8 volts (supplying < 1.6 mA at 0.4 volts). The inputs may be inverted by installing a 74LS367A in position 8E in place of the 74LS368A. No storage flip-flops are provided; the computer senses the input lines at the time a PEEK(49335) is executed. This time can be controlled by waiting for the DATA READY bit thru WAIT 49335,128,128 as discussed in II. The state of the input lines is indicated by the 6 right-most white bar-LED's on the ADIOS front-panel; a lighted LED indicates a "1" input.

VI. DIGITAL OUTPUT

The 16-bit digital output word is stored in two bytes; each byte is in a 74273 octal flip-flip IC within ADIOS. One byte, bits DO0 - DO7, is controlled by a POKE 49332,B command where B is the decimal value of the byte (B = 0 to 255); these bits are available on pins F1 - F8 of the F front-panel connector. The second byte, bits DO8 - DO15, is addressed at 49333, and is available on pins F9 - F16. The flip-flop outputs can sink 16 mA at 0.4V and drive 0.8 mA at 2.4V. All 16 bits are indicated by front-panel bar LED's; a lighted LED indicates a "1".

The flip-flop outputs are connected to three types of drivers within ADIOS. Bits DO0 - DO7 drive an octal tri-state bus driver, the 74LS241 in location 7C (substitute 74LS240 to invert bits), with outputs on pins F21 - F28. The tri-state driver is held disabled by a 4.7K resistor to +5V on its $\bar{G}$ input; the driver may be enabled by connecting pin F29 to pin F35 (ground).

Bits DO8 - DO11 drive a quad relay driver, the UHP-507, which can switch 100 volts at 250 mA output pins are F31 - F34. The driver contains transient protection diodes which should be connected to the positive relay supply voltage thru pin F30. The negative relay supply voltage should be connected to pin F35 which is tied to chassis ground.

Bits DO11 and DO12 drive two solid-state relays, Teledyne 643-1, which can switch 60 volts at 200 mA. The switch terminals are available on pins F36(-) and F37(+) for DO11, F17(-), and F18(+) for DO12. The switch terminals may float up to 2500 volts with respect to ground but the voltage polarity across the open contacts must be as indicated. Other Teledyne relays which are pin-compatible and handle AC voltages are described in a data sheet in IX.

The BIN analog multiplexer is connected to bits DO13 - DO15. These bits may also be used as digital outputs (pins F14 - F16) but do not feed a driver.

VII. CALIBRATION

ADIOS contains 12 4-turn pots, located as shown in Figure 4, which adjust zero and gain for the two analog outputs (4 adjustments) and two analog inputs, each having two ranges (8 adjustments). It is most convenient to first calibrate the analog outputs using an accurate 4-digit DVM and then use these outputs as voltage standards for input calibration. A program such as ADIOS TEST, listed in Appendix 2, is useful as it allows the outputs to be set by keyboard entry and displays the input readings.

Output calibration is as follows:

1. Command output to 0; adjust COUT ZERO and DOUT ZERO for 0 $\pm$ 1 mV output.
2. Command output to 9900 mV; adjust COUT GAIN and DOUT GAIN for 9900 $\pm$ 2 mV output.
3. To check operation, command output to -9900 mV; outputs should be -9900 $\pm$ 3 mV.

The 0 to +10 volt input range should be calibrated next as these adjustments also affect the $\pm$ 10 volt range adjustments (which do not affect 0 to +10 calibration). The 4 internal DIP switches should be set in the red-dot position

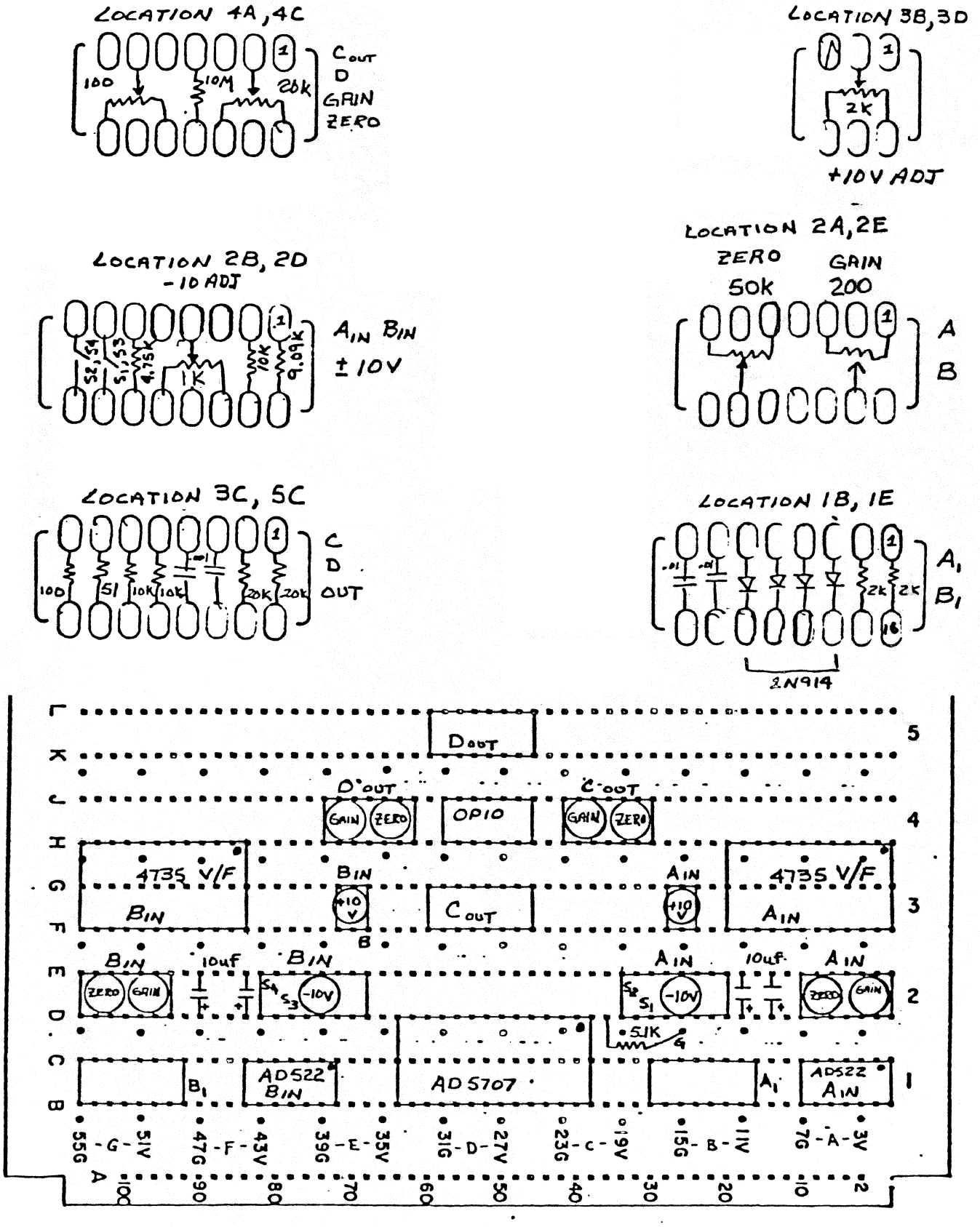


Fig. 4. Analog component and calibration adjustment location guide. A digital IC layout is given in Appendix 4.

(S2 and S4 open, S1 and S3 closed) and then proceed as follows:

4. Command output to 50 mV; adjust AIN and BIN ZERO for 50 $\pm$ 1 output display.

5. Command output to 9900 mV; adjust AIN and BIN GAIN for a 9900 $\pm$ 2 display.

6. Repeat 4, above.

Next, the -10 volt to +10 volt range is calibrated; the internal DIP switches should be set away from the red-dot position. The ADIOS TEST program scales input counts assuming the 0 to +10 volt range; this is accounted for in the desired outputs described below:

7. Command output to -9900 mV and adjust the -10V pots for an output display of 50 $\pm$ 1.

8. Command output to 9900 mV and adjust the +10V pots for a display of 9950 $\pm$ 3.

9. Repeat 7, above.

After completion of calibration, operation can be checked by putting DIP switches in the red-dot position and running the RAMP mode of ADIOS TEST. Finally, the DIP switches should be set for the desired mode of operation; typically this will be with AIN in the 0 to +10 mode and BIN in the bipolar mode.

Appendix 1. Initialization Program - ADIOS INITB

ADIOS-INITB is a binary (machine language) program that initializes the AM9513. This is necessary in order for ADIOS to input analog signals and control synchronization. The program loads sixteen, 16-bit internal registers of the 9513 with certain values dictating the exact internal configuration of the AM9513. Two of the registers are loaded with values that control the duration of COUNT and BLANK. This initialization program also arms the counters to commence operation of the COUNT-BLANK cycle.

In order to use "ADIOS-INITB," one must first put it on a disk. This can be done by typing the object code (shown in Fig. 5) into memory with the SYSEM MONITOR and then issuing a "BSAVE ADIOS-INITB, A$1F32, L$55" command.

Once the program is in memory, one can modify the COUNT and BLANK initialization values. Table IV shows the addresses of ADIOS-INITB which contain these values that are loaded into the AM9513 upon execution ("CALL 8018"). Refer to the BASIC program listing, line 310, in Appendix II, for information on how to utilize ADIOS-INITB from a BASIC program.

Figure 5 contains an assembly listing of ADIOS-INITB. The actual binary program is enclosed in a box.

TABLE IV. ADIOS-INITB Initialization Addresses

Address	Contents*
7988	COUNT time MSB
7989	COUNT time LSB
7990	BLANK time MSB
7991	BLANK time LSB

*values are in units of 10 mS.

```
Hex.  Machine code listing
addr.
                        1000
                        1010 *  G.WEINREB    8/11/80    "ADIOS-INITB"
                        1020 *  INITIALIZE 9513 ROUTINE;   ASSEMBLER: "ASMDISK 4.0"
                        1030 *     CARD IN SLOT 3
                        1040 *
                        1043       .OR $1F32
                        1047 *  OBJECT CODE IS 85=$55 BYTES PLACED IN ADDRESS $1F32 -
                        1050 *---------9513 I/O ADDRESSES-----
C0BE-                   1060 COMM .EQ $C0BE      COMAND REGISTER
C0B6-                   1070 DATA .EQ $C0B6      DATA REGISTERS
                        1080 *
                        1090 *------DATA FOR 9513'S REGISTERS--
                        1100 *-----DATA IN TABLE IS IN IN FORMAT WHERE LSB IS FIRST
1F32- E6 0F             1110 CM1   .HS E60F  <]  TEST MODE
1F34- 64 00             1120 LD1   .HS 6400      1 SECOND COUNT
1F36- 64 00             1130 HD1   .HS 6400      1 SECOND BLANK   > Modifiable
1F38- AD 42             1140 CM2   .HS AD42  <]
1F3A- 00 00             1150 LD2   .HS 0000
1F3C- 00 00             1160 HD2   .HS 0000
1F3E- A8 83             1170 CM3   .HS A883  <]
1F40- 00 00             1180 LD3   .HS 0000
1F42- 00 00             1190 HD3   .HS 0000
1F44- AD 84             1200 CM4   .HS AD84  <]
1F46- 00 00             1210 LD4   .HS 0000
1F48- 00 00             1220 HD4   .HS 0000
1F4A- A8 65             1230 CM5   .HS A865  <]
1F4C- 00 00             1240 LD5   .HS 0000
1F4E- 00 00             1250 HD5   .HS 0000
1F                      1260
1F50- 00 90             1280 MAMO  .HS 0090  <]  MASTER MODE REGISTER
                        1290 *
                        1300 *---------INIT. PROGRAM--------*
                        1310 *
1F52- A9 FF             1320 INIT LDA #$FF
1F54- 8D BE C0          1330      STA COMM       MASTER RESET
1F57- A9 01             1340      LDA #$01
1F59- 8D BE C0          1350      STA COMM       SET DATA POINTER
                        1360 *--------LDA REGISTERS-------*
1F5C- A2 00             1370      LDX #$00       CLR X
1F5E- BD 32 60          1380 BEGN LDA CM1,X      GET DATA
1F61- 8D B6 C0          1390      STA DATA       PUT IN 9513 REG:STER
1F64- E8                1400      INX
1F65- A9 33             1410      LDA #$33       CLR Z FLAG
1F67- E0 1E             1420      CPX #30        FINISHED?
1F69- F0 03             1430      BEQ DONE       IF SO, END
1F6B- 4C 5E 60          1440      JMP BEGN       DO IT AGAIN !
                        1450 *-----SET MM REGISTER-------*
1F6E- A9 17             1460 DONE LDA #$17
1F70- 8D BE C0          1470      STA COMM       SET DATA POINTER TO MM REGISTER
1F73- AD 50 60          1480      LDA MAMO
1F76- 8D B6 C0          1490      STA DATA       PUT IN MM REG.
                        1500
1F79- AD 51 60          1510      LDA MAMO+1
1F7C- 8D B6 C0          1520      STA DATA       PUT IN MM REG
                        1530 *-------ARM COUNTERS-------*
1F7F- A9 7F             1540      LDA #$7F
1F81- 8D BE C0          1550      STA COMM       ARM COUNTERS
1F84- 60                1555      RTS            END OF PROGRAM
                        1560      .EN            END OF INIT
```

"<]" values control the internal configuration of the AM9513.

Fig. 5. ADIOS-INITB Assembly Listing

```
40  REM    ADIOS TEST PROGRAM OF 3/23/81
50  GOTO 230: REM  INITIALIZE
100  PRINT "THIS PROGRAM ALLOWS A FIXED NUMBER OR A 0 TO 9900MV RAMP
 TO BE OUTPUT FROM C AND D. THESE SHOULD BE CONNECTED TO A AND B INPUTS.
 THE FIXED NUMBER OR RAMP IS ALSO APPLIED TO THE TWO DIGITAL OUTPUT
 BYTES.";
101  PRINT "DIGITAL INPUT BITS ARE ALSO READ AND DISPLAYED. COUNT=400
 AND BLANK =80;CHANGE IN 340 IF YOU WISH. PROGRAM  SCALING ASSUMES
 ADIOS IS IN 0 TO +10V   MODE (ALL DIP SWITCHES ON)"
104  PRINT
110  INPUT "RAMP(R) OR FIXED(F) INPUT? ";X$
112  PRINT
120  IF X$ = "R" GOTO 900
125  IF X$ = "F" GOTO 200
130  GOTO 110: REM    INVALID REPLY;TRY AGAIN

199  REM  FIXED OUTPUT ROUTINE
200  PRINT "FIXED OUTPUT. USE CONTROL C TO STOP;GOTO 200 TO CHANGE
 VALUE"
210  INPUT "MILLIVOLTS? ";F
211  GOSUB 4200
215 MV = AIN * CS:MY = BIN * CS
216 DG% = DI% - 128
218  PRINT F;"    ";MV;"    ";MY;"    ";DG%
220  GOTO 211: REM  REPEAT

230  REM  INITILIZATION ROUTINE
240 D$ =  CHR$ (4)
250  TEXT : HOME : PRINT
310  REM  NEXT INITILIZES A/D INTERFACE  AND SETS UP INTEGRATION CYCLE
320  GOSUB 7000: REM  POKE COPY OF ADIOS-INITB
330  REM   BLOADED 85 = $55 BYTES IN 7986 = $1F32
340 COUNT = 400:BLANK = 80
350 CS = 10 / COUNT
360 COUNT = COUNT / 10:BLANK = BLANK / 10
370 CH% = COUNT / 256:BL% = BLANK / 256
380  REM  NEXT LOADS COUNT AND BLANK TIMES INTO ADIOS
390  POKE 7988,COUNT - 256 * CH%: POKE 7989,CH%
400  POKE 7990,BLANK - 256 * BL%: POKE 7991,BL%
410  CALL 8018: REM  STARTS ADIOS
420  REM  GOSUB 5300 TO TURN ON PRINTER
430  REM  CALL 1013 TURNS OFF PRINTER
450  POKE 33,40: REM  NORMAL TEXT WINDOW
500  REM  CONSTANTS FOR DATA TRANSFER
510 MC = 3.2768:MJ = 128:MK = 256:MM = 65536
600  GOTO 100
899  REM

900  REM  RAMP TEST
910  PRINT "COUT AND DOUT WILL RAMP FROM 0 TO 9900MV IN A SELECTED
  STEP SIZE. IF AIN AND BIN DISAGREE WITH COUT AND DOUT BY MORE THAN
  DMAX=10MV (CHANGE IN 1010) THEN: "
911  PRINT
913  INPUT "ERROR MESSAGE IS NONE(0),BEEP(1), OR PRINTER LINE(2)? ";J
915  PRINT
920  INPUT "STEP SIZE IN MILLIVOLTS? ";ST
1005 NR = 0: REM  NR IS NUMBER OF READS SINCE LAST ERROR
1010 DMAX = 50
1020  FOR F = 000 TO 9900 STEP ST
```

```
1040  GOSUB 4200
1060 MV = AIN * CS:MY = BIN * CS
1070 DG% = DI% - MJ%: REM  SUBTRACT DATA READY BIT
1080  PRINT F - ST;"   ";MV;"   ";MY;"   ";DG%
1090  IF F = 0 GOTO 1220
1100 D =  ABS (F - ST - MV)
1110  IF D > DMAX THEN  CALL  - 211: GOSUB 1500
1150 E =  ABS (F - ST - MY)
1160  IF E > DMAX THEN  CALL  - 211: GOSUB 1500
1210 NR = NR + 1
1220  NEXT F
1230  GOTO 1010: REM  REPEAT RAMP

1500  REM  ERROR MESSAGE
1510  ON J GOTO 1587,1560
1520 NR = 0: RETURN : REM   NO MESSAGE IF J=0
1560  GOSUB 5300: REM  TURN ON PRINTER
1570  PRINT F - ST;"  ";MV;"  ";MY;"  ";DG%;"    ";NR
1580  CALL 1013
1587  CALL  - 1059: REM  BEEP!
1589 NR = 0
1590  RETURN : REM

4200  REM      DATA TRANSFER ROUTINE WITH PARAMETERS M(1 FOR NOISE
 SOURCE ON),F(OUTPUT TO LO) AND AIN (INPUT FROM RECEIVER)
4201 FC = F: IF F < 0 THEN FC = F + 20000
4202 MT = FC * MC: REM    OUTPUT F TO COUT
4203 MH% = MT / MK:ML% = MT - MK * MH%
4204 OH% = F / MK:OT% = F - MK * OH%: REM  F MODULO 256 FOR DIGITAL
 OUTPUT
4205  REM  NEXT 4 LINES TO SET UP 9513
4210  POKE 49342,20: REM   ADDRESSES 9513 HD4
4220 ZZ =  PEEK (49334): REM  ZZ IS DUMMY
4230  POKE 49334,172: REM  CALL BIT SET HIGH
4240  IF  PEEK (49335) < 128 THEN 4500
4250  WAIT 49335,128,128: REM   WAIT UNTIL  DATA READY BIT =0 AT BLANK
 TIME START
4260  POKE 49335,128: REM  RESET DATA    READY BIT
4270  POKE 49332,OT%: REM   OUTPUT BITS D00 TO D07
4280  POKE 49333,OT%: REM   OUTPUT BITS D08 TO D015
4290 DI% =  PEEK (49335): REM  DIGITAL INPUT
4300  POKE 49328,ML%: REM    COUT LSBYTE
4310  POKE 49329,MH%: REM   COUT MSBYTE
4313  POKE 49330,ML%: REM  COUT LSBYTE
4315  POKE 49331,MH%: REM   COUT MSBYTE
4320  REM  BLANK TIME MAY NOW END
4330  POKE 49342,18: REM  ADDRESS 9513   TO OUTPUT LSWORD OF AIN
4340 V1 =  PEEK (49334):V2 =  PEEK (49334)
4350  POKE 49342,19: REM  ADDRESS 9513   TO OUTPUT MSWORD OF AIN
4360 V3 =  PEEK (49334)
4365 AIN = V1 + MK * V2 + MM * V3
4366  POKE 49342,20: REM  ADDRESS 9513 FOR BIN
4368 Y1 =  PEEK (49334):Y2 =  PEEK (49334)
4370  POKE 49342,21
4372 Y3 =  PEEK (49334)
4376 BIN = Y1 + MK * Y2 + MM * Y3
4378  POKE 49342,20: REM    ADDRESS 9513   HD4
4380 ZZ =  PEEK (49334): REM  DUMMY PEEK
4390  POKE 49334,168: REM  CLEAR CALL BIT
4400  RETURN
4500  REM  TURN ON MISSED DATA LIGHT
```

```
4505  PRINT "MISSED DATA",COUNT,BLANK
4510  POKE 49342,18: REM   ADDRESS HOLD1
4520 ZZ =  PEEK (49334): REM  DUMMY
4530  POKE 49334,172: REM  CLOCKS MISSED DATA ONE-SHOT
4540  POKE 49342,18
4550 ZZ =  PEEK (49334)
4560  POKE 49334,168: REM  CLEARS MISSED DATA CLOCK
4570  POKE 49335,0: REM  CLEAR FLAG
4580  GOTO 4250
5299  REM

5300  REM       TURNS ON TRENDCOM 200 PRINTER
5310  REM  :GOTO 5400: REM  FOR APPLE PRINTER
5315  PR# 1: PRINT  CHR$ (0): REM  FIRST CHARACTER NOT PRINTED
5320  POKE 1913,6: POKE 1785,72: REM  MARGINS
5330  POKE 1657,80: REM  LINE LENGTH
5340  RETURN
5400  REM  TURN ON APPLE PRINTER
5410  PRINT  CHR$ (4);"PR#1"
5420 0$ =  CHR$ (17): REM  PRINT 0$ TO DUMP GRAPHICS
5430  POKE  - 12524,0: REM  BLACK ON WHITE PLOT
5440  POKE  - 12528,7: REM  DARK PRINT
5450  POKE  - 12527,8: REM  LEFT MARGIN
5460  RETURN
5999  REM

6000  REM  FORMATTED LIST
6005  POKE 33,33
6010  GOSUB 5300: REM  TURN ON PRINTER
6060  LIST
6065  PRINT : PRINT
6190  CALL 1013
6195  END : REM

6999  REM   NEXT READS ADIOS INITB AS DATA STATEMENTS
7000  FOR I = 7986 TO 8070: READ A: POKE I,A: NEXT : RETURN
7010  DATA 230,15,100,0,100,0,173,66,0,0,0,0,168,131,0,0,0,0,173,132,0,0,0
,0,168,101,0,0,0,0,0,144,169,255,141,190,192,169,1,141,190,192,162,0,189,5
0,31,141,182,192,232,169,51,224,30,240,3,76,94,31,169,23,141,190,192,173,8
0,31,141,182,192,173
7020  DATA  81,31,141,182,192,169,127,141,190,192,96,2,205
```

Appendix III - AM9513 Utilization

This section describes the AM9513 utilization in the "Free Run" mode of synchronization as described in Section II. The 9513 is a fairly complex chip described in a 26-page data brochure available from Advanced Micro Devices (5 pages of this are included in Appendix 5.H). This brochure should be read in order to understand this Appendix. However, these steps are not necessary unless modifications must be made to ADIOS.

Figure 6 shows the AM9513 configuration as used in the ADIOS "Free Run" mode; a timing diagram is shown in Figure 7. The first counter group is used to generate the COUNT/$\overline{\text{BLANK}}$ signal. The duration of COUNT is determined by the contents of the LOAD register where the duration of BLANK is determined by the HOLD register. When the counter is armed, it will be loaded with the contents of the LOAD or HOLD register (depending on the current state of OUT1) and begin counting down. When TC (0001) is reached, the output will begin to toggle and the counter will be reloaded with the other register and will commence to count down. This cycle will be repeated continuously until the counter is either reset or disarmed. The count-source of counter 1 is software selectable. However, in this manual, 100 HZ (F5) is used. This is derived from an external 1 MHz crystal oscillator which is divided down.

Counters 2, 3, 4, and 5 count the frequencies produced by the two V/F converters. Only counters 2 and 3 will be discussed since the operation of counters 4 and 5 is identical. Counters 2 and 3 are cascaded to provide 32 bits (4.295×10^9) of potential counting storage for the AIN frequency. With a 1 MHz V/F, one could take data for a maximum period of 71 minutes.

The frequency from the AIN V/F is inhibited by the C/$\overline{B}$ signal. The two counters use operation mode "Q" so that the gate ("SAVE") is used to place the counter contents into the HOLD register and the first pulse into the counter (from the input) is used to clear the counter by initiating a reload from the empty LOAD register. The "pulse adders" are used to provide this CLR (Clear) pulse. This all takes place within the 5 μs after COUNT time ends and is illustrated in Figure 8.

The computer can read the contents of the HOLD registers at anytime that is convenient until the next COUNT to BLANK transition occurs. OUT3 ($\overline{\text{MISS}}$ DATA) and OUT5 ($\overline{\text{CALL}}$) cna be in either the state of GND (CM bit 2 = 0) or HIGH IMPEDANCE (CM bit 2 = 1) and are controlled by the computer writing data into the AM9513 Command registers.

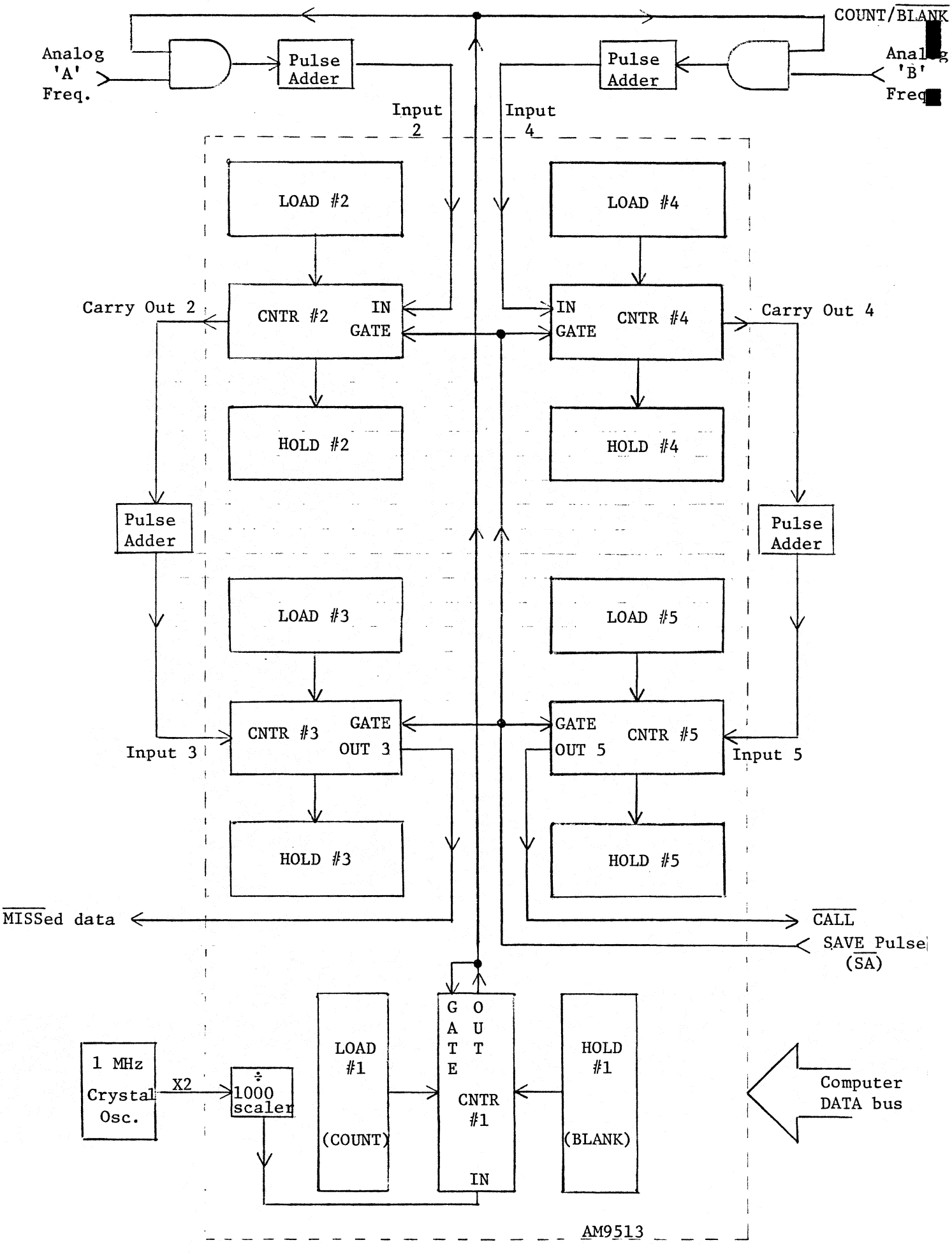
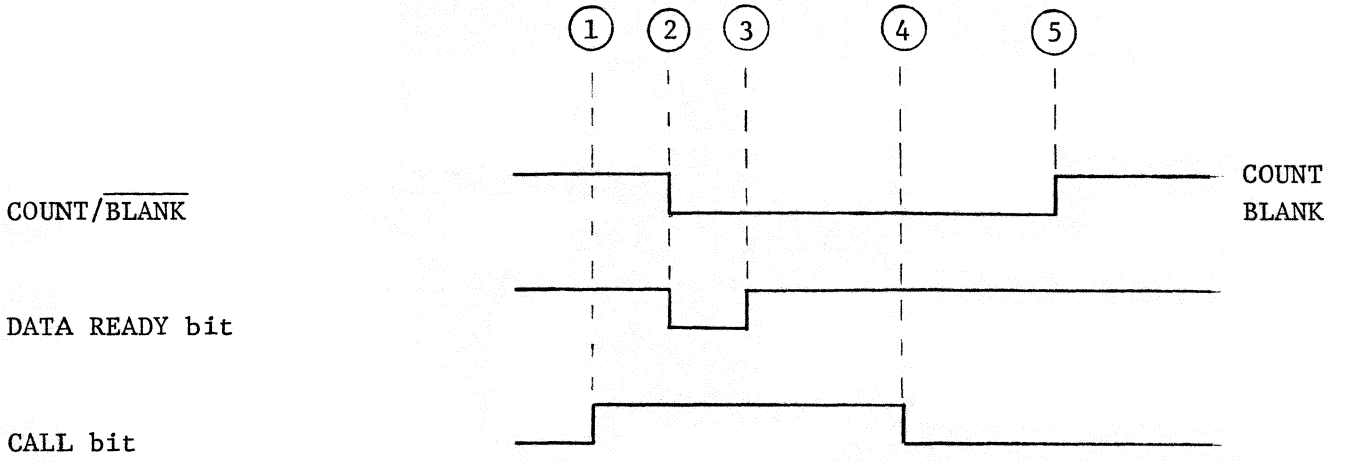


Fig. 6. AM9513 Configuration



(1) The computer sets the CALL bit and begins to wait until BLANK commences. If the DATA READY bit is low at this point, a cycle has been missed, (by the computer) and the MISSed Data line is pulsed. The WAIT LED is illuminated between the marks (1) and (2) .

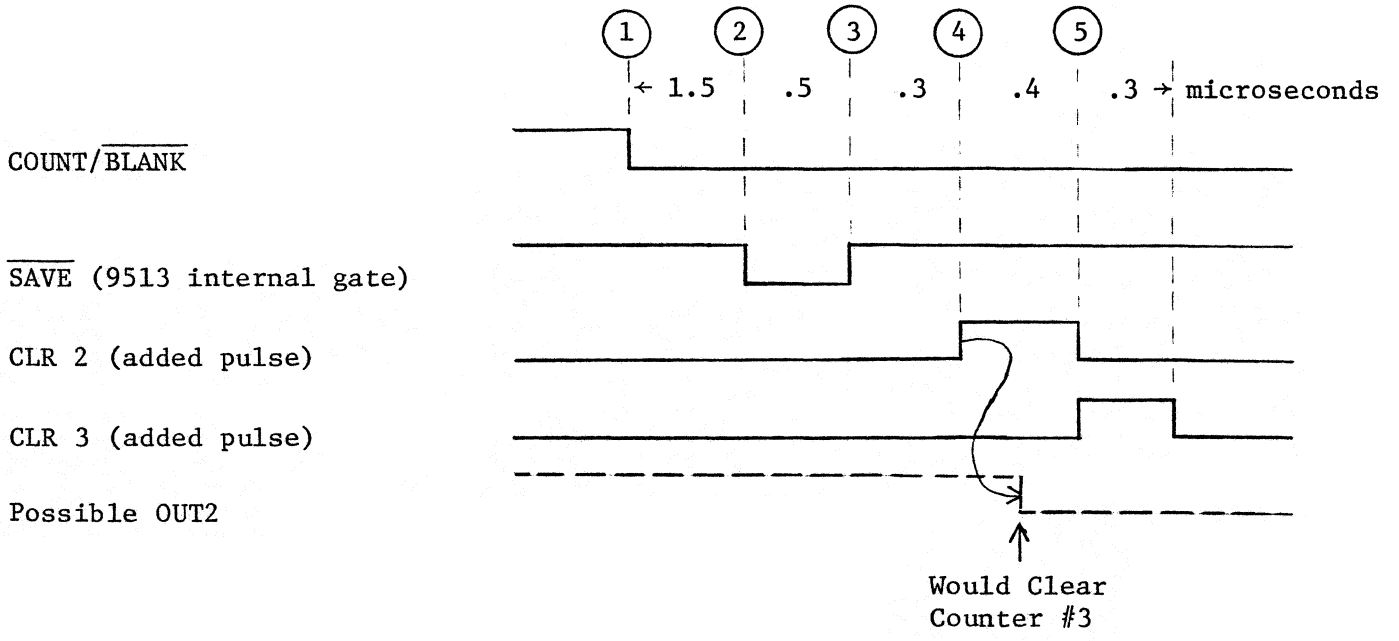
(2) The 4 counters stop counting, are saved and cleared, all within 5 μs. The DATA READY bit is set in order to tell the computer that it can begin outputting new data.

(3) The DATA READY bit is cleared under software control.

(4) All data has been outputted. The CALL bit is cleared under software control. The TSFR LED is initiated to illuminate for .5 seconds. The computer can input data from the analog inputs between now and the next COUNT to BLANK transition.

(5) All outputs should be settled. The counters commence counting. The COUNT LED illuminates.

Fig. 7. ADIOS-APPLE Synchronization



(1) The counter's input is gated off.

(2) A pulse is applied to the internal gate of Counters 2 and 3. This pulse, labeled "SAVE", causes the contents of the counters to be placed in the HOLD registers at mark (3) .

(4) A pulse is applied/added to the input of Counter 2. This first pulse of integration clears the counter. The pulse is not recorded.

(5) A pulse is applied/added to the input of Counter 3. This clear pulse is inhibited by OUT2. If OUT2 is clocked by the CLR 2 pulse, Counter 3 will automatically be cleared.

NOTE: When a counter reaches FFFF, it will commit itself to outputting a terminal count pulse initiated by the next input clock pulse. Once committed, it cannot be disrupted by:

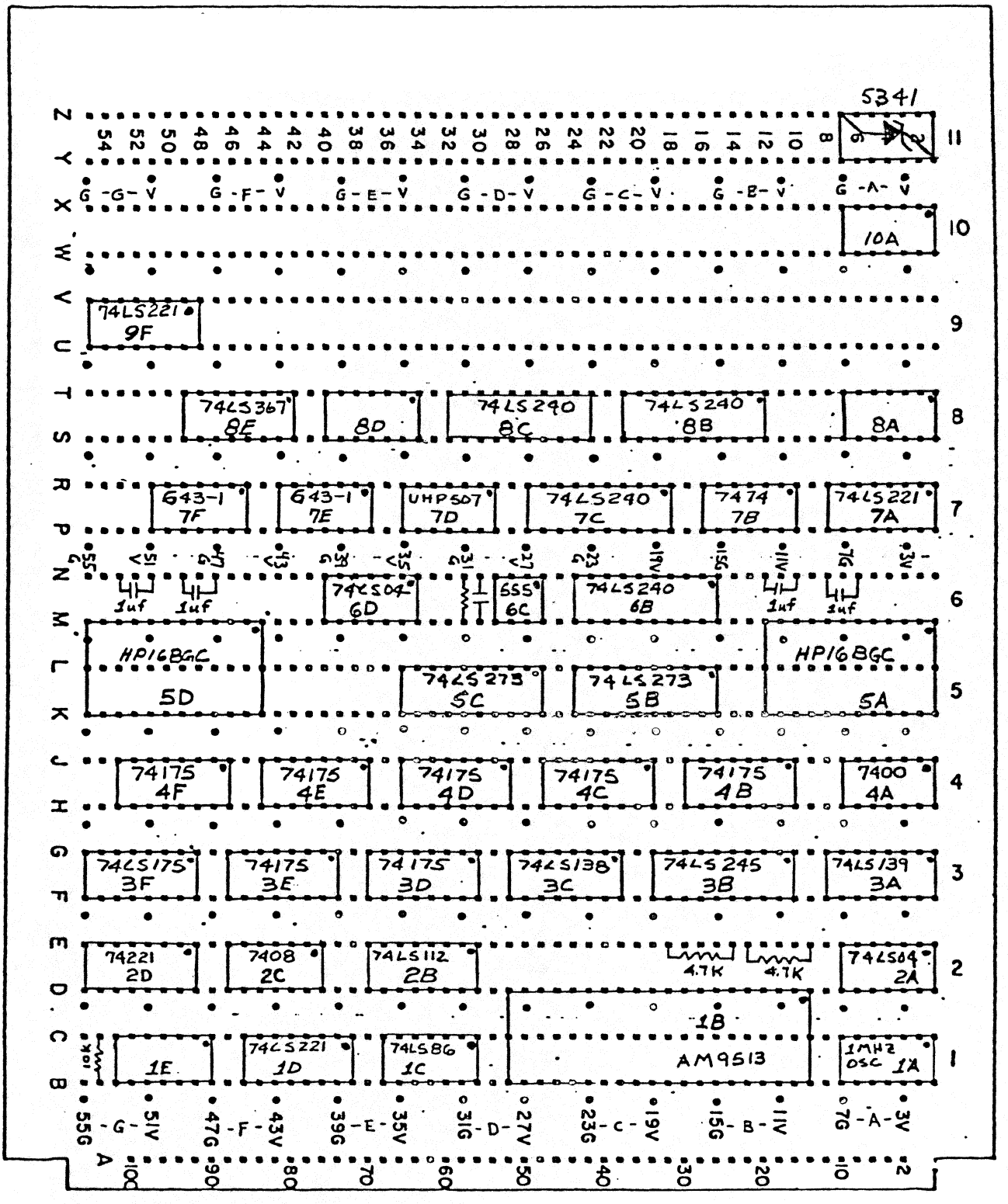
a) the internal gate signal ("SAVE")

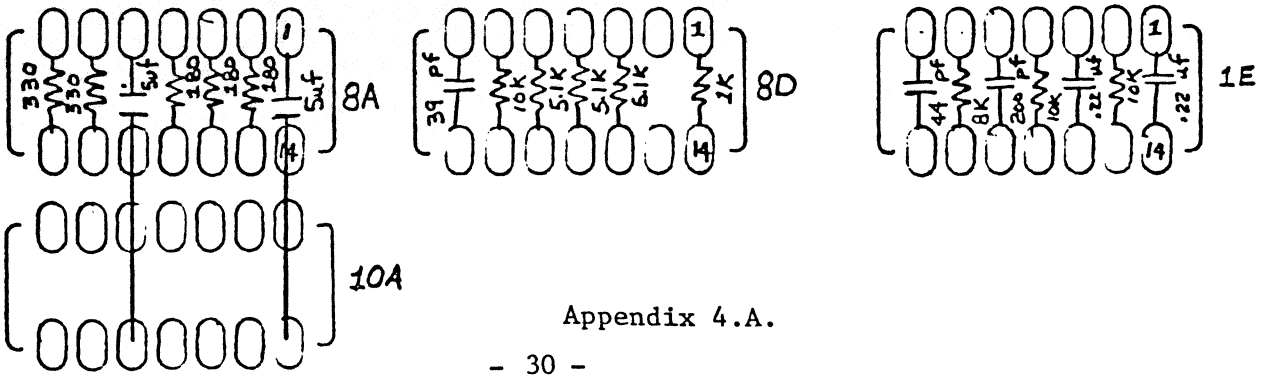
b) the clearing of the counter

c) the saving of the counter's contents

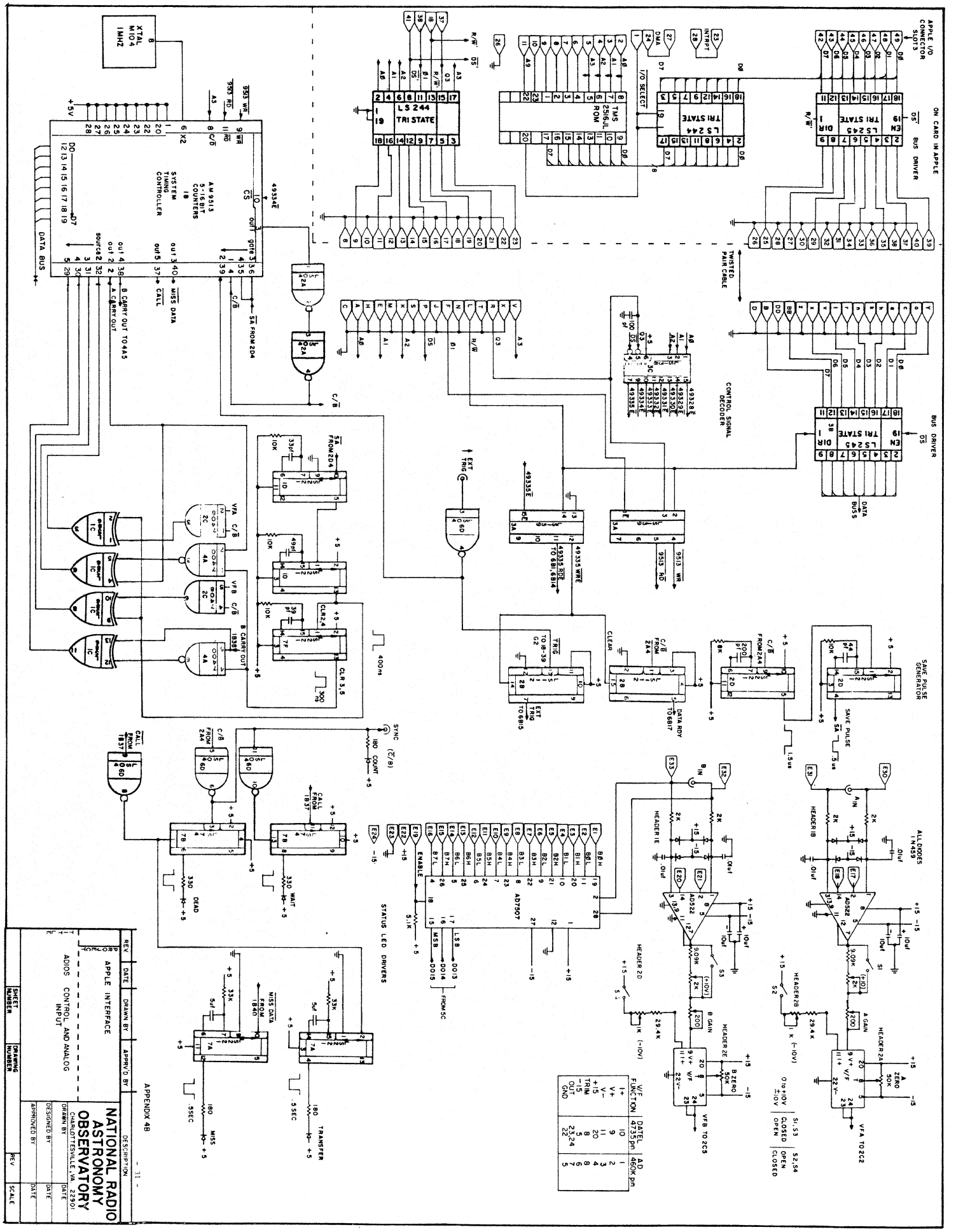
Due to this characteristic, OUT2 must inhibit CLR 3 for OUT2 becomes the "extra" pulse initiated by CLR 2 and not intended to be counted.

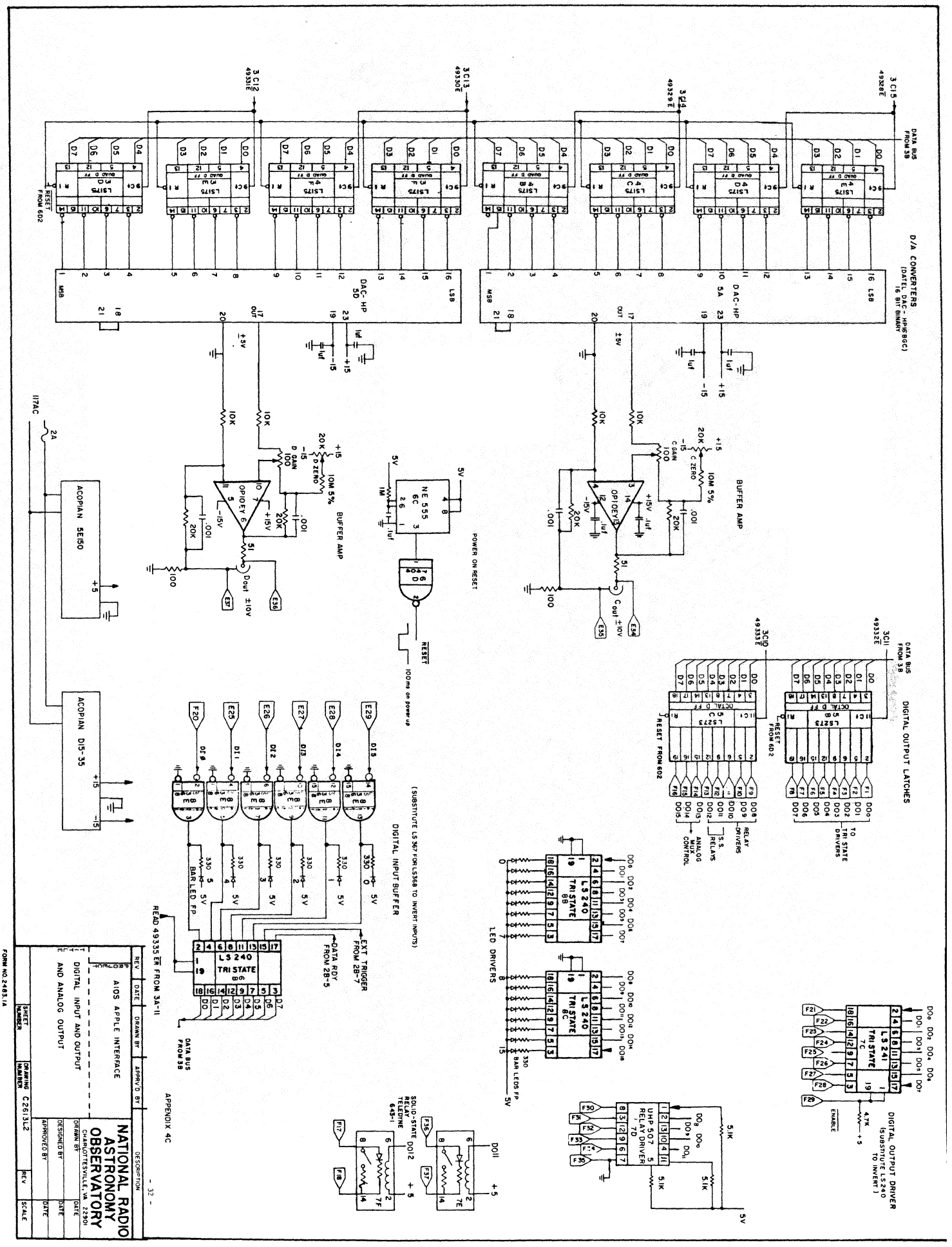
Fig. 8. Timing Diagram of AM9513 Counting Operation.


5341
10A
74LS221 9F
74LS367 8E
8D
74LS240 8C
74LS240 8B
8A
6431 7F
6431 7E
UHP507 7D
74LS240 7C
7474 7B
74LS221 7A
1uf
74LS04 6D
555 6C
74LS240 6B
HP16BGC 5D
74LS273 5C
74LS273 5B
HP16BGC 5A
74175 4F
74175 4E
74175 4D
74175 4C
74175 4B
7400 4A
74LS175 3F
74175 3E
74175 3D
74LS138 3C
74LS245 3B
74LS139 3A
74221 2D
7408 2C
74LS112 2B
4.7K
74LS04 2A
1B
AM9513
1E
74LS221 1D
74LS86 1C
1MHZ OSC 1A
-G- 51V
-F- 43V
-E- 35V
-D- 27V
-C- 19V
-B- 11V
-A- 3V


330
.05uf
1uf
681
681
680
.5uf
8A
39 pf
1K
1K
1K
1K
1K
8D
44 pf
8K
20pf
18K
.22
10K
.22uf
1E
10A

Appendix 4.A.


APPLE I/O CONNECTOR SLOT 3
ON CARD IN APPLE
BUS DRIVER
LS 244 TRI STATE
TMS 2516 ROM
I/O SELECT
INTRPT
DMA
TWISTED PAIR CABLE
CONTROL SIGNAL DECODER
DATA BUSS
XTAL M104 1MHZ
AM 9513 5-16 BIT COUNTERS 10
SYSTEM TIMING CONTROLLER
DATA BUS
MISS DATA
CALL
B CARRY OUT TO 4A3
A CARRY OUT
SA FROM 2D4
SAVE PULSE GENERATOR
SAVE PULSE
1.5 us
3 us
ALL DIODES 1N459
HEADER 1B
HEADER 1E
HEADER 2D
HEADER 2B
HEADER 2A
A ZERO
B ZERO
A GAIN
B GAIN
VFA TO 2C2
VFB TO 2C5
AD522
AD7507
STATUS LED DRIVERS
ENABLE
LSB
MSB
DO13
DO14
DO15
FROM 5C
EXT TRIG
TRIG TO 8-39 G2
CLEAR
DATA RDY TO 68B7
EXT TRIG TO 68B5
49335 WRE TO 68L, 68M
9513 WR
SYNC (C/B)
180 COUNT
DEAD
WAIT
MISS DATA FROM 1B40
180 MISS
.55EC
180 TRANSFER
.5 SEC
400ns
300 ns
CLR 3,5
CLR 2,4
VF/F FUNCTION
DATEL 473 pin
AD 460K pin
S1, S3 CLOSED OPEN
S2, S4 OPEN CLOSED
0 to +10V ±10V
APPENDIX 4B
- 31 -
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA 22901
APPLE INTERFACE
ADIOS CONTROL AND ANALOG INPUT
DRAWN BY
DESIGNED BY
APPROVED BY
SHEET NUMBER
DRAWING NUMBER
SCALE
REV
DATE
DESCRIPTION


D/A CONVERTERS
(DATEL DAC-HPC86GC)
16 BIT BINARY
DAC-HP
DATA BUS FROM 3B
DIGITAL OUTPUT LATCHES
DIGITAL OUTPUT DRIVER
(SUBSTITUTE LS240 TO INVERT)
BUFFER AMP
POWER ON RESET
DIGITAL INPUT BUFFER
(SUBSTITUTE LS 367 FOR LS368 TO INVERT INPUTS)
LED DRIVERS
SOLID-STATE RELAY TELEDYNE 643-1
UHP 507 RELAY DRIVER
ACOPIAN 5E150
ACOPIAN D15-35
APPENDIX 4C
NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA 22901
AIOS APPLE INTERFACE
DIGITAL INPUT AND OUTPUT AND ANALOG OUTPUT
DRAWING NUMBER C26131.2
FORM NO.2483.1A

Appendix 5. Manufacturers Data

Appendix 5.B. Consists of pages 1, 5, and 6 of a six-page report. The complete report can be obtained from Teledyne Philbrick, Allied Drive at Route 128, Dedham, Massachusetts 02026.

Appendix 5.D. Consists of pages 1, 2, and 4 of a four-page report. The complete report can be obtained from Datel Intersil, 11 Cabot Boulevard, Mansfield, MA 02048.

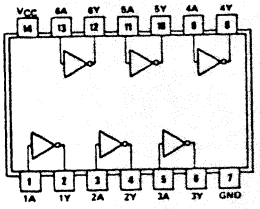
Appendix 5.H. Consists of pages 1-5 of a 26-page report. The complete report can be obtained from Advanced Micro Devices, Inc., 901 Thompson Place, P. O. Box 453, Sunnyvale, California 94086.

Appendix 5.I. Analog Devices 460K V/F converter used as a substitute for Teledyne 4735 due to unavailability.

HEX INVERTERS

04

positive logic:
$Y = \overline{A}$



SN5404 (J) SN7404 (J, N)
SN54H04 (J) SN74H04 (J, N)
SN54L04 (J) SN74L04 (J, N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)

See page 6-2

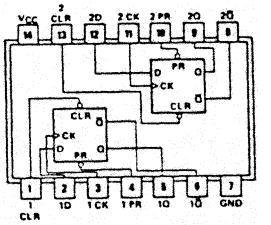
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56

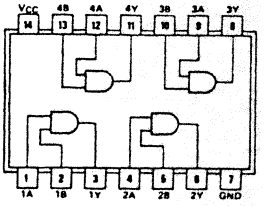


SN5474 (J) SN7474 (J, N)
SN54H74 (J) SN74H74 (J, N)
SN54L74 (J) SN74L74 (J, N)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)

QUADRUPLE 2-INPUT POSITIVE-AND GATES

08

positive logic:
$Y = AB$



SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

See page 6-10

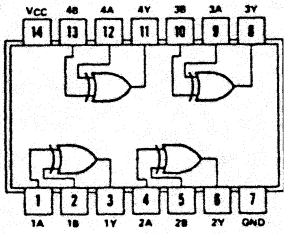
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



SN5486 (J, W) SN7486 (J, N)
SN54LS86 (J, W) SN74LS86 (J, N)
SN54S86 (J, W) SN74S86 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

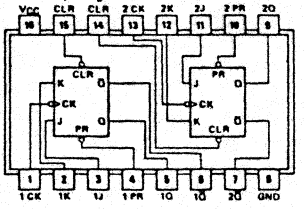
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$
H	↑	L				

See pages 6-56 and 6-58

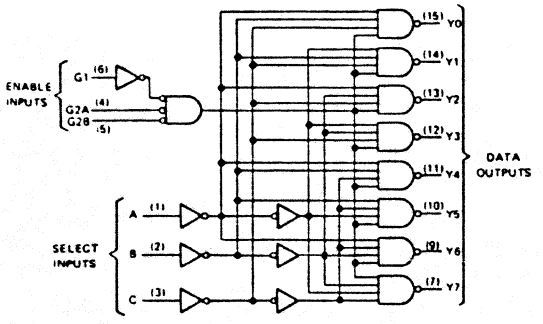


SN54LS112A (J, W) SN74LS112A (J,N
SN54S112 (J, W) SN74S112 (J, N)

Appendix 5.A.

74LS138

'LS138, 'S138



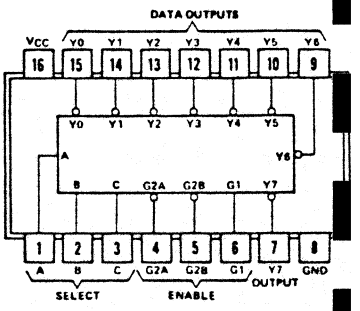
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

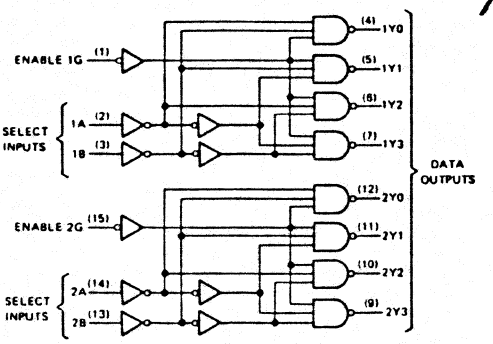
SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

74LS139

'LS139, 'S139

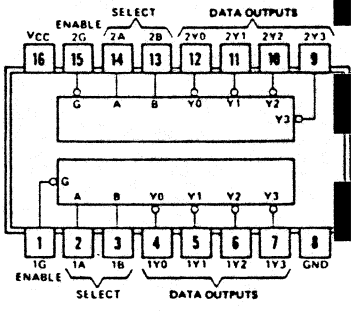


'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

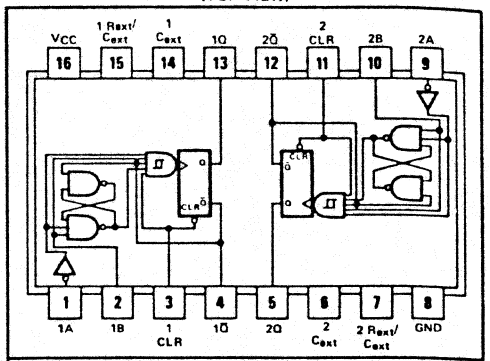
INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74LS139, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)



SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



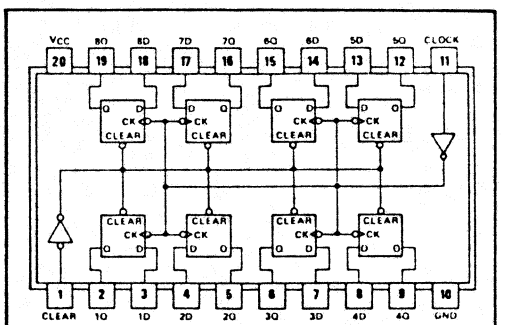
positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

Also see description and switching characteristics

SN74273, SN74LS273 . . . J OR N PACKAGE



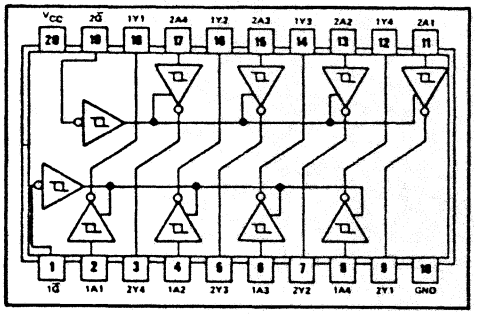
positive logic: see function table

FUNCTION TABLE
(EACH FLIP-FLOP)

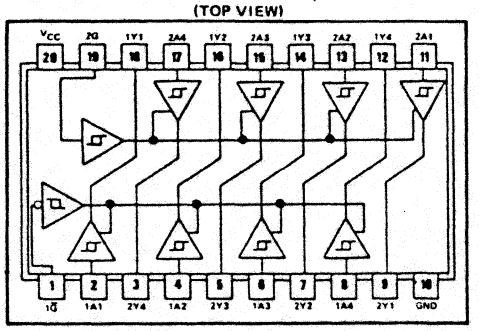
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Appendix 5.A.

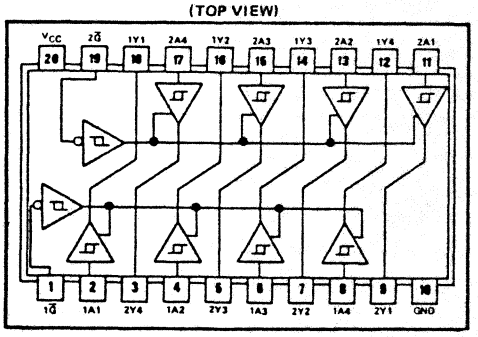
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



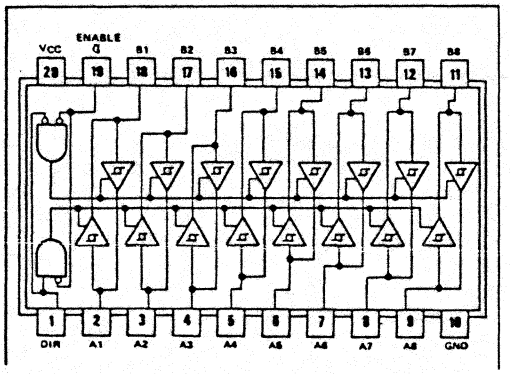
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)



SN74LS244 . . . J OR N
(TOP VIEW)



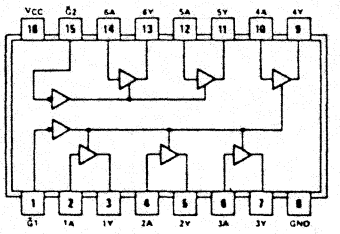
SN74LS245 . . . J OR N PACKAGE
(TOP VIEW)



PIN ASSIGNMENTS (TOP VIEWS)

HEX BUS DRIVERS

367 NONINVERTED DATA OUTPUTS
4-LINE AND 2-LINE ENABLE INPUTS
3-STATE OUTPUTS

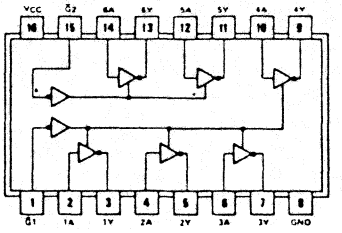


SN54367A (J, W) SN74367A (J, N)
SN54LS367A (J, W) SN74LS367A (J, N)

See page 6-36

HEX BUS DRIVERS

368 INVERTED DATA OUTPUTS
4-LINE AND 2-LINE ENABLE INPUTS
3-STATE OUTPUTS



SN54368A (J, W) SN74368A (J, N)
SN54LS368A (J, W) SN74LS368A (J, N)

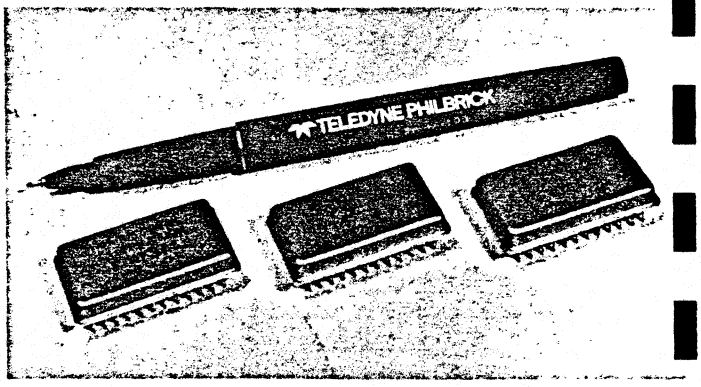
See page 6-36

Appendix 5.A.

TELEDYNE PHILBRICK

10kHz 100kHz 1MHz

4731/4733/4735 HIGH RELIABILITY HYBRID VOLTAGE TO FREQUENCY CONVERTERS



This series of low drift voltage-to-frequency converters provide an output-pulse-train repetition rate that is a precision linear function of the input voltage. These low drift, ultra linear, 10 kHz/100 kHz/1 MHz Full Scale V-to-F's have the ability to handle positive, negative, and differential input signals over a wide range of power supply voltages (±9 V to ±18 V). They operate over the wide temperature range of –55°C to +125°C.

With 126 dB of dynamic range, 70 dB CMRR, and 100% overrange, these V-to-F's provide linear operation with input voltages from ±10 μV to +20V. The current pin (the summing point of an op amp) resolves currents as low as 1000 pA (4731/4733), which makes operation with full scale input voltages from less than 250 mV to greater than 100 volts possible.

The 4731/4733's 0.005% nonlinearity is the equivalent of 16 bits end point linearity, while differential nonlinearity and dynamic range approach 20 bits. With this combination of features and specifications, the 4731/4733/4735 stand alone as sixth generation devices, capable of operation from power supply voltages as low as ± 9 V.

	NOMINAL FREQUENCY/ MAX. OVERRANGE	NONLINEARITY ±% F.S. Typical	Guaranteed		FULL SCALE Temp. Coef. ±PPM/°C Typical	Guaranteed
4731	10 kHz/21 kHz	.002	.005	④ Hot	4	15
				Cold	7	25
4733	100 kHz/210 kHz	.002	.005	④ Hot	6	20
				Cold	10	30
4735	1 MHz/2.1 MHz	.005	.015	⑤	30	50

For maximum reliability and performance these V-to-Fs are offered with 100% screening similar to MIL-STD-883 Method 5008. Refer to Table 2 for details as to methods and test conditions.

MODEL	OPERATING TEMPERATURE RANGE	SCREENED to MIL-STD-883 METHOD 5008
4731 4733 4735	–55°C to +125°C	Internal Visual Stabilization Bake Constant Acceleration Seal, Fine and Gross Leak External Visual
4731-83 4733-83 4735-83	–55°C to +125°C	Internal Visual Stabilization Bake Constant Acceleration Seal, Fine and Gross Leak Burn-In Temperature Cycling External Visual

Table 1.

FEATURES

- 100% Screening Similar to MIL-STD-883, Method 5008
- Power Supply Range ±9 V to ±18 V
- Ultra Linear
- 100% Overrange
- 126 dB Dynamic Range
- 70 dB CMRR
- Low Full Scale Drift
- Low Zero Offset Voltage Drift
- TTL, CMOS, HNIL Compatible Output

APPLICATIONS

- No Drift Integrate/Hold
- High Common Mode Voltage Isolation
- 2-Wire Digital Transmission
- Analog-to-Digital Converters—20 Bit
- Optical Data Link

HOW TO USE THE 4731/4733/4735

When used as shown in Figure 1A & 1B, the factory trimmed V-to-F operates as specified without additional components. Pin 9 the $+V_{in}$ trim and pin 12 the $+V_{in}$ are both inputs for a positive input signal. Pin 12 can be used when accuracy to ±0.1% of F.S. is needed with no external components. Pin 9 is usually used when greater accuracy is required using an external trim, see Figure 2A.

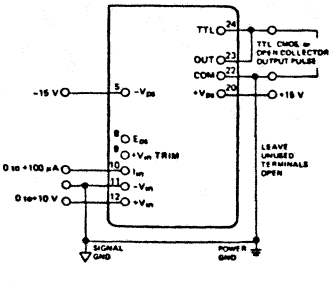


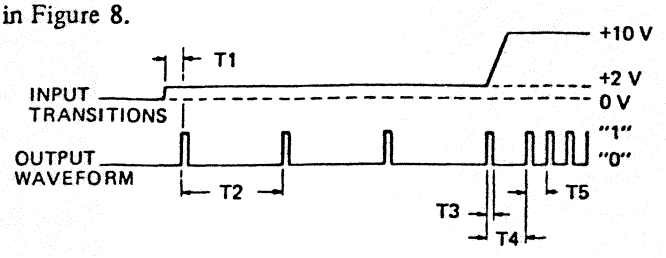
Figure 1A. Positive Input Signals Figure 1B. Negative Input Signals

Output Protection ($+V_{CC}$, Common, $-V_{CC}$)

The V-to-F output (collector of Q2) may be shorted to ground indefinitely without damage, however, since Q2 is ON most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5 seconds. A short to TTL (pin 24) and $-V_{CC}$ simultaneously will cause instant catastrophic failure.

Square Wave Output

The output of the 4731/4733/4735 is a train of pulses 20 μsec/2 μsec/.2 μsec (see Figure 7). A symmetrical (square wave) output for driving highly capacitive or noisy transmission lines is obtained with a D or JK flip flop as shown in Figure 8.



Typical Time in Micro-Seconds

	T1	T2	T3	T4	T5
4731	0 to 500	500	20	≈200	100
4733	0 to 50	50	2	≈30	10
4735	0 to 5	5	0.2	≈3	1

Figure 7. Typical Waveforms, Showing Timing Relationships

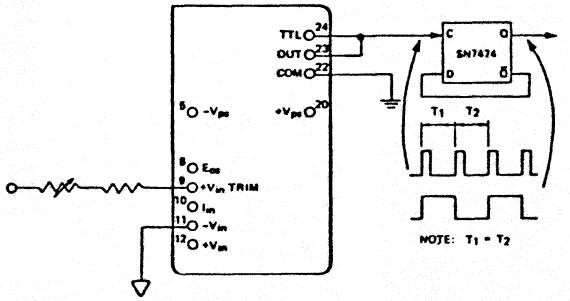
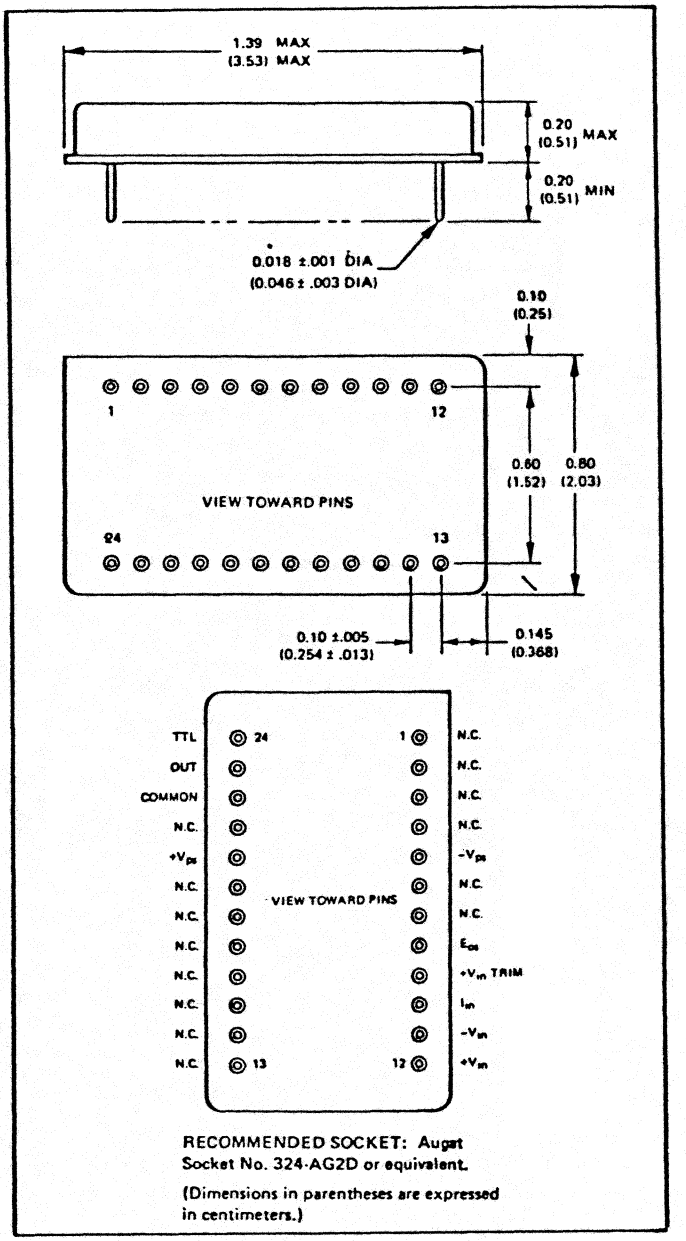


Figure 8. Square Wave Output Using D - Type Flip Flop



RECOMMENDED SOCKET: Augat Socket No. 324-AG2D or equivalent.

(Dimensions in parentheses are expressed in centimeters.)

SCREENING SIMILAR TO MIL-STD-883 METHOD 5008		
Test	Methods and Conditions	Purpose
*Internal Visual	Method 2017	Removes potentially defective units with respect to materials, construction, and workmanship.
*Stabilization Bake	Method 1008, Condition C 24 hours at 150 °C	Preconditioning treatment to stabilize circuit components prior to conducting further testing and trimming.
*Constant Acceleration	Method 2001, Condition A Y_1 Axis, 5,000 g	Removes potential failures due to weak wire or chip bonding.
*Seal, Fine and Gross	Method 1014, Fine Leak Condition A & C Bomb time 1 hr. at 30 psi; Leak Rate $< 5 \times 10^{-7}$ cc/sec; Gross Leak, Condition C_1, no bubbles	Verifies Integrity of hermetic package
Burn In	Method 1015 Condition B 160 hours at 125 °C	Reduces infant mortality rate
Temperature Cycling	Method 1010, Condition B 10 cycles from $-55\,^{\circ}C\ ^{+0\,^{\circ}C}_{-5\,^{\circ}C}$ to $+125\,^{\circ}C\ ^{+3\,^{\circ}C}_{-0\,^{\circ}C}$	Removes potential failures due to weak wire or chip bonding.
*External Visual	Method 2009	Removes defective units with respect to materials, construction, and workmanship.

*These tests are for both standard and "–83" models 4731, 4733 and 4735 Screening Program to MIL-STD-883

Table 2.

SPECIFICATIONS @ +25 °C, $\pm V_{cc}$, ±15 V (unless otherwise indicated)

	TYPICAL	GUARANTEED
FULL SCALE (FS)		
Ideal Transfer Function	---	$f_{out} = \frac{(V_{in})(f_A)}{10\ V} = \frac{(I_{in})(f_A)}{I_{fs}}$ ⑦
		f_A = 10 kHz (4731)/100 kHz (4733)/1 MHz (4735)
$+V_{in}$ trim	---	9.9 V ±0.5% trimmable to 10.00 V
$+V_{in}$	---	10.00 V ±.05 V
$+I_{in}$	---	100 µA ±25% (4731/4733); 1 mA ±25% (4735)
Range (for specified nonlinearity) ①		
$+V_{in}$ Terminal	+10 µV to +21 V	+100 µV to +12 V
$-V_{in}$ Terminal @ V_{cc} = ±18 V	−10 µV to ($-V_{cc}$ +5.0 V)	−100 µV to ($-V_{cc}$ +7.0 V)
$+I_{in}$ Terminal	+1 nA to +210 µA (4731/4733)	+1 nA to 120 µA (±25%) (4731/4733)
	10 nA to +2.1 mA (4735)	10 nA to 1.2 mA (4735)
Differential $\lvert(+V_{in}) - (-V_{in})\rvert$ ②	±12 V	±11 V, ($\pm V_{cc}$ fault)
Over Range Max., $+V_{in}$, ($-V_{in}$ = 0)	$+V_{in}$ = 21 V, f_{out} = 21 kHz/210 kHz/2.1 MHz	$+V_{in}$ = +20 V, f_{out} = 20 kHz/200 kHz (4731/4733); $+V_{in}$ = +15 V, f_{out} = 1.5 MHz (4735)
Dynamic Range	126 dB	100 dB
Common Mode Voltage ③	($+V_{cc}$ −4 V), ($-V_{cc}$ +5 V)	($+V_{cc}$ −5 V), ($-V_{cc}$ +7 V)
CMRR, CMV = ±10 V	70 dB	60 dB

NONLINEARITY ±%FS	4731/4733	4735	4731/4733	4735
$+V_{in}$ (+100 µV to 12 V)	.002	.005	.005	.015
$+V_{in}$ (+100 µV to 12.0 V) ⑧ ⑨	.002	.005	.005	.015
$-V_{in}$ (−100 µV to $-V_{cc}$ +7.0 V)	.01	.02	.02	.05
$+I_{in}$ (1 nA to 120 µA) (4731/4733)	.002	---	.005	---
$+I_{in}$ (1 nA to 120 µA) (4731/4733) ⑧ ⑨	.002	---	.005	---
$+I_{in}$ (10 nA to 1.2 mA) (4735)	---	.005	---	.015
$+I_{in}$ (10 nA to 1.2 mA) (4735) ⑨ ⑩	---	.005	---	.015
$+V_{in}$ (+100 µV to +12.0 V) ⑩	.005	.01	.01 Hot; .03 Cold	.02
$+V_{in}$ (+100 µV to 20 V) (4731/4733) ⑧ ⑨	.02	---	.05	---
$+V_{in}$ (+100 µV to 15 V) (4735) ⑧ ⑨	---	.02	---	.05

INPUT	
Zero Offset Voltage, Initial Untrimmed	±1 mV
Impedance @ $+V_{in}$	---
Impedance @ $-V_{in}$	100 MΩ
Impedance @ $+I_{in}$ (op amp summing point)	Virtual Ground
	±5 mV (trimmable to zero)
	100 kΩ±25% (4731/4733); 10 kΩ±25% (4735)
	10 MΩ
	< 0.1 Ω

STABILITY OF FULL SCALE FACTOR	4731		4733		4735	4731		4733		4735
	Hot	Cold	Hot	Cold	⑪	Hot	Cold	Hot	Cold	⑪
Temperature Coefficient ($+V_{in}$, $-V_{in}$) ±PPM/°C ⑩	4	7	6	10	30	15	25	20	30	50
Temperature Coefficient ($+I_{in}$) ±PPM/°C ⑩	4	7	6	10	30	---	---	---	---	---
Temperature Coefficient ($+V_{in}$, $-V_{in}$) ±PPM/°C ⑩	8	10	12	15	30	25	50	30	50	50
Power Supply Sensitivity ±PPM/%ΔV_{cc} ④	10		10		15	20		20		35
Drift: Per Day/Per Month ±PPM	10/30		10/30		10/30	---		---		---
Warm Up Time to .01%/.002% of F.S.	1 s/100 s		1 s/100 s		1 s/100 s	---		---		---

STABILITY OF ZERO OFFSET VOLTAGE µV/°C	4731/4733	4735	4731/4733	4735
Temperature Coefficient µV/°C ⑩	±6	±10	±20	±50
Temperature Coefficient µV/°C ⑩	±20	±15	±100 Hot; ±50 Cold	±50
Power Supply Sensitivity ±µV/%ΔV_{cc} ④	3	5	20	10
Drift: Per Day/Per Month	20 µV/60 µV	20 µV/60 µV	---	---

RESPONSE	
Settling Time to .01% for FS step input	---
Overload Recovery (V_{in} = +100 V to V_{in} = +10) or (I_{in} = 1 mA to I_{in} = 100 µA)	0.14 ms (4731/4733); 70 µs (4735)
	1 to 2 pulses of new frequency +5 µs
	0.5 ms (4731/4733); 0.2 ms (4735)

OUTPUT WAVEFORM	
	TTL compatible pulses adaptable to CMOS, HNIL (see Figure 4)
High (positive logic "1")	---
	+2.4 V to +5 V (up to 10 TTL Load)
Low (positive logic "0")	---
	≤ 0.4 V @ −16 mA Sink Current
Pulse Width	---
	(4731/10 µs to 30 µs, 4733/1 µs to 3 µs, 4735/0.1 µs to .3 µs)
Source Impedance (High)	---
	3.5 kΩ±20% (4731/4733); 680 Ω±20% (4735)

POWER REQUIREMENT	
Voltage Range ($\pm V_{cc}$)	±7 V to ±18 V
	±9 V to ±18 V
Voltage Asymmetry (Δ between $\lvert+V_{cc}\rvert$&$\lvert-V_{cc}\rvert$	---
	±2 V
Current ($\pm I_{cc}$) @ V_{cc} = ±15 V	±17 mA (4731/4733); ±35 mA (4735)
	±25 mA (4731/4733); 45 mA (4735)

ENVIRONMENT/RELIABILITY	
Operating Temperature	---
	−55 °C to +125 °C
Storage Temperature Absolute Max.	---
	−65 °C to +150 °C

Input Protection: All inputs may be shorted to $\pm V_{cc}$ indefinitely without damage

Output Protection: May be shorted to ground indefinitely; to $+V_{cc}$ for 5 s

Suggested Power Supplies: 2403 or 2301.

Request AN-20 for V to F applications.

NOTES

① After trim @ 10 Hz and 10 kHz (4731)/100 Hz and 100 kHz (4733)/1 kHz and 1 MHz (4735)
② See Figure 5G for definition
③ Constant voltage at Zero trim pin
④ Measured from −25 °C to +85 °C, Hot (+25 °C to +85 °C) & Cold (−25 °C to +25 °C)
⑤ Measurement, made for $\pm V_{cc}$ = ±9 V to ±18 V
⑥ Measured for −55 °C to +125 °C, Hot (+25 °C to +125 °C) & Cold (−55 °C to +25 °C)
⑦ I_{fs} = 100 µA for 4731 and 4733, 1 mA for 4735
⑧ Specified over entire temperature range, −55 °C to +125 °C

TELEDYNE PHILBRICK

Allied Drive at Route 128, Dedham, Massachusetts 02026
Tel: (617)329-1600 TWX:(710)348-6726 Telex: 92-4439

ANALOG DEVICES

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

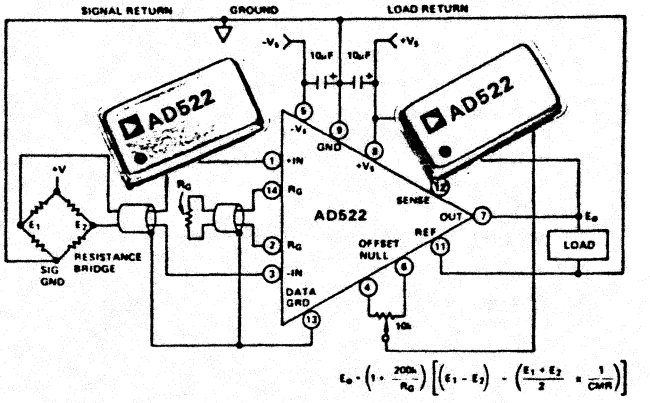
- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)
- Hermetically-Sealed, Electrostatically Shielded DIP

Versatility

- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR
- Low Cost: $13.00 (100's, A)



$$E_o = \left(1 + \frac{200k}{R_G}\right)\left[(E_1 - E_2) - \left(\frac{E_1 + E_2}{2} - \frac{1}{CMR}\right)\right]$$

PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

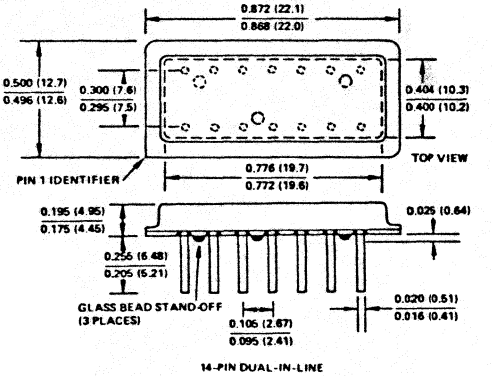
The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\,\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

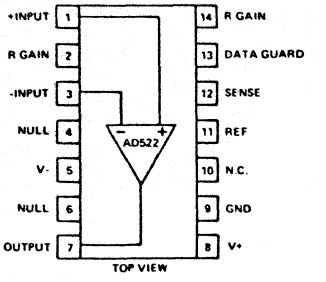
The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the military/aerospace temperature range of -55°C to +125°C. All versions are packaged in a hermetically-sealed, electrostatically shielded 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN CONFIGURATION



Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 TWX: 710/394-6577
West Coast 213/595-1783 Mid-West 312/894-3300 Texas 214/231-5094

SPECIFICATIONS (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25°C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_g}$	•	•
Gain Range	1 to 1000	•	•
Equation Error			
G = 1	0.2% max	0.05% max	••
G = 1000	1.0% max	0.2% max	••
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	••
G = 100	0.01%	0.005%	••
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	•	•
G = 1000	50ppm/°C (25ppm/°C typ)	•	•
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	•	•
DYNAMIC RESPONSE (See Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	•	•
G = 100	3kHz	•	•
Full Power GBW	1.5kHz	•	•
Slew Rate	0.1V/μs	•	•
Settling Time to 0.1%, G = 100	0.5ms	•	•
to 0.01%, G = 100	5ms	•	•
to 0.01%, G = 10	2ms	•	•
to 0.01%, G = 1	0.5ms	•	•
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±400μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
1 < G < 1000	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	•	•
G = 1000	±0.2μV/%	•	•
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\Omega$	•	•
Common Mode	$10^9\Omega$	•	•
Input Voltage Range			
Maximum Differential Input, Linear	±10V	•	•
Maximum Differential Input, Safe	±20V	•	•
Maximum Common Mode, Linear	±10V	•	•
Maximum Common Mode Input, Safe	±15V	•	•
Common Mode Rejection Ration, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	•
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	•	•
G = 1000	1.5μV	•	•
10Hz to 10kHz (rms)			
G = 1	15μV	•	•
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	•	-55°C to +125°C
Operating	-55°C to +125°C	•	•
Storage	-65°C to +150°C	•	•
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	•	•
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA
PRICE			
(1-24)	$29.25	$36.00	$45.00
(25-99)	$23.40	$28.80	$36.00
(100-999)	$19.50	$24.00	$30.00

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

SPECIFICATIONS (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25°C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_g}$	•	•
Gain Range	1 to 1000	•	•
Equation Error			
G = 1	0.2% max	0.05% max	••
G = 1000	1.0% max	0.2% max	••
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	••
G = 100	0.01%	0.005%	••
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	•	•
G = 1000	50ppm/°C (25ppm/°C typ)	•	•
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	•	•
DYNAMIC RESPONSE (See Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	•	•
G = 100	3kHz	•	•
Full Power GBW	1.5kHz	•	•
Slew Rate	0.1V/μs	•	•
Settling Time to 0.1%, G = 100	0.5ms	•	•
to 0.01%, G = 100	5ms	•	•
to 0.01%, G = 10	2ms	•	•
to 0.01%, G = 1	0.5ms	•	•
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±400μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	•	•
G = 1000	±0.2μV/%	•	•
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\Omega$	•	•
Common Mode	$10^9\Omega$	•	•
Input Voltage Range			
Maximum Differential Input, Linear	±10V	•	•
Maximum Differential Input, Safe	±20V	•	•
Maximum Common Mode, Linear	±10V	•	•
Maximum Common Mode Input, Safe	±15V	•	•
Common Mode Rejection Ration, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	•
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	•	•
G = 1000	1.5μV	•	•
10Hz to 10kHz (rms)			
G = 1	15μV	•	•
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	•	-55°C to +125°C
Operating	-55°C to +125°C	•	•
Storage	-65°C to +150°C	•	•
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	•	•
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA
PRICE			
(1-24)	$29.25	$36.00	$45.00
(25-99)	$23.40	$28.80	$36.00
(100-999)	$19.50	$24.00	$30.00

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

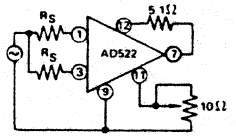


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

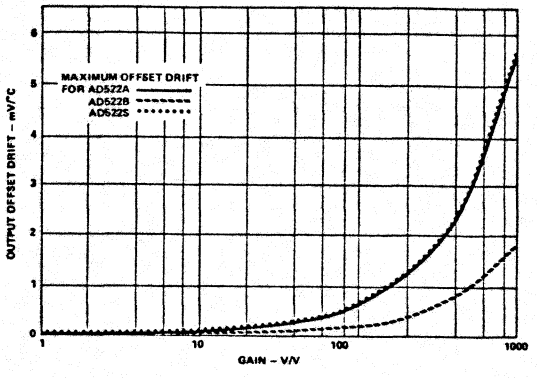


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

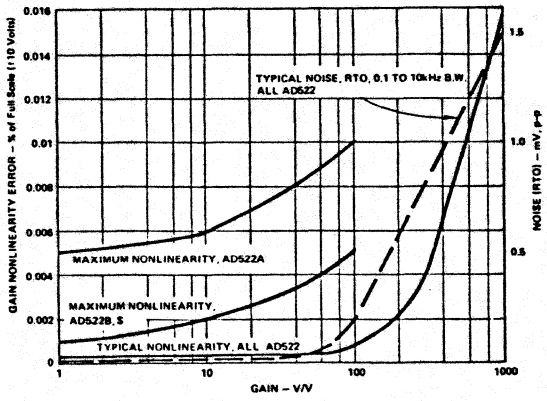


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

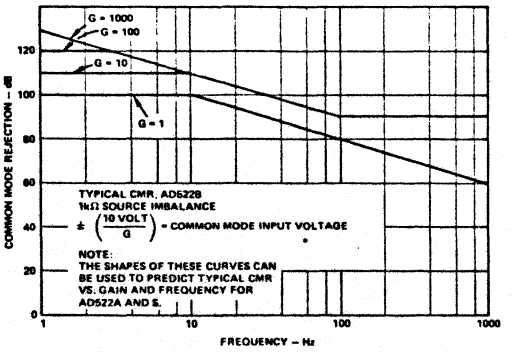


Figure 5. Common Mode Rejection vs. Frequency and Gain

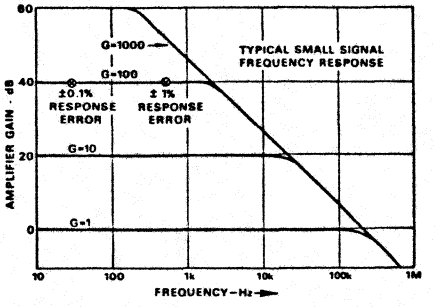


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

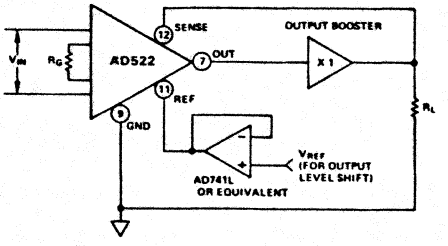


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

16-Bit, Microelectronic Digital-to-Analog Converters DAC-HP16B And DAC-HP16D

FEATURES

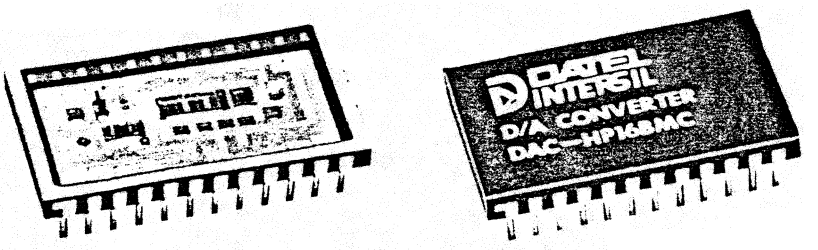
- 16 Bit Binary Model
- 4 Digit BCD Model
- Voltage Output
- 15ppm/°C max. Gain Tempco
- Linearity to ±0.003%

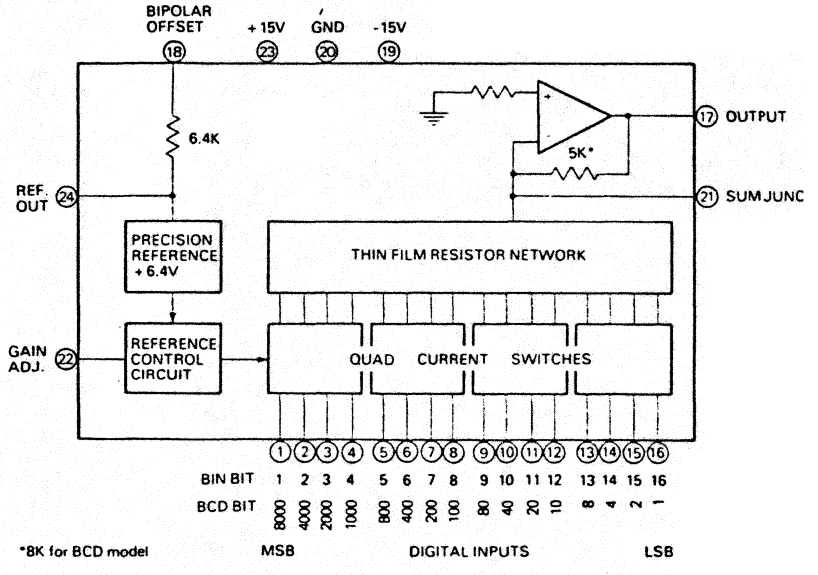
GENERAL DESCRIPTION

The DAC-HP series are high resolution hybrid D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24 pin double spaced ceramic DIP package. There are two basic models in the series. The DAC-HP16B has 16 bit binary resolution with ±0.003% linearity while the DAC-HP16D has 4 digit BCD resolution with ±0.005% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10V and ±5V respectively. Binary versions with a bipolar output voltage range of ±10V are available, denoted by the suffix "−1" after the model designation. The BCD version operates in the unipolar mode only with 0 to +10V output.

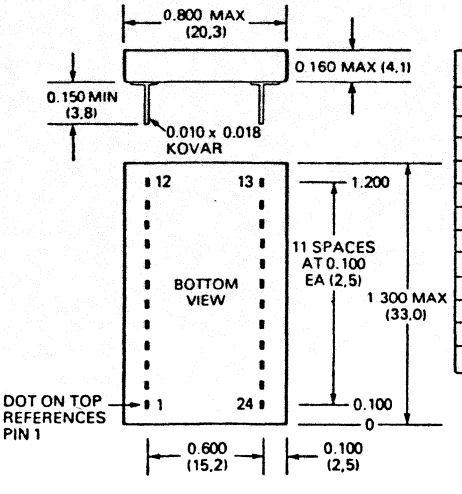
The DAC-HP design incorporates thin film hybrid technology which has been in volume production. Selected low tempco nichrome-on-silicon thin film resistor networks are combined with tightly matched quad current switches to achieve 16 bit resolution. The thin film resistors together with the low tempco zener reference circuit result in a maximum gain tempco of ±15ppm/°C for the DAC. The thin film resistors are functionally laser trimmed for optimum converter linearity.

The resolution, stability, and voltage output of these converters make them ideal for precision applications such as speech and waveform reconstruction, precision ramp generators, and computer controlled testing. They are available in three operating temperature ranges: 0 to 70°C, −25 to +85°C, and −55 to +125°C. High reliability versions are also available under Datel Intersil's "S" program and MIL-STD-883 level B screening. Power requirement is ±15VDC.





MECHANICAL DIMENSIONS INCHES (MM)



NOTE PINS HAVE 0.025 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF
7	BIT 7 IN	19	−15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM JUNCTION
10	BIT 10 IN	22	GAIN ADJ
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF OUT

SPECIFICATIONS DAC-HP SERIES

	DAC-HP16B (Binary)	DAC-HP16D (BCD)
MAXIMUM RATINGS		
Positive Supply, pin 23	+18V	*
Negative Supply, pin 19	−18V	*
Digital Input Voltage, pins 1-16	+5.5V	*
Output Current, pin 17	±20mA	*
INPUTS		
Resolution	16 bits	4 digits
Coding, unipolar output	Comp. Binary	Comp. BCD
Coding, bipolar output	Comp. Off. Binary	—
Input Logic Level, bit ON ("0")[1]	0V to +0.8V @ −1mA	
Input Logic Level, bit OFF ("1")[1]	+2.4V to +5.5V @ +40μA	
Logic Loading	1 TTL load	*
OUTPUT		
Output Voltage Range, Unipolar[2]	0 to +10V	*
Output Voltage Range, Bipolar	±5V	—
Output Voltage Range, "−1" Suffix	±10V	*
Output Current, min.	±5 mA	*
Output Impedance	0.05 ohm	
PERFORMANCE		
Linearity Error, max.	±0.003%	±0.005%
Monotonicity, 10°C to 40°C	14 bits	16 bits
Gain Error, before trimming	±0.1%	*
Zero Error, before trimming	±0.1%	*
Gain Tempco, max.[3]	±15ppm/°C	*
Gain Tempco, max. BGC, DGC	±20ppm/°C	*
Zero Tempco, unipolar, max.	±5ppm/°C of FSR[4]	*
Offset Tempco, bipolar, max.	±8ppm/°C of FSR[4]	—
Differential Linearity Tempco	±2ppm/°C of FSR[4]	*
Settling Time, 10V change[5]	15μsec.	15μsec.
Slew Rate	20V/μsec.	*
Power Supply Rejection	±0.002% FSR/%	*
POWER REQUIREMENT (Quiescent, all bits HI)	+15VDC at 38mA −15VDC at 38mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0°C to 70°C (BMC, DMC, BGC, DGC) -25°C to +85°C (BMR, DMR) -55°C to +125°C (BMM, DMM)	
Storage Temperature Range	-65°C to +150°C	
Package Type	24 pin ceramic	
Pins	0.010 x 0.018 inch diameter Kovar	
Weight	0.2 oz. (6g.)	

*Specifications same as first column.

NOTES:
1. Drive from TTL output with only the DAC-HP as load.
2. Unipolar output range for suffix "—1" models, 0 to +10V, is reached at ½ scale input.
3. For all models except DAC-HP16BGC & DAC-16DGC.
4. FSR is 0 to +FS or -FS to +FS voltage.
5. To 0.005% FSR.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1μF (tantalum type) at the +15V and −15V supply pins. The capacitors should be connected as close to the pins as possible. In high frequency noise environments an additional .01μF ceramic capacitor should be used in parallel with each tantalum bypass.

2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 20 where they all must connect together.

3. The external gain adjustment shown in the diagrams gives an adjustment of ±0.2% of full scale range. The converters are internally trimmed to ±0.1% at full scale. A wider range of adjustment may be achieved by decreasing the value of the 510K ohm resistor.

4. The zero adjustment, or offset adjustment, has an adjustment range of ±0.35% of full scale range. The unipolar zero is internally set to zero within ±0.1% of full scale range.

5. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. Current drawn from pin 24 should be limited to ±10μA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current of most of the popular operational amplifier types.

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE	SEAL	PRICE (1-24)
DAC-HP16BGC	0 to 70C	EPOXY	$ 72.50
DAC-HP16BMC	0 to 70C	HERM.	$131.00
DAC-HP-16BMR	-25 to +85C	HERM.	$164.00
DAC-HP16BMM	-55 to +125C	HERM.	$230.00
DAC-HP16BMC-1	0 to 70C	HERM.	$136.50
DAC-HP16BMR-1	-25 to +85C	HERM.	$169.00
DAC-HP16BMM-1	-55 to +125C	HERM.	$235.00
DAC-HP16DGC	0 to 70C	EPOXY	$ 72.50
DAC-HP16DMC	0 to 70C	HERM.	$131.00
DAC-HP16DMR	-25 to +85C	HERM.	$164.00
DAC-HP16DMM	-55 to +125C	HERM.	$230.00

Mating Socket: DILS-3 (24 pin socket) $1.95 each

Trimming Potentiometer: TP50K $3.00 each

For high reliability versions of the DAC-HP series, including units screened to MIL-STD-883, Level B, contact factory.

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

CODING TABLES

BIPOLAR OUTPUT— Complementary Offset Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "−1" MODELS
0000 0000 0000 0000	+FS−1LSB	+4.99985V	+9.99969V
0011 1111 1111 1111	+½FS	+2.50000	+5.00000
0111 1111 1111 1111	0	0.00000	0.00000
1011 1111 1111 1111	−½FS	−2.50000	−5.00000
1111 1111 1111 1110	−FS+1LSB	−4.99985	−9.99969
1111 1111 1111 1111	−FS	−5.00000V	−5.00000V

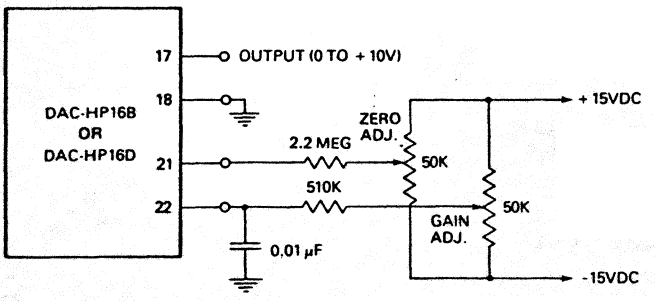
UNIPOLAR OUTPUT—Complementary BCD

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0110 0110 0110 0110	+FS−1LSB	+9.999V
1000 1010 1111 1111	+¾FS	+7.500
1010 1111 1111 1111	+½FS	+5.000
1101 1010 1111 1111	+¼FS	+2.500
1111 1111 1111 1110	+1LSB	+1.00mV
1111 1111 1111 1111	0	0

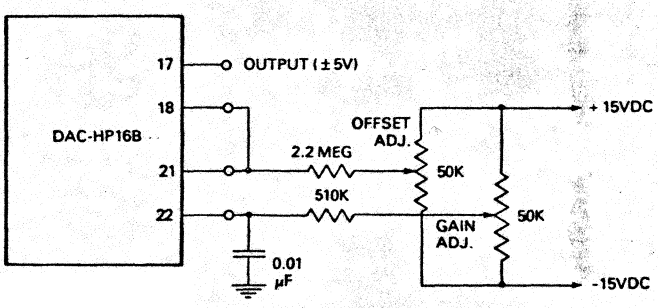
UNIPOLAR OUTPUT—Complementary Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0000 0000 0000 0000	+FS−1LSB	+9.99985V
0011 1111 1111 1111	+¾FS	+7.50000
0111 1111 1111 1111	+½FS	+5.00000
1011 1111 1111 1111	+¼FS	+2.50000
1111 1111 1111 1110	+1LSB	+153μV
1111 1111 1111 1111	0	0

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

Connect the converter as shown in the application diagrams. For bipolar operation connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation connect Bipolar Offset (pin 19) to Ground (pin 20). In making the following adjustments, refer to the coding tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output.
2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 (complementary binary) or 0110 0110 0110 0110 (complementary BCD) and adjust the GAIN ADJ. potentiometer to give +9.99985V output (complementary binary) or +9.999V output (complementary BCD).

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the Digital Input Code to 1111 1111 1111 1111 and adjust the OFFSET ADJ. potentiometer to give the −F.S. output shown in the coding table above for the model being calibrated.
2. **Gain Adjustment.** Set the Digital Input Code to 0000 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give the +FS-1 LSB output shown in the coding table above for the model being calibrated.

DATEL INTERSIL
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• Houston, (713)781-8886 • Dallas, TX (214)241-0651 OVERSEAS: DATEL (UK) LTD—TEL ANDOVER (0264)51055
• DATEL SYSTEMS SARL 602-57-11 • DATELEK SYSTEMS GmbH (089)77-60-95 • DATEL KK Tokyo 793-1031

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-506A/HI-507A

16 Channel Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK BEFORE MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME 500ns TYP.
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE 4mA TYP.
- STANDBY POWER 7.5mW TYP.

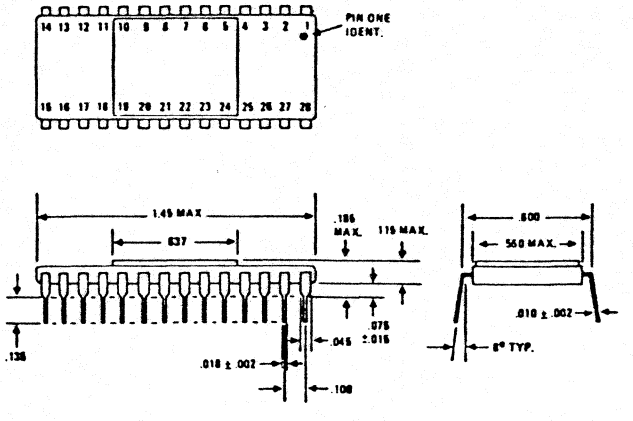
DESCRIPTION

The HI-506A and HI-507A analog multiplexers are constructed with the Harris Dielectric Isolation, Complementary MOS process. Digital and Analog inputs are protected from overvoltage inputs that exceed either supply voltage with no channel interaction. Channel interaction is also eliminated in the event of power loss. The HI-506A is a single-ended 16 channel multiplexer while the HI-507A is a differential 8 channel version. The devices are packaged in a 28 pin dual-in-line package and are available in both military and commercial temperature ranges.

PACKAGE

CODE 1L

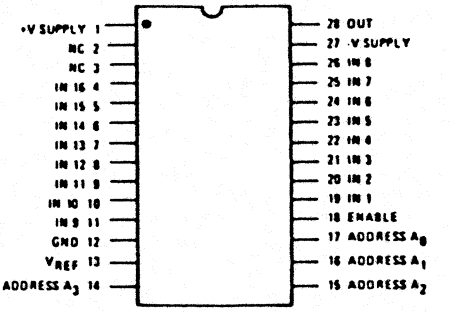
28 LEAD D.I.P.



PIN OUT/TRUTH TABLE

HI-506A

Top View

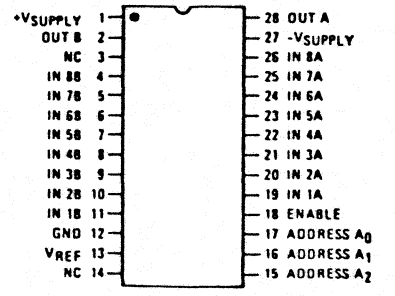


15 16 17 18

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

Top View



A_2	A_1	A_0	EN	"ON" SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 40V

V_{REF} to Ground +20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { $V_{Supply}(+)$ +4V; $V_{Supply}(-)$ -4V

Analog Input Overvoltage:

V_S { $V_{Supply}(+)$ +20V; $V_{Supply}(-)$ -20V

Total Power Dissipation* 1200mW

Operating Temperature:

HI-506A/HI-507A-2 -55°C to +125°C

HI-506A/HI-507A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified.

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		1.8	2.0	KΩ
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			± 250			± 250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (TTL Drive (Note 7))	Full			0.8			0.8	V
V_{AH}, Input High Threshold (TTL Drive (Note 7))	Full	4.0			4.0			V
V_{AL} (MOS Drive (Note 3))	+25°C			0.8			0.8	V
V_{AH} (MOS Drive (Note 3))	+25°C	6.0			6.0			V
* I_A, Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON (EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF (EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
"Off Isolation" (Note 4)	+25°C		65			65		dB
$C_{S (OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D (OFF)}$, Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS (OFF)}$, Input to Output Capacitance	+25°C		1			1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
* I_+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
* I_-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	2.0	mA
* I_+, Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
* I_-, Standby (Note 6)	Full		0.02	1.0		0.02	2.0	mA

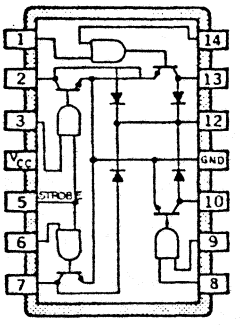
NOTES
1. V_{OUT} = ±10V, I_{OUT} = -100 μA
2. Analog Overvoltage = ± 33V
3. V_{REF} = +10V
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz
5. V_{EN} = +4.0V
6. V_{EN} = 0.8V
7. To drive from DTL/TTL circuits, 1KΩ Pull-up resistors to +5.0V supply are recommended

*100% Tested For DASH 8

Appendix 5.E.

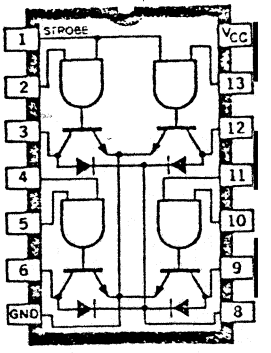
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNITS
Supply Voltage (V_{CC}):				
UHC-407, UHC-507	4.5	5.0	5.5	V
UHD-407, UHD-507	4.5	5.0	5.5	V
UHP-407, UHP-507	4.75	5.0	5.25	V
Operating Temperature Range:				
UHC-407, UHC-507.....	−55	25	+125	°C
UHD-407, UHD-507.....	−55	25	+125	°C
UHP-407, UHP-507	0	25	+70	°C
Current into any output (on state):		150	250	mA
Voltage on any output (off state):				
UHC-407, UHD-407, UHP-407			40	V
UHC-507, UHD-507, UHP-507			100	V



DWG. NO. A-7972

UHC-407
UHC-507



DWG. NO. A-7973

UHD-407 UHD-507
UHP-407 UHP-507

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

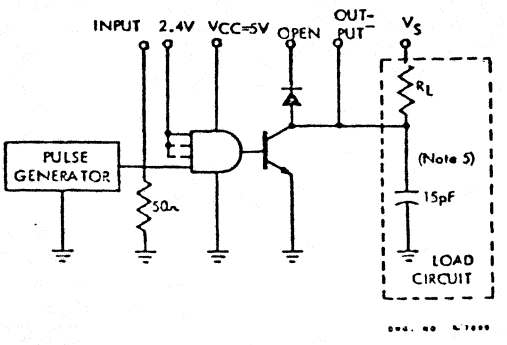
Characteristic	Symbol	Test Conditions: Temp.	V_{CC}	Driven Input	Other Input	Output	Limits: Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"1" Output Reverse Current Types UHC-407, UHD-407, and UHP-407	I_{off}		MIN	0.8V	V_{CC}	40V			50	μA	
"1" Output Reverse Current Types UHC-507, UHD-507, and UHP-507	I_{off}		MIN	0.8V	V_{CC}	100V			50	μA	
"0" Output Voltage Types UHP-407 and UHP-507	V_{on}		MIN	2.0V	2.0V	150mA			0.4	V	
			MIN	2.0V	2.0V	250mA			0.6	V	
"0" Output Voltage Types UHC-407 UHD-407, UHC-507, and UHD-507	V_{on}		MIN	2.0V	2.0V	150mA			0.5	V	
			MIN	2.0V	2.0V	250mA			0.7	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX		4.5V			−0.55	−0.8	mA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	2
			MAX	5.5V	0V				1	mA	
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				160	μA	2
			MAX	5.5V	0V				1	mA	
Diode leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	6
Diode Forward Voltage Drop	V_D	NOM	NOM	0V	0V			1.5		V	7
"1" Level Supply Current	$I_{CC(1)}$	NOM	NOM	0V	0V			6		mA	1, 3
"0" Level Supply Current	$I_{CC(0)}$	NOM	NOM	5V	5V			20		mA	1, 3

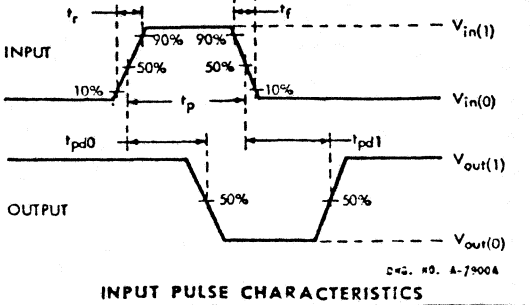
SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits: Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}						4
Types UHC-407, UHD-407, UHP-407		C_L=15pF, R_L=6W, 265Ω, R_S=40V		85		ns	
Types UHC-507, UHD-507, UHP-507		C_L=15pF, R_L=15W, 670Ω, R_S=100V		195		ns	
Turn-off Delay Time	t_{pd1}						4
Types UHC-407, UHD-407, UHP-407		C_L=15pF, R_L=6W, 265Ω, R_S=40V		95		ns	
Types UHC-507, UHD-507, UHP-507		C_L=15pF, R_L=15W, 670Ω, R_S=100V		220		ns	

NOTES:

1. Typical values are at V_{CC}=5.0V, T_A=25°C.
2. Each input tested separately.
3. Each gate.
4. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
5. Capacitance values specified include probe and test fixture capacitance.
6. Diode leakage current measured at $V_R = V_{off(min)}$.
7. Diode forward voltage drop measured at I_f=200mA.





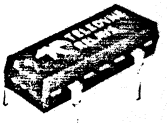
DWG. NO. A-7900A

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7 ns	t_p = 1 μs
$V_{in(1)}$ = 3.5V	t_r = 14 ns	PRR = 500kHz

TELEDYNE RELAYS

SERENDIP® Commercial/Industrial DIP Solid State Relays



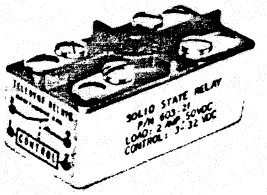
Subminiature solid state relays in standard TO-116 DIP packages. Featuring all solid state circuitry with hybrid microcircuit construction, and high input/output isolation (up to 2500 volts/10^9 ohms). Six models available providing choice of output: bipolar (ac or dc), ac (triac), and dc (transistor). Bipolar (640/644 series) and dc (643 series) are direct pin-for-pin replacements for standard DIP reed relays. AC versions (641 series) are UL Recognized — File #E55197.

PART NUMBER	INPUT DATA		OUTPUT (LOAD) RATINGS			
	VOLTAGE (VDC)	MAX. CURRENT (MADC @ 5V)	AC/DC	CURRENT @ 10V INPUT	CURRENT @ 5V INPUT	VOLTAGE
640-1	3.8-10	22	BIPOLAR (AC or DC)	80 MA	40 MA	$\pm 50\ V_{PEAK}$
641-1	3.8-10	15	AC	0.5 A (Note 1)	0.5 A	$140\ V_{RMS}$
641-2	3.8-10	15	AC	0.5 A (Note 1)	0.5 A	$280\ V_{RMS}$
643-1	3.8-10	15	DC	400 MA	200 MA	$60\ V_{DC}$
643-2	3.8-10	15	DC	100 MA	50 MA	$250\ V_{DC}$
644-1	3.8-6	18	BIPOLAR (AC or DC) (Note 2)	5 MA	5 MA	$\pm 5\ V_{PEAK}$

Notes:
1. 1 amp with heat sink. Standard DIP heat sink, Model 640HS, available as accessory.
2. Features low offset voltge (100 microvolts typical).

Solid State DC Relay

603 Series - Optically Isolated



Solid state DC relays featuring LED optical isolation. SPST, normally open. Available in 2 and 5 amp steady state current ratings, up to 50 vdc. Sensitive 3-32 vdc control input is compatible with both low and high level logic systems. As an added option, controlled rise and fall time is offered to limit in-rush currents for lamp loads and switching transients for inductive loads. Package configuration provides either screw or quick disconnect terminals for chassis or panel mounting or solder pins for direct PC board mounting.

Size: 1″ (25.4 mm) x 2″ (50.8 mm) x .9″ (22.9 mm).

PART NUMBER	OUTPUT CURRENT RATING (AMPS)	
603-1	2	
603-2	5	
603-21	2	Controlled Rise & Fall Time
603-22	5	

Basic part number provides screw terminals.
Add suffix "P" for PC board pins, "Q" for quick disconnect terminals.

Am9513

System Timing Controller
Advanced Micro Devices
Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package
- 100% MIL-STD-883 reliability assurance testing

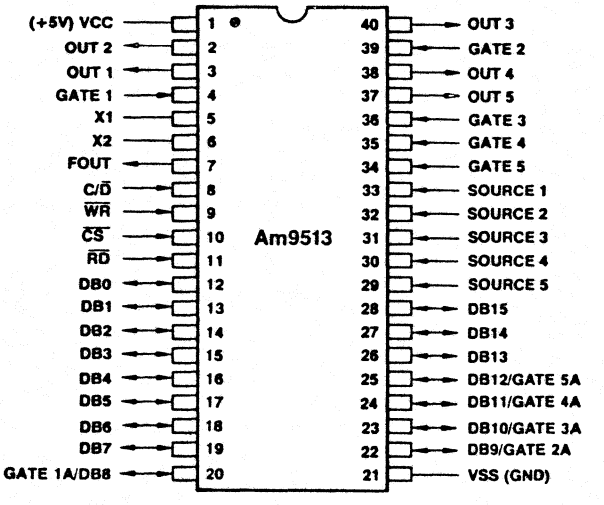
GENERAL DESCRIPTION

The Am9513 System Timing Controller is an LSI circuit designed to service many types of courting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the Am9513 to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide either pulses or levels. The counters can be programmed to count up or down in either binary or BCD. The accumulated count may be read without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits.

TABLE OF CONTENTS

CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation. MOS-172

Figure 1.

ORDERING INFORMATION

Package Type	Temperature Range	Counting Frequency	
		7MHz	
Molded	$0°C \leq T_A \leq +70°C$	AM9513PC	
Hermetic*		AM9513DC	
		AM9513CC	
Hermetic	$-55°C \leq T_A \leq +125°C$	AM9513DM	

*Hermetic = Ceramic = DC = CC = D-40-1.

GENERAL BLOCK DIAGRAM

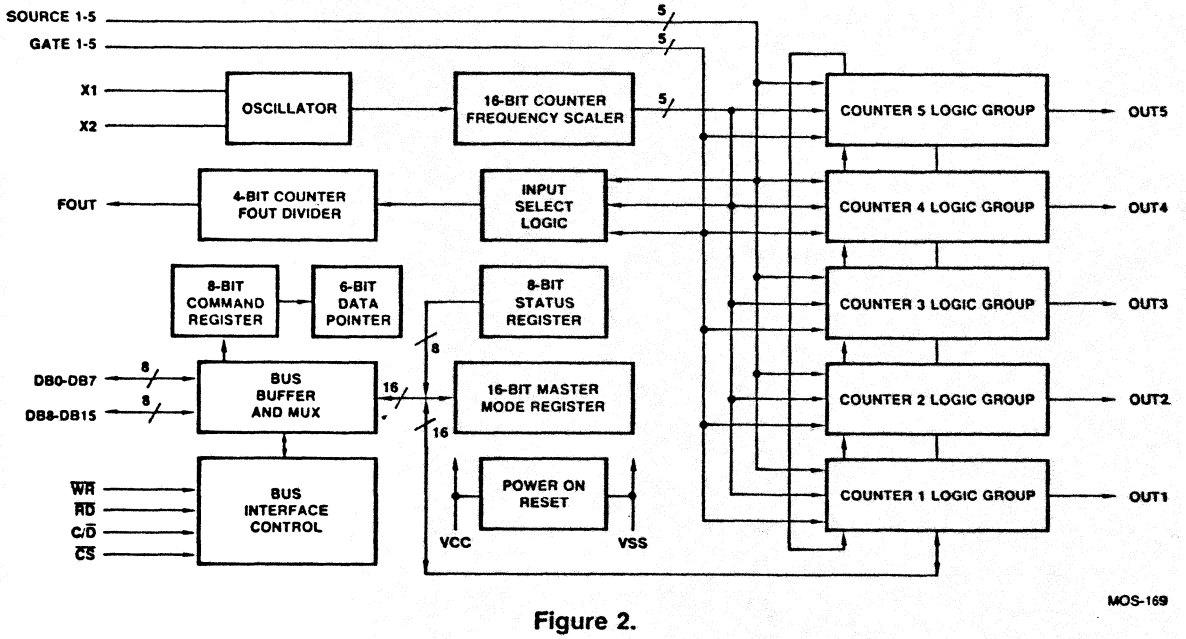


Figure 2.

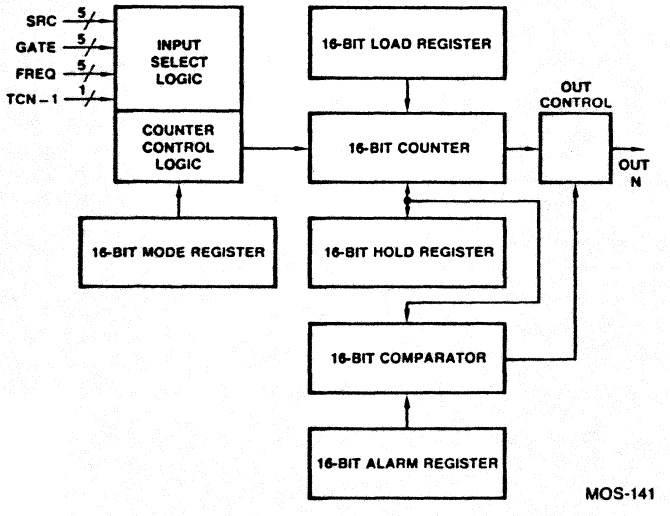


Figure 3. Counter Logic Groups 1 and 2.

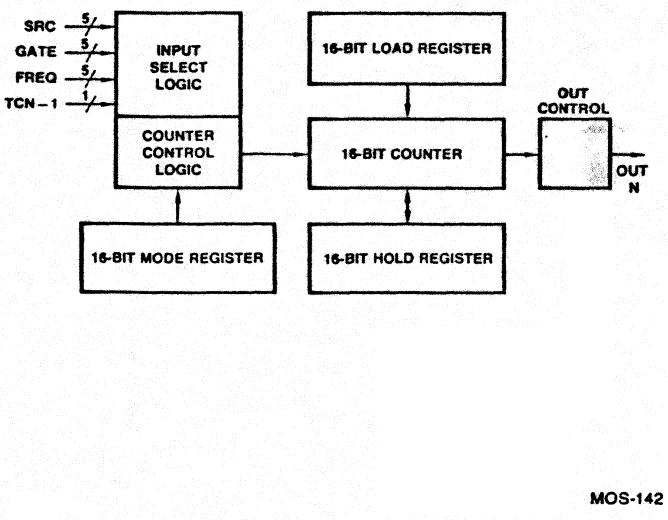


Figure 4. Counter Logic Groups 3, 4 and 5.

INTERFACE SIGNAL DESCRIPTION

Figure 5 summarizes the interface signals and their abbreviations for the STC. Figure 1 shows the signal pin assignments for the standard 40-pin dual in-line package.

VCC: +5 volt power supply

VSS: Ground

X1, X2 (Crystal)

X1 and X2 are the connections for an external crystal used to determine the frequency of the internal oscillator. The crystal should be a parallel-resonant, fundamental-mode type. An RC or LC or other reactive network may be used instead of a crystal. For driving from an external frequency source, X1 should be left open and X2 should be connected to a TTL source and a pull-up resistor.

FOUT (Frequency Out, Output)

The FOUT output is derived from a 4-bit counter that may be programmed to divide its input by any integer value from 1 through 16 inclusive. The input to the counter is selected from any of 15 sources, including the internal scaled oscillator frequencies. FOUT may be gated on and off under software control and when off will exhibit a low impedance to ground. Control over the various FOUT options resides in the Master Mode register. After power-up, FOUT provides a frequency that is 1/16 that of the oscillator.

GATE1-GATE5 (Gate, Inputs)

The Gate inputs may be used to control the operations of individual counters by determining when counting may proceed. The same Gate input may control up to three counters. Gate pins may also be selected as count sources for any of the counters and for the FOUT divider. The active polarity for a selected Gate input is programmed at each counter. Gating function options allow level-sensitive gating or edge-initiated gating. Other gating

modes are available including one that allows the Gate input to select between two counter output frequencies. All gating functions may also be disabled. The active Gate input is conditioned by an auxiliary input when the unit is operating with an external 8-bit data bus. See Data Bus description. Schmitt-trigger circuitry on the GATE inputs allows slow transition times to be used.

SRC1-SRC5 (Source, Inputs)

The Source inputs provide external signals that may be counted by any of the counters. Any Source line may be routed to any or all of the counters and the FOUT divider. The active polarity for a selected SRC input is programmed at each counter. Any duty cycle waveform will be accepted as long as the minimum pulse width is at least half the period of the maximum specified counting frequency for the part. Schmitt-trigger circuitry on the SRC inputs allows slow transition times to be used.

OUT1-OUT5 (Counter, Outputs)

Each 3-state OUT signal is directly associated with a corresponding individual counter. Depending on the counter configuration, the OUT signal may be a pulse, a square wave, or a complex duty cycle waveform. OUT pulse polarities are individually programmable. The output circuitry detects the counter state that would have been all bits zero in the absence of a reinitialization. That information is used to generate the selected waveform type. An optional output mode for Counters 1 and 2 overrides the normal output mode and provides a true OUT signal when the counter contents match the contents of an Alarm register.

DB0-DB7, DB8-DB15 (Data Bus, Input/Output)

The 16, bidirectional Data Bus lines are used for information exchanges with the host processor. HIGH on a Data Bus line corresponds to one and LOW corresponds to zero. These lines act as inputs when $\overline{WR}$ and $\overline{CS}$ are active and as outputs when $\overline{RD}$ and $\overline{CS}$ are active. When $\overline{CS}$ is inactive, these pins are placed in a high-impedance state.

After power-up or reset, the data bus will be configured for 8-bit width and will use only DB0 through DB7. DB0 is the least significant and DB7 is the most significant bit position. The data bus may be reconfigured for 16-bit width by changing a control bit in the Master Mode register. This is accomplished by writing an 8-bit command into the low-order DB lines while holding the DB13-DB15 lines at a logic high level. Thereafter all 16 lines can be used, with DB0 as the least significant and DB15 as the most significant bit position.

When operating in the 8-bit data bus environment, DB8-DB15 will never be driven active by the Am9513. DB8 through DB12 may optionally be used as additional Gate inputs (see Figure 6). If unused they should be held high. When pulled low, a GATENA signal will disable the action of the corresponding counter N gating. DB13-DB15 should be held high in 8-bit bus mode whenever CS and WR are simultaneously active.

$\overline{CS}$ (Chip Select, Input)

The active-low Chip Select input enables Read and Write operations on the data bus. When Chip Select is high, the Read and Write inputs are ignored. The first Chip Select signal after power-up is used to clear the power-on reset circuitry.

$\overline{RD}$ (Read, Input)

The active-low Read signal is conditioned by Chip Select and indicates that internal information is to be transferred to the data bus. The source will be determined by the port being addressed and, for Data Port reads, by the contents of the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.

$\overline{WR}$ (Write, Input)

The active-low Write signal is conditioned by Chip Select and indicates that data bus information is to be transferred to an internal location. The destination will be determined by the port being addressed and, for Data Port writes, by the contents of the Data Pointer register. $\overline{WR}$ and $\overline{RD}$ should be mutually exclusive.

C/$\overline{D}$ (Control/Data, Input)

The Control/Data signal selects source and destination locations for read and write operations on the data bus. Control Write operations load the Command register and the Data Pointer. Control Read operations output the Status register. Data Read and Data Write transfers communicate with all other internal registers. Indirect addressing at the data port is controlled internally by the Data Pointer register.

Signal	Abbreviation	Type	Pins
+5 Volts	VCC	Power	1
Ground	VSS	Power	1
Crystal	X1, X2	I/O, I	2
Read	$\overline{RD}$	Input	1
Write	$\overline{WR}$	Input	1
Chip Select	$\overline{CS}$	Input	1
Control/Data	C/$\overline{D}$	Input	1
Source N	SRC	Input	5
Gate N	GATE	Input	5
Data Bus	DB	I/O	16
Frequency Out	FOUT	Output	1
Out N	OUT	Output	5

Figure 5. Interface Signal Summary.

Package Pin	Data Bus Width (MM14)	
	16 Bits	8 Bits
12	DB0	DB0
13	DB1	DB1
14	DB2	DB2
15	DB3	DB3
16	DB4	DB4
17	DB5	DB5
18	DB6	DB6
19	DB7	DB7
20	DB8	GATE 1A
22	DB9	GATE 2A
23	DB10	GATE 3A
24	DB11	GATE 4A
25	DB12	GATE 5A
26	DB13	(VIH)
27	DB14	(VIH)
28	DB15	(VIH)

Figure 6. Data Bus Assignments.

FUNCTIONAL DESCRIPTION

The Am9513 block diagrams (Figures 2, 3 and 4) indicate the interface signals and the basic flow of information. Internal control lines and the internal data bus have been omitted. The control and data registers are all connected to a common internal 16-bit bus. The external bus may be 8 or 16 bits wide; in the 8-bit mode the internal 16-bit information is multiplexed to the low order data bus pins DB0 through DB7.

An internal oscillator provides a convenient source of frequencies for use as counter inputs. The oscillator's frequency is controlled at the X1 and X2 interface pins by an external reactive network such as a crystal. The oscillator output is divided by the Frequency Scaler to provide several sub-frequencies. One of the scaled frequencies (or one of ten input signals) may be selected as an input to the FOUT divider and then comes out of the chip at the FOUT interface pin.

The STC is addressed by the external system as two locations: a control port and a data port. The control port provides direct access to the Status and Command registers, as well as allowing the user to update the Data Pointer register. The data port is used to communicate with all other addressable internal locations. The Data Pointer register controls the data port addressing.

Among the registers accessible through the data port are the Master Mode register and five Counter Mode registers, one for each counter. The Master Mode register controls the programmable options that are not controlled by the Counter Mode registers.

Each of the five general-purpose counters is 16 bits long and is independently controlled by its Counter Mode register. Through this register, a user can software select one of 16 sources as the counter input, a variety of gating and repetition modes, up or down counting in binary or BCD and active-high or active-low input and output polarities.

Associated with each counter are a Load register and a Hold register, both accessible through the data port. The Load register is used to automatically reload the counter to any predefined value, thus controlling the effective count period. The Hold register is used to save count values without disturbing the count process, permitting the host processor to read intermediate counts. In addition, the Hold register may be used as a second Load register to generate a number of complex output waveforms.

All five counters have the same basic control logic and control registers. Counters 1 and 2 have additional Alarm registers and comparators associated with them, plus the extra logic necessary for operating in a 24-hour time-of-day mode. For real-time operation the time-of-day logic will accept 50Hz, 60Hz or 100Hz input frequencies.

Each general counter has a single dedicated output pin. It may be turned off when the output is not of interest or may be configured in a variety of ways to drive interrupt controllers, Darlington buffers, bus drivers, etc. The counter inputs, on the other hand, are specifically not dedicated to any given interface line. Considerable versatility is available for configuring both the input and the gating of individual counters. This not only permits dynamic reassignment of inputs under software control, but also allows multiple counters to use a single input, and allows a single gate pin to control more than one counter. Indeed, a single pin can be the gate for one counter and, at the same time, the count source for another.

A powerful command structure simplifies user interaction with the counters. A counter must be armed by one of the ARM commands before counting can commence. Once armed, the counting process may be further enabled or disabled using the hardware gating facilities. The ARM and DISARM commands permit software gating of the count process in some modes.

The LOAD command causes the counter to be reloaded with the value in either the associated Load register or the associated Hold register. It will often be used as a software retrigger or as counter initialization prior to active hardware gating.

The DISARM command disables further counting independent of any hardware gating. A disarmed counter may be reloaded using the LOAD command, may be incremented or decremented using the STEP command and may be read using the SAVE command. A count process may be resumed using an ARM command.

The SAVE command transfers the contents of a counter to its associated Hold register. This command will overwrite any previous Hold register contents. The SAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host CPU at some later time.

Two combinations of the basic commands exist to either LOAD AND ARM or to DISARM AND SAVE any combination of counters. Additional commands are provided to: step an individual counter by one count; set and clear an output toggle; issue a software reset; clear and set special bits in the Master Mode register; and load the Data Pointer register.

CONTROL PORT REGISTERS

The STC is addressed by the external system as only two locations: a Control port and a Data port. Transfers at the Control port (C/$\overline{D}$ = High) allow direct access to the command register when writing and the status register when reading. All other available internal locations are accessed for both reading and writing via the Data port (C/$\overline{D}$ = Low). Data port transfers are executed to and from the location currently addressed by the Data Pointer register. Options available in the Master Mode register and the Data Pointer control structure allow several types of transfer sequencing to be used. See Figure 7.

Transfers to and from the control port are always 8 bits wide. Each access to the Control port will transfer data between the Command register (writes) or Status register (reads) and Data Bus pins DB0-DB7, regardless of whether the Am9513 is in 8- or 16-bit bus mode. When the Am9513 is in 8-bit bus mode, Data Bus pins DB13-DB15 should be held at a logic high whenever $\overline{CS}$ and $\overline{WR}$ are both active.

Command Register

The Command register provides direct control over each of the five general counters and controls access through the Data port by allowing the user to update the Data Pointer register. The "Command Description" section of this data sheet explains the detailed operation of each command. A summary of all commands appears in Figure 21. Six of the command types are used for direct software control of the counting process. Each of these six commands contains a 5-bit S field. In a linear-select fashion, each bit in the S field corresponds to one of the five general counters (S1 = Counter 1, S2 = Counter 2, etc.). When an S bit is a one, the specified operation is performed on the counter so designated; when an S bit is a zero, no operation occurs for the corresponding counter.

Data Pointer Register

The 6-bit Data Pointer register is loaded by issuing the appropriate command through the control port to the Command register. As shown in Figure 7, the contents of the Data Pointer register are used to control the Data Port multiplexer, selecting which internal register is to be accessible through the Data Port.

The Data Pointer consists of a 3-bit Group Pointer, a 2-bit Element Pointer and a 1-bit Byte Pointer, depicted in Figure 8. The Byte Pointer bit indicates which byte of a 16-bit register is to be transferred on the next access through the data port. Whenever the Data Pointer is loaded, the Byte Pointer bit is set to one, indicating a least-significant byte is expected. The Byte Pointer toggles following each 8-bit data transfer with an 8-bit data bus (MM13 = 0), or it always remains set with the 16-bit data bus option (MM13 = 1). The Element and Group pointers are used to select which internal register is to be accessible through the Data Port. Although the contents of the Element and Group Pointer in the Data Pointer register cannot be read by the host processor, the Byte Pointer is available as a bit in the Status register.

Random access to any available internal data location can be accomplished by simply loading the Data Pointer using the command shown in Figure 9 and then initiating a data read or data write. This procedure can be used at any time, regardless of the setting of the Data Pointer Control bit (MM14). When the 8-bit data bus configuration is being used (MM13 = 0), two bytes of data would normally be transferred following the issuing of the "Load Data Pointer" command.

To permit the host processor to rapidly access the various internal registers, automatic sequencing of the Data Pointer is provided. Sequencing is enabled by clearing Master Mode bit 14 (MM14) to zero. As shown in Figure 10, several types of sequencing are available depending on the data bus width being used and the initial Data Pointer value entered by command.

When E1 = 0 or E2 = 0 and G4, G2, G1 point to a Counter Group, the Data Pointer will proceed through the Element cycle. The Element field will automatically sequence through the three values 00, 01 and 10 starting with the value entered. When the transition from 10 to 00 occurs, the Group field will also be incremented by one. Note that the Element field in this case does not sequence to a value of 11. The Group field circulates only within the five Counter Group codes.

If E2, E1 = 11 and a Counter Group is selected, then only the Group field is sequenced. This is the Hold cycle. It allows the Hold registers to be sequentially accessed while bypassing the Mode and Load registers. The third type of sequencing is the Control

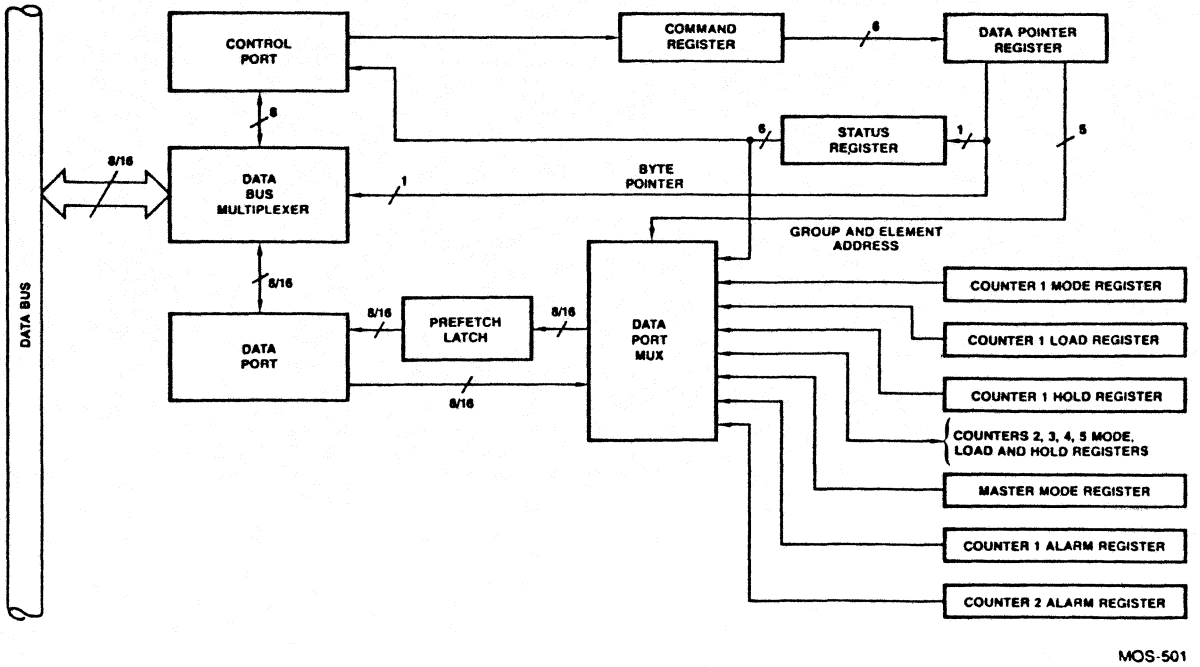


Figure 7. Am9513 Register Access.

High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

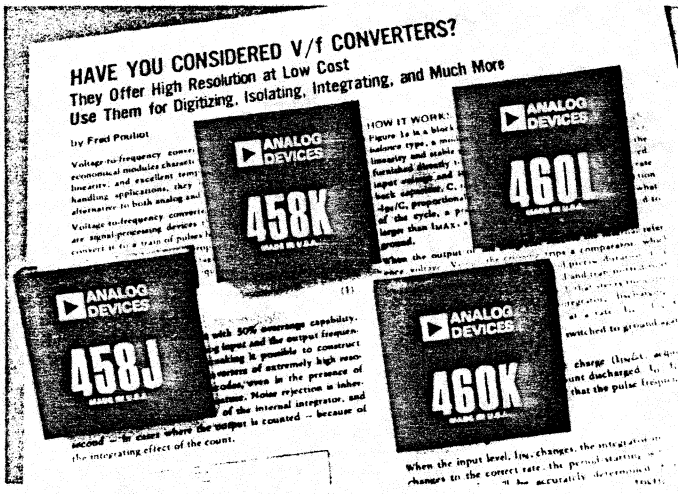
MODELS 458 and 460

FEATURES

High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
Low Nonlinearity: 100ppm max, Model 458
150ppm max, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS

Fast Analog-to-Digital Converter
High Resolution Optical Data Link
Ratiometric Measurements
2-Wire High Noise Immunity Digital Transmission
Long Term Precision Integrator



GENERAL DESCRIPTION

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of ±0.01% maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of ±0.015% over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industries' first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to ±10V, as well as ground referenced positive, 0 to +11V or negative, 0 to -11V signals. Both models also accept positive current signals: 0 to +0.5mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

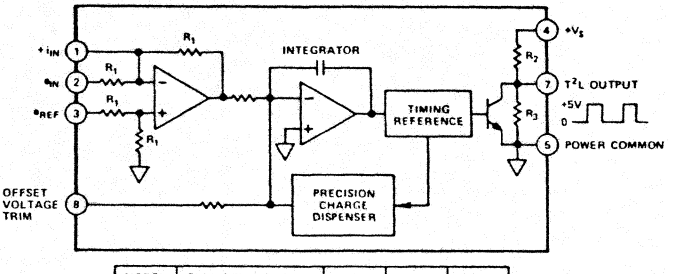
The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems – two wire data transmission over long wires; in 5½ digit DVM's – featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications – accurate ratiometric measurements over wide dynamic range.

DESIGN APPROACH - PRECISION CHARGE BALANCE

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stability - see Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to ±5V.



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram - Models 458, 460

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Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise noted)

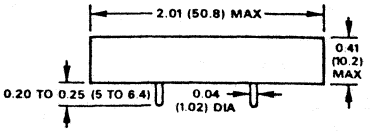
MODEL	100kHz Full Scale 458 J	K	L	1MHz Full Scale 460 J	K	L
TRANSFER FUNCTION						
Voltage Input	$f_{OUT} = (10^4 Hz/V)\ e_{IN}$			$f_{OUT} = (10^5 Hz/V)\ e_{IN}$		
Current Input	$f_{OUT} = (2 \times 10^5 Hz/mA)\ i_{IN}$			$f_{OUT} = (10^6 Hz/mA)\ i_{IN}$		
ANALOG INPUT						
Configuration	Differential			Differential		
Voltage Signal Range						
e_{IN} Terminal (e_{REF} = 0)	0 to +10V dc min			0 to +10V dc min		
e_{REF} Terminal (e_{IN} = 0)	0 to -10V dc min			0 to -10V dc min		
Differential ($e_{IN} - e_{REF}$)	0 to +10V dc min			0 to +10V dc min		
Overrange	+10% min			+10% min		
Current Signal Range (i_{IN})	0 to +0.5mA min			0 to +1mA min		
Common Mode Voltage	±10V			±10V		
Common Mode Rejection	40dB			40dB		
Impedance, e_{IN} Terminal	20kΩ			10kΩ		
e_{REF} Terminal	40kΩ			20kΩ		
i_{IN} Terminal	0Ω			0Ω		
Max Safe Input	$\pm V_S$			$\pm V_S$		
ACCURACY						
Warm Up Time	5 Seconds to 0.01%			2 Minutes to 0.02%		
Nonlinearity, e_{IN} = +0.1mV to +11V	±0.01% of Full Scale, max			±0.015% of Full Scale, max		
e_{IN} = -0.1mV to -11V	±0.01% of Full Scale			±0.015% of Full Scale		
Full Scale Error[1]	+0.1% to +2%, max			+0.1% to +2%, max		
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max	±10ppm/°C max	±5ppm/°C max	±50ppm/°C max	±25ppm/°C max	±15ppm/°C max
vs. Supply Voltage	±15ppm/%			±25ppm/%		
vs. Time	±10ppm/day			±10ppm/day		
Input Offset Voltage[2]	±10mV max			±10mV max		
vs. Temperature (0 to +70°C)	±30μV/°C max			±30μV/°C max		
vs. Supply Voltage	±10μV/%			±10μV/%		
vs. Time	±20ppm/day			±10ppm/day		
RESPONSE						
Settling Time, ±0.01% +10V Step	3 Output Pulses Plus 2μs			2 Output Pulses Plus 2μs		
Overload Recovery Time	10ms			1ms		
FREQUENCY OUTPUT[3]						
Waveform	TTL/DTL Compatible Pulses			TTL/DTL Compatible Pulses		
Pulse Width	5μs			500ns		
Rise and Fall Time	300ns/50ns			60ns/50ns		
Pulse Polarity	Positive			Positive		
Logic "1" (High) Level	+2.4V min			+2.4V min		
Logic "0" (Low) Level	+0.4V max			+0.4V max		
Capacitive Loading	500pF max			200pF max		
Fan Out Loading	10 TTL Loads min			10 TTL Loads min		
Impedance	3kΩ (High State)			670Ω (High State)		
POWER SUPPLY[4]						
Voltage, Rated Performance	±15V dc			±15V dc		
Voltage, Operating	±(13 to 18)V dc			±(13 to 18)V dc		
Current, Quiescent	(+25, -8)mA			(+25, -8)mA		
TEMPERATURE RANGE						
Rated Performance	0 to +70°C			0 to +70°C		
Operating	-25°C to +85°C			-25°C to +85°C		
Storage	-55°C to +125°C			-55°C to +125°C		
MECHANICAL						
Case Size	2" x 2" x 0.4"			2" x 2" x 0.4"		
Weight	45 Grams			45 Grams		
Mating Socket	AC1016			AC1016		

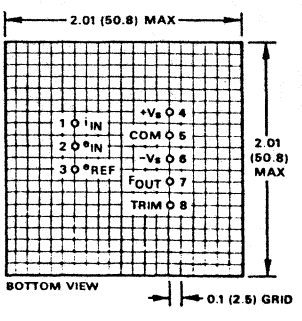
[1] Adjustable to zero using 500Ω potentiometer.
[2] Adjustable to zero using 50kΩ potentiometer.
[3] Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the $+V_S$ supply. Output is not protected for shorts to the $-V_S$ supply.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





Appendix 5.I.

VOLTAGE TO FREQUENCY OPERATION

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits. Adding a resistor from the output terminal, pin 7, to the +15V supply (1.2kΩ model 458; 820Ω model 460), shifts the output swing from 0 to +5V to 0 to +12V, providing a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

BASIC V/F HOOK-UP AND OPTIONAL TRIMS

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale (e_{IN} = 10V) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on.

V/F INTERCONNECTIONS

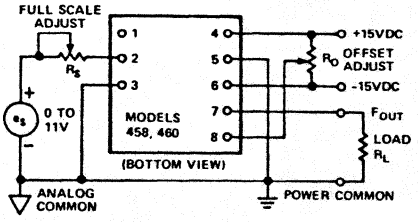


Figure 2. Positive Input Signal

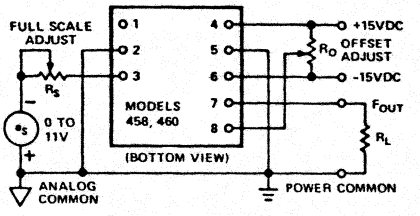


Figure 3. Negative Input Signal

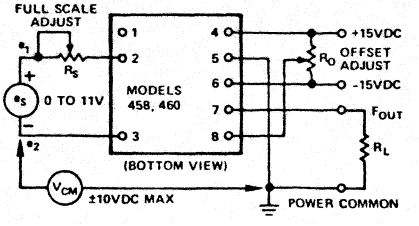


Figure 4. Floating Input Signal

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, < 50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, < 50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TERMINAL TO -15V

Using a precision, stable voltage source, set the input voltage e_S, to 10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 sec (model 458) or 0.01 sec (model 460). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

DIFFERENTIAL INPUT

The e_{IN} and e_{REF} input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

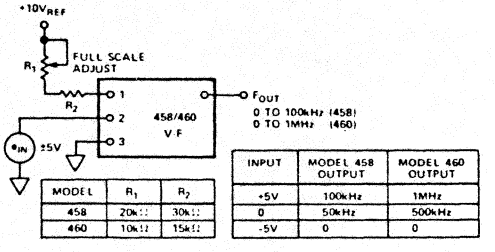
To apply the 458 or 460 voltage inputs differentially, the e_{IN} pin must always be positive with respect to the e_{REF} pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to ±10V max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{\text{INPUT SIGNAL}} + \underbrace{\left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}} \right] K_g$$

$K_g = 10^4$ Hz/V; model 458
10^5 Hz/V; model 460

OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal, $+i_{IN}$, may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.



MODEL	R_1	R_2
458	20kΩ	30kΩ
460	10kΩ	15kΩ

INPUT	MODEL 458 OUTPUT	MODEL 460 OUTPUT
+5V	100kHz	1MHz
0	50kHz	500kHz
-5V	0	0

Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200μs before input scaling, to 20μs with scaling.

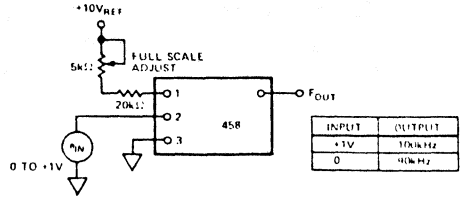


Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.

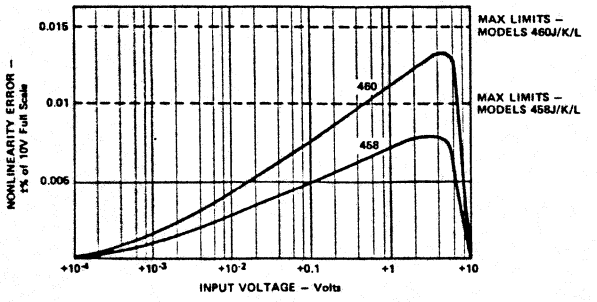


Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.

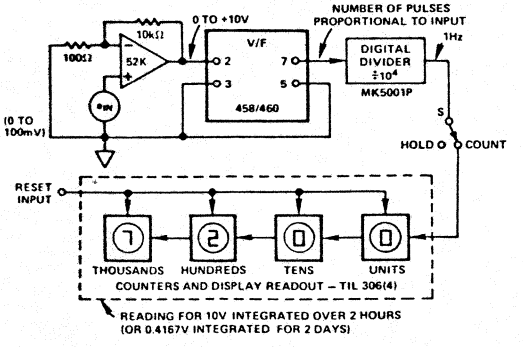


Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units

RATIOMETRIC MEASUREMENTS

The circuit shown in Figure 9 illustrates a simple and inexpensive way of using two 100kHz V/F converters to achieve ratiometric measurements with less than 0.1% error over a dynamic range of 10,000 to 1. One converter is used as the input V/F to a digital counter and display, while a second converter, with a digital divide-by-N circuit is used as the time base for the counter. The counting time is one half the output period of the divide-by-N circuit, resulting in an output count of $2NV_1/V_{REF}$.

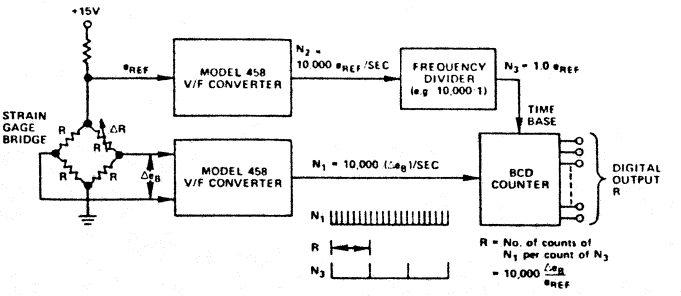


Figure 9. High Resolution, Wide-Range Ratiometer Using Model 458 V/F Converter

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

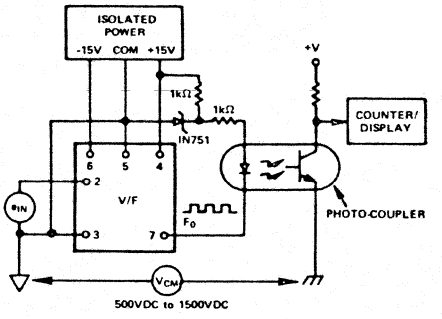


Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500VDC CMV Isolation

APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.

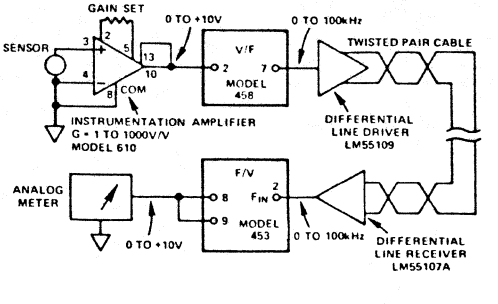


Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System