NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 209

SPECTRUM EXPANDER FOR 256-CHANNEL (100 kHz PER CHANNEL) MULTIFILTER RECEIVER

RICHARD J. LACASSE

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SPECTRUM EXPANDER FOR 256-CHANNEL (100 kHz PER CHANNEL) MULTIFILTER RECEIVER

Richard J. Lacasse

1.0 Introduction

The purpose of this report is to document the specifications and operations of a Spectrum Expander designed to increase the resolution of a filter bank receiver. First, the basic theory of operation is explained. Then specifications are presented. Black box and detailed electronics descriptions are included. Appendix A shows mechanical construction details.

2.0 Basic Theory of Operation

The heart of the Spectrum Expander is a memory system. Samples of the input voltage are digitized and written into successive locations in memory, looping back to the beginning of memory when the end is reached. Similarly, these samples are read out of memory. By means of a slightly involved memory control scheme which is discussed later, memory can be written into at rate R_i and read out at rate R_0, essentially simultaneously. The ratio R_0/R_i, which we call E, is the factor by which the spectrum is expanded, as explained below.

An ideal spectrum expander would have the following input-output relationship:

$$S_0(f) = S_i\left(\frac{f}{E}\right)$$

where $S_0(f)$ and $S_i(f)$ are output and input spectra, respectively. When implemented as discussed above, however, the following relationship applies:

$$S_0(f) = \sum_{n=-\infty}^{\infty} S_i^{\,s}\,[f - n\varepsilon(E-1)]\,\mathrm{sinc}^2\left(\frac{f - nE\varepsilon}{\varepsilon}\right)$$

where

$S_i^s(f)$ is the spectrum of the sampled input.

$\varepsilon \triangleq R_i/M$ where M is the memory length.

$\text{sinc}^2(x) = \frac{\sin x}{x}$ (See Ref. 1.)

This can be interpreted, albeit a little loosely, as that the output spectrum is equal to the expanded input spectrum, weighted by a train of sinc^2 functions spaced $E\varepsilon$ (or equivalently, R_0/M) apart. In fact, this is about what is seen on a spectrum analyzer, as shown in Figure 1. One of the design goals then is to choose parameters such that successive sinc^2 functions fall into successive channels of the filter receiver. In this case the filter receiver involved has a filter separation of 100 kHz. The spectrum expander was designed with

$$M = 1024$$

$$R_0 = 102.4 \text{ MHz}$$

to also give 100 kHz spacing.

3.0 Specifications

This section describes the capabilities and requirements of the Spectrum Expander, as well as the function of all connectors, switches, etc. Reference to Figures 2 and 3 is helpful in the following.

3.1 General

The Spectrum Expander provides manual or computer controlled spectrum expansion of a 150 MHz IF signal. Expansion factors available are 4, 8, 16. Arbitrary expansion factors may be achieved using external oscillators and and filters, within the limits described below. A warm-up period of $\geq$ 10 min is required by the oscillators internal to the Spectrum Expander.

3.2 Front Panel

POWER CIRCUIT BREAKER: Controls 115 V AC, 60 Hz power to all modules.

MODE CONTROL TOGGLE SWITCH: Determines computer (remote) or manual (local) control of the expansion factor.

EXPANSION FACTOR ROTARY SWITCH: In manual mode, determines the expansion factor.

MANUAL LED: Indicates that the expansion factor is selected by the EXPANSION FACTOR ROTARY SWITCH.

COMPUTER LED: Indicates that the expansion factor is remotely selected.

EXPANSION FACTOR LED's: Indicate which expansion factor is selected, in either manual or computer mode.

VIDEO INPUT MONITOR BNC: A 50 ohm output useful for monitoring the unexpanded baseband. Leave terminated when not in use.

VIDEO OUTPUT MONITOR BNC: A 50 ohm output, useful for monitoring the expanded baseband. Leave terminated when not in use.

SIGNAL LEVEL METER: Monitors the level of the expanded baseband signal. The green area indicates the normal operating range. A zero reading is obtained in BYPASS mode.

VARIABLE ATTENUATOR: Attenuates the IF input signal. It should be adjusted to keep the signal level meter in the normal operating range.

3.3 Rear Panel

IF IN BNC: A 50 ohm input which accepts the spectrum to be expanded. The following limitations apply:

Center Frequency = 150 MHz.

Signal Power Level $\geq$ -59 dBm/MHz.

IF OUT BNC: A 50 ohm output consisting of the expanded spectrum, centered at 150 MHz with a power level of approximately -45 dBm when the signal level meter reads midscale.

COMPUTER INPUT CONNECTOR: Four signals, CCON+, CCON-, POK+, POK-, are emitted from this connector. CCON+ is a TTL high when COMPUTER mode is selected via the front panel switch, and is a TTL low in MANUAL mode. POK+ is a TTL high when the signal level meter reads in the green area, and is low otherwise.

COMPUTER INPUT CONNECTOR (continued):
CCON- and POK- are logical complements of CCON+ and POK+, respectively.

In computer mode, this connector accepts six signals, CMOØ+, CMOØ-, CMO1+, CMO1-, CMO2+, CMO2-, from the controlling device. These are used to set the expansion factor according to the following table:

CMOØ1	CMO1+	CMO2+	Expansion Factor
0	0	0	Bypass
0	0	1	x4
0	1	0	x8
0	1	1	x16
1	0	0	External

TABLE 3.1: Computer mode control signals. A "0" represents a TTL low and a "1" a TTL high. CMOØ-, CMO1-, and CMO2- are the logical complements of CMOØ+, CMO1+, and CMO2+, respectively,

See Figure A3 for the pin-outs of this connector.

EXTERNAL MODE INPUTS: The following inputs are required only when the EXTERNAL expansion factor is selected. Reference to Figure 4 is useful in understanding their functions.

EXTERNAL FILTER BNC's: A filter between these two BNC's determines the bandwidth of the signal to be expanded.

EXTERNAL OSC. BNC: This oscillator determines the center-frequency of the spectrum to be expanded. The following limitations apply:

Waveform	Sine wave.
Power Level	7 ± 1 dBm.
Frequency	$5 \text{ MHz} \leq f \leq 100 \text{ MHz}$.

F_0 BNC: This oscillator determines the memory read-out rate.

The output spectra has a comb spacing of $F_0/1024$. The following limitations apply:

Waveform	Sine or square.
Power Level	7 ± 1 dBm.
Frequency	$5 \text{ MHz} \leq f < 120 \text{ MHz}$.

F_I BNC: This oscillator determines the sampling rate and this must be picked to satisfy the Nyquist criterion. The following limitations also apply:

F_IBNC (continued):

Waveform	Sine or square.
Power Level	7 ± 1 dBm.
Frequency	5 MHz ≤ f ≤ 30 MHz, or .625 F_0, whichever is less.

The expansion factor achieved is F_0/F_I.

4.0 Block Diagram Description

The purpose of this section is to give an overview of the Spectrum Expander's operation, without getting overly bogged down in details. It is divided into three subsections describing the IF Input Electronics, the Digital Electronics, and the IF Output Electronics. Figure 4 complements this description.

4.1 IF Input Electronics

The IF Input Electronics amplifies, filters, and frequency shifts the input signal to generate an input acceptable to the Digital Electronics. Signal flow is as follows. The IF IN signal first encounters the Input Switch. This switch routes the signal directly back to the IF OUT when the Bypass Expansion Factor is selected; otherwise, the signal is sent through the remainder of the Spectrum Expander electronics. Assuming Bypass is not selected, the signal goes through a variable attenuator, which is used to set signal power levels, and then through at 150/10 MHz filter. Subsequently, the signal is amplified and mixed from a center frequency of 150 MHz to 30 MHz. It then goes through a 20 dB attenuator whose primary function is to attenuate LO leakage from the previous stage. Then it goes to the Filter Board where it is further amplified, and filtered by one of four filters, as determined by the Expansion Factor. Three of the filters are physically mounted on the Filter Board, while a fourth may be externally mounted on the rear panel. The filter selected determines the bandwidth to be expanded, so its 1 dB bandwidth equals the desired output bandwidth, 25.6 MHz, divided by the Expansion Factor. The signal then flows through

a 6 dB level setting attenuator and to the Second Mixer where it is further amplified and mixed to a center frequency of (25.6 MHz)/(Expansion Factor). (The center frequency of the expanded signal is 25.6 MHz.) One of three oscillators contained in the Spectrum Expander, or an external oscillator, is switched in to accomplish this mix. The mixer has two outputs. One goes to the front panel Video Input Monitor, and the other to the Digital Board.

4.2 Digital Board

The primary function of the Digital Board is to frequency expand its input signal basically by recording it and repeatedly playing it back at a faster rate. This is implemented by sampling the input signal at a rate, R_I, quantizing the samples to four bits and writing the bits into a high speed digital memory. Memory timing is such that information can be read out at a rate R_0, while information is being written at rate R_I. The frequency expansion factor resulting from this scheme is R_0/R_I. The memory output is D to A converted to produce the expanded output.

A number of other functions are included on the digital board. Among these are the interfaces to the computer, IF section, and front panel. An output level detector is also included.

4.3 IF Output Electronics

The Output IF section is quite simple. Primarily it mixes the output of the digital board to a center frequency of 150 MHz and attenuates the signal to keep the output of the spectrum expander at a level compatible with the 100 kHz Filter Bank. It also filters the signal to clean-up unwanted products, harmonics, and LO leakage. The output IF section also buffers the output of the digital section to drive the front panel Video Output Monitor.

5.0 Detailed Description of the Electronics

This section describes, in fair detail, the electronics in all the NRAO designed modules in the Spectrum Expander. First the operation of the One Diode Switch and the Three Diode Switch, circuits which are used in several modules, are discussed. Then a subsection is devoted to each NRAO designed module.

5.1 One Diode Switch

A schematic of the One Diode Switch is shown in Figure 5. The switch presents either a low or high impedance to a signal passing from S1 to S2. The heart of the switch is the MPN 3401 PIN diode, CR1. When reverse-biased, it acts as a high impedance ($\sim$ 1 pF at 10 V) and when forward biased it acts as a low impedance ($\sim$ 3 nH + 0.7 Ω at 7 mA). When Q1 is cut-off, CR1 is reverse-biased by R2 and R1, and when Q1 is saturated, CR1 is forward-biased by R1, R3, and Q1. C1 and C2 are DC blocking capacitors; C3 and C4 are bypass capacitors. Typically, insertion loss is 1.2 dB and isolation is 24 dB at 150 MHz.

5.2 Three Diode Switch

A schematic of the Three Diode Switch is shown in Figure 6. This switch also presents either a low or high impedance to signals passing from S1 to S2, with the MPN 3401 diodes acting as the basic switch elements. In the high impedance state, Q1 is cut-off, allowing R1 and R3 to back bias CR1 and CR3, respectively, and allowing CR2 to be forward biased through R2. In the low impedance state, Q1 is saturated, forward biasing CR1 and CR3. The voltage drop across R2 is about 17 V, causing CR2 to be back-biased. Typically, insertion loss is 1.6 dB and isolation > 70 dB at 150 MHz.

5.3 Input Switch

The Input Switch schematic is shown in Figure 7. It incorporates one 3-diode switch and two 1-diode switches. The 3-diode switch provides for high isolation between input and output in non-bypass modes. In the bypass mode,

little isolation is needed since the second LO's are turned off, resulting in zero output from the spectrum expander. One-diode switches are included, then, only to achieve a reasonable VSWR.

5.4 First Mixer

The First Mixer schematic is shown in Figure 8. It simply incorporates two stages of gain (∿ 15 dB each) followed by a mixer and another stage of gain (∿ 15 dB). A 20 dB pad follows this mixer, primarily to attenuate the LO leakage components from the mixer.

5.5 Filter Board

The Filter Board schematic is shown in Figure 9. It incorporates input and output buffer amplifiers, three on-board filters, jacks for an external filter, and associated switches. The 3-diode switches preceding the inputs of the filters provide high isolation between the parallel paths. These switches along with the 1-diode switches following the filter outputs also maintain a reasonable VSWR. The π-resistor networks following the 30/6.4 MHz and 30/3.2 MHz filters maintain constant power levels for Expansion Factors of 4, 8, and 16.

5.6 Oscillator Switch

The schematic for the Oscillator Switch is shown in Figure 10. It consists of four 1-diode switches, whose purpose is to maintain a good VSWR for the active oscillator. The unused oscillators are turned off so the switches are not required to provide very high isolation.

5.7 Second Mixer

The schematic for the Second Mixer is shown in Figure 11. The input signal flows through the first gain stage (∿ 15 dB) and then is mixed with the output of the Oscillator Switch. The output of this mixer is then amplified, low-pass filtered, further amplified, and resistively split two ways. The splitter outputs are buffered before being output from the module.

5.8 Oscillator Power Supply

The Oscillator Power Supply schematic is shown in Figure 12. It takes a 28 V input and regulates it down to 12 V. The regulation is done in the LM317 monolithic voltage regulator. The regulator output can be switched from 12 V to about 1.5 V by means of an external transistor switch across R2. This capability is used to turn off some of the oscillators when they are not needed. Capacitors serve their obvious decoupling purposes while the diode protects the LM317 against a short in the 28 V supply.

5.9 -2 V Regulator

The -2 V Regulator schematic is shown in Figure 13. Operation is as follows. The LM 324 op-amp senses the voltage difference between the circuit's -2 V output and a -2 V reference generated by a resistive divider from ground to -5.2 V. The op-amp output then drives the Darlington transistor pair to produce the desired output. Circuit stability is provided by R1 and C1a; R4, R5, and C2 provide protection against voltage offsets which can be caused by voltage spikes at the op-amp output.

5.10 -5.2 V Delay Circuit

The schematic for this circuit is shown in Figure 14. Its function is to delay the application of the AC power to the -5.2 V supply until the other supplies have come up. (If this delay is not present, the +5 V supply never achieves +5 V.) The implementation is straightforward. R1 and C1 sense the rise of the +28 V supply, and delay the turn on of the diode in the opto-isolator. Once on, the opto-isolator allows gate current to flow in the SC240B triac, and thus allows AC power to flow through the triac to the -5.2 V supply.

5.11 Output Mixer

The Output Mixer schematic is shown in Figure 15. Circuit operation is as follows. The input signal is divided resistively at the input. Part of

it goes through a buffer amplifier to serve as a video output monitor. The rest of the signal is mixed with a 124.4 MHz signal to achieve a center frequency of 150 MHz. The mixer's output is attenuated to keep the Output Mixer's output power in the same range as the input to the Spectrum Expander.

5.12 Digital Board

Schematics of the various circuits on the Digital Board are shown in Figures 16A to 16E. A timing diagram is included in Figure 17. A variety of functions are served by this board. Primarily, it quantizes an input signal, writes it in a memory, and reads it back faster than it wrote it in. In addition, the board contains digital interfaces to the front panel, computer, and IF electronics. Finally, it contains a circuit to monitor its output level. Each of these functions is described below.

5.12.1 Digital Interfaces

Schematics of the digital interfaces are shown in Figure 16A. Monitor outputs to the computer are driven by U3. Inputs from the computer are received by U1 and U2. These receivers drive three inputs of the U4 multiplexer. Three other inputs of U4 are driven by the front panel Expansion Factor switch. The front panel Mode Control switch drives the select input of U4, enabling either the computer or front panel signals. U4 drives the U5 decoder as well as some gates in the memory control section. The outputs of U5 control four groups of drivers. First among these are the LED drivers, U6, and the oscillator regulator drivers, U7. Also, the optically isolated drivers of the Inpu Switch (U7, U8, U9, U10 and associated components) and the Filter Board and Oscillator Switches (U10 to U14 and associated components) are controlled.

5.12.2 Memory Controller

The function of the Memory Controller is to generate read and write addresses and appropriate timing waveforms for the memory. Its schematic is shown in Figures 16B and C, and a timing diagram in Figure 17.

An ECL clock waveform is obtained from either the 102.4 MHz input or the F_0 input as follows. The F_0 input is terminated by R169, and level shifted by C9, R170 and R171. The 102.4 MHz input goes into a similar circuit. U83 enables either U84 or U85, whose outputs are OR-tied. The enabled unit produces the ECL waveform. This clock is distributed by E63.

The clock waveform is divided by 2, 4 and 8 by the binary counter consisting of U89, U90, U91, and U92, for use in various timing functions.

The input sampling rate is generated as follows. Possible sampling rates are generated from the binary counter mentioned above and, in external mode, from the F_I input. The F_I input is translated to ECL by U87 and associated parts and fed to U97, a 4:1 multiplexer. Counter outputs Q1 and QØ are also fed to U97. Finally, $\overline{Q\emptyset}$, from the counter is divided by two and fed to the multiplexer. The output of U97 (the input sampling rate) is determined by its A and B inputs which are driven by the U83 level converters. U98 buffers U97's output, and drives the A/D converter's "START" input, via a level converter, U26.

The output of U98 also drives U110, a ÷8 circuit. U110's output controls the memory input latches U36 to U41. U88 uses both the input and ouptut of U110 to produce a $\frac{5}{8}$ duty cycle waveform, WRITEN.

Write enable pulses are generated, based on timing from the binary counter and the WRITEN signal, by U93 and U92. This logic guarantees that the memory will work in external mode, so long as $F_I \leq .625\ F_0$, even with F_0 and F_I asynchronous with respect to each other.

Write memory addresses are generated by the U101 and U102 binary counters using FS/8 (from U98) as a clock. Read addresses are generated similarly by U99 and U100 using a buffered $\overline{Q\emptyset}$ as a clock. Read and write addresses are multiplexed by U103 to U109 based on timing from U96. As a result, the address inputs of the memories alternately see read and write addresses.

5.12.3 A/D, Memory and D/A

The schematics of these circuits are shown in Figures 16C and D. The VIDEO IN signal is level shifted and terminated by C7, R36 and R37. The The level shifted signal drives U23, the A/D. A rising edge on the START input of U23 causes the signal at the ANALOG IN input to be sampled and quantized to four bits. The same rising edge clocks the result of the previous conversion into the buffer, U23. The outputs of U24 are level shifted from TTL to ECL by U25. Each of the outputs of U25 follows a similar path, so we will follow only the output of pin 2. It goes to the shift input of an 8-bit shift register consisting of U28 and U29. If the shift/operate switch, S9, is in the operate position, this data is shifted into the register. If S9 is in the test position, test inputs from switches S1 to S8 are loaded into the register. The outputs of the register are clocked into the latch, U36 and U37, where they are available to be written into memory. When the write address is present at the memory address lines and $\overline{WE}$ goes low, the contents of the latches are written into memory. When the read address is present at the memory address lines, data are read out of memory into the 8-bit shift register, U74 and U75. Bits are shifted out of this register into the register, U82, where they are combined with outputs of the other shift registers to again form a 4-bit word. This word is converted to TTL levels by U94 before going into a resistor network which effects a D/A conversion.

5.13.4 Level Monitor

Figure 16E shows the schematic of the circuit which drives the front panel level meter and tells the computer when the IF level is in an acceptable range. It monitors the output of the digital board so that it will also indicate many sorts of problems in the digital board.

The technique used is to first digitally full-wave rectify the 4-bit words. The rectified word is then D/A converted to a current which is

subtracted from a temperature-compensated reference current. The difference current is converted to a voltage which is compared against some reference voltages and which also drives the front panel meter through a reference resistor. The rectification is done by enabling 3 gates of U120 with the MSB, EX3. The D/A conversion is accomplished by the R-C networks following the gates. The temperature-compensated reference current is generated by the fourth gate of U120 and the associated R-C network. It is inverted by an op-amp, U121, and the currents are differenced at the inverting input of the second op-amp of U121. This op-amp effects the current-to-voltage conversion. U122 and associated components provide two reference voltages for comparison, by U123 and U124, with the op-amp output. The outputs of U123 and U124 are tied together so that the combined output goes high only when the IF level is in an acceptable range. The front panel meter is driven from the op-amp through R286.

6.0 Acknowledgements

P. S. Henry and H. E. Rowe of Bell Laboratories supplied a great deal of information helpful in realizing this spectrum expander. This information included the formulation of the theory of operation as well as details on their construction of a similar instrument. Bob Mauzy, Mike Balister, Ron Weimer, Dwayne Schiebel, and Tony Miano were helpful in the design. Bill Vrable and Winston Cottrell did an excellent job putting it all together.

7.0 Reference

P. S. Henry, "Variable Resolution Capability for Multichannel Filter Spectrometers," Rev. Sci. Instr., pp. 185-192, February 1979.

APPENDIX A

This appendix includes a number of details on the mechanical construction of the Spectrum Expander. The component layout of the Digital Board and module layout of the IF section are shown in schematic drawings. Photographs show the layout of major modules in the chassis. Finally, a wiring diagram is included.

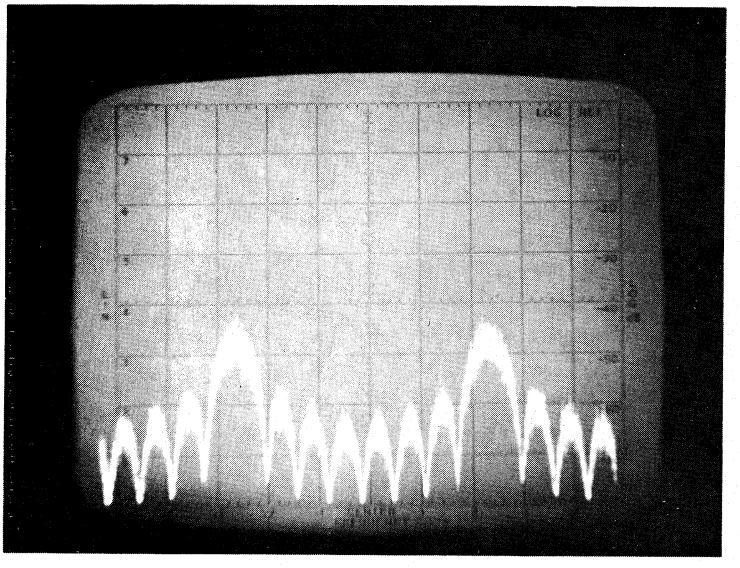


Figure 1. Spectrum Expander output as viewed on a spectrum analyzer.

Vertical scale: 10 dB/div.
Horizontal scale: 10 kHz/div.

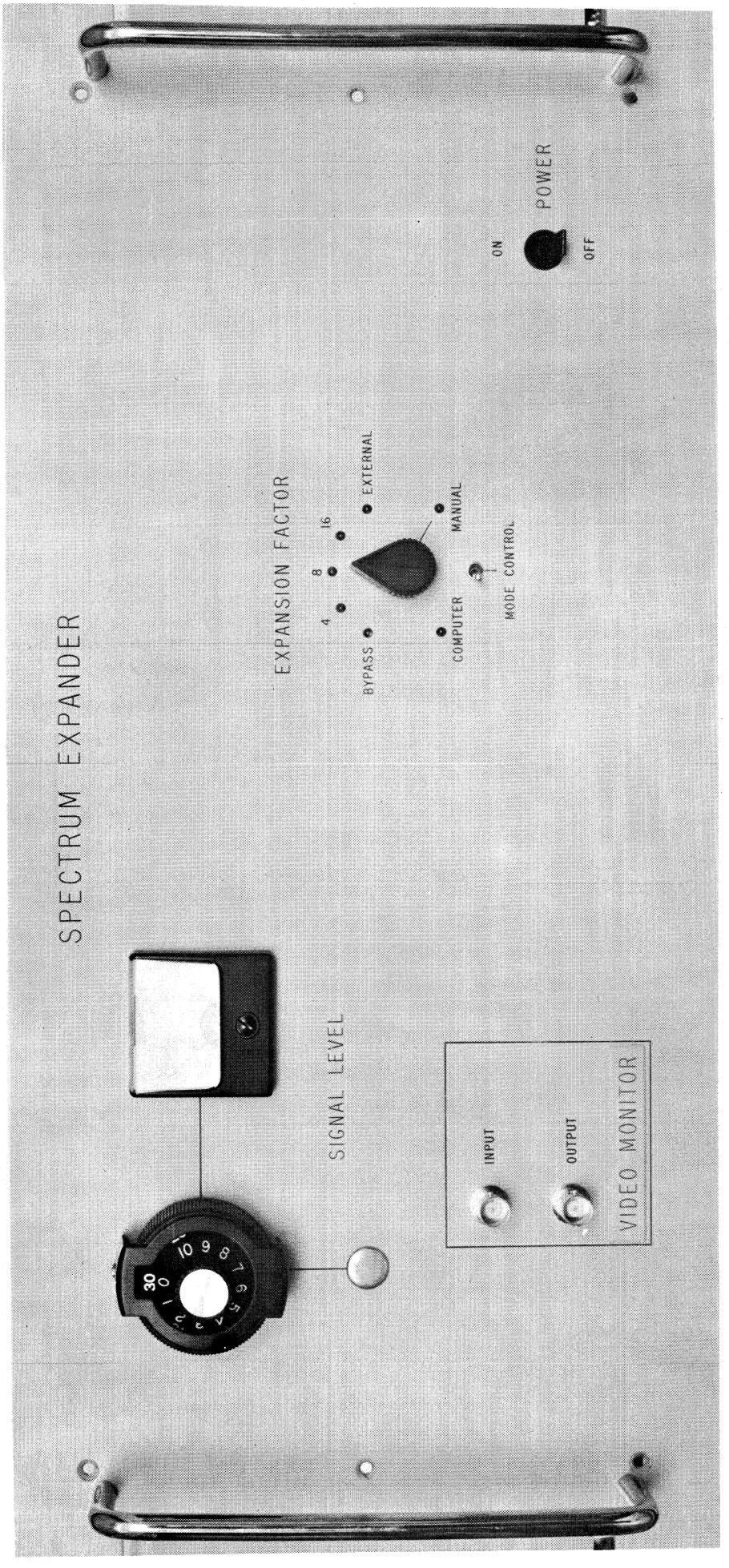


FIG. 2 SPECTRUM EXPANDER, FRONT PANEL

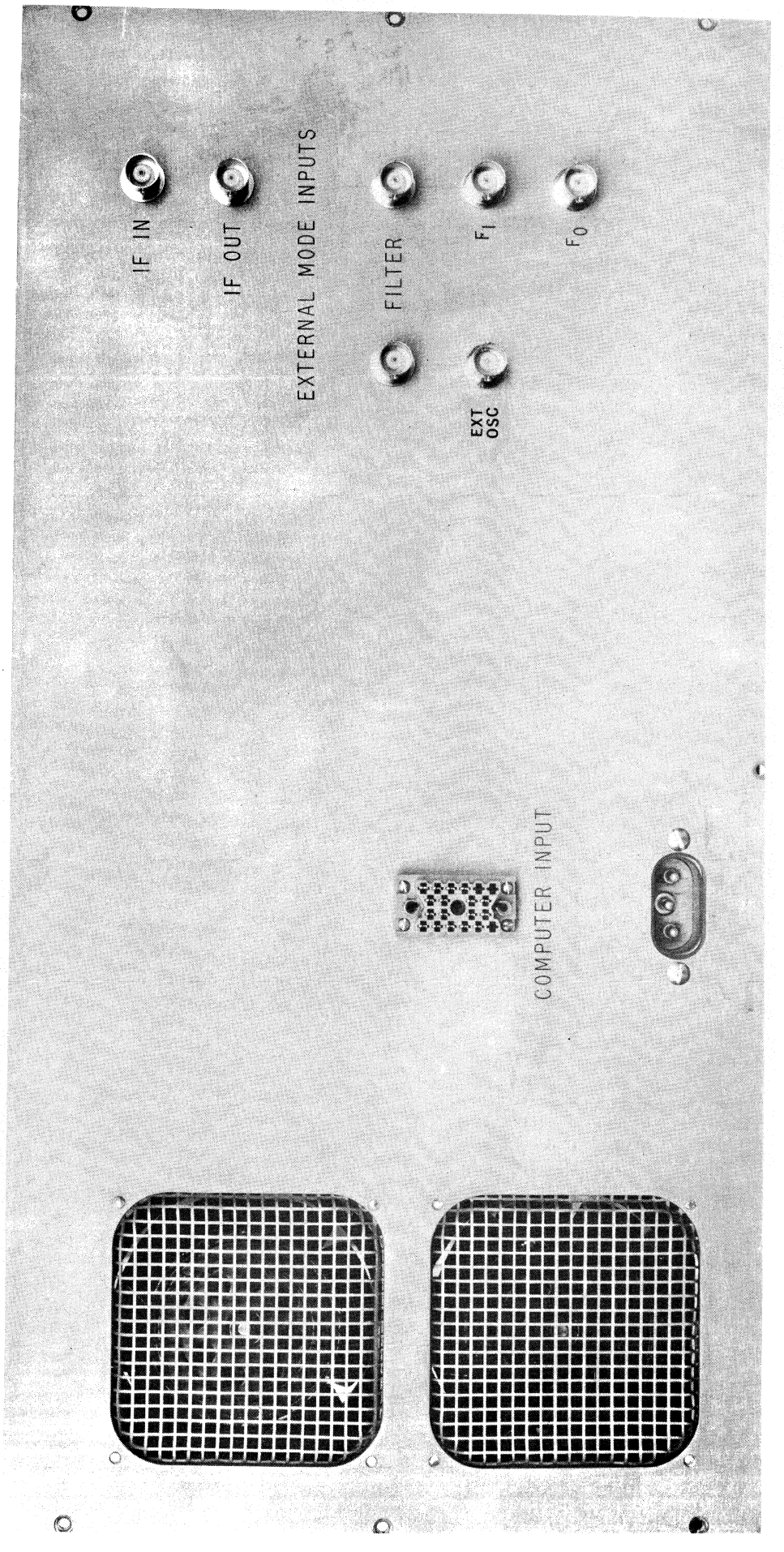
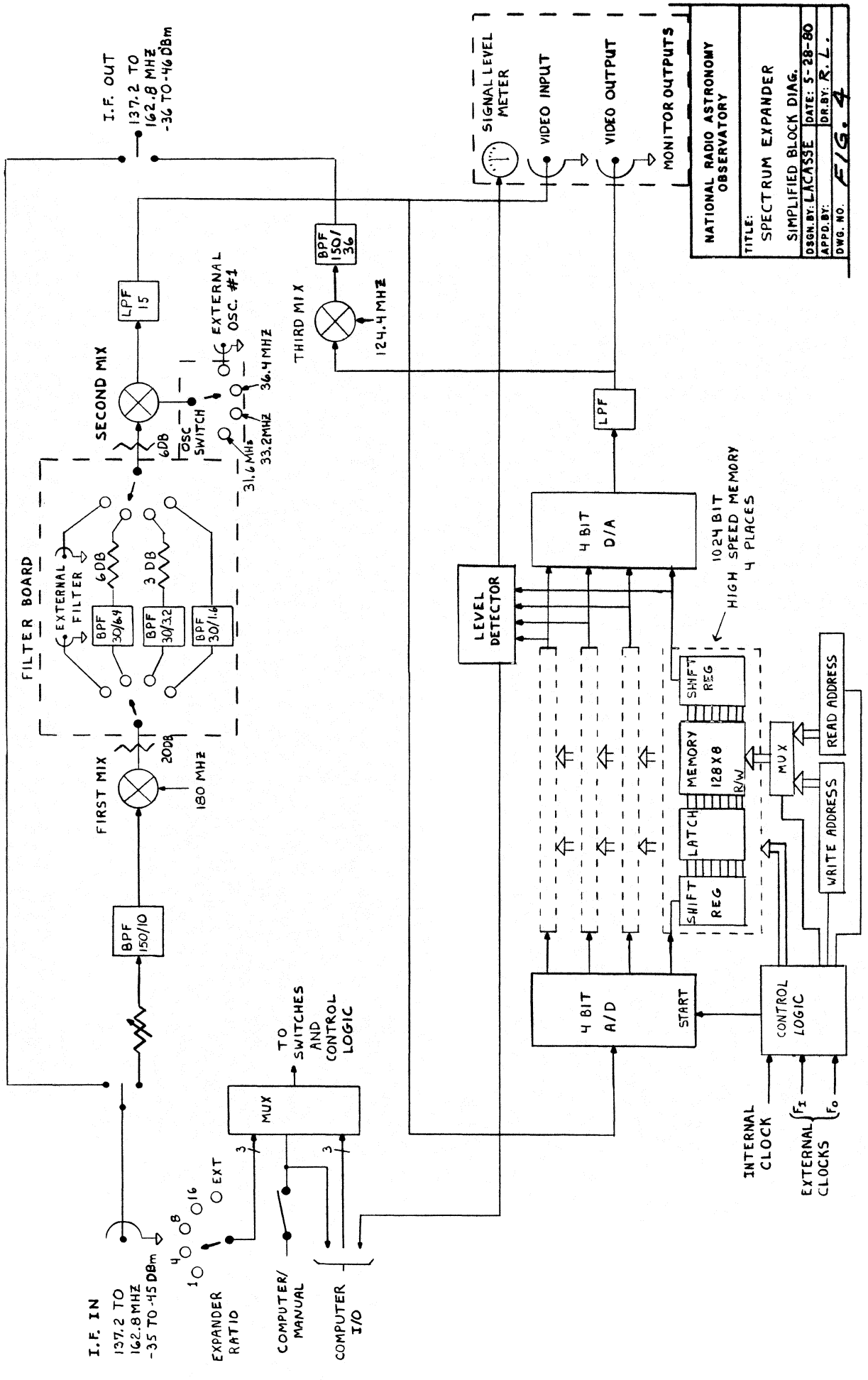


FIG. 3 SPECTRUM EXPANDER, REAR PANEL


I.F. OUT
137.2 TO 162.8 MHZ -36 TO -46 DBm
I.F. IN
137.2 TO 162.8 MHZ -35 TO -45 DBm
EXPANDER RATIO
COMPUTER/ MANUAL
COMPUTER I/O
TO SWITCHES AND CONTROL LOGIC
MUX
EXT
FILTER BOARD
EXTERNAL FILTER
BPF 30/64
BPF 30/32
BPF 30/16
6DB
3 DB
20DB
FIRST MIX
180 MHZ
BPF 150/10
SECOND MIX
LPF 15
6DB
OSC SWITCH
EXTERNAL OSC. #1
31.6 MHz
33.2MHZ
36.4MHZ
THIRD MIX
124.4 MHZ
BPF 150/36
SIGNAL LEVEL METER
VIDEO INPUT
VIDEO OUTPUT
MONITOR OUTPUTS
LPF
4 BIT D/A
LEVEL DETECTOR
1024 BIT HIGH SPEED MEMORY 4 PLACES
SHIFT REG
MEMORY 128X8 R/W
LATCH
SHIFT REG
MUX
READ ADDRESS
WRITE ADDRESS
4 BIT A/D
START
CONTROL LOGIC
INTERNAL CLOCK
EXTERNAL CLOCKS
FI
FO
NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: SPECTRUM EXPANDER
SIMPLIFIED BLOCK DIAG.
DSGN. BY: LACASSE
DATE: 5-28-80
APPD. BY:
DR. BY: R. L.
DWG. NO. FIG. 4

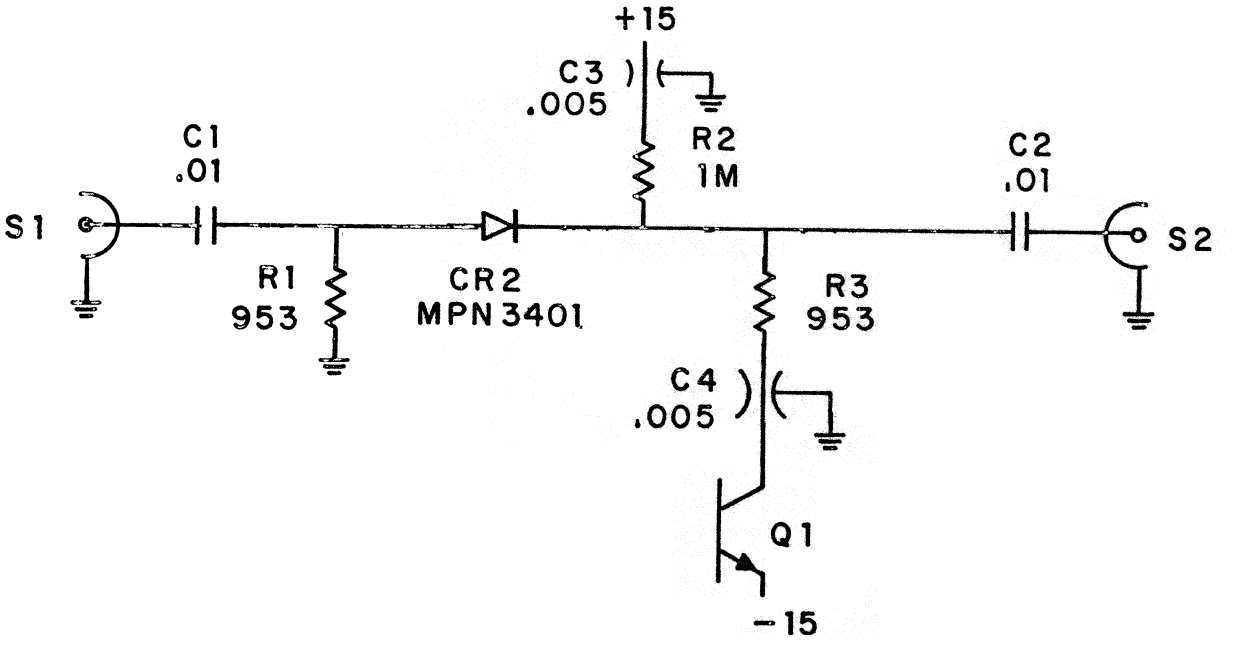


FIG. 5 ONE DIODE SWITCH SCHEMATIC

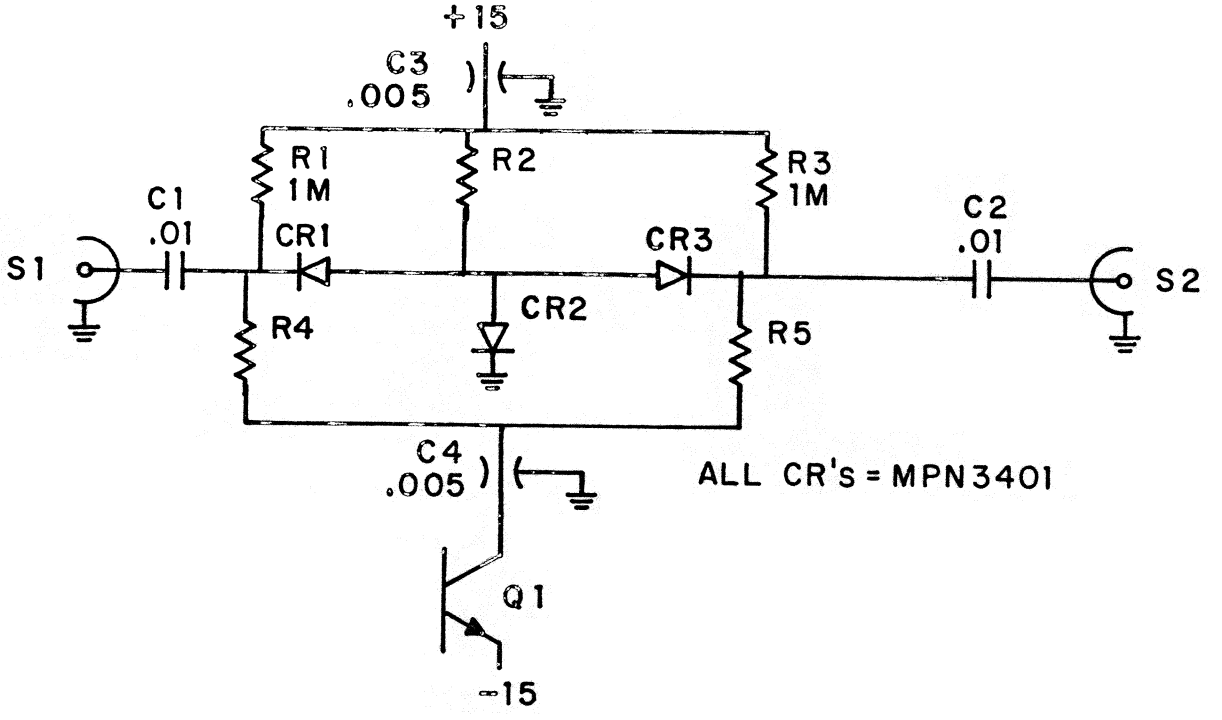
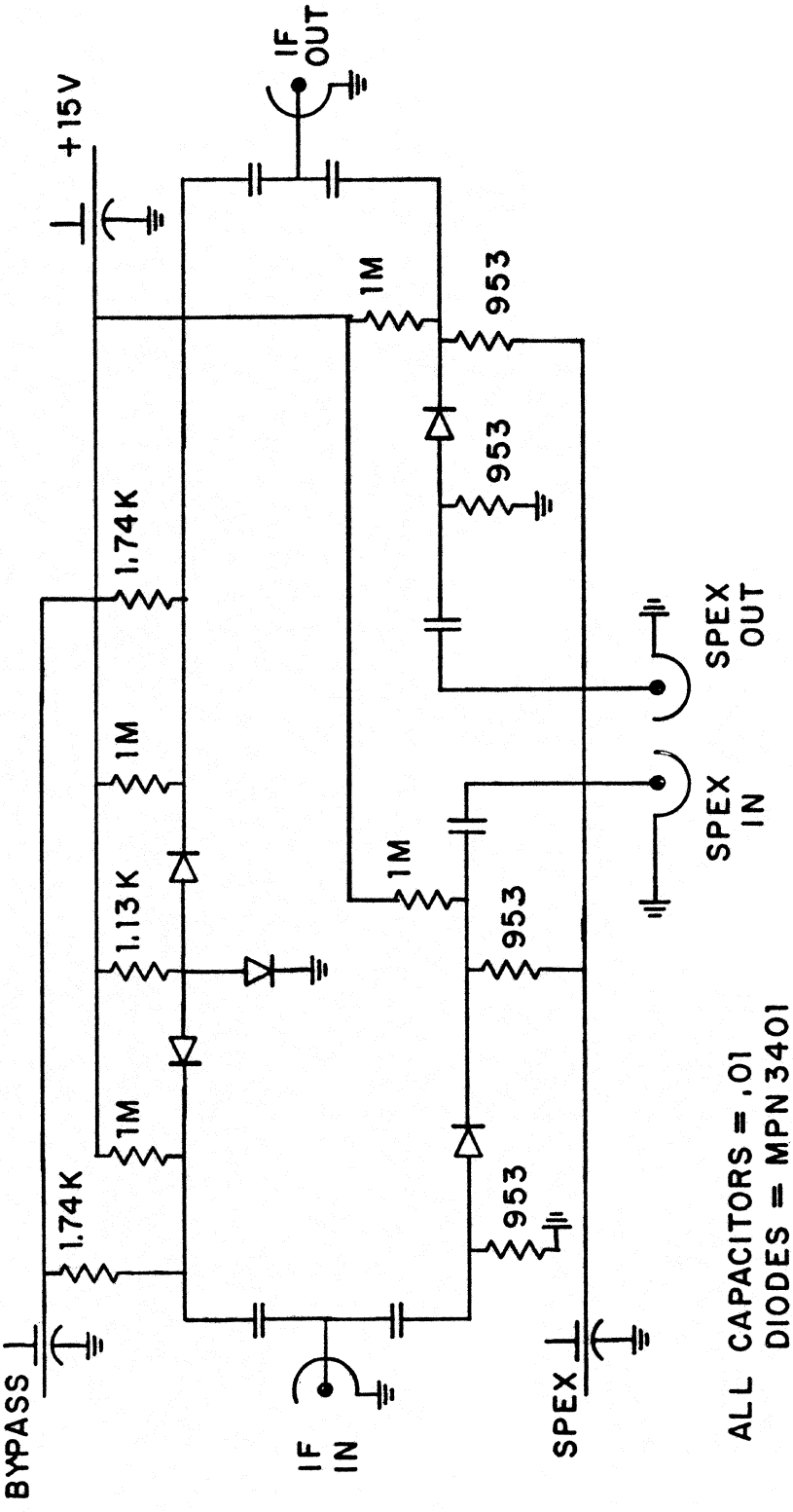
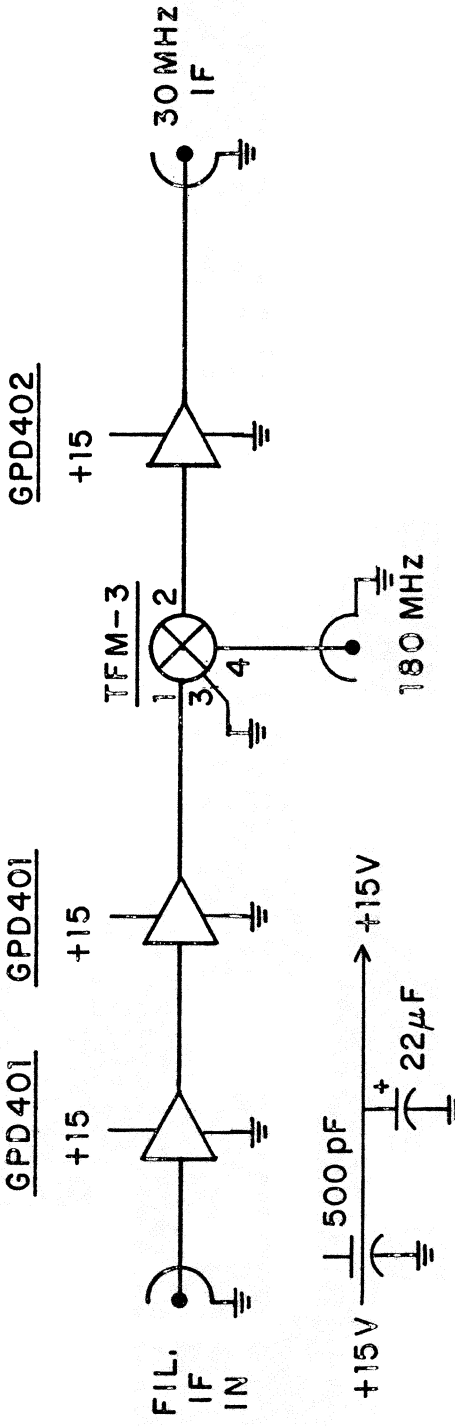


FIG. 6 THREE DIODE SWITCH SCHEMATIC



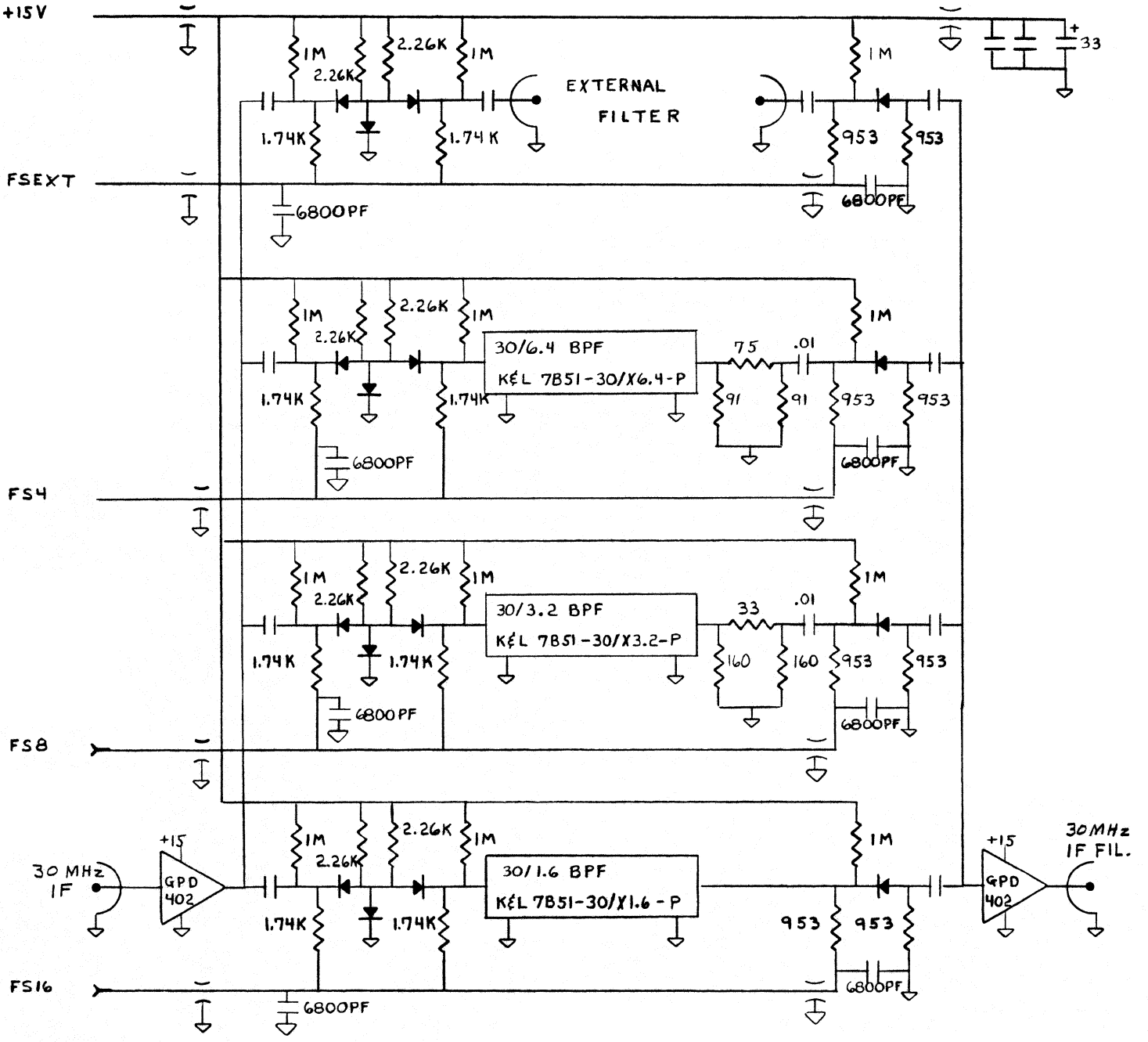
SPECTRUM EXPANDER, INPUT SWITCH

FIG. 7



SPECTRUM EXPANDER, FIRST MIXER

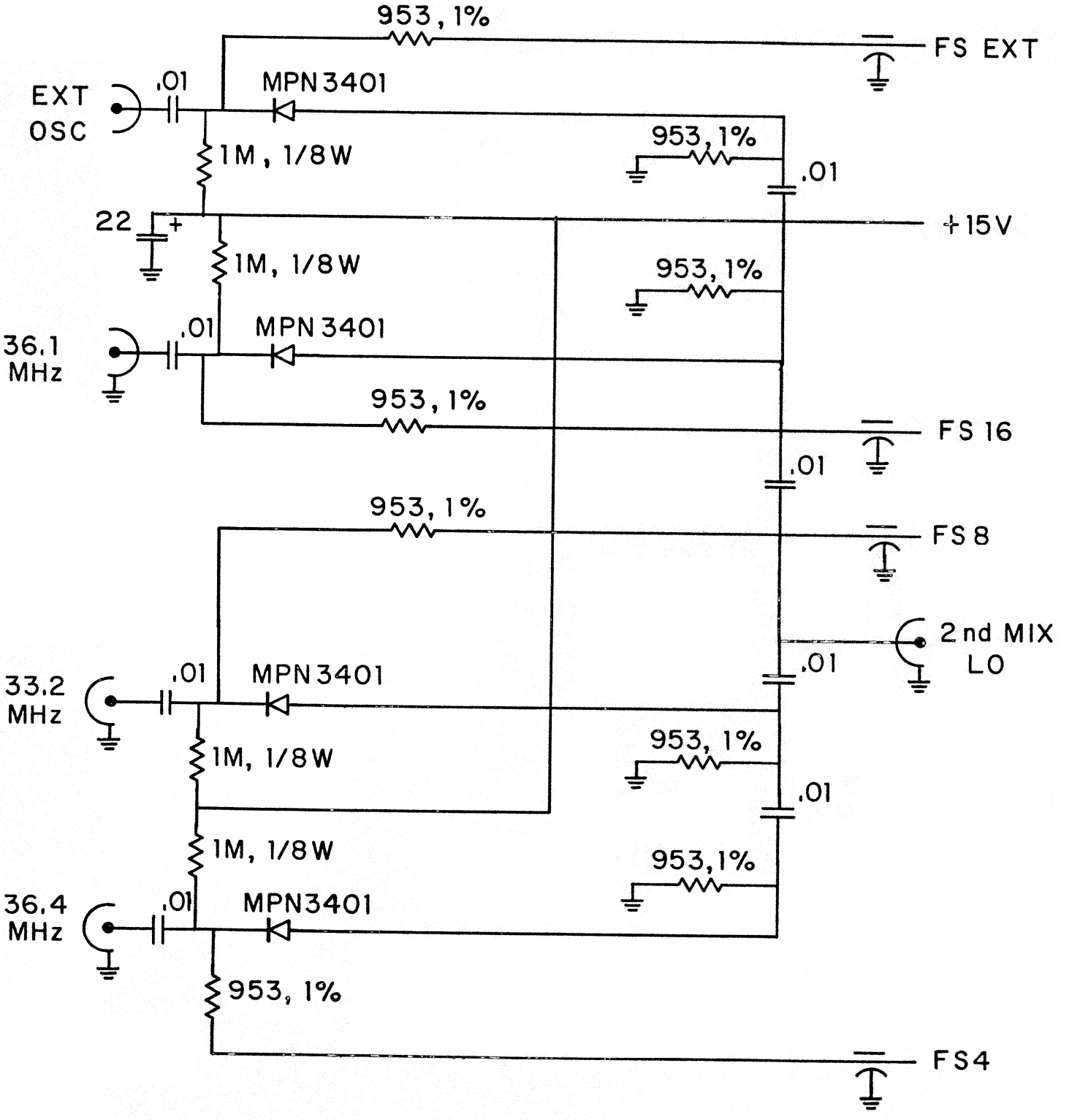
FIG. 8



NOTES:

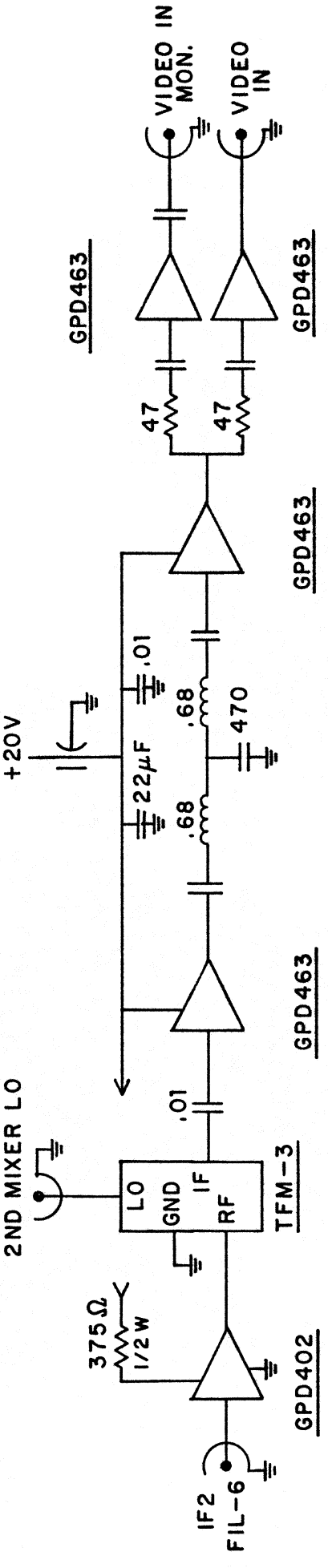
1- UNLESS OTHERWISE SPECIFIED,
ALL DIODES ARE MPN 3401
ALL CAPS. ARE .01μF, UNLESS OTHERWISE SPECIFIED
1.74K, 2.26K, AND 953 OHM RESISTORS ARE RN60C
OTHER RESISTORS ARE CARBON, 5%.
FEEDTHRU CAPACITORS ARE ERIE 2425-001-X5W0-502 AA

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: SPECTRUM EXPANDER, FILTER BOARD	
DSGN. BY: LACASSE	DATE: 3-19-80
APPD. BY:	DR. BY: R. L.
DWG. NO. FIG. 9	



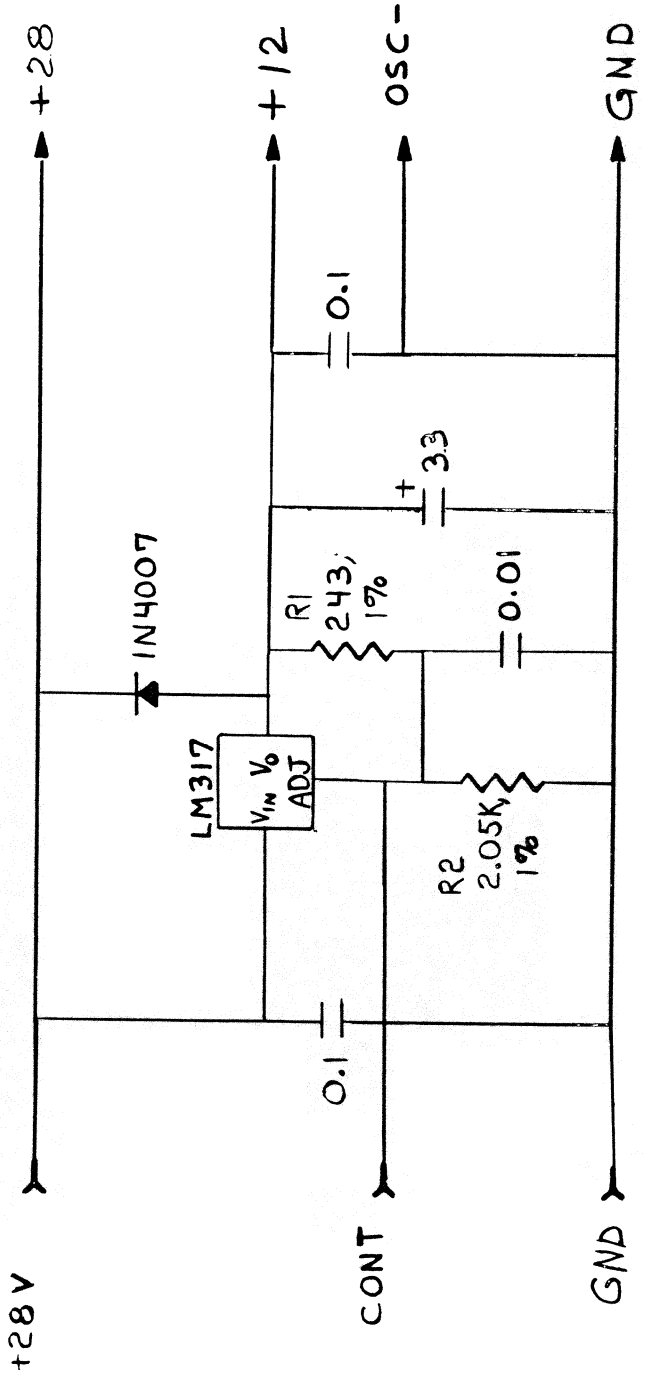
SPECTRUM EXPANDER, OSCILLATOR SWITCH

FIG. 10

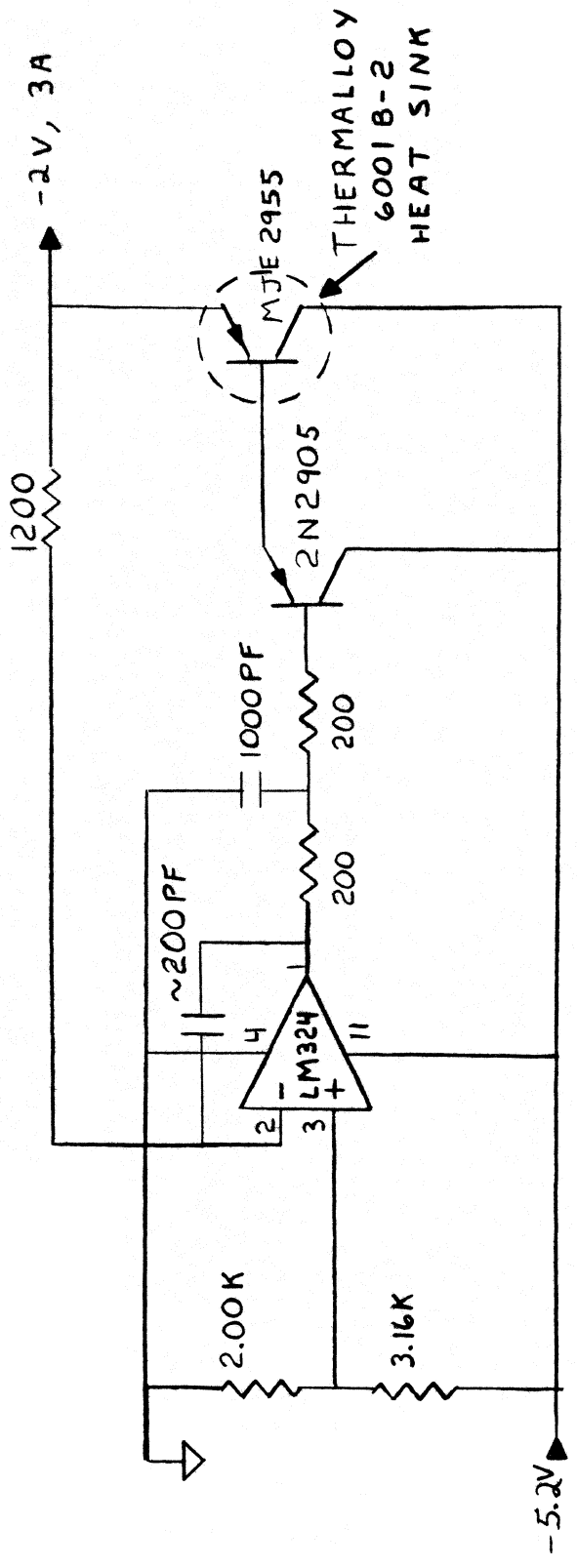


SPECTRUM EXPANDER, SECOND MIXER

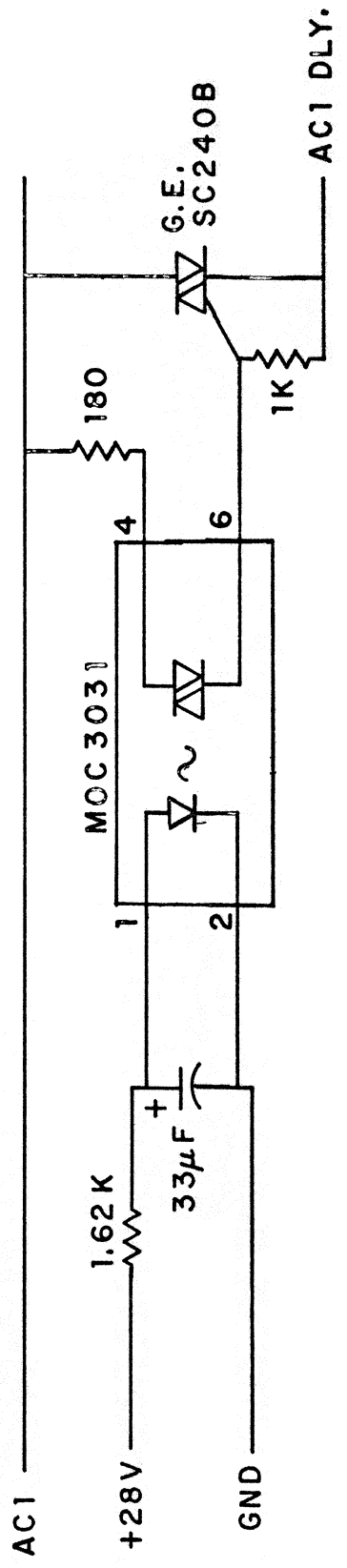
FIG. 11



NATIONAL RADIO ASTRONOMY OBSERVATORY		
TITLE: SPECTRUM EXPANDER, OSCILLATOR SUPPLY		
DSGN.BY: LACASSE	DATE: 3-12-80	
APPD.BY:	DR.BY: R.L.	
DWG. NO. FIG. 12		

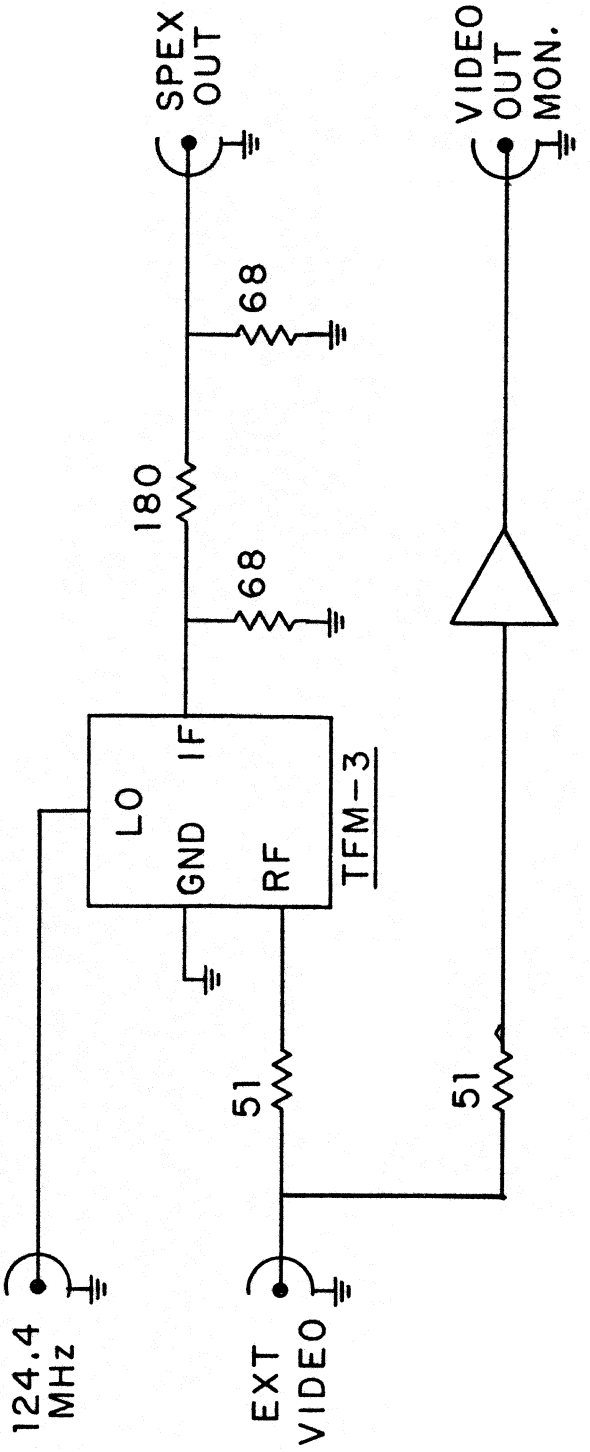


NATIONAL RADIO ASTRONOMY OBSERVATORY		
TITLE: SPECTRUM EXPANDER, -2V REGULATOR		
DSGN.BY: R. LACASSE	DATE: 2-25-80	
APPD.BY:	DR.BY: R.L.	
DWG. NO. FIG. 13		



-5.2V DELAY CIRCUIT

FIG. 14



SPECTRUM EXPANDER, OUTPUT MIXER

FIG. 15

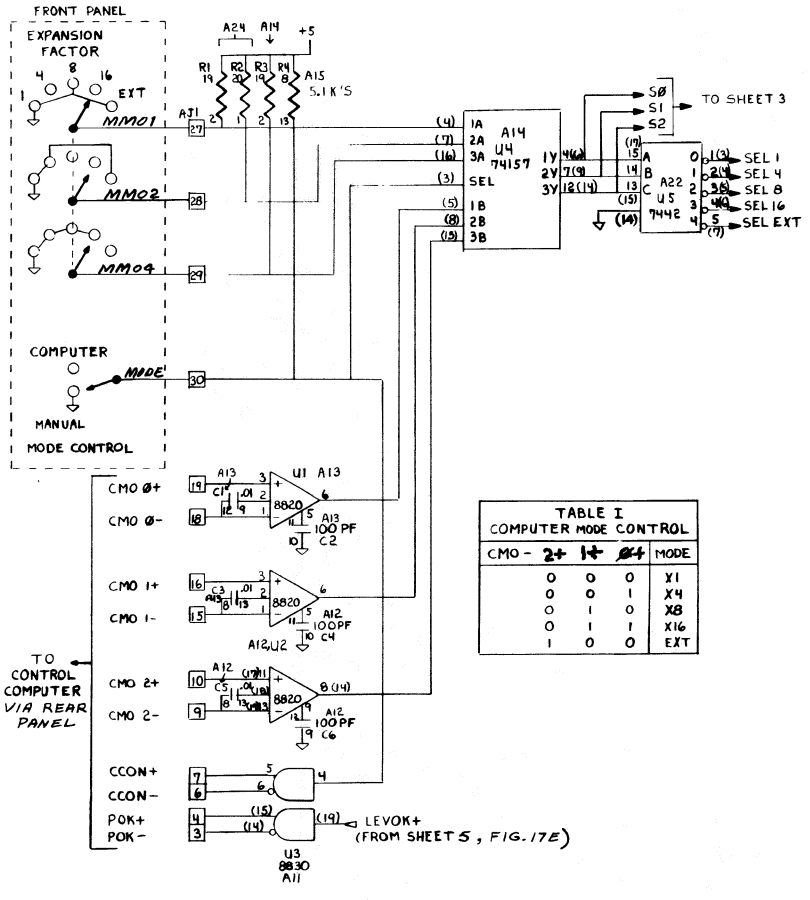
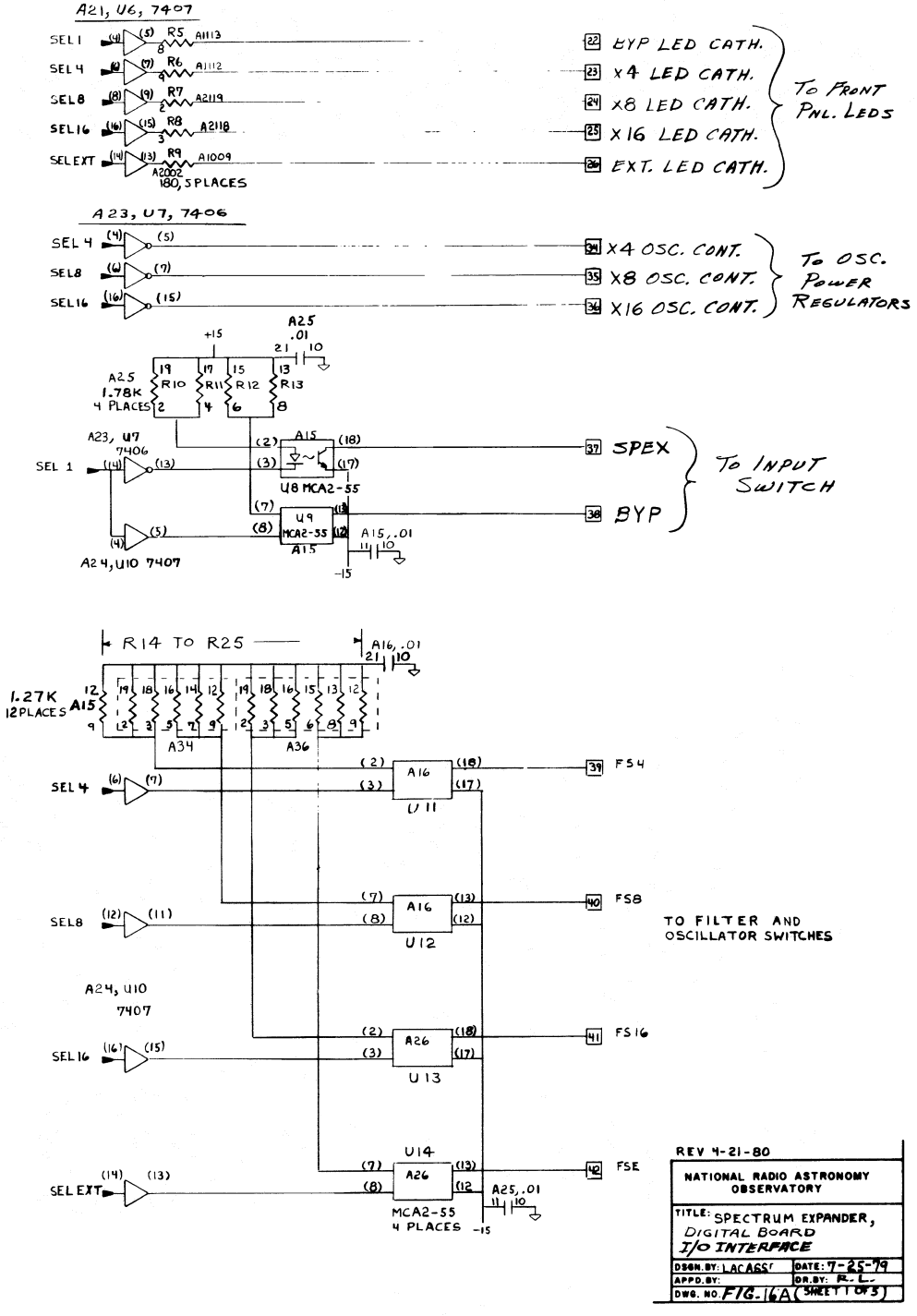


TABLE I COMPUTER MODE CONTROL				
CMO- 2+	1+	0+	MODE
0	0	0	X1
0	0	1	X4
0	1	0	X8
0	1	1	X16
1	0	0	EXT

NOTES:
1- PIN NUMBERS IN PARENTHASES ARE BOARD NUMBERS.

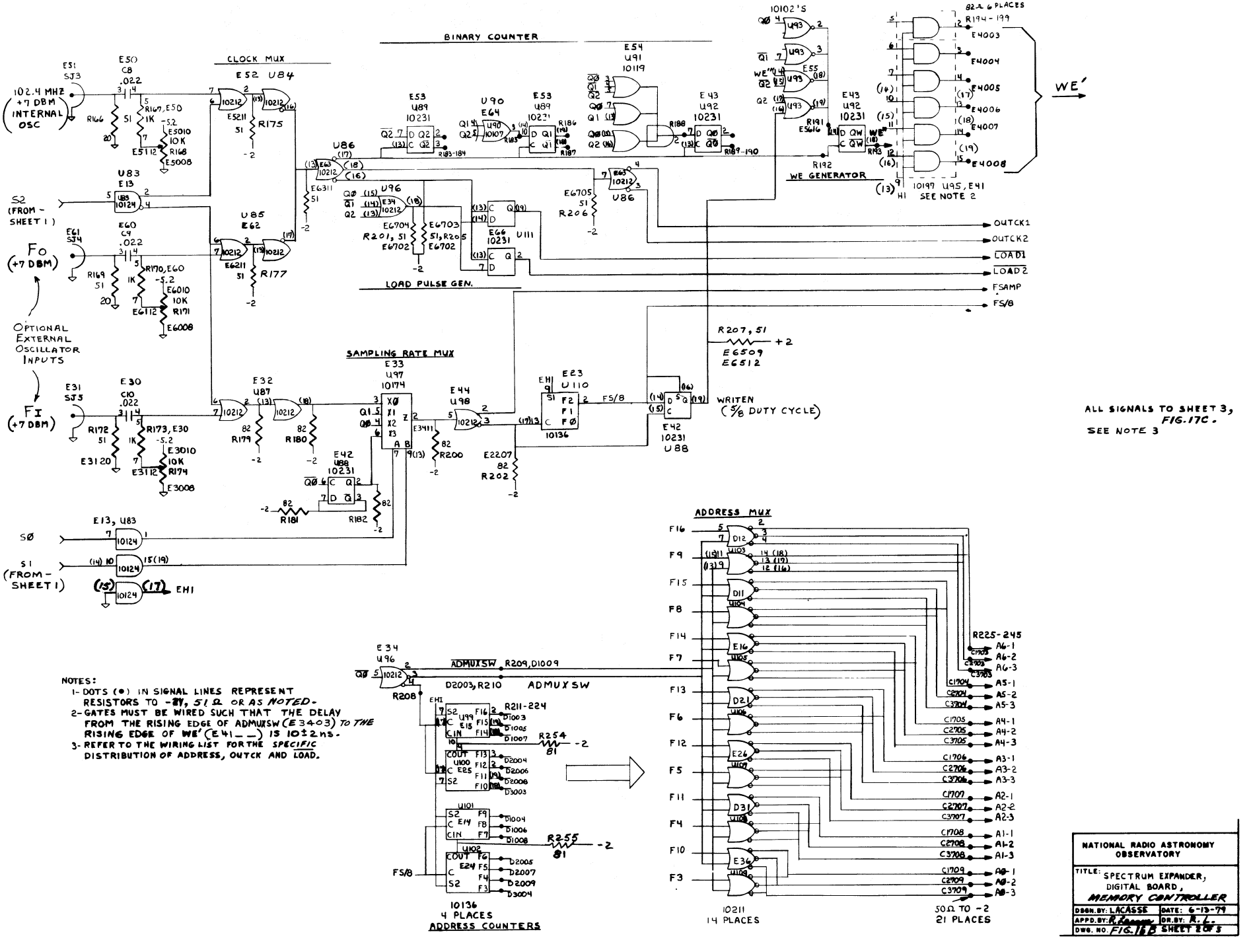


REV 4-21-80

NATIONAL RADIO ASTRONOMY OBSERVATORY

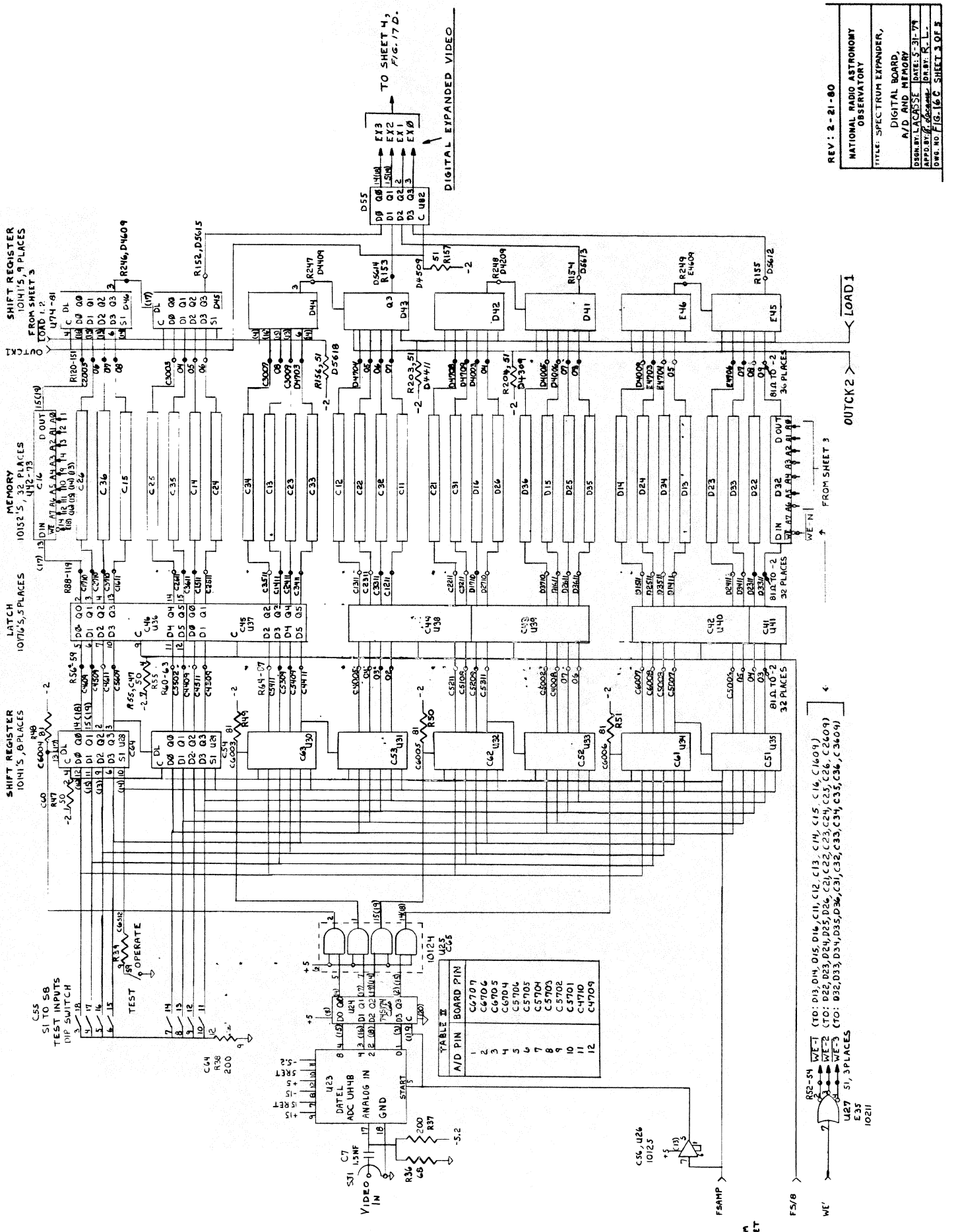
TITLE: SPECTRUM EXPANDER, DIGITAL BOARD I/O INTERFACE

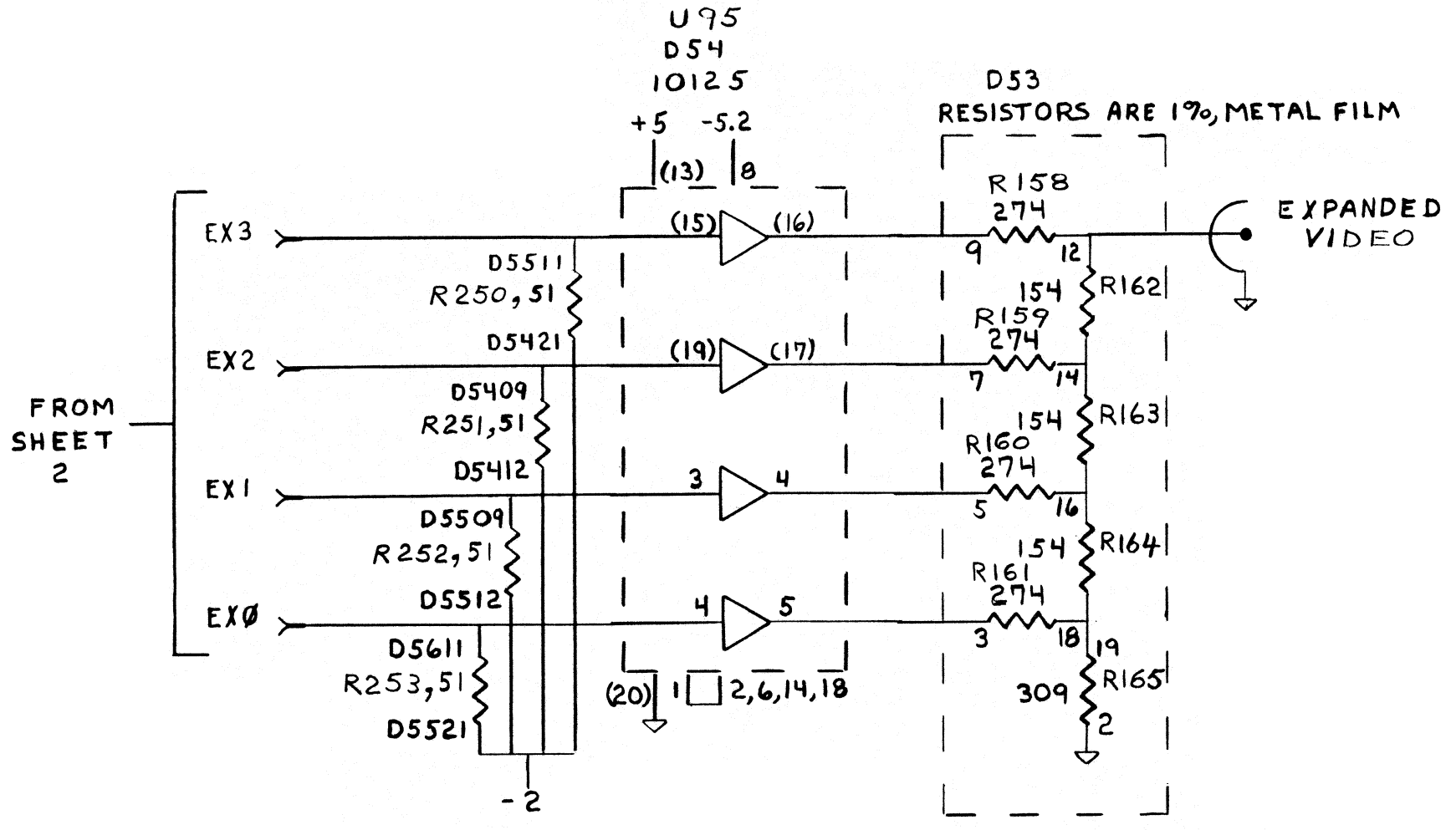
DSGN. BY: LACAGST	DATE: 7-25-79
APPD. BY:	DR. BY: R. L.
DWG. NO. FIG. 16A	(SHEET 1 OF 3)



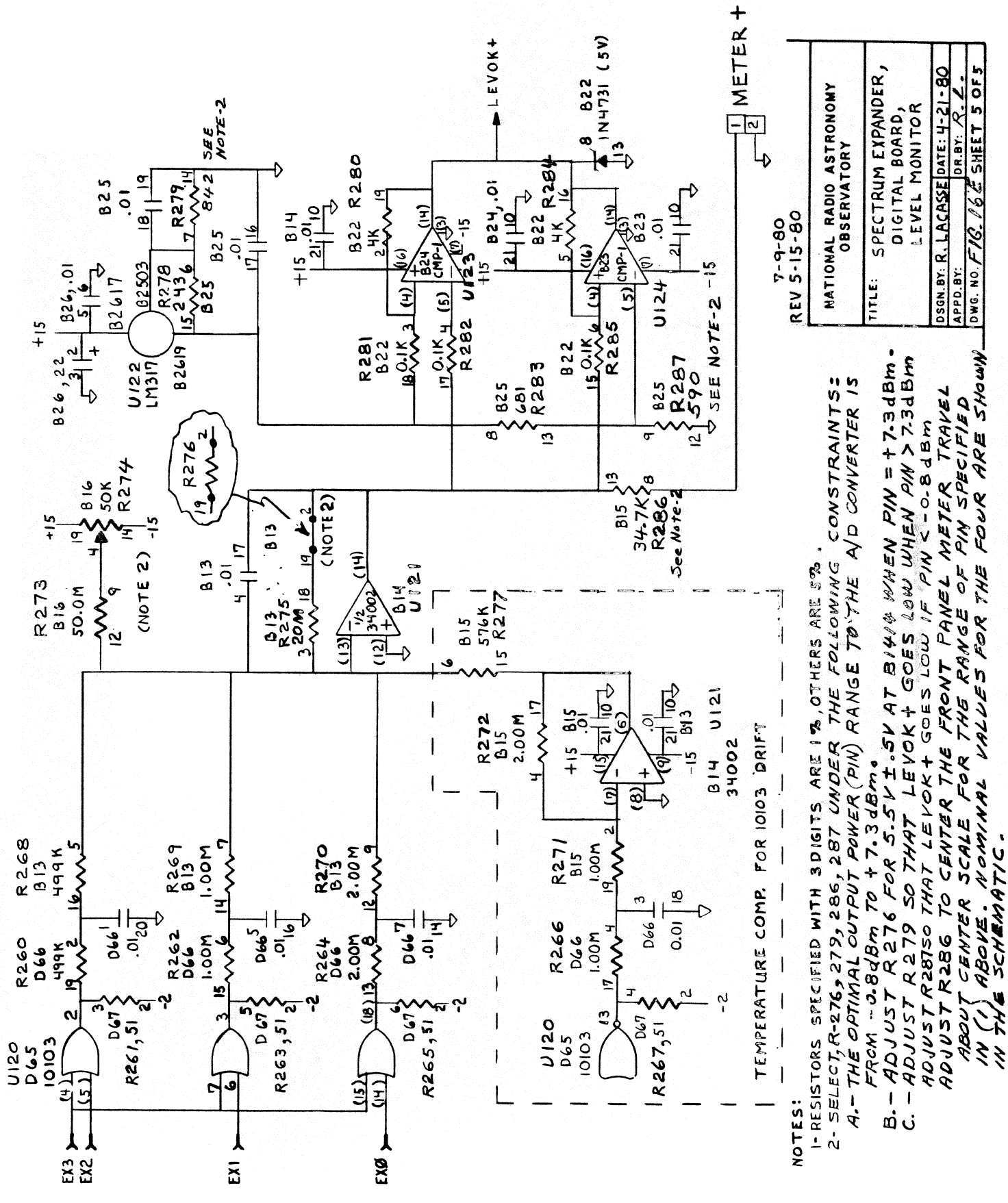
NOTES:
1- DOTS (•) IN SIGNAL LINES REPRESENT RESISTORS TO -2V, 51 Ω OR AS NOTED.
2- GATES MUST BE WIRED SUCH THAT THE DELAY FROM THE RISING EDGE OF ADMUXSW (E3403) TO THE RISING EDGE OF WE' (E41__) IS 10±2 ns.
3- REFER TO THE WIRING LIST FOR THE SPECIFIC DISTRIBUTION OF ADDRESS, OUTCK AND LOAD.

NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: SPECTRUM EXPANDER, DIGITAL BOARD, MEMORY CONTROLLER	
DSGN. BY: LACASSE	DATE: 6-13-79
APPD. BY: R. Thompson	DR. BY: R.L.
DWG. NO. FIG. 16B	SHEET 2 OF 5


DIGITAL EXPANDED VIDEO
TO SHEET 4, FIG. 17 D.
FROM SHEET 3
LOAD 1
OUTCK2
SHIFT REGISTER 10141'S, 8 PLACES
LATCH 10174'S, 5 PLACES
MEMORY 10132'S, 32 PLACES
SHIFT REGISTER 10141'S, 9 PLACES
TEST INPUTS DIP SWITCH
S1 TO S8
TEST
OPERATE
VIDEO IN
DATEL ADC UH48
ANALOG IN
GND
START
TABLE II
A/D PIN
BOARD PIN
FSAMP
FS/8
WE'
WE-1
WE-2
WE-3
3 PLACES
REV: 2-21-80
NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: SPECTRUM EXPANDER, DIGITAL BOARD, A/D AND MEMORY
DWG. NO FIG. 16 C SHEET 3 OF 5



NATIONAL RADIO ASTRONOMY OBSERVATORY	
TITLE: SPECTRUM EXPANDER, DIGITAL BOARD, D/A CONVERTER	
DSGN.BY: R. LACASSE	DATE:
APPD.BY: R. Lacasse	DR.BY: R. L.
DWG. NO. FIG. 16 D	SHEET 4 OF 5



NOTES:
1- RESISTORS SPECIFIED WITH 3 DIGITS ARE 1%, OTHERS ARE 5%.
2- SELECT R-276, 279, 286, 287 UNDER THE FOLLOWING CONSTRAINTS:
A.- THE OPTIMAL OUTPUT POWER (PIN) RANGE TO THE A/D CONVERTER IS FROM -0.8 dBm TO +7.3 dBm.
B.- ADJUST R276 FOR 5.5V ± .5V AT B14 WHEN PIN = +7.3 dBm.
C.- ADJUST R279 SO THAT LEVOK+ GOES LOW WHEN PIN > 7.3 dBm
ADJUST R285 SO THAT LEVOK+ GOES LOW IF PIN < -0.8 dBm
ADJUST R286 TO CENTER THE FRONT PANEL METER TRAVEL ABOUT CENTER SCALE FOR THE RANGE OF PIN SPECIFIED IN (1) ABOVE. NOMINAL VALUES FOR THE FOUR ARE SHOWN IN THE SCHEMATIC.

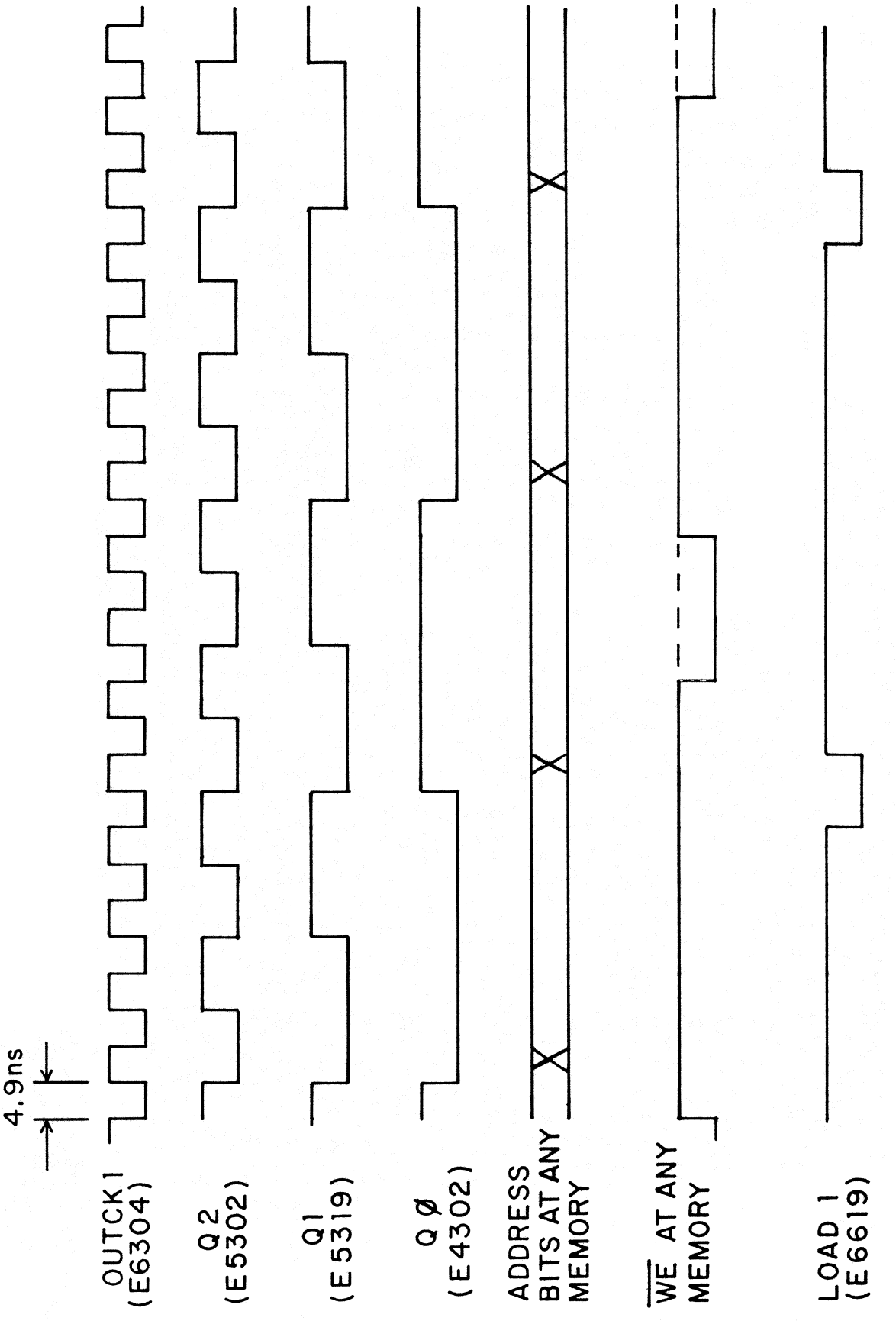
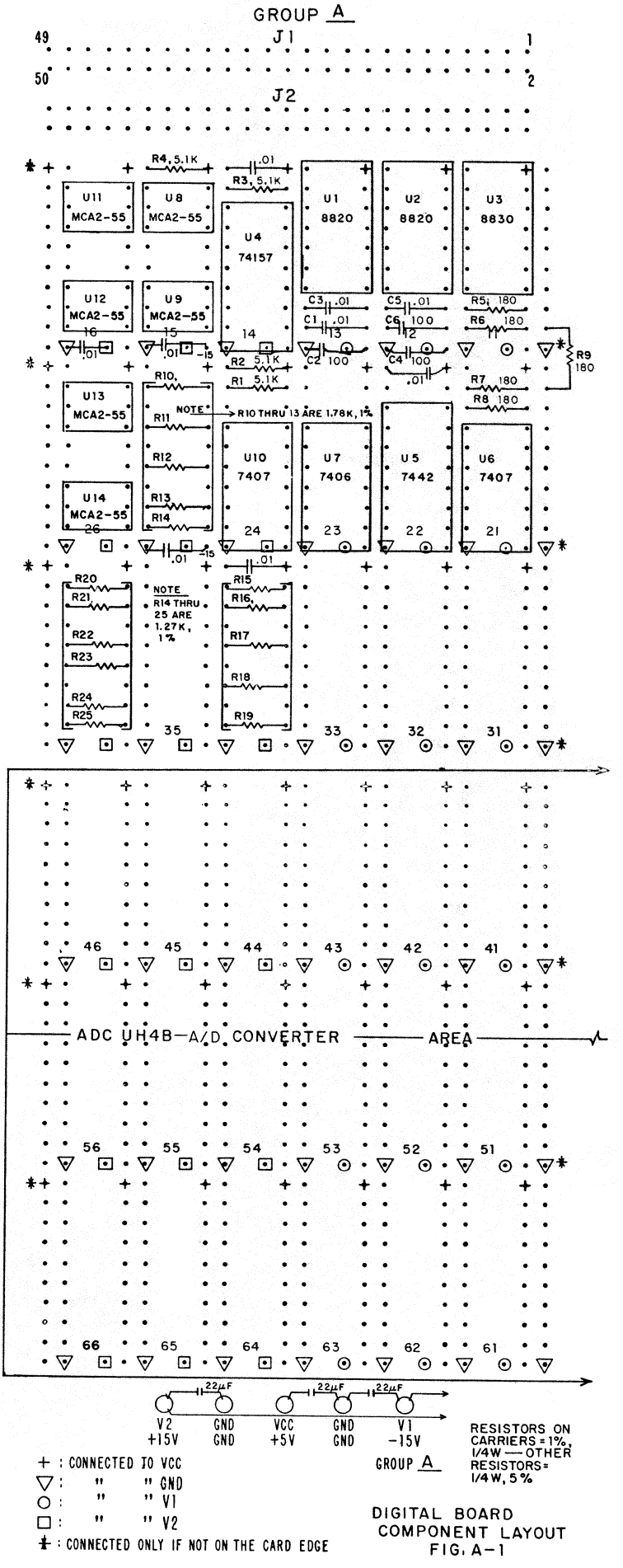


FIG.17 DIGITAL BOARD TIMING



DIGITAL BOARD COMPONENT LAYOUT
FIG. A-1

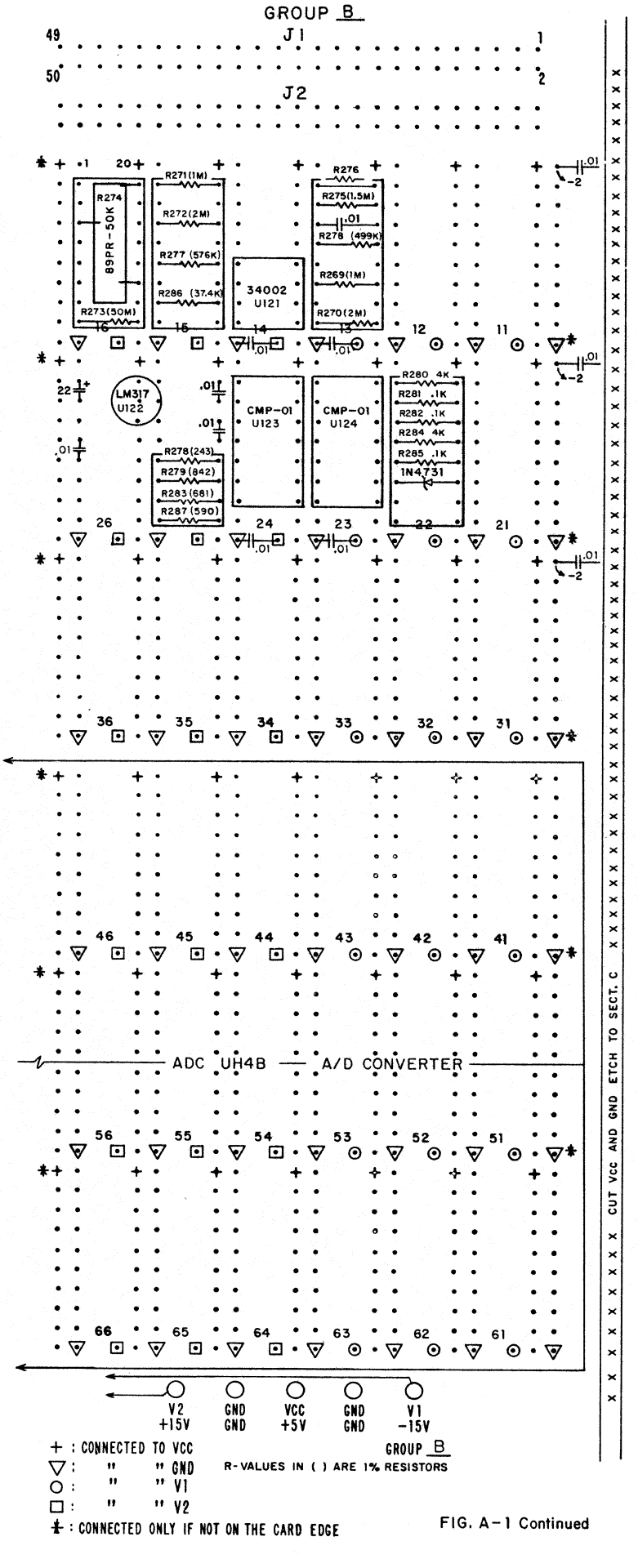


FIG. A-1 Continued

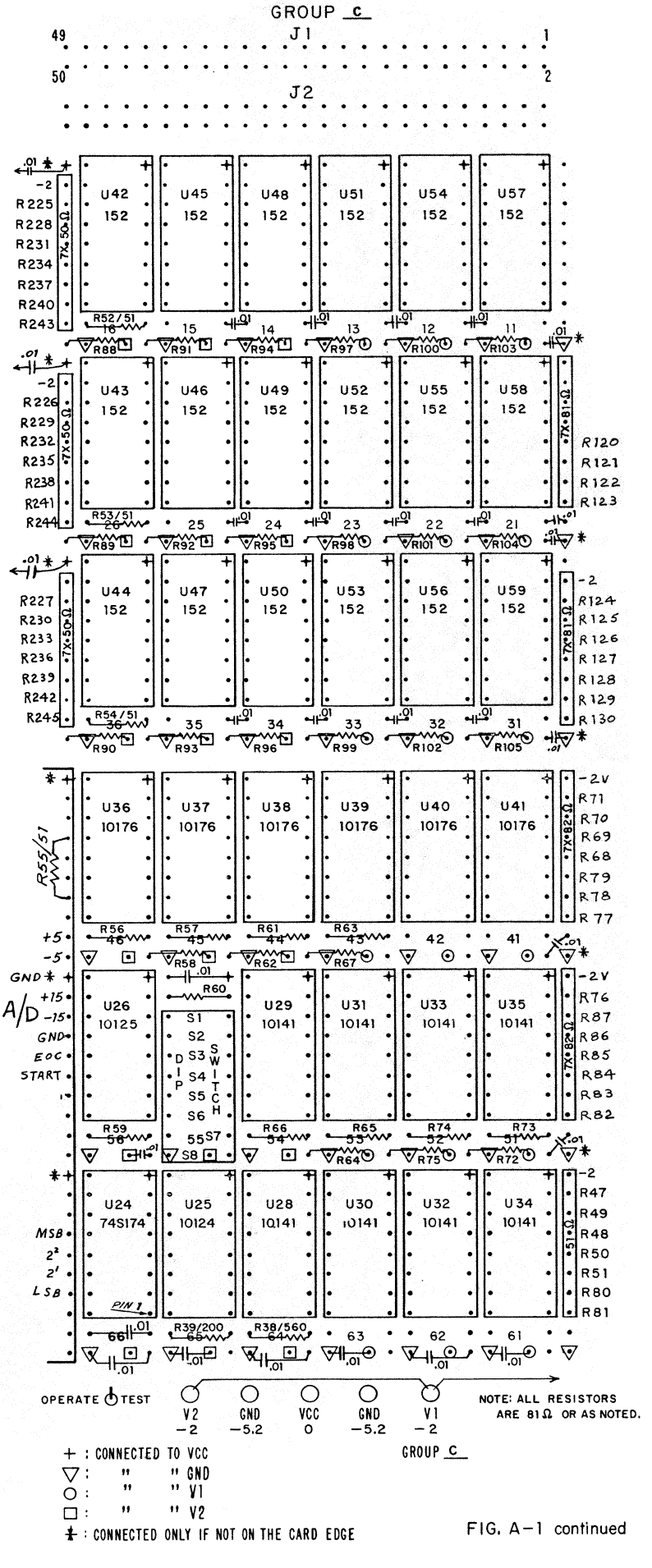


FIG. A−1 continued

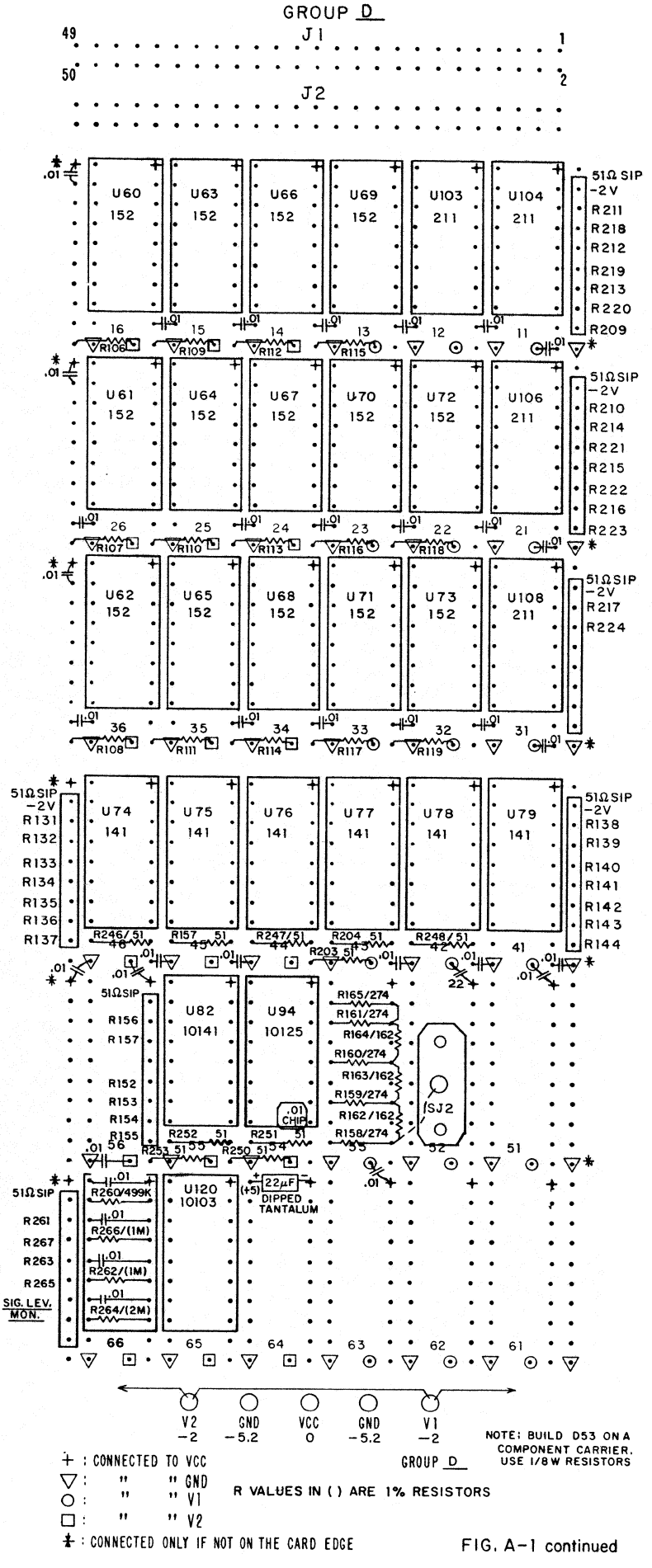


FIG. A-1 continued

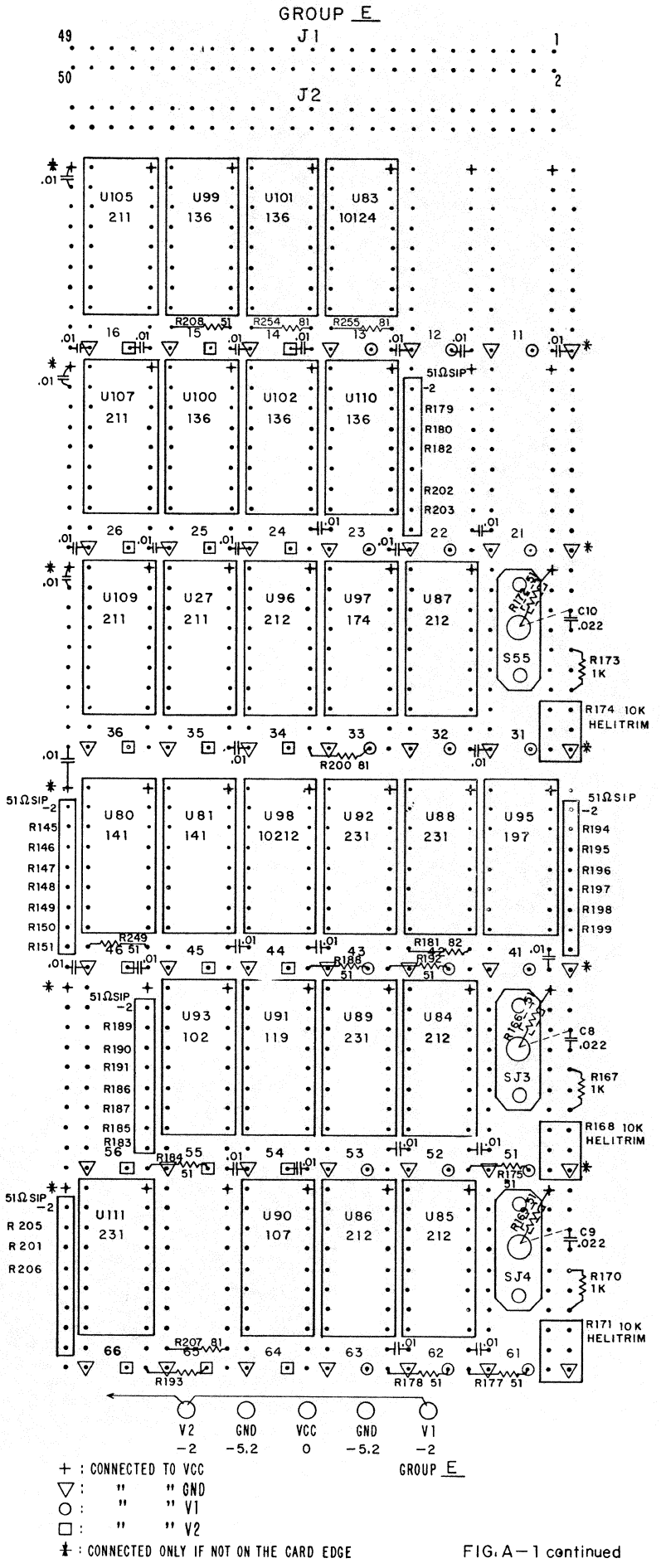
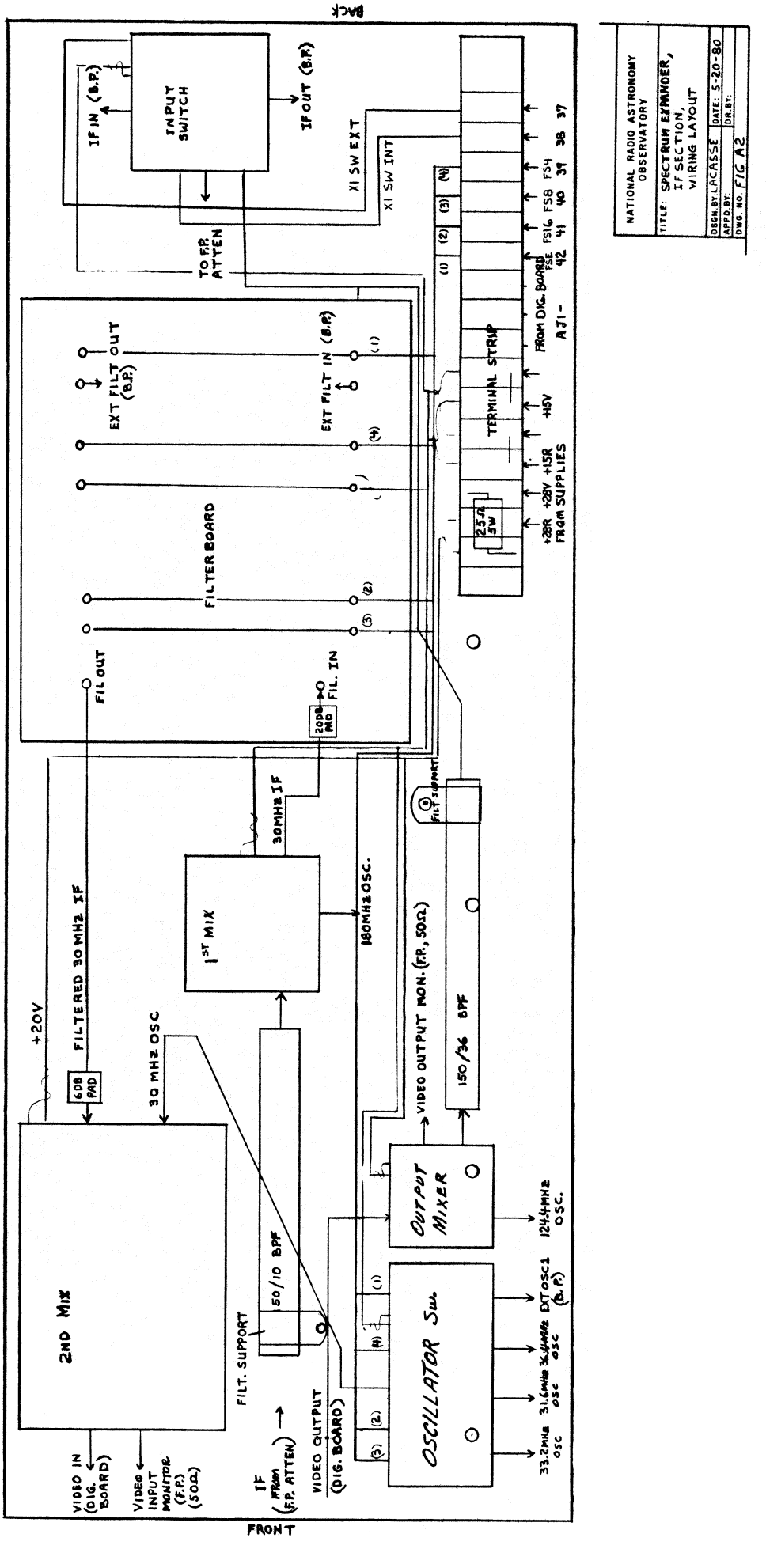


FIG. A−1 continued



NATIONAL RADIO ASTRONOMY OBSERVATORY

TITLE: SPECTRUM EXPANDER, IF SECTION, WIRING LAYOUT

DSGN BY: LACASSE | DATE: 5-20-80
APPD. BY: | DR. BY:
DWG. NO FIG A2

KEY FOR FIGURE A3

1. Digital Board
2. -2 V Regulator
3. TB1
4. TB2
5. -5.2 V Delay Circuit
6. Front Panel Assembly
7. -5.2 V Supply
8. +28 V Supply
9. +5 V Supply
10. +15 V Supply
11. ± 15 V Supply
12. Oscillators and Osc. Supplies
13. Back Panel Assembly
14. Oscillator Switch
15. Output Mixer
16. 150/10 Filter
17. Second Mixer
18. 6 dB Attenuator
19. 150/36 Filter
20. 20 dB Pad
21. First Mixer
22. Filter Board
23. TB4
24. Input Switch
25. TB3

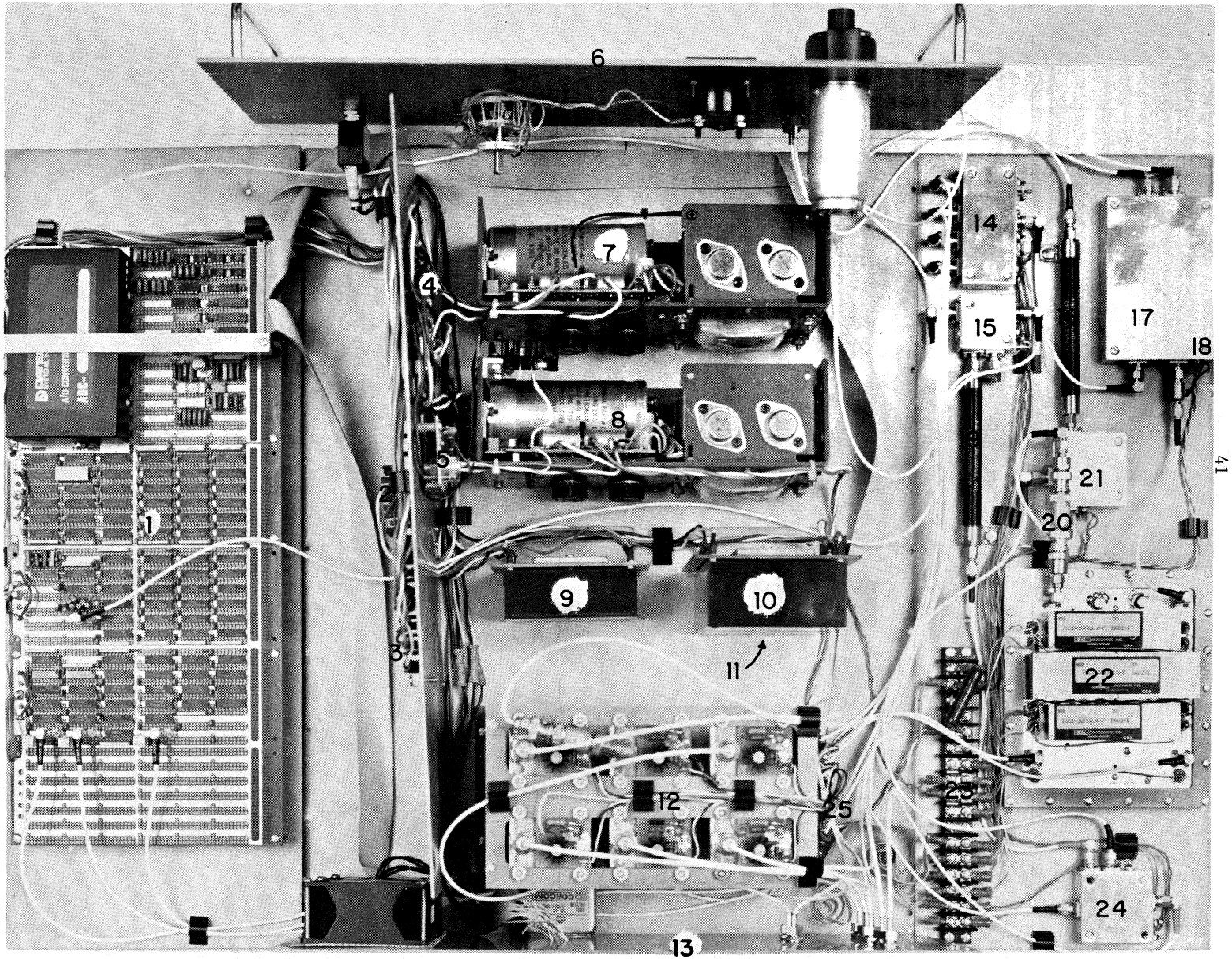


FIG. A3 SPECTRUM EXPANDER, EXPLODED VIEW

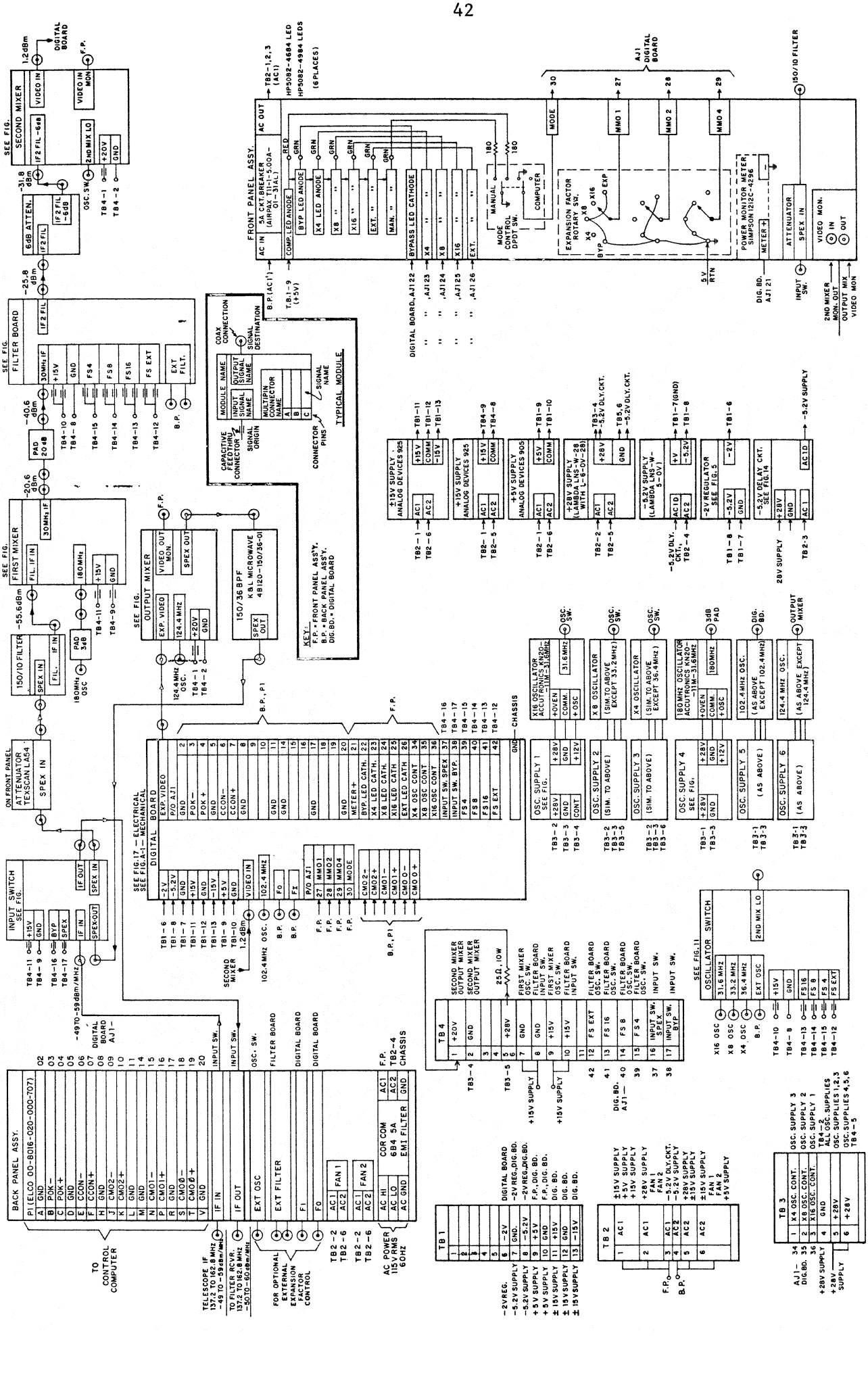


FIG. A4 INTERCONNECTION DIAGRAM