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THE 600 MHz NOISE PERFORMANCE OF GaAs MESFET's AT ROOM TEMPERATURE AND BELOW

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CHAPTER I

INTRODUCTION

1.1 Introduction and Purpose

For several years, the GaAs MESFET has been used to obtain high-gain low-noise amplification at microwave frequencies. Its performance far surpasses that of the bipolar transistor at frequencies of 4 GHz and above. However, little work has been done in realizing the GaAs FET's potential at frequencies of 1 GHz and below. The ready supply of inexpensive bipolar amplifiers with decent performance and the inherent problems associated with building a FET amplifier at low frequency (e.g., high Q input, poor stability, difficulty in obtaining a simultaneous low noise and power match) has caused the development of such low frequency FET amplifiers to lag far behind their high frequency counterparts.

The purpose of this project is to study the noise properties of FET's at frequencies near 500 MHz and also to determine the temperature dependence of this noise. It is also desirable to build a very low noise amplifier with greater than 15 dB of gain and good input and output match. This would be used as a front-end amplifier for radio astronomy applications. Specifically, amplifiers having noise temperatures of 50°K or less are needed for observations of pulsars and sources of continuum radiation.

1.2 Summary of Report

The following three chapters will now be briefly described. The purpose of chapter 2 is to furnish the reader with the basic principles of physics

involved in GaAs MESFET's. A discussion of FET operation, equivalent circuit, and material structure is followed by the noise theory for three different frequency ranges. The conclusion of the chapter describes what happens when the FET is cooled and it also provides a calculation of the thermal resistance of the FET.

Chapter 3 presents an amplifier centered at 500 MHz and capable of very low noise operation. The purpose of the design, the problems involved, and the measured results are all discussed. The concept of source inductive feedback is described in section 3.4. Also, an analysis of the noise increase due to losses in the input circuit is given.

Chapter 4 describes where most of the effort of this project was spent and where the most success was achieved. A 600 MHz amplifier of a different design was built. It exhibited nearly 60°K noise temperature at 298°K. However, when cooled, its noise temperature is lower than any other amplifier ever reported in this frequency band. Specifically, at ambient temperatures below 100°K, the amplifier noise temperature is below 20°K. Chapter 4 describes the design of this amplifier, its operation when cooled, the problems involved with oscillations, experimental results, and several other important topics.

CHAPTER II

FET DEVICE THEORY

2.1 Principles of FET Operation

Shockley proposed the first junction field-effect transistor device in 1952 [1]. It consisted of a semiconductor channel, the depth (and therefore resistance) of which is controlled by the reverse bias applied to the anode of a p-n diode which acts as a gate. The only difference between the JFET and the MESFET (metal semiconductor field effect transistor) which is the device to be studied in this paper, is that the p-type gate is replaced by a deposited metal gate (typically aluminum) which forms a Schottky junction. Figure 1 is a simplified device schematic showing the metal gate over the n-type channel.

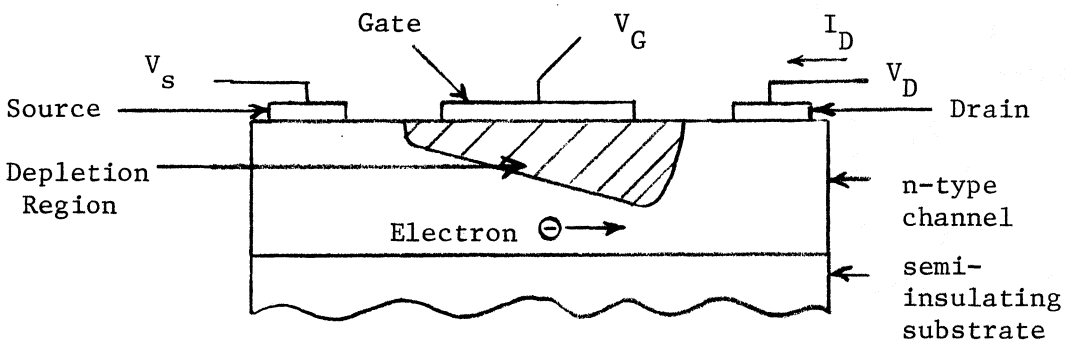


Figure 1. Simplified device schematic.

The current in this device is carried by majority carrier electrons that flow from source to drain when a positive potential V_{DS} is applied. This current is controlled by the depletion layer under the Schottky gate. The voltage on the gate determines how far the depletion region extends into the n-type channel. At low values of V_{DS}, the n channel acts as a linear resistor. As V_{GS} is made more negative, the gate depletion region extends further into the channel

and the current decreases. The depletion layer is wider at the drain end because the drain is biased positive with respect to the source, hence the reverse bias across the Schottky junction is larger at the drain end than at the source. The decrease in conductive cross section with position in the channel must be compensated by an increase of electric field and electron velocity to maintain a constant current through the channel. As drain voltage increases further, electron velocity saturates, and $V = V_S$ under the drain end of the gate. Further increase in V_d causes only a small increase in drain current as the depletion region continues to widen and change shape. As V_d increases in the saturation region, a larger number of electrons are injected into the velocity limited region which produces a finite drain to source resistance. Figure 2 shows the current-voltage characteristics for a typical MESFET.

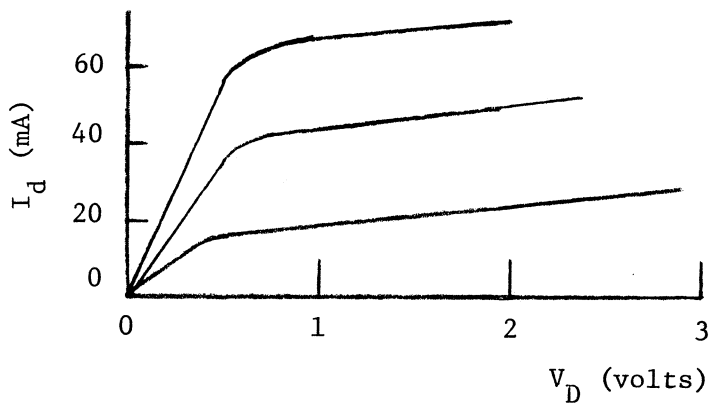


Figure 2. Typical MESFET current-voltage characteristics.

I_{dss} = saturated drain current when $V_g = 0$.

V_p = voltage sufficient to extend the gate depletion region across the entire channel causing $I_d = 0$.

In a GaAs MESFET, the velocity saturation behavior is more complicated than that of silicon due to the intervalley electron transfer at high electric fields. The equilibrium electron velocity reaches a peak at an electric field

of 3 kV/cm but then decreases to a value equal to the saturation velocity in silicon. See Figure 3.

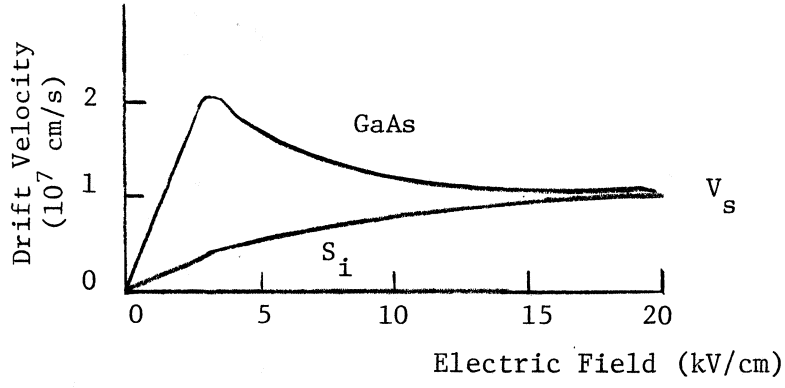


Figure 3. Equilibrium electron drift velocity versus electric field in GaAs and silicon.

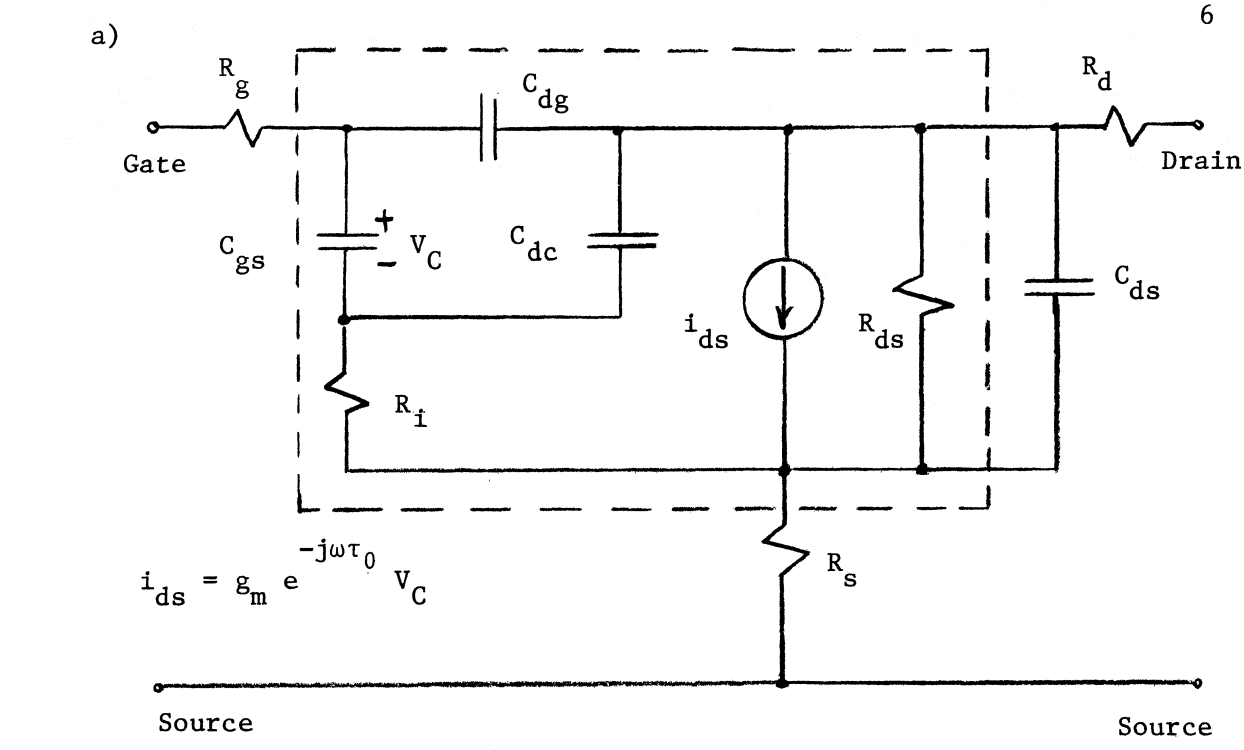
Modern microwave FET's have gate lengths of 1 μm or less. For geometries this small, the electrons do not have time to reach equilibrium velocity. This non-equilibrium effect has been simulated by Monte Carlo methods [2]. This effect causes a shortening of the electron transit time through the high field region.

2.2 FET Equivalent Circuit

The high frequency equivalent circuit for the MESFET along with the physical origins of the circuit elements are shown in Figure 4.

2.3 Material Parameters

MESFET's are fabricated by the planar process on a thin conducting GaAs epitaxial layer which has been grown on a thick semi-insulating GaAs substrate. Epi layers less than one micron thick are required to give devices with low operating voltages and good noise and gain performance. The semi-insulating GaAs substrate is doped with chromium. Impurities can diffuse out of the substrate during epi growth and decrease the active layer electron mobility near the



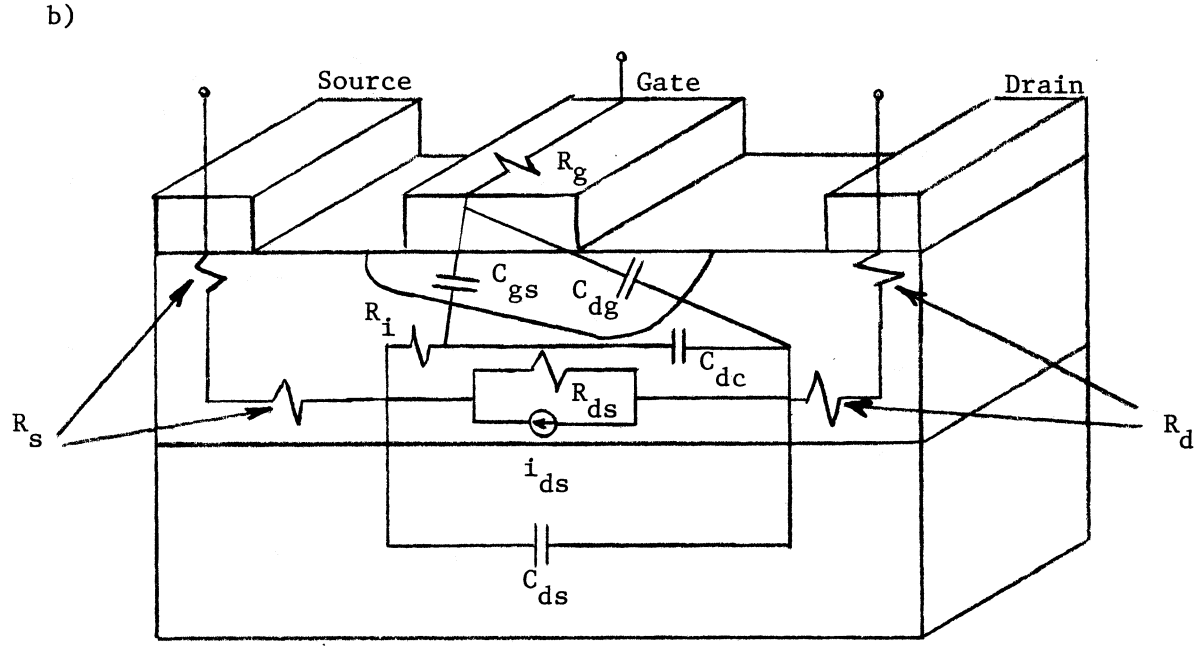


Figure 4. (a) Is the equivalent circuit of a MESFET.
(b) Illustrates the physical origin of the circuit elements.

epi-substrate interface. In many devices, a buffer layer of relatively pure GaAs (compared to the substrate) is grown on the substrate prior to the active layer growth. It acts as a barrier against the diffusion of impurities enabling near theoretical values of electron mobility to be obtained in the active layer.

Microwave FET's use GaAs because electrons have six times higher low field mobility (8800 cm^2 $[V\text{-}sec]^{-1}$ compared to 1350) and a two times higher maximum drift velocity as compared to silicon. Only n-type GaAs FET's are desirable since the hole mobility in GaAs is twenty times less than the electron mobility (400 cm^2 $[V\text{-}sec]^{-1}$ compared to 8800). The saturated velocities of electrons in GaAs and Si are equal. However, the higher mobility and maximum drift velocity of electrons in GaAs yield far superior high frequency performance.

The source to gate spacing and the gate length, L, should be small in order to minimize the source resistance and the electron transit time through the channel. Most devices currently on the market have 1 μm gate lengths, although some .5 μm devices are available and .2 μm devices have been fabricated in research and development labs. For short gate length devices, the current gain bandwidth, f_T, is proportional to $\frac{1}{L}$ [3]. Hence, through reduction of physical size and improved fabrication technology, FET's operating at 26 GHz with noise figures of 3 dB can be expected this year [4].

2.4 High Frequency Noise Theory

The sources of noise in FET's at high frequencies and at low frequencies are well understood and have been verified experimentally. However, there exists a frequency range from 20 MHz to 3 GHz in which very little experimental work and virtually no theoretical work has been done to explain the noise sources. It is within this frequency range that the work of this project is conducted. First, we will consider the well understood theories.

There are basically four types of noise that are important in the frequency range above 3 GHz for the intrinsic FET (neglecting parasitics). The first is thermal noise. The thermal motion of charge carriers will lead to a fluctuating emf across the ends of any hot resistance in thermal equilibrium. Hence, in the channel of the FET, a thermal noise voltage is developed in each incremental volume. Since the gate voltage is a constant, a fluctuation in the depletion layer voltage is developed which modulates the conductive cross section of the channel. The result is an amplified noise voltage at the drain [5].

The second contribution is hot electron noise. Most microwave FET's have gate lengths on the order of one micron or less which leads to high field strengths. At increased electric fields, the electrons are unable to dissipate all of their acquired energy to the lattice. Therefore, the electron population and the lattice are no longer in equilibrium although the entire electron population is in equilibrium with itself at a higher temperature. The "hot" electrons therefore exhibit more thermal noise than would electrons at the lattice temperature [6].

A third noise source that causes an increase in the electron temperature is called intervalley scattering noise. At low fields, the noise temperature increases with electric field in a similar way as in silicon due to the hot electron noise. But near the saturation electric field, the increase in noise temperature is very steep. In GaAs, as E approaches E_{SAT}, a considerable number of carriers are scattered from the central conduction band valley of the E-K diagram to a satellite valley. In the satellite valley, the mobility of the electrons drops to some fraction of the central valley mobility due to their increased effective mass. The current contribution of these carriers is nearly zero. This process is similar to the generation-recombination process in which carrier

density fluctuations generate noise. The net result of intervalley scattering is to further increase the effective noise temperature of the electrons [7], [8].

When analyzing high frequency FET noise, one must separate the transistor into two regions. In region I the electron velocity is not saturated, and in region II it is saturated. See Figure 5.

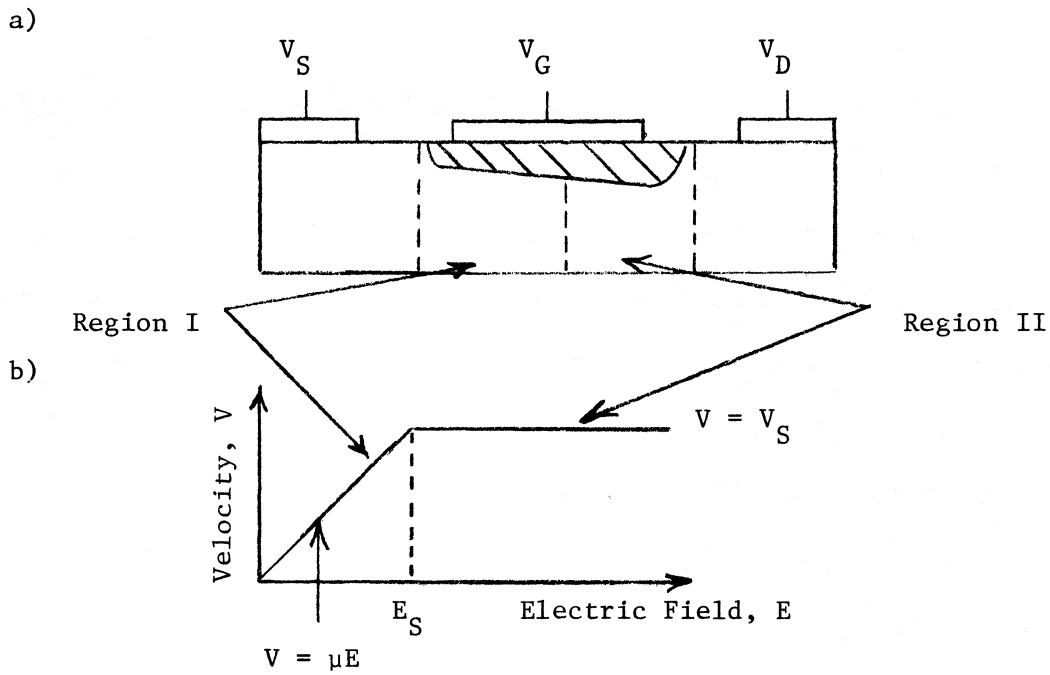


Figure 5. (a) The two section model of the FET.
(b) The linear approximation of the velocity field characteristic.

At large drain voltages, region II exists and the electrons there are at their limiting velocity. The electric field has no influence on the carrier drift velocity. Thus, this region cannot be treated as an ohmic conductor. The noise is properly formulated as high field diffusion noise, our fourth source of noise.

Pucel, et al. [9] has shown that the diffusion noise may be represented as a uniform distribution of spontaneously generated dipole layers. These dipoles drift unchanged to the drain electrode from their point of generation within the channel. The dipoles are created because of the thermal fluctuations of velocity, i.e., the distribution of electrons is not homogeneous at any instant of time. The dipoles sweep through region II at the saturated electron velocity so that the opposite charges do not have time to diffuse together and cancel. The dipole potential causes a potential to be induced on the open circuit drain electrode. Pucel, et al. has found that the noise generated by this mechanism increases linearly with drain current.

If noise voltages are generated locally in the channel, a fluctuation in the depletion layer width and a compensating charge variation on the gate electrode result. If the input is short circuited, we have a capacitive (displacement) noise current flowing in the input circuit which is partially correlated to the drain noise current [10].

Parasitic resistances of the FET also add to the noise temperature. The resistance due to the long, narrow gate metallization, R_g, and the resistance from the source ohmic contact plus the active layer between source contact and gate, R_s, generate thermal noise. These resistances are shown in Figure 4.

Pucel, et al. have combined the theories described above and have derived an equation for the minimum noise temperature for a FET.

$$T_{min} = 2\, T_0\, G_n\, (R_c + R_{opt}) \qquad \text{Eq. (1)}$$

$$T_0 = 290\ ^\circ K$$

$$G_n = \frac{K_g\, w^2\, C_{gs}^{\,2}}{g_m} = \text{noise conductance from Rothe-Dahlke representation. (See Appendix A.)} \qquad \text{Eq. (2)}$$

$$R_c = \text{correlation resistance} = \text{Re}\ (Z_c) = \text{Re}\left\{R_g + R_s + \frac{K_c}{Y_{11}}\right\} \quad \text{Eq. (3)}$$

$$R_{opt} = \text{optimum source resistance} = \left\{R_c^2 + \frac{r_n}{G_n}\right\}^{1/2} \quad \text{Eq. (4)}$$

Pucel, et al. uses the correlation impedance convention for noise description [11] which is not the same as the description used in this paper. Specifically, do not mistake r_n used by Pucel, et al. and R_N used later in this paper. (See Appendix A for a discussion of the noise description used in this report.) R_g and R_s are the gate and source parasitic resistances which were previously described.

$$Y_{11} = \frac{I_1}{V_1}\Big/_{V_2 = 0}$$

C_{gs} = gate to source capacity

w = radian frequency

g_m = transconductance

R_i = intrinsic gate to source resistance

K_c, K_g, K_r = functions of bias and geometry which are plotted in Pucel, et al.

Figure 6 explains the physical meaning of the above parameters in a noise equivalent circuit for the FET.

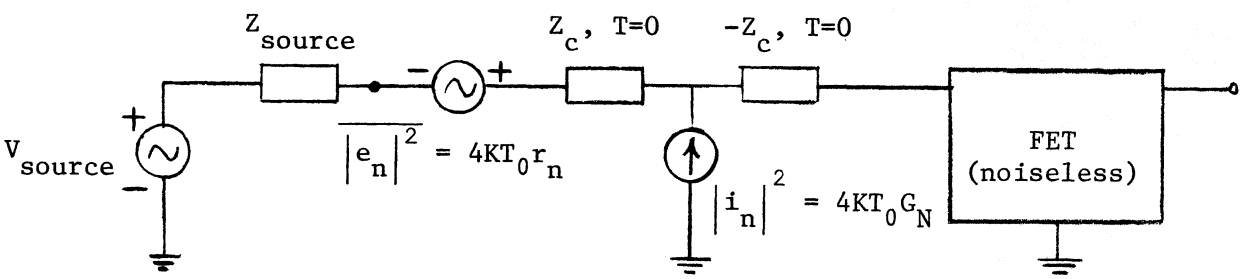


Figure 6. Noise equivalent circuit used by Pucel, et al., in deriving equation 6.

When typical FET parameters (e.g., for the HFET-1000 by Hewlett-Packard) are substituted into the above equations, we find that

$$R_{opt} \simeq \left[\frac{r_n}{G_n}\right]^{1/2} >> R_c \qquad \text{Eq. (5)}$$

and

$$T_{min} \simeq 2T_0 \left[G_n r_n\right]^{1/2} \qquad \text{Eq. (6)}$$

The only frequency dependent term in this equation is G_n which is proportional to the square of frequency. Hence, T_{min} is directly proportional to frequency. If one calculates the largest possible value of T_{min} using worst case values of FET parameters, one obtains T_{min} = 10°K at 500 MHz and T_{min} = 12°K at 600 MHz.

Another form of the high frequency noise equation has been developed by Fukui [12]. This form expresses the noise dependence upon material and geometrical parameters in a more direct manner. Fukui's equation is given below.

$$T_{min} = 290\ K\ f\ L^{5/6} \left\{\frac{N}{a}\right\}^{1/6} W^{1/2} \left[R_g + R_s' + R_{con}\right]^{1/2} \qquad \text{Eq. (7)}$$

Again we note that T_{min} is proportional to frequency.

$$R_g = \text{gate metal resistance} = \frac{3.3\ W\rho}{hL} \qquad \text{Eq. (8)}$$

R_s' = gate to source parasitic resistance not including contact resistance

$$= \frac{1.8\ L_{sg}}{W\ N\ a_1}$$

Below are parameter definitions along with the approximate values for the HFET-1000.

K = noise coefficient = .033 for good FET's.

f = frequency in GHz = .5 and .6.

L = gate length in μm = 1.

N = free carrier concentration x 10^{16} cm^{-3} in active channel = 10.

a = active layer thickness under gate in μm = .2.

W = unit gate width in mm = .25.

τ = gate metallization resistivity x 10^{-6} $\Omega \cdot cm$ = 2.62 for Al.

h = gate metallization thickness in μm = .5.

L_{sg} = spacing between gate and source in μm = .5.

a_1 = thickness of channel between source and gate in μm = .3.

R_{con} = specific contact resistivity x 10^{-6} $\Omega \cdot cm$ for source and drain contacts = 5.

a_2 = thickness of channel under source in μm = .3.

Many of the above parameters are explained in Figure 7.

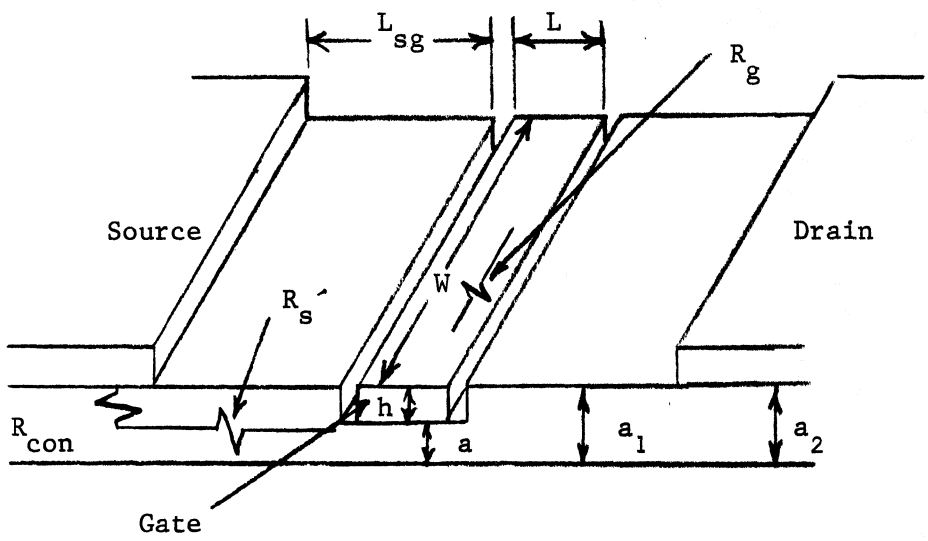


Figure 7. Physical description of the parameters appearing in equation (7).

We calculate $R_g = 4.32\ \Omega$, $R_s' = 3.6\ \Omega$, $R_{con} = 2.19\ \Omega$, $R_{tot} = 10.1\ \Omega = R_g + R_s' + R_{con}$; $T_{min} = 14.6°K$ at 500 MHz, $T_{min} = 17.5°K$ at 600 MHz.

Note that both equations describing the high frequency FET noise behavior predict a very low noise temperature at 500 and 600 MHz.

2.5 Low Frequency Noise Theory

In the frequency range of 20 MHz and below, the high frequency noise mechanisms are no longer important. Sah [13] has shown that the major low frequency noise contribution in a silicon JFET comes from the fluctuation of Shockley-Read-Hall recombination-generation centers in the gate depletion region. In the depletion region, the electron and hole emission processes are the most important since the high electric field depletes the electron and hole populations in this region making the capture process improbable. The random voltages generated in each incremental volume of the depletion region due to the g-r processes modulates the depletion layer width and the channel width by a small amount. The current passed through this varying resistance produces an output noise power proportional to $\tau(1 + \omega^2 \tau^2)^{-1} f\{V_d, I_d, V_g\}$.

$$\tau = [C_p p_1 + C_n n_1]^{-1} \quad p_1 = n_i \exp\left\{\frac{E_t - E_i}{kT}\right\} \quad n = n_i \exp\left\{\frac{E_i - E_t}{kT}\right\} \qquad \text{Eq. (10)}$$

τ = fluctuation time constant of the single level Shockley-Read-Hall center.

C_p, C_n = capture probabilities for holes and electrons, respectively.

n_i = intrinsic carrier concentration.

E_t = quasi-Fermi level for SRH center.

E_i = intrinsic Fermi level.

$f\{V_D, I_D, V_G\}$ = function of FET bias.

The time constant, τ, is a strong function of temperature as seen above in the equations for P_1 and n_1. As temperature changes, we expect a noise maximum when $\tau = \omega^{-1}$.

From measurements made with GaAs MESFET's at frequencies below 1 MHz [14], it was found that at higher temperatures (150°K to 300°K) 1/f noise is observed. This could be due to contact noise or a continuum of trapping energy levels. Measurements at lower temperatures (80°K to 150°K) indicate the presence of several distinct generation-recombination processes characterized by different time constants.

Another noise mechanism not included in the high frequency theory describes charge fluctuations in the channel. Van der Ziel [15] has analyzed the effect of carrier population fluctuations in the channel due to random generation-recombination or trap processes. The resulting noise power spectrum is proportional to $I_D V_{DS} \frac{\tau}{1 + \omega^2 \tau^2}$; $I_D V_{DS}$ being the power dissipated in the channel and τ is the time constant of the fluctuation process. Measurements [16] have verified this dependence upon dissipated power.

2.6 Noise at 600 MHz

Noise measurements in the 20 MHz to 3 GHz frequency range are more difficult to perform than at other frequencies because of the FET's very low noise temperature. At much lower frequencies, the noise levels are so large that the measurement of the channel as a hot resistor can be made directly (e.g., by connecting a spectrum analyzer across the FET terminals with the gate shorted.) At very high frequencies, tuning for optimum source impedance and minimum noise temperature can be done with a slide screw tuner or a double stub tuner. Then the noise parameter T_{min} is known and Z_{opt} can be determined by disconnecting the FET

from the tuner and measuring the source impedance with a network analyzer. The losses of these tuners provide only a small correction factor for the amplifier noise. In the 20 MHz to 3 GHz range, the noise is very small and the channel cannot easily be measured as a hot resistor over a wide frequency range. Also, the losses in a tuner mechanism contribute a greater percentage of the total measured noise. It would be quite difficult to operate a tuner within a cryogenic refrigerator. Therefore, individual amplifiers must be built at each frequency in order to explore the FET's noise performance.

It would be informative to review noise measurements made in this frequency range by other authors. It is well known that below 3 GHz the FET noise temperature no longer decreases linearly with frequency. Instead, it falls off more slowly. In his review paper, Cooke [4] describes measurements of noise between 30 MHz and 6 GHz. By measuring many samples, he found the minimum noise temperature to vary drastically between devices at frequencies below 1 GHz. Figure 8, taken from his paper, illustrates that the lowest noise temperature measured at 600 MHz was about 55°K whereas the highest was 120°K. Measurements were made at room temperature.

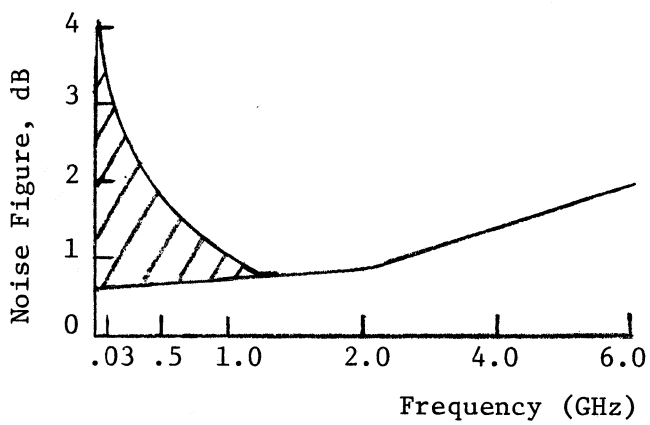


Figure 8. A plot of Cooke's noise figure measurements over a wide frequency range for several FET's.

Sando [17] has built a 432 MHz amplifier using an NEC 24406 chip. He has demonstrated a minimum noise temperature of 50°K at this frequency. Anastassiou and Strutt [18] report minimum noise temperatures of 90°K at 500 MHz using FET's from Plessey. The lowest reported noise temperature at low frequency is from Hoult and Richards [19] who built a 120 MHz preamplifier cooled in liquid nitrogen (77°K). They measured 21°K using a Plessey FET. We conclude that the noise temperature expected from a FET at low frequency is greatly dependent upon the conditions and techniques of fabrication of that individual FET.

By comparing the room temperature noise measurements measured above with the numbers predicted from the high frequency theory (i.e., 50° to 90°K vs. 15°K at 600 MHz) it is apparent that there exists some unexplained source generating this excess noise. From experimental data, Pucel, et al. have claimed that sources at the epitaxial layer-substrate interface, presumably traps, can generate drain current noise whose spectrum extends from 30 MHz to 5 GHz. Luxton [20] has improved FET noise figures at microwave frequencies by growing a high resistivity epitaxial buffer layer between the substrate and the channel. Perhaps this buffer zone decreases the trapping probability of states located at the substrate interface. The noise produced by such traps should follow the theoretical derivation of Van der Ziel which has already been discussed (i.e., carrier fluctuation noise in the channel). In conclusion, the FET noise in this frequency band is not well understood. Significant steps toward reducing this noise through changes in FET design or processing are unlikely unless further information is found.

2.7 FET Noise at Reduced Temperatures

A major advantage possessed by GaAs MESFET's over silicon bipolar transistors or FET's is that the device can operate at very low temperatures with an

expected reduction in noise. For silicon at temperatures below 125°K, electrons are frozen out of the conduction band and holes out of the valence band. This leaves a semiconductor with very few carriers and uncapable of supporting device action. However, in GaAs no freeze out occurs due to the extremely small energy gap between the donor levels and the conduction band for most n-type dopants used in FET's (6 meV for sulphur, selenium, and tin; 3 meV for Telerium [21]).

Since the physical mechanisms of 600 MHz noise at room temperature are not understood, it is difficult to predict what is going to happen when the FET is cooled. However, perhaps by comparing theoretical expectations of certain noise mechanisms with experimental data, something can be said about the dominant FET noise mechanisms. Thermal noise will definitely be reduced as temperature drops. The thermal noise in the output circuit of the FET will be proportional to $\frac{T}{g_m}$ where T is the ambient temperature and g_m the FET transconductance [5]. Not only does T decrease but g_m should increase due to the increased free carrier mobility and saturated velocity in GaAs. The decrease in mobility is due to fewer collisions with a less energetic lattice and should be proportional to $T^{-3/2}$, hence $g_m \propto \mu \propto T^{-3/2}$. Past a certain temperature, the mobility again begins to decrease and is proportional to $T^{3/2}$. In this region, scattering from impurities is dominant. The output circuit thermal noise should decrease more slowly when the transconductance begins to decrease with temperature.

The thermal noise produced in the input gate to source circuit by the parasitic resistances R_g and R_s will cool linearly with temperature. In this case $T_{noise} \propto T_{ambient}$.

Finally, it was previously mentioned that generation-recombination and trap noise will have a peak at some temperature due to the temperature dependence of the time constant. The noise should fall off as we move away from the peak in either direction for a single energy level process.

Experiments have proven the effectiveness of cooling FET amplifiers. Noise temperatures of 25°K at 1.4 GHz [22], 30°K at 4 GHz [23], and 60°K at 12 GHz [24] have been reported. The 12 GHz measurement was made at an ambient temperature of 90°K; the other two were at 77°K. This should be compared to room temperature values of 50°K, 150°K, and 350°K, respectively.

2.8 FET Thermal Resistance

Since one of the major purposes of this research is to measure FET performance at cryogenic temperatures, one must calculate the thermal resistance of the FET chip itself (assuming the chip is contacted along its entire bottom surface). One must take into account the fact that the heat is generated in a very narrow channel near the surface of the FET. The heat must be conducted to the opposite side of the FET which is soldered to a large heat sink. Cooke [4] has obtained an equation for the thermal resistance of a FET chip. He assumes that the thermal model of the microwave FET is analogous to the RC model of a transmission line. The equation which is obtained for a single gate FET is based upon Cohn's calculation for the characteristic impedance of a microstrip line [25].

$$\theta = \text{thermal resistance} = \frac{K(k)}{2W_g K_{Th} K(k')} \qquad \text{Eq. (11)}$$

$$k = \operatorname{sech} \frac{\pi L_g}{4F}, \qquad k' = \tanh \frac{\pi L_g}{4F}$$

K = complete elliptical integral of the first kind.

Given below are parameter definitions and actual values for the HFET-1000:

L_g = gate length = 1 μm

W_g = gate width = 500 μm

F = chip thickness = .13 mm

K_{Th} = thermal conductivity = $10 \frac{W}{cm\ °K}$ [26] for semi-insulating C_r doped GaAs substrate at 20°K.

We calculate $\theta = 4.14 \frac{°K}{W}$.

CHAPTER III

A 500 MHz AMPLIFIER

3.1 General Description

The first experimental goal of this project was to design and build an amplifier with a frequency response centered at 500 MHz and optimized for low noise performance. By taking noise measurements at four separate values of source impedance, one can obtain all four noise parameters of the FET. A block diagram of the high frequency circuit is shown in Figure 9.

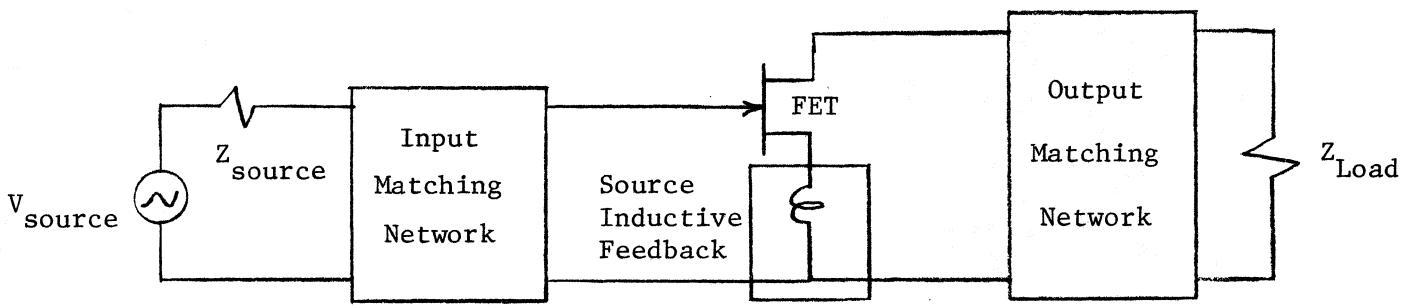


Figure 9. Block diagram of the 500 MHz amplifier.

The input matching network is used to change the value of the source impedance, Z_s, seen by the FET whereas the output matching network is used to obtain optimum power match and maximum output return loss (i.e., to match the output of the FET to the load impedance which is 50 Ω for most systems).

In this amplifier, the input matching network is a tee network shown in Figure 10 consisting of one capacitor and two inductors. The tee network transforms the source impedance from a value of R_{source} (typically 50 Ω) to a value of

$$Z_s = j\omega L_1 + \frac{j\omega R_{source} L_2 + \frac{L_2}{C_1}}{R_{source} + j\left(\omega L_2 - \frac{1}{\omega C_1}\right)} \qquad \text{Eq. (12)}$$

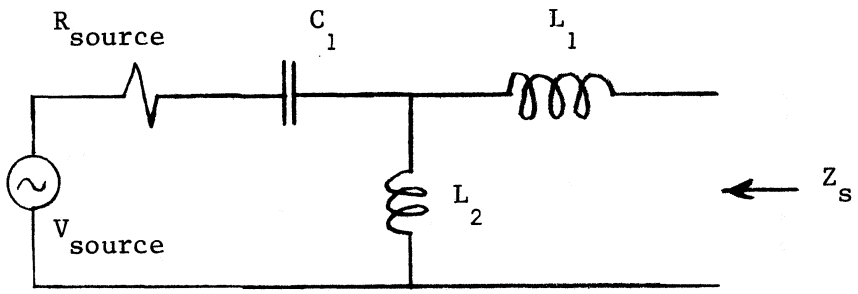


Figure 10. Schematic of the input matching network.

3.2 Specific Design

For design purposes, a simplified version of the FET equivalent circuit can be used as is shown below in Figure 11.

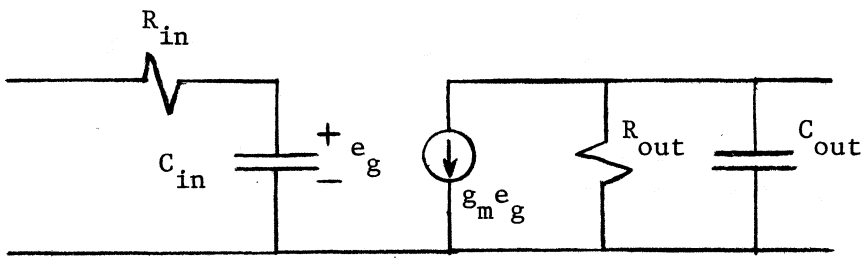


Figure 11. Simplified FET equivalent circuit.

Values for the equivalent circuit can be calculated from the measured s-parameters published by the manufacturer. The HFET-1000 from Hewlett-Packard was the chip most often used during this project. The circuit values calculated from the 2 GHz s-parameters measured at optimum noise bias are: R_{in} = 15 Ω,

C_{in} = .5 pF, R_{out} = 300 Ω, C_{out} = .15 pF, and g_m = 27 mmhos. We note that the input of the FET is an extremely high Q circuit (Q = 42 at 500 MHz). Therefore, it is difficult to obtain a good power match over a broad frequency range.

The FET was mounted on a standard, glass filled, gold plated, TO-5 transistor header. It is attached using Epo-Tek [27] conductive epoxy. Conductive epoxy is necessary in order to maintain a good ground on the gold plated bottom of the FET. There is an N - N^+ junction at the active layer — substrate boundary. The back side ground keeps the depletion layer (which extends into the channel due to the work function difference between the regions) at a constant depth. Hence, there is no back gate bias modulation of the current.

One mil aluminum wires were bonded from header posts to the 4 mil square FET drain and gate pads using an ultrasonic wedge bonder. The two source pads must be stitched together to obtain full usage of the FET's channel width. A wire is then bonded from source pad to header to add inductance into the source lead. The reason for this inductance is discussed in section 3.4. Figure 12 shows the FET mounted on the header. Figure 13 illustrates the pad configuration of the HFET-1000.

The header adds shunt capacity to both the input and the output circuits where the leads come through the header. This capacitance has been measured to be .5 pF on a low frequency bridge. However, measurements using a network analyzer indicate that this capcitance is closer to .7 pF. This added capacity increases the Q of both the input and the output circuits and must be taken into account while calculating the source impedance presented to the FET. The series inductance of the header leads is negligible at 500 MHz.

The layout of this amplifier is similar to a 1.4 GHz FET amplifier design by D. Williams [22]. A printed circuit board is mounted in a Modpak [29] module. The circuit board is tin plated, 62 mils thick, copper clad RT Duroid [36] with

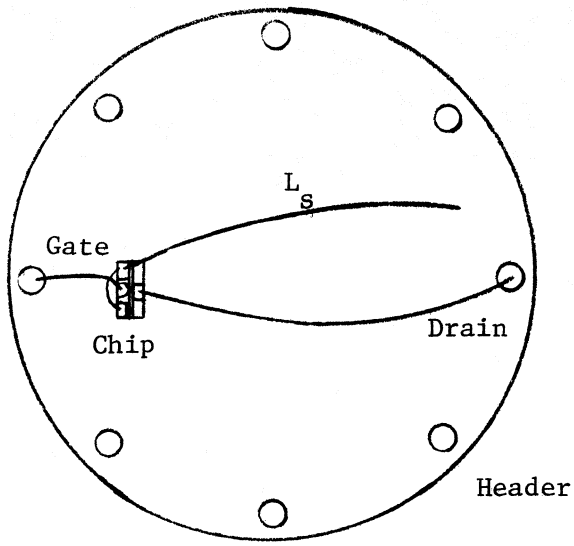
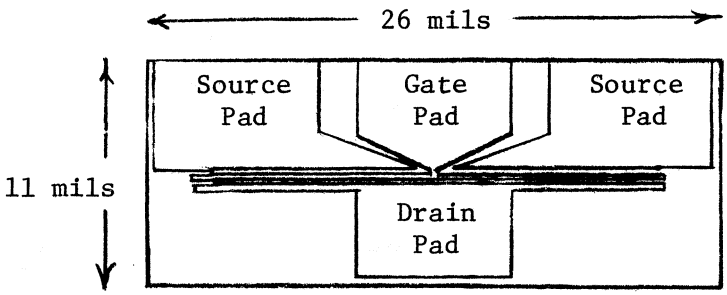


Figure 12. FET mounted on header with bonding wires.

a)



b)

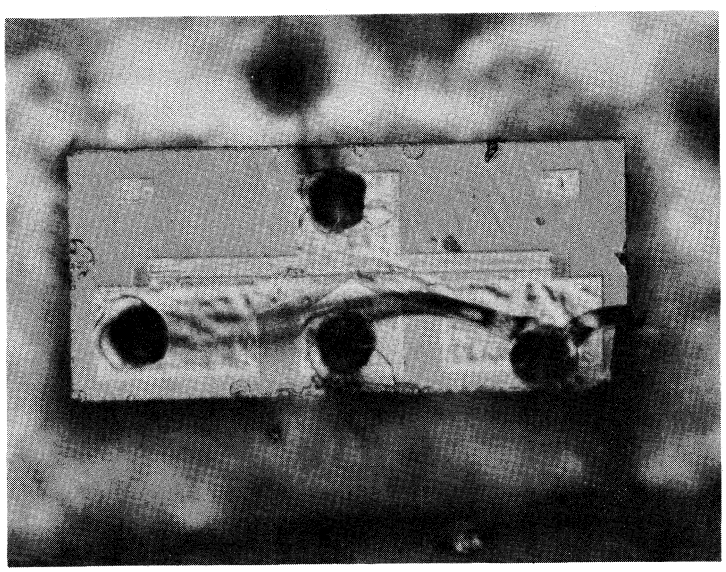


Figure 13. (a) HFET-1000 bonding pad layout and dimensions.
(b) Photograph of HFET-1000 with bonding wires.
Magnification = 100X.

a very low loss teflon glass dielectric (loss tangent = 9×10^{-4} over a broad frequency range). The board acts primarily as a physical support for the lumped elements that make up this circuit at 500 MHz.

Chip capacitors from American Technical Ceramics [30] were used. Coils were wound by hand using 8 mil diameter phosphor bronze wire. Phosphor bronze was chosen because its springy mechanical quality enables the small coils to be handled without changing the shape or inductance of the coil. To get an idea of what size coil will provide how much inductance, the equation

$$L = \frac{n^2 r^2}{9r + 10\ell}\ \mu H \quad [3] \qquad \text{Eq. (13)}$$

was used where all dimensions are in inches and

n = number of turns

r = coil radius.

ℓ = length of the inductor.

However, for coils of only 2 or 3 turns, this equation introduces significant errors. Correct values were found by measuring coil impedance versus frequency on a network analyzer from which the inductance can be calculated.

A circuit schematic of the entire amplifier is shown in Figure 14. Figure 15 is a view of the physical layout of the front and back of the amplifier circuit board. At the input of the circuit, we have the three elements of the input matching network: C_1, L_1, and L_2. C_{pad} (= .2 pF) is a parasitic capacity which is also present in the output circuit. The physical source of this capacitance is the 100 x 200 mil metal pads as seen in Figure 15. An approximation of this capacitance is found by using either the parallel plate formula or

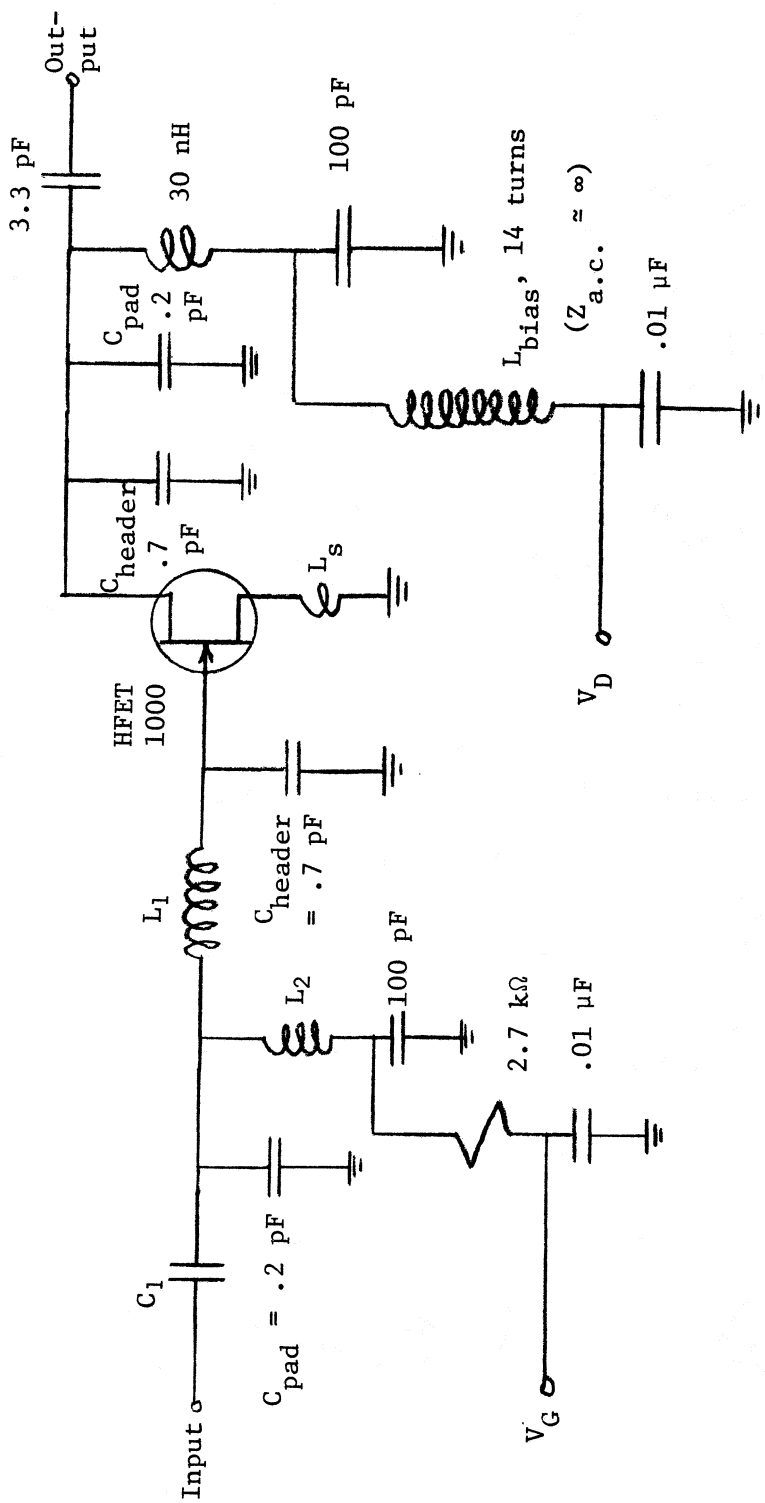
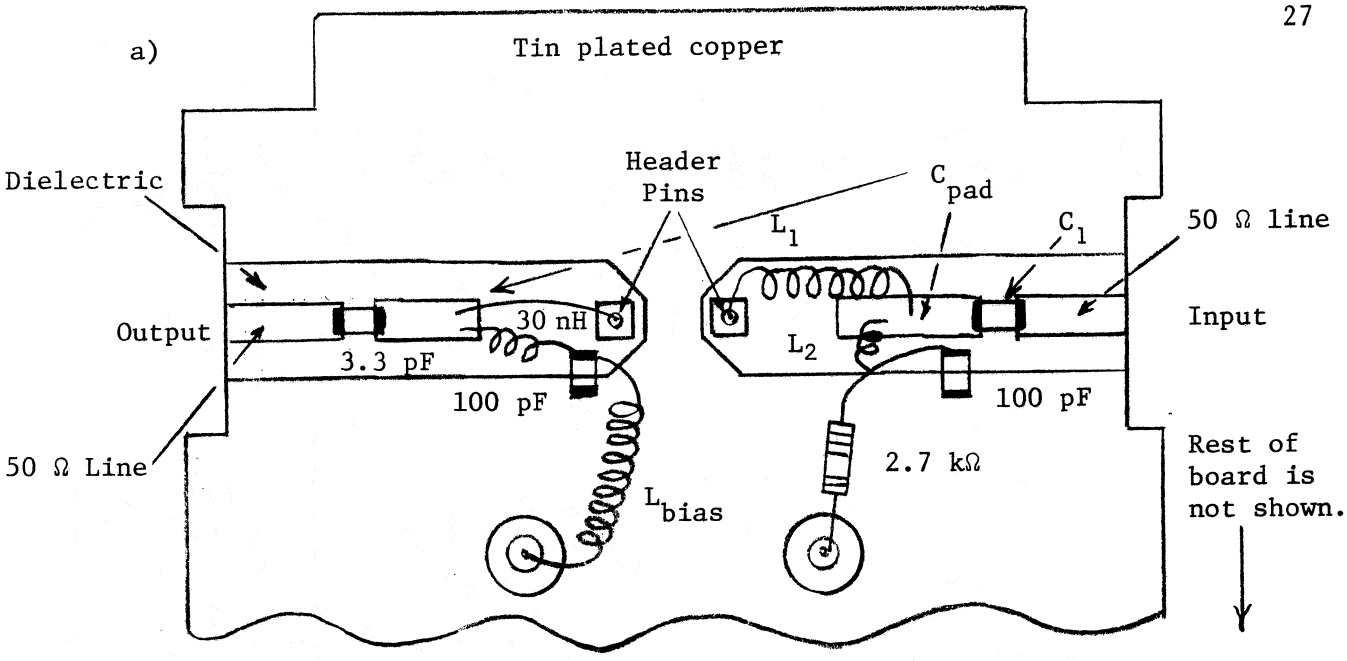


Figure 14. Total circuit schematic of the 500 MHz amplifier described in this chapter.



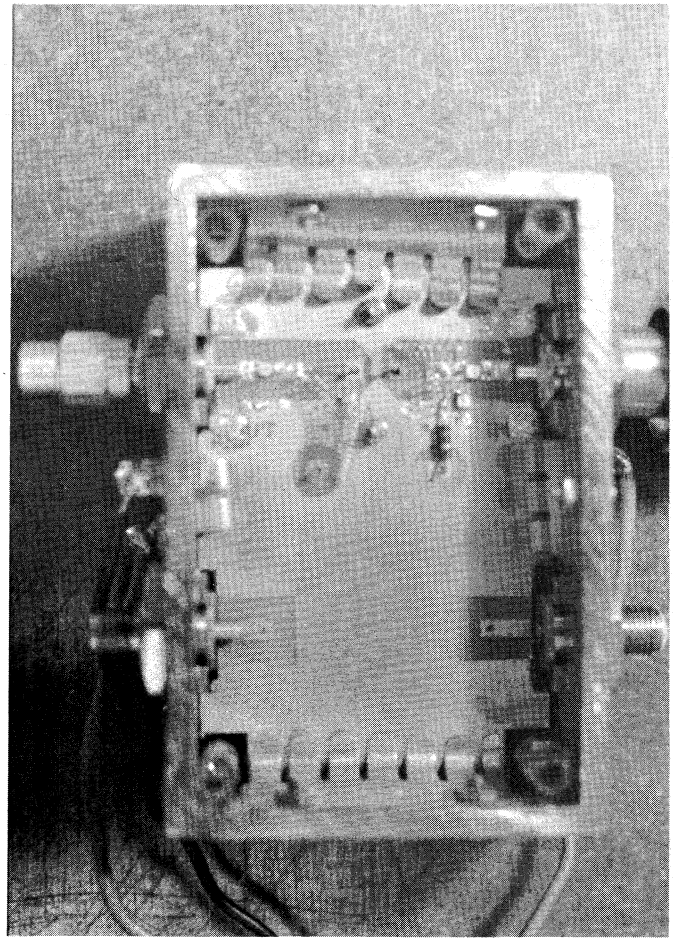
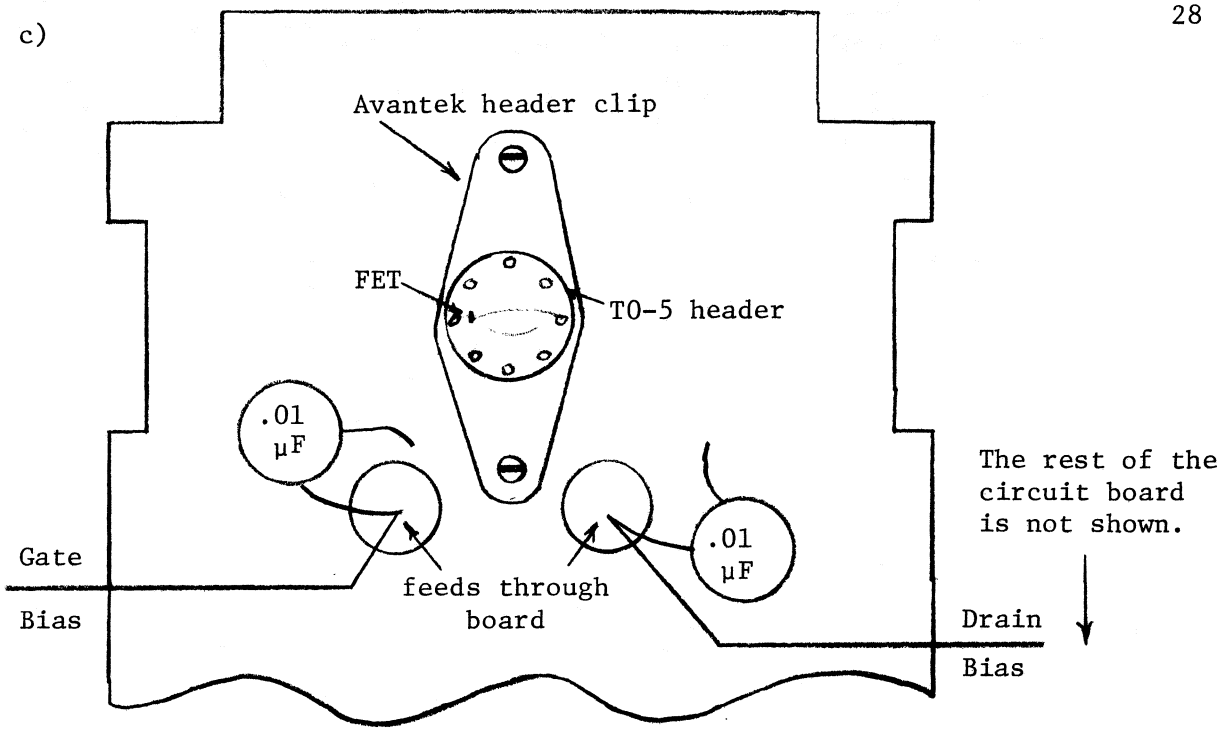


Figure 15. (a) Physical layout of the top of the amplifier circuit board.
(b) Photograph of the top half of the amplifier.

c)



d)

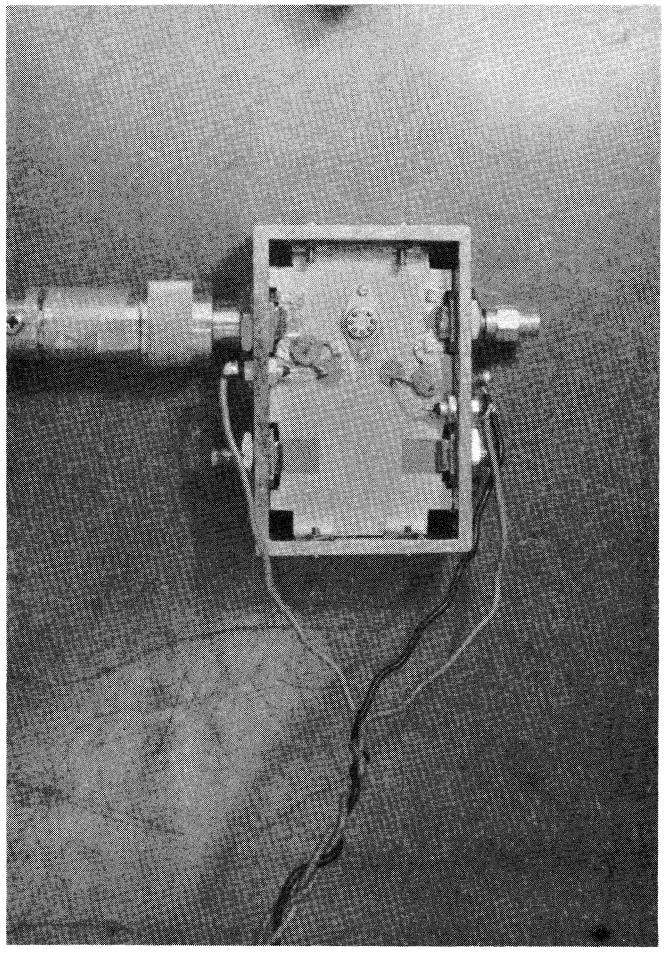


Figure 15. (c) Physical layout of bottom of amplifier circuit board.
(d) Photograph of bottom of amplifier.

using transmission line concepts. The 100 pF capacitor provides an a.c. ground for L_2. The gate bias line has a .01 μF shunt capacitor to protect the gate from bias transients. A 2.7 KΩ series resistor protects the gate from a large current in the case of an accidental forward bias. The .7 pF header capacitance is shown both in the input and output circuits. The FET is biased in the common source configuration and the source inductance is shown.

Power match for the output circuit is produced by a shunt 30 nH inductor and a series 3.3 pF capacitor. If the output impedance of the FET is Z_{out}, these two circuit elements transform 50 Ω to a value of Z^*_{out} at 500 MHz. See Figure 16.

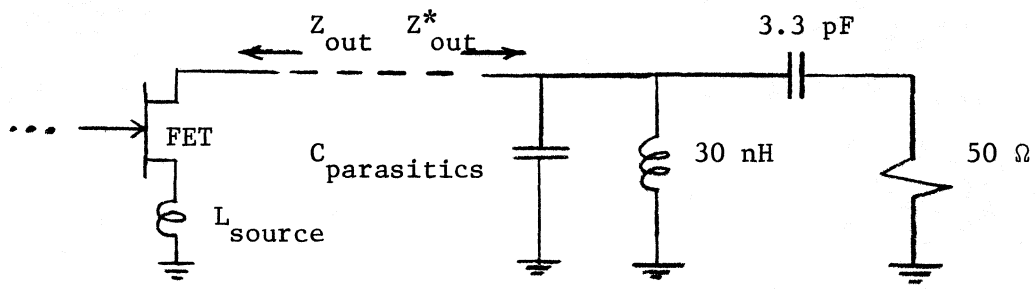


Figure 16. Illustration of the output matching network for the 500 MHz amplifier.

The 100 pF capacitor provides an a.c. ground. The large inductor in the drain circuit is designed to have its resonant frequency very near 500 MHz so that its a.c. impedance is very large. Experiments show that resonance occurs when the length of the wire in the coil is a quarter wavelength, i.e.,

$$2\pi rn = \frac{\lambda_{res}}{4} \quad [31] \qquad \text{Eq. (14)}$$

The drain bias passes through this coil and the 30 nH coil, while the 3.3 pF capacitor serves as a d.c. block for the amplifier output. Therefore, this

output matching network topology is quite convenient. Likewise, the input circuit topology also serves a dual purpose with C_1 acting as a d.c. block and L_2 as part of the gate bias network. The .01 μF capacitor is used to protect the drain of the FET from harmful transients.

Type N and SMA connectors are used for the input and the output, respectively. Silver bearing solder is necessary when soldering to the chip capacitors. This prevents the silver in the capacitor contacts from leeching out into a non-silver solder. A low temperature Indalloy solder is used to solder to the header pins to minimize heat transfer to the chip. Lloyds #6 or Supersafe 30 flux is acceptable for all solder joints but flux residue must be removed with methyl alcohol or any other appropriate solvent. Finger stock connects the edges of the circuit board to the amplifier box in order to maintain a good ground plane and to prevent oscillations (high frequency resonant lengths may occur between ground points if finger stock is not used). The ground planes on both sides of the board are soldered together near the input and output connectors. D.C. characteristics and transconductance of the FET are light sensitive, hence the amplifier box is totally enclosed to provide consistent operating conditions.

3.3 Losses in the Input Circuit

Any circuit losses in the input of an amplifier will cause an increase in the noise temperature. Small losses in the amplifier output are not very important because when the noise contributed by these losses is referred back to the input, it must be divided by the gain of the amplifier. In the 500 MHz amplifier, the capacitors are lossless to a good approximation; however, the inductors possess a finite amount of resistance. This increase in noise temperature due to input circuit losses will be estimated.

First the quality factor of a coil will be found. One of the series coils used in the input circuit as L_1 had 90 nH of inductance, 7.7 turns, a length of .30 inches, and a diameter of .142 inches. The theoretical Q of this coil if it were made out of copper and at a frequency of 500 MHz was found to be 388 using reference [32]. Q is proportional to $\rho^{-1/2}$ where ρ = resistivity. Therefore, correcting for the difference in resistivity between copper and phosphor bronze, one obtains a value of 166. Hence, the coil reactance at 500 MHz is 283 Ω and the coil resistance is 1.7 Ω.

First we calculate the increase in FET noise temperature, T_N, caused by the addition of a series resistance, r, in the input circuit. Values of R_N, G_N, and ρ are assumed known for the FET. The problem is solved by setting the noise output available power of the two networks shown in Figure 17 to be equal.

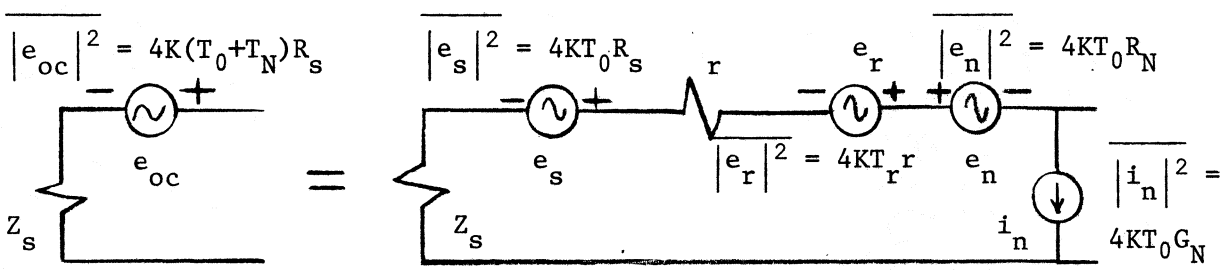


Figure 17. Noise equivalence used to calculate the added noise temperature, ΔT, caused by an input series resistor, r.

By making the above comparison, we are only making use of the definition of noise temperature. The generator, e_r, is the noise produced by the series resistance, whereas the generators e_n and i_n are noise sources produced by the FET. We obtain

$$\frac{\overline{|e_{oc}|^2}}{4K} = R_s (T_0 + T_N) = R_s T_0 + rT_r + \frac{\overline{|i_n (r + Z_s) + e_n|^2}}{4K} \qquad \text{Eq. (15)}$$

since e_n and i_n are correlated but the noise produced by R_s and r is not correlated with any other source.

$$R_s T_N = rT_r + |r+Z_s|^2 T_0 G_N + R_N T_0 + 2T_0 \, Re \left\{ \rho (r+Z_s) \sqrt{R_N G_N} \right\} \qquad \text{Eq. (16)}$$

If r = 0, then

$$R_s T_N' = |Z_s|^2 T_0 G_N + R_N T_0 + 2Re \left\{ \rho Z_s \sqrt{R_N G_N} \right\} \qquad \text{Eq. (17)}$$

$$R_s (T_N - T_N') = R_s \Delta T = rT_r + 2R_s \, rT_0 G_N + r^2 T_0 G_N + 2\sqrt{R_N G_N} \, Re \, (\rho r) \qquad \text{Eq. (18)}$$

$$\Delta T = \frac{rT_r}{R_s} + 2rT_0 G_N + \frac{r^2 \, T_0 \, G_N}{R_s} + \frac{2\sqrt{R_N \, G_N}}{R_s} \, T_0 \, r \, \rho_r \qquad \text{Eq. (19)}$$

T_r = temperature of series resistance, r.

ΔT = added noise temperature due to r.

In chapter IV, we find that typical noise parameters for the HFET-1000 at 500 MHz and room temperature are R_{opt} = 75 Ω, R_N = 90 Ω, $G_N = 8 \times 10^{-4}$ ℧, ρ_r = .10. Using r = 1.7 Ω and $R_s = R_{opt}$, we calculate ΔT = 7.7°K. We also note that 85% of this change in noise temperature comes from the first term of equation 19. If the amplifier is cooled to 77°K, this first term is reduced to 1.75°K since thermal noise cools linearly with temperature. If one now wants to represent the entire circuit with a new set of noise parameters R_N', G_N', ρ', Z_{opt}', etc., which includes the noise of the series resistor, we find:

$$R_N' = r \frac{T_r}{T_0} + R_N + r^2 \, G_N + 2r \, \rho_r \sqrt{R_N G_N} \qquad \text{Eq. (20)}$$

$$G_N' = G_N \qquad \text{Eq. (21)}$$

$$\rho' = \frac{\rho\sqrt{R_N} + r\sqrt{G_N}}{\left[r\frac{T_r}{T_0} + R_N + r^2 G_N + 2r\sqrt{R_N G_N}\,\rho_r\right]^{1/2}} \qquad \text{Eq. (22)}$$

For typical FET parameters, we find that the coil losses cause a negligible change in X_{opt} and a small increase in R_{opt}.

This excess noise (7.7°K) due to the series coil causes a 10% error in FET noise measurements at 500 MHz (T_{min} is typically 60 to 70°K at this frequency). As the real source impedance decreases, this contribution becomes larger. At a temperature of 20°K, and assuming FET parameters at this temperature of $R_{opt} = 50 = R_s$, $G_N = 3 \times 10^{-4}$, and $R_N = 15\ \Omega$, we obtain $\Delta T = 1$°K which is a correction that is smaller than the accuracy of our measurement system.

The problem involving a parallel lossy coil is very similar to the one handled above. The result is that the noise added by such a lossy coil is

$$\Delta T = \frac{gT_g}{G_s} + \frac{R_N T_0}{G_s}(g^2 + 2g G_s) + \frac{2T_0}{G_s}\sqrt{R_N G_N}\,\rho_r\, g \qquad \text{Eq. (23)}$$

where g = conductance of lossy coil $= \frac{1}{Q\omega L}$ Eq. (24)

To get an idea of how much noise a parallel coil could add, suppose a 13 nH coil with a Q of 103 is placed in parallel to the FET. Assume $G_s = \frac{1}{50\ \Omega}$, then we obtain $\frac{g}{G_s} T = 20$°K. If a smaller coil is used, even more noise will be added and the quality of the noise measurements will be drastically reduced.

The problem involving two lossy coils, one shunt and one series, is much more difficult to analyze. The inductance can no longer be included with the source circuit and the noisy resistance included in the FET circuit. The

solution to this problem and the optimization of the amplifier performance including circuit losses is not well understood and would make a good topic for future research.

The circuit loss noise can be decreased by the ratio $\left[\frac{\rho_{br}}{\rho_{Au}}\right]^{1/2} = 1.96$ (the square root of the ratio of resistivities of bronze and gold) if the lossy coils are gold plated. Copper and silver also have high conductivity but their surfaces tarnish too easily resulting in higher equivalent surface resistivities. The increase in noise temperature due to the series coil is now only 3.9°K. (The design of chapter IV contains only such a series coil.) The plating should be at least three skin depths thick. For gold at 500 MHz, the skin depth = δ = 3.5 μm, hence, a gold layer of 10 μm on the coils would be sufficient.

3.4 Source Inductive Feedback

An inherent difficulty in designing low noise, well matched amplifiers is that in general, the optimum source impedance for noise performance differs from the optimum power match source impedance. For example, the real input impedance of the FET is close to 10 Ω whereas the noise optimum real source impedance is much larger. This leads to a bad input match which is very undesirable in radio astronomy applications. Since the feed antenna is usually mismatched to the transmission line, any mismatch at the amplifier front end will set up standing waves and greatly reduce system performance.

The solution lies in increasing the real input impedance of the FET by adding inductive feedback into the source lead. The equivalent circuit is shown below in Figure 18.

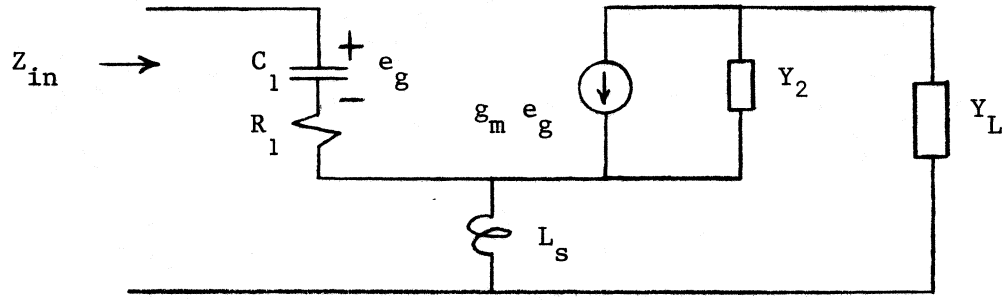


Figure 18. The equivalent circuit used to calculate the increase in the FET real input impedance when source inductive feedback is added.

If one assumes that the impedance of L_s is small compared to Y_2^{-1} and Y_L^{-1}, then an expression for Z_{in} is

$$Z_{in} = R_1 + \frac{1}{j\omega C_1} + j\omega L_s + \frac{L_s g_m}{C_1\left(1 + \frac{Y_2}{Y_L}\right)} + \frac{(\omega L_s)^2 Y_2}{1 + \frac{Y_2}{Y_L}} \qquad \text{Eq. (25)}$$

The fourth and fifth terms of the above expression add to the real part of Z_{in}. We see that both the real and imaginary parts of Z_{in} change with the addition of L_s. Z_{in} is now dependent upon the output circuit values. For normally used values of L_s (1 to 2 nH) the contribution to X_{in} is small, whereas R_{in} is greatly increased. If R_{in} is increased to the value of R_{opt}, then we will obtain noise and power match at the same source impedance.

The addition of a lossless element to an amplifier has been proved to have no effect upon the minimum noise measure of an amplifier by Haus and Adler [33].

The noise measure, M, is given by

$$M = \frac{T_{min}}{T_0\left(1 - \frac{1}{G}\right)} \qquad \text{Eq. (26)}$$

G = amplifier gain

For the case of the FET, L_s will cause a small decrease in gain with a correspondingly small decrease in minimum noise temperature. Vendelin [34] has shown that source inductive feedback changes the noise optimum source impedance to

$$Z_{opt}' = Z_{opt} - j\omega L_s \quad \text{where} \quad |\omega L_s| << |Z_{opt}| \qquad \text{Eq. (27)}$$

Therefore, the feedback has very little effect on the amplifier noise performance and parameters but it greatly improves the input match.

In the 500 MHz amplifier, the feedback inductance is that of the long source bonding wire from chip to header. In order to calculate the inductance, this system may be considered as a wire over a ground plane transmission line. The inductance per unit length is given by [32]

$$L = \frac{Z_0}{C} = \frac{1}{C}\,\frac{138}{\varepsilon_r^{1/2}}\log_{10}\left(\frac{4h}{d}\right) \qquad \frac{\text{inductance}}{\text{unit length}} \qquad \text{Eq. (28)}$$

ε_r = relative dielectric constant

d = wire diameter

h = separation of wire from ground plane

Typical values for the above parameters are $\varepsilon_r = 1$, d = 1 mil, and h = 15 mils.

This provides L = 8.2 nH/cm. If wire length = 100 mils, then L_s = 2.1 nH. This should provide a real input impedance to the FET of approximately 100 Ω.

3.5 Results

Noise, gain, and reflection loss measurements were made on an HFET-1000 chip as the input matching tee network was changed to six different values. Details of measurement techniques are described in Appendix B. In order to obtain the four noise parameters, a linear equation involving four unknowns must be derived from equation 29 given below. This equation and the noise parameters involved are explained in Appendix A.

$$T_n = T_{min} + \frac{G_N}{R_s} T_0 \left[(R_s - R_{opt})^2 + (X_s - X_{opt})^2\right] \qquad \text{Eq. (29)}$$

$$= T_{min} + \frac{G_N T_0}{R_s} \left[R_s^2 + X_s^2 - 2R_s R_{opt} - 2X_s X_{opt} + R_{opt}^2 + X_{opt}^2\right]$$

$$= T_{min} + \frac{G_N T_0}{R_s} |Z_s|^2 - 2G_N T_0 R_{opt} - \frac{2X_s X_{opt} G_N T_0}{R_s} + \frac{G_N |Z_{opt}|^2 T_0}{R_s}$$

$$T_n = Q_1 + \frac{T_0}{R_s} Q_2 + \frac{|Z_s|^2 T_0}{R_s} Q_3 - \frac{2X_s}{R_s} T_0 Q_4 \qquad \text{Eq. (30)}$$

$$Q_1 = T_{min} - 2G_N R_{opt} T_0 \qquad \text{Eq. (31)}$$

$$Q_2 = G_N |Z_{opt}|^2$$

$$Q_3 = G_N$$

$$Q_4 = G_N X_{opt}$$

Now we have a linear system of four equations and four unknowns. For a similar argument, see reference [35]. If four values of T_N are measured for

four values of Z_s, then the system of equations can be solved.

$$[T_N] = [A]\,[Q]\ ; \qquad [Q] = [A]^{-1}\,[T_N] \qquad \text{Eq. (32)}$$

A BASIC program was written for the HP-9830 to do the matrix inversion and perform the computations necessary to find [Q] and the noise parameters. This program is listed in Appendix C.

Measurements of Z_s were performed by removing the header from the circuit, and making open circuit and short circuit input impedance measurements with a network analyzer. Using this time consuming and arduous method, values for all circuit elements in the input were found. Table 1 is a list of the circuit elements used in the six different input matching networks as denoted in Figure 10.

TABLE 1

Circuit elements for the six input matching networks.

	Net. 1	2	3	4	5	6
C_1 (pF)	12	43	70	70	9.0	6.2
L_1 (nH)	55	90	90	55	90	106
L_2 (nH)	13	13	7.4	7.4	26	45

Table 2 is a list of source impedances presented to the FET as a function of frequency. The source impedance calculations were done using the circuit simulation program BAMP. Also given are the measured noise temperatures and

TABLE 2

NOISE MEASUREMENTS VS. FREQUENCY AND SOURCE IMPEDANCE FOR THE SIX INPUT MATCHING NETWORKS.

Network	Frequency	Z_s	T_N (measured) T_{amb} = 298°K	T_N (corrected) T_{amb} = 298°K	T_N (measured) T_{amb} = 77°K	T_N (corrected) T_{amb} = 77°K
	450	66 + j 276	188		85.1	
	500	92 + j 341	126	103	49.4	45.4
	550	139 + j 428	72		28.0	
1	650	225 + j 547	71		54.1	
	700	404 + j 710	94		57.5	
	750	826 + j 873	133		123.0	
	400	58 + j 446	181		71.0	
	450	106 + j 617	111		47.7	
2	500	227 + j 920	138	118	107.0	104.0
	550	691 + j1570			206.0	
	600	large	305		293.0	
	400	20 + j 425	605		161.0	
	450	39 + j 593	338		111.0	
3	500	88 + j 900	339	279	174.0	165.0
	550	293 + j1650	604		484.0	
	600	large	842		648.0	
	450	19 + j 265	822		423.0	
	500	30 + j 334	393	325	171.0	160.0
4	550	48 + j 429	254		61.9	
	600	85 + j 575	194		57.8	
	650	172 + j 822	232		161.0	
	350	172 + j 365	90.6		62.6	
	400	240 + j 412	63.4		42.7	
5	450	326 + j 488	67.3		31.2	
	500	482 + j 605	80.8	70	40.0	38.0
	400	329 + j 287	71.4			
6	450	386 + j 391	68.3			
	500	564 + j 544	86.7	79		

the measured noise temperature minus the calculated noise added due to a series lossy coil and the parallel lossy coil separately using equations 19 and 23, respectively. (These corrections are only calculated for the 500 MHz data.)

Similar measurements were made at 77°K and the data is also reported in Table 2. These low temperature experiments were made by immersing the amplifier in a liquid nitrogen bath. The liquid surrounds the FET, hence one does not have to worry about thermal resistances. A large decrease in measured noise temperature was observed. This stimulated the author to probe deeper into the FET noise dependence on ambient temperature. This is discussed in the following chapter.

The FET noise parameters at both temperatures are calculated for f = 500 MHz using any four sets of Z_s and T_n and then averaging values. Table 3 gives the results.

TABLE 3

Measured noise parameters at 500 MHz for the HFET-1000 ($T_{ambient}$ = 298°K and 77°K).

Parameter	T = 298°K	T = 77°K
T_{min} (°K)	55	21
R_{opt} (Ω)	225	205
X_{opt} (Ω)	510	465
G_N (℧)	4.7×10^{-4}	3.2×10^{-4}
R_N (Ω)	150	83
ρ_r	.127	-.18
ρ_I	.914	.915

The accuracy of the above noise parameter calculations is questionable for several reasons. (1) Measurements given in the next chapter for several HFET-1000 chips indicate $Z_{opt} = 75 + j\ 300$. (2) Measurements made at 1.4 GHz [22] support the fact that $R_{opt} = 70\ \Omega$. (3) There is great difficulty in obtaining an accurate circuit description using the network analyzer when there are six elements in the input circuit. (4) The theory of noise contributed by input circuit loss is not exactly understood. Despite the inaccuracy in obtaining noise parameters, the circuit topology described in this chapter is convenient for the construction of a low noise, compact amplifier in this frequency range. An accurate estimate for T_{min} was obtained using this device.

R.F. gain, noise temperature, input return loss, and output return loss for the six different input tee networks are plotted in Figures 19, 20, and 21. The gain curve for each matching network reaches a maximum at a lower frequency than the noise temperature minimum. Therefore, $X_{opt,noise} > X_{opt,power}$ although their values are fairly close. The bandwidth of the gain curve depends upon which matching network is considered. The 3 dB bandwidth decreases as the maximum gain increases. Network 2 provided an amplifier with 22 dB maximum gain but only 55 MHz bandwidth whereas network 1 provides 21 dB maximum gain and 130 MHz 3 dB bandwidth. From the data it seems that the bandwidth is determined by whether or not the input and output circuits are matched at the same frequency. In designing an amplifier for actual use, one would take care to match input and output properly. Then the gain bandwidth would depend mainly upon the high Q input circuit.

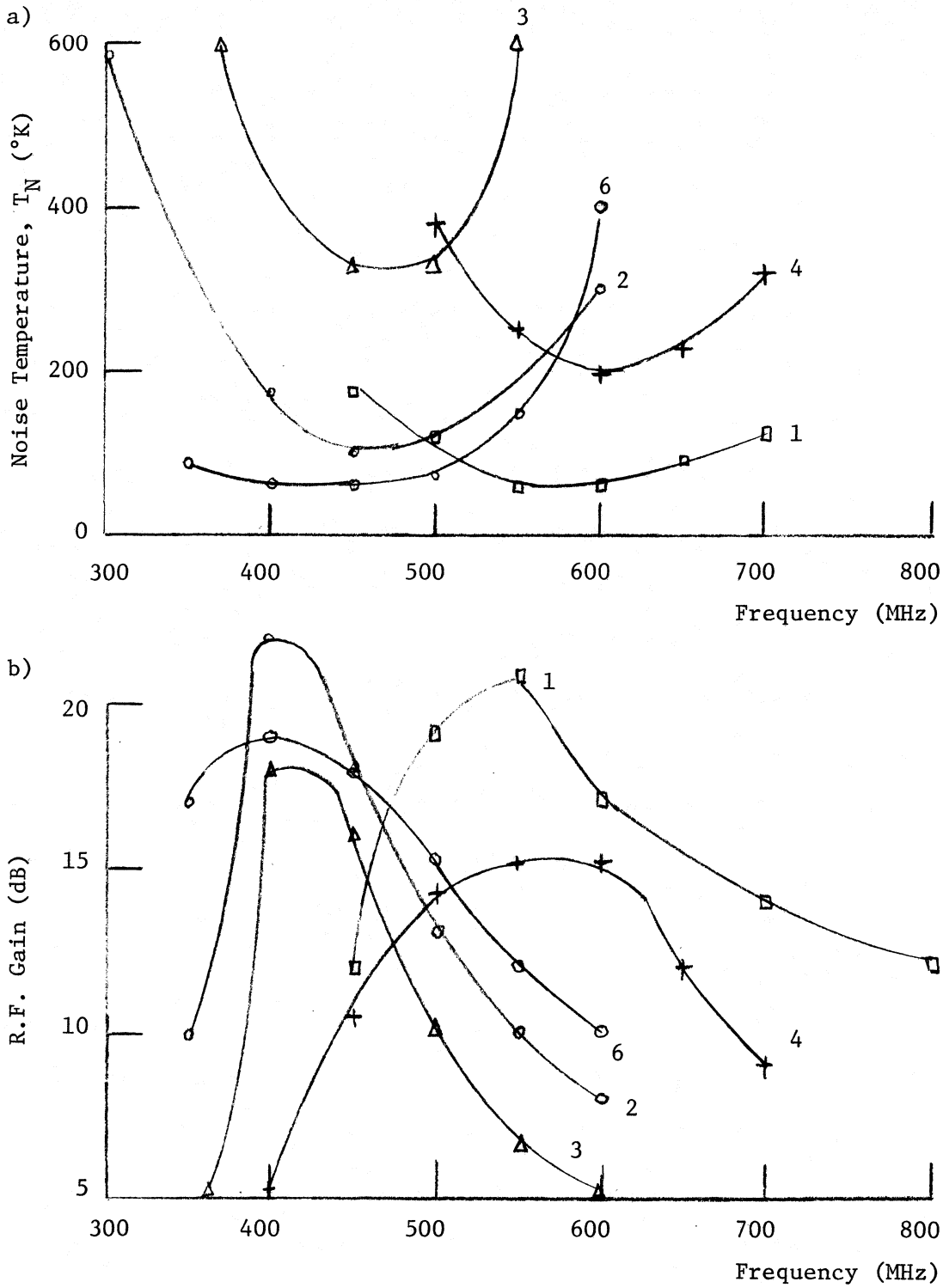


Figure 19. (a) and (b) are plots of noise temperature and r.f. gain versus frequency for the 500 MHz amplifier at room temperature. The numbers 1 through 6 indicate which input matching network was used to obtain that curve.

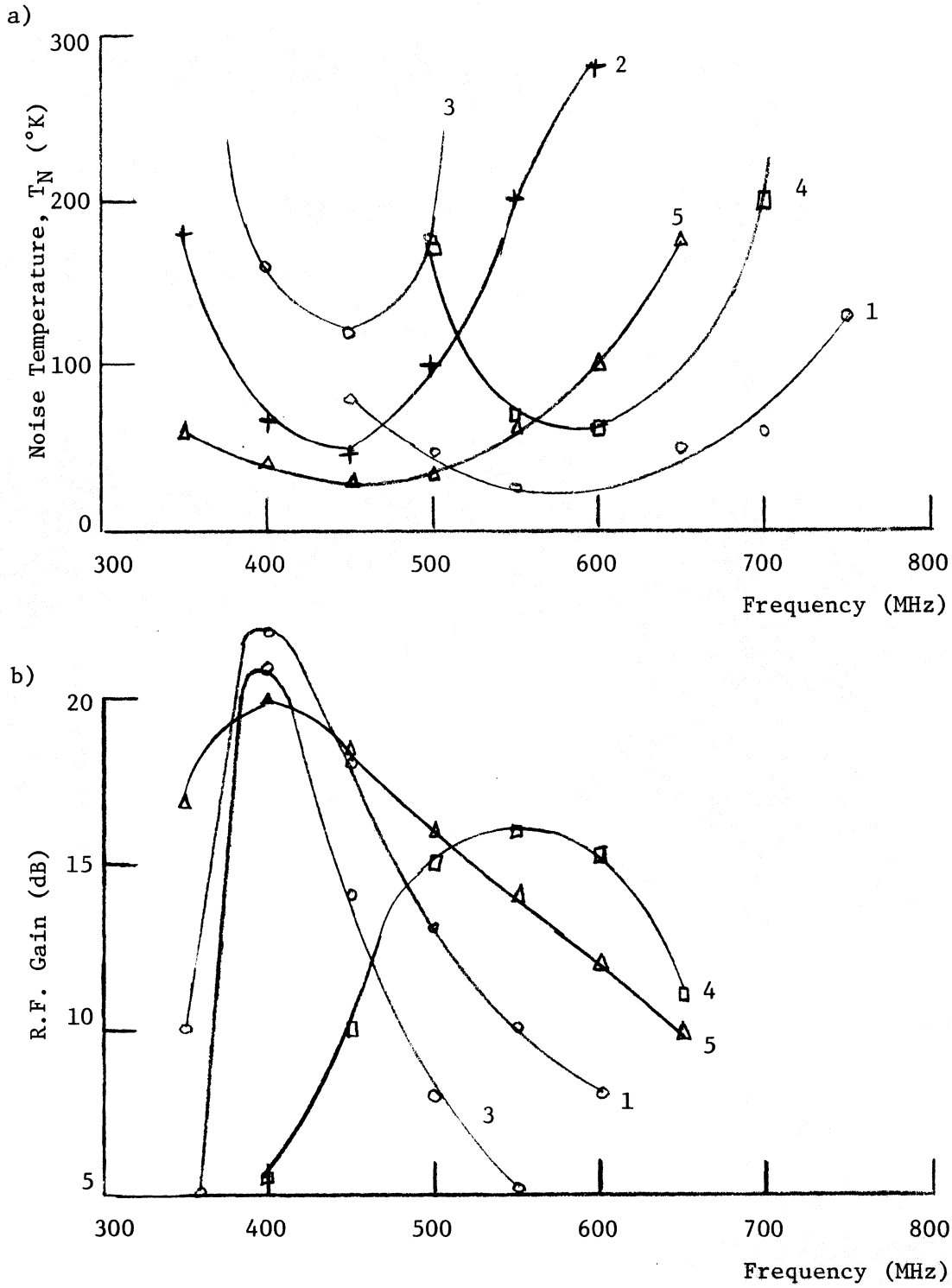


Figure 20. (a) and (b) are plots of noise temperature and r.f. gain vs. frequency when the 500 MHz amplifier is cooled to 77°K. Numbers indicate input matching section.

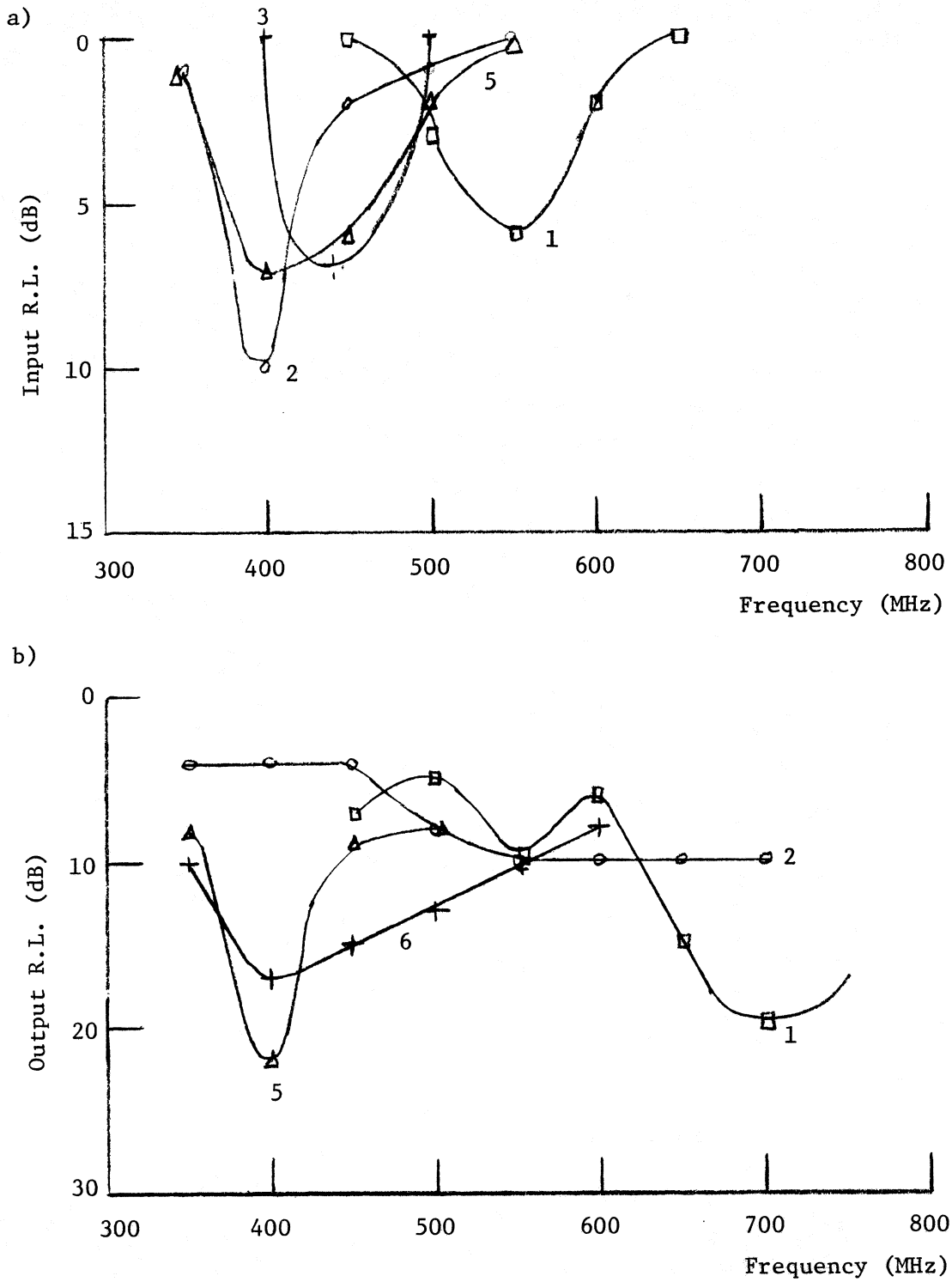


Figure 21. (a) and (b) are the input and output return loss of the 500 MHz amplifier vs. frequency. Measurements were made at room temperature. Numbers indicate which input matching network was used.

CHAPTER IV

A 600 MHz AMPLIFIER

4.1 General Description

The determination of the FET noise parameters by measuring the noise temperature at four values of source impedance was found to be prone to large experimental errors. Hence, an alternate method was selected and a 600 MHz amplifier was built to implement this method. The center band frequency was changed because a 600 MHz amplifier was more useful for radio astronomy applications.

If one looks at the noise temperature dependence upon source impedance given in equation 29

$$T_N = T_{min} + \frac{G_N T_0}{R_s} [(R_s - R_{opt})^2 + (X_s - X_{opt})^2]$$

it is obvious that if R_s is held constant and X_s is swept through a range of impedances, the T_N vs. X_s curve will be a parabola. The minimum of the parabola is located at $X_s = X_{opt}$. Likewise, if X_s is held constant but R_s is swept through a range of impedances, T_N will trace out an unsymmetrical curve due to the $\frac{1}{R_s}$ term multiplying the bracketed quantity. These curves are shown below in Figure 22.

The noise parameters of a two port can easily be found if an amplifier is built in which R_s and X_s can be varied independently of each other. R_{opt} is found by holding X_s constant and measuring noise versus R_s. Then with $R_s = R_{opt}$, noise versus X_s is measured. The minimum of the parabola will be at X_{opt}, and the noise temperature will equal T_{min} at this point. The fourth noise parameter, G_N, can be found from any noise measurement far from the optimum source impedance.

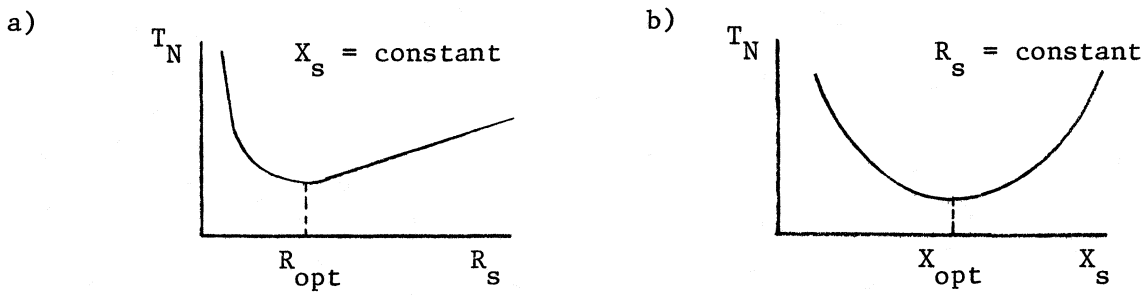


Figure 22. (a) Theoretical noise temperature vs. R_s as X_s is held constant and (b) noise temperature vs. X_s as R_s is held constant.

This concept of noise parameter measurement is achieved in the 600 MHz amplifier by using a quarter-wave adjustable impedance transmission line (to supply the variable real source impedance) followed by a series coil. A different imaginary source impedance is obtained by substituting in a different coil. The two series components are the only elements in the input r.f. circuit. All shunt inductances and capacitances are minimized to reduce any dependence of R_s on X_s and vice versa. The characteristic impedance of the quarter wave line is changed by moving the ground plane away or towards a parallel copper strip. The real impedance seen at the FET end of the quarter wave line is

$$R_s = \frac{Z_0^2}{Z_L} \qquad \text{Eq. (33)}$$

Z_0 = characteristic impedance of transmission line.

Z_L = input load impedance = 50 Ω.

This method of noise analysis greatly reduces the time necessary to characterize a single FET. More FET's and a wider range of temperatures can be examined using this technique.

4.2 Specific Design

4.2.1 Quarter Wave Transformer

The block diagram of the amplifier must be the same as that shown in Figure 9 with an input mathing network for low noise, an output matching network for power match, and source inductive feedback for a good input match.

The amplifier is housed in a single block of aluminum containing two milled out cavities. The large cavity contains the adjustable quarter wave line. The small cavity houses the rest of the amplifier. The amplifier section is accessible from top and bottom to facilitate the substitution of FET's.

The transformer is five inches long, or a quarter wavelength at 600 MHz. The ground plane is formed by a moveable aluminum slide which is guided by two brass rods. The brass rods slide through reamed holes in the block and the slide position is controlled by a non-rotating micrometer. Electrical contact between the slide and the block is made by finger stock which is screwed into the recessed ends of the slide. Contact need only be made at the two ends of the ground plane since this microstrip-like geometry is a quasi-TEM structure. The magnetic field is in the direction perpendicular to the plane of the paper (as is viewed in Figure 23); hence, current will flow only along the length of the ground plane.

The signal is propagated by a two wire transmission line consisting of the ground plane and a rectangular copper strip which is supported by a piece of RT Duroid [36] circuit board parallel to the ground plane. See Figure 23.

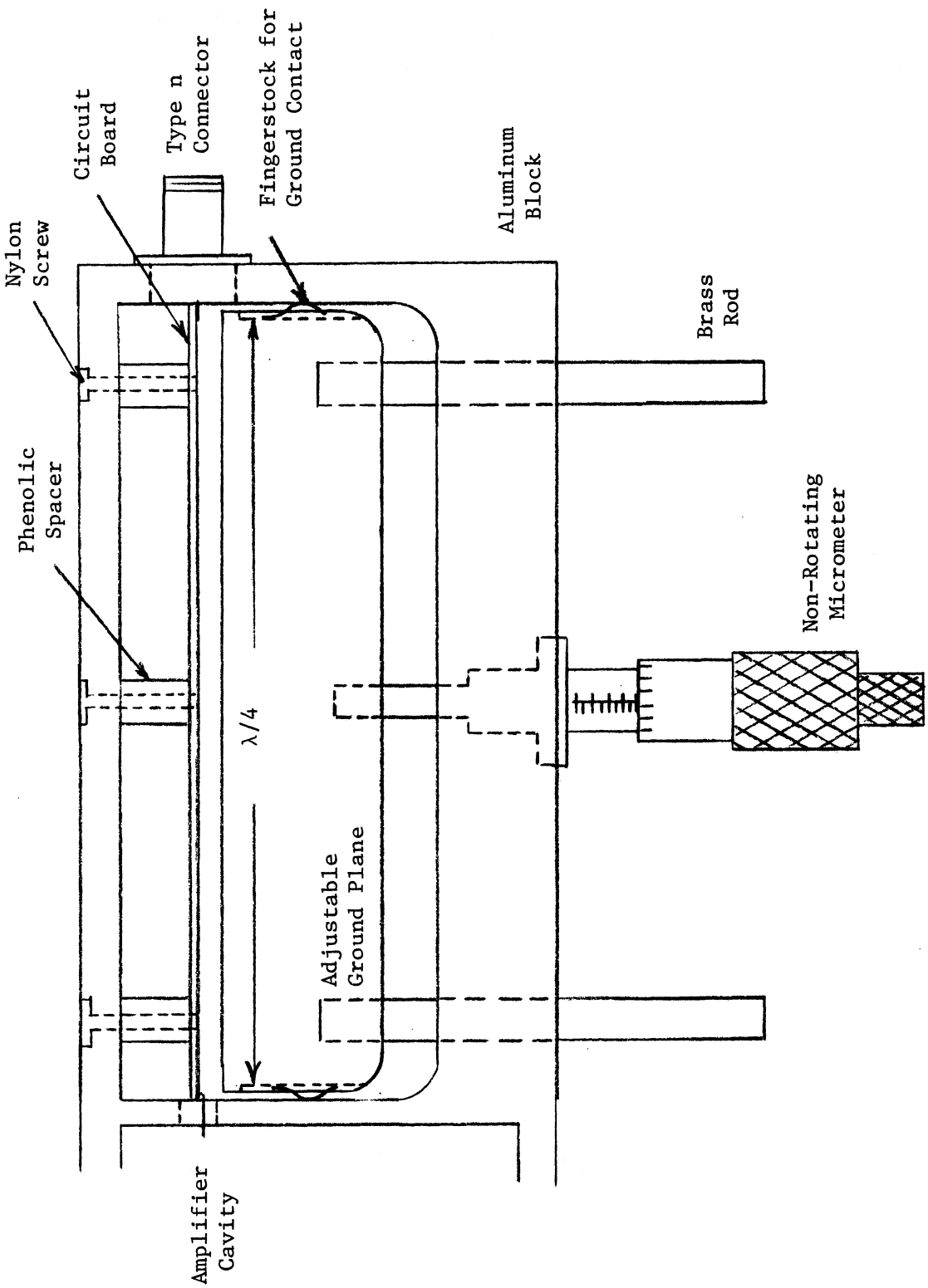


Figure 23. The adjustable impedance quarter-wave transformer cavity is illustrated. The amplifier cavity is not shown.

The holes in the block and in the slide into which the brass rods and the micrometer fit were bored and reamed at the same time to insure parallel movement without binding. Aluminum was chosen as the block material for the following reasons: (1) it is easily machined, (2) readily available and inexpensive, (3) low resistivity, and (4) it does not easily corrode. The drawback is that a thin oxide layer prevents one from soldering to aluminum. Therefore, all electrical contacts to the block were made with screws or mechanical pressure. Quarter inch brass rods were chosen because aluminum and brass make a good sliding fit and their coefficients of thermal expansion are very close (to be further discussed in section 4.3).

The circuit board is kept parallel to the ground plane by (1) milling a 1/16" groove 60 mils deep into the block and pressing the board into the groove. (2) Also, three phenolic spacers are milled to a length of 440 mils and placed between the block and the back of the circuit board. A nylon screw passes through each spacer, threads into the circuit board, and keeps the board exactly 440 mils from the block. Using the above precautions, the circuit board and ground plane were found to be parallel to within 3 mils over their entire 5" length.

A 200 mil wide copper strip is etched on both sides of the dielectric board. The strip on the back side is present because when dielectrics are cooled, they contract a great deal more than metals. An unsymmetrical geometry could cause a warp in the transmission line. Having metal strips on both sides of the circuit board provides symmetrical support. The back strip is open circuited on both sides; however, its presence does alter the electrical characteristics of the transmission line. The problem of the symmetrical three wire transmission line with the third line being open circuited at both ends

has been analyzed previously [37]. It was found that the electrical length of the line remains the same, only the characteristic impedance of the line is changed to the average of the even and the odd TEM mode characteristic impedances. In our case, the geometry is unsymmetrical since the moveable ground plane may be closer to the copper strips than the aluminum wall on the opposite side. However, it is a safe approximation to assume the electrical length will remain constant and the actaul characteristic impedance of the line is determined from experiment.

When the ground plane is very close to the center conductor, the transmission line characteristics can be calculated using microstrip formulas since most of the electric field is contained in the region between the center strip and the slide. When the slide is far away from the center strip, the structure more closely resembles a stripline transmission line or a rectangular strip surrounded by four walls. The circuit board has a dielectric constant of 2.2 and is only 62 mils thick; hence, for approximate calculations we can assume an air dielectric line ($\varepsilon_r = 1.0$).

Table 4 provides calculated values of characteristic impedance and real source impedance as a function of distance, h, between ground plane and center conductor. See Figure 24 for an illustration of the transmission line geometry. Values of h can be between 0 and 500 mils. For $h < 150$ mils, the microstrip formulation [38] is used, whereas if $h > 150$ mils, stripline equations and curves [39] determine the calculated values. Figure 25 compares the theoretical approximations of the characteristic impedance of the transmission line with experimental values measured using a network analyzer.

The last column in Table 4 contains theoretical values for the conductor loss of the transmission line. These values were calculated using the surface

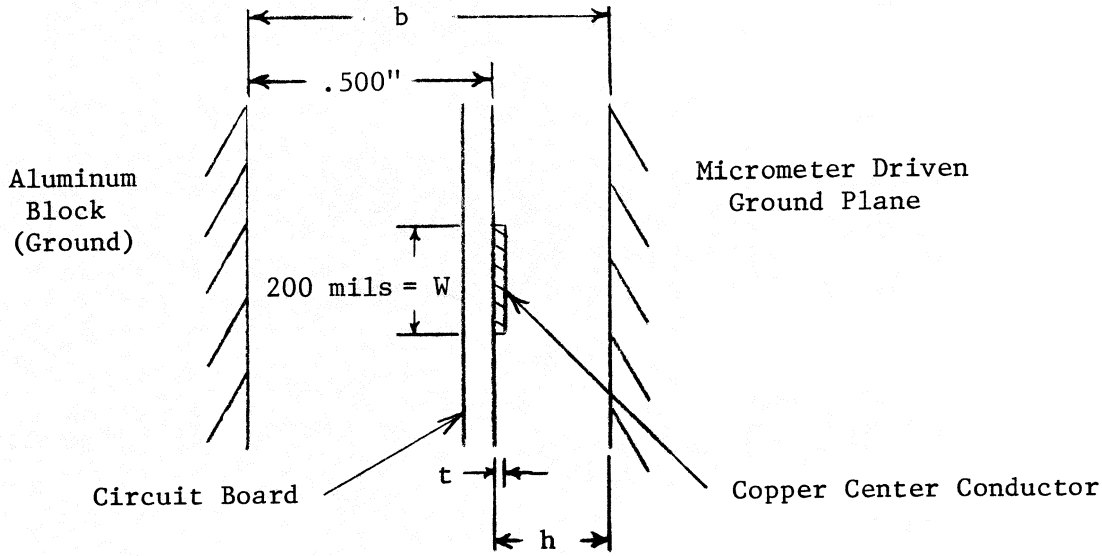


Figure 24. Details of the transmission line geometry and definitions for the parameters used in Table 4.

TABLE 4

Transmission line characteristic impedance vs. distance, h, using the (a) microstrip approximation and (b) the stripline formulation.

a)

h (mils)	$\frac{W}{h}$	Z_g	$Re(Z_s)=\frac{Z_g^2}{50}$	$\frac{h}{t}$	α_c (dB)
20	10	30	18	14.3	.035
40	5	50	50	28.6	.0183
80	2.5	70.7	100	57.1	.0107
95	2.1	86.6	150	67.8	.00935
118	1.7	100	200	84.3	.00835

b)

h (mils)	$\frac{W}{b}$	$\frac{t}{b}$	Z_g	$Re(Z_s)=\frac{Z_g^2}{50}$	α_c (dB)
200	.286	.002	132	348	.00592
300	.250	.00175	140	392	.00557
400	.222	.00155	146	426	.00516
500	.200	.00140	152	462	.00496

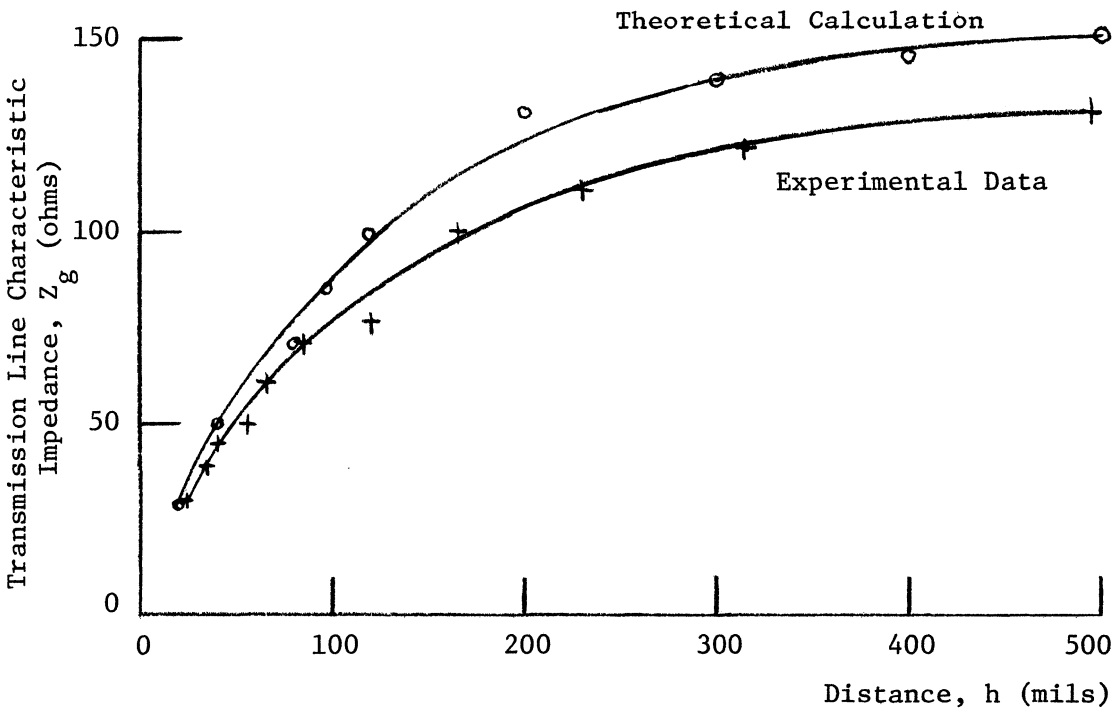


Figure 25. The calculated and measured dependence of transmission line characteristic impedance upon the separation, h, between center conductor and the movable ground plane.

resistivity of copper since it is assumed that most of the losses occur in the narrow center conductor rather than in the large aluminum ground plane. The dielectric loss, α_D, is zero for an air microstrip line. For the stripline approximation, virtually all of the volume is air; hence, $\alpha_D \simeq 0$. However, if the entire volume was filled with teflon glass dielectric, the dielectric loss would be

$$\alpha_D = 27.3 \sqrt{\varepsilon_r} \frac{\tan \delta}{4} = 9.11 \times 10^{-3} \text{ dB} \qquad \text{Eq. (34)}$$

Since no more than $\frac{60}{700} = 8.6\%$ of the total volume contains dielectric, a rough estimate of α_D is 7.83×10^{-4} dB or approximately 13% of α_c. The calculation of transmission line loss is important in determining the contribution of noise from this source to the measured noise temperature.

The center conductor of the transmission line is tapered at the amplifier end. This will reduce the parasitic capacity between the end of the transmission line and the shield which separates the two cavities. The purpose of the shield is to prevent coupling of the electromagnetic fields along the transmission line with circuit elements in the amplifier, and vice versa. A wire connecting the tapered end of the transmission line with the rest of the amplifier passes through a hole in the shield. This hole must be drilled through the far wall and then through the shield wall. The hole in the far wall houses a feedthrough capacitor which brings in the gate bias. The wire passing through the hole in the shield introduces a small amount of series inductance and shunt capacitance but this addition appears to be negligible.

Theoretical calculations of the impedance presented by the quarter-wave transformer versus frequency suggest that the transformer will be capable of

very broad band matching. For a characteristic impedance of 70.7 Ω, Z_s = 100 Ω at 600 MHz, R_s > 95 Ω for 550 MHz < f < 650 MHz, Z_s = 81 + j24 at 400 MHz and Z_s = 78 - j25 at 800 MHz.

4.2.2 Amplifier Cavity

The amplifier cavity is designed to introduce as few shunt parasitics as possible into the input circuit. The use of a header to mount the FET was abandoned because of the large shunt capacity. Instead, a rivet made of OFHC copper is used and is shown in Figure 26. The chip is soldered to a protruding rib in the center of the rivet. See Appendix D for chip handling procedures and soldering instructions. Small rectangular dielectric bars are epoxied parallel to this rib. Copper pads on the dielectric bars provide a conducting surface to which external circuit elements may be soldered. One mil gold or aluminum wires are ultrasonically bonded from the copper pads to the chip bonding pads. The rivet plus bonded chip can be easily removed from the amplifier. Three screws attach the rivet to the bottom of the circuit board. The rib and dielectric pads fit up through a milled hole in the amplifier circuit board so that the copper pads and the FET are flush with the top surface of the amplifier board. The area beneath the gate copper pad is milled away, greatly reducing the shunt capacity of this pad.

The circuit diagram of the amplifier along with a schematic showing the position of all circuit elements is given in Figures 27 and 28, respectively. Much similarity exists between the 500 MHz and 600 MHz amplifiers. Following the quarter wave transformer, there is an 82 pF series d.c. blocking capacitor and the series coil which provides X_s. Again, all the metal beneath the 100 x 100 mil pads to which the blocking capacitor is soldered has been milled away

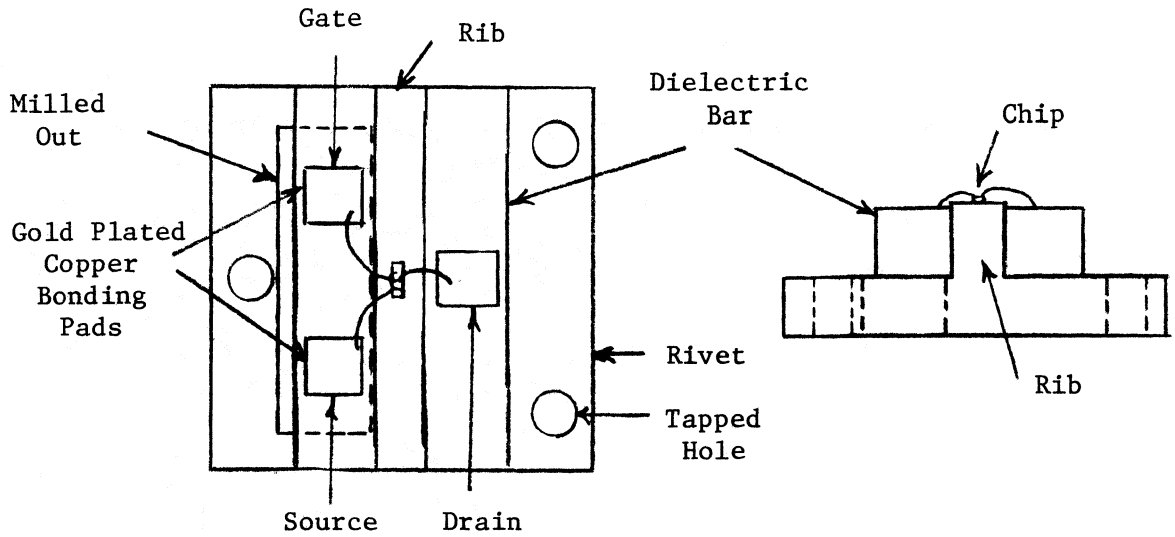


Figure 26. Two views of the chip soldered onto the copper rivet. Also shown are 1-mil wires bonded from the FET to the pads on the dielectric bars.

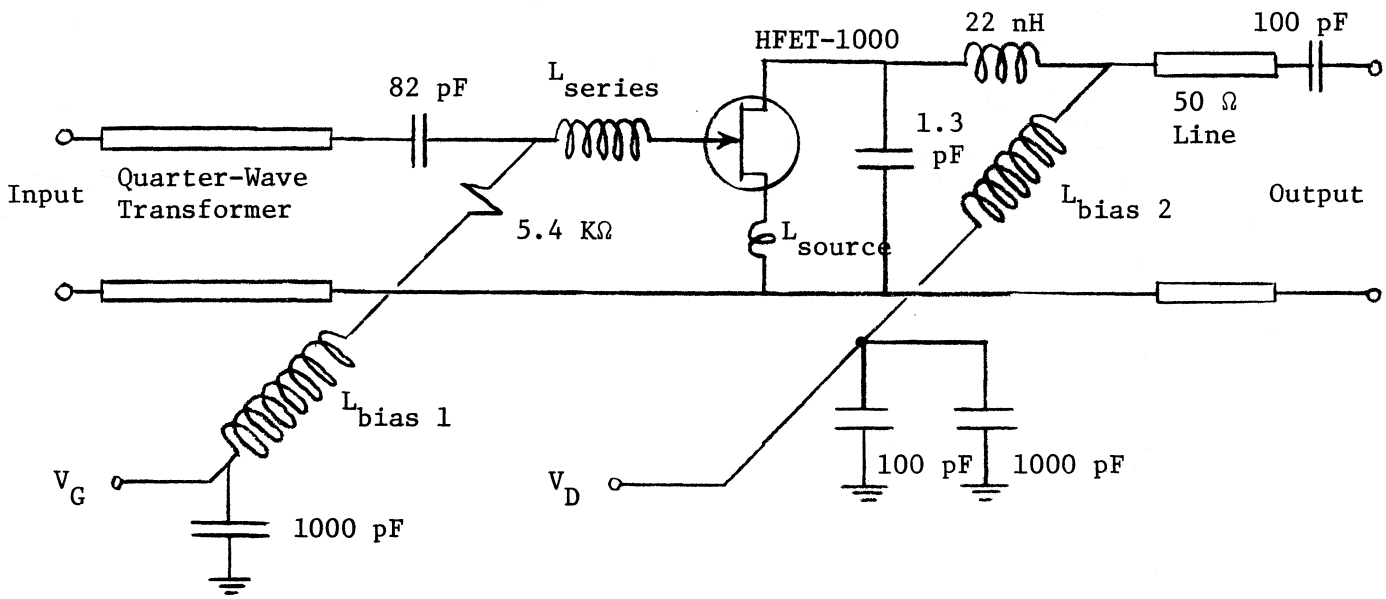


Figure 27. Circuit schematic of the 600 MHz amplifier.

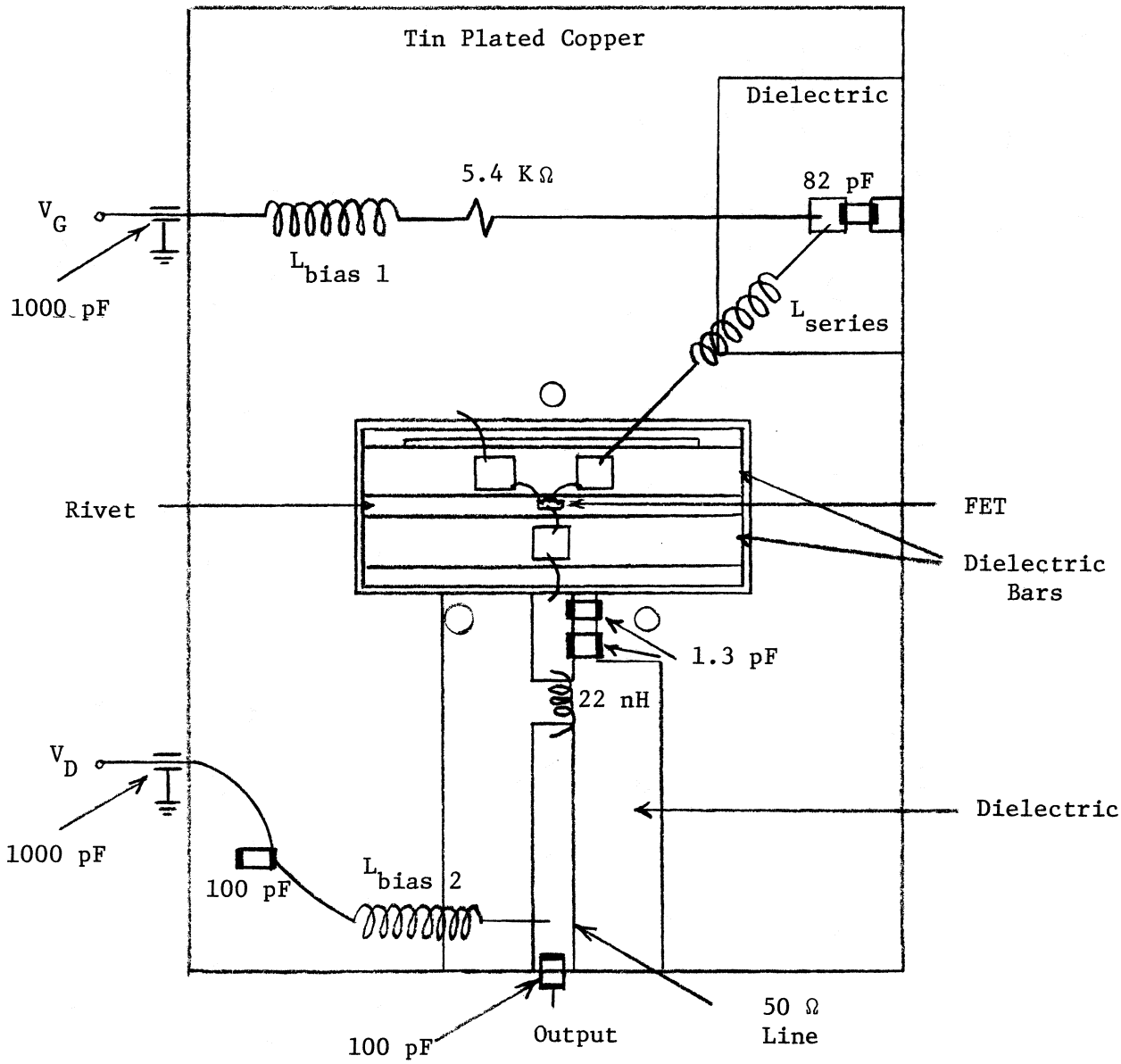


Figure 28. Physical layout of the amplifier cavity for the 600 MHz amplifier.

to reduce capacitance. The gate bias network contains a 1000 pF shunt feed-through capacitor for a good a.c. ground, a series 14 turn, .14 inch diameter coil which is nearly parallel resonant at this frequency (it passes only d.c.), and a 5.4 KΩ resistor to limit forward gate current and protect the gate from transients. Source inductive feedback is provided mainly by the 1 mil wire from chip to the copper pad on the dielectric bar. Added inductance is contributed by the much larger wire connecting the copper pad to the ground plane. Small diameter wires contribute more inductance as seen in equation 28. Output power match is provided by a simple shunt 1.3 pF capacity followed by a series 22 nH coil. The reason for choosing this configuration is high frequency stability as discussed in section 4.4. A section of 50 Ω transmission line is followed by a 100 pF d.c. blocking capacitor which is soldered to an SMA connector. Drain bias is supplied via shunt 1000 pF and 100 pF capacitors which provide a.c. ground and protect the FET from transients. They are followed by a large (nearly resonant) coil which passes only d.c.

Good ground contact is provided by 13 screws which connect the top and bottom of the RT Duroid circuit board to the aluminum block. Many ground points are necessary in order to prevent high frequency resonant lengths which may cause oscillation. Using several screws was deemed a simpler solution than using finger stock in this very small cavity. Figure 29 is a photograph of the amplifier cavity and Figure 30 is a picture of the entire 600 MHz amplifier.

4.2.3 Amplifier Performance

The input unloaded Q of the FET is calculated to be approximately 44. When loaded by the quarter wave transformer set at $R_{opt} \simeq 75\ \Omega$ and when the

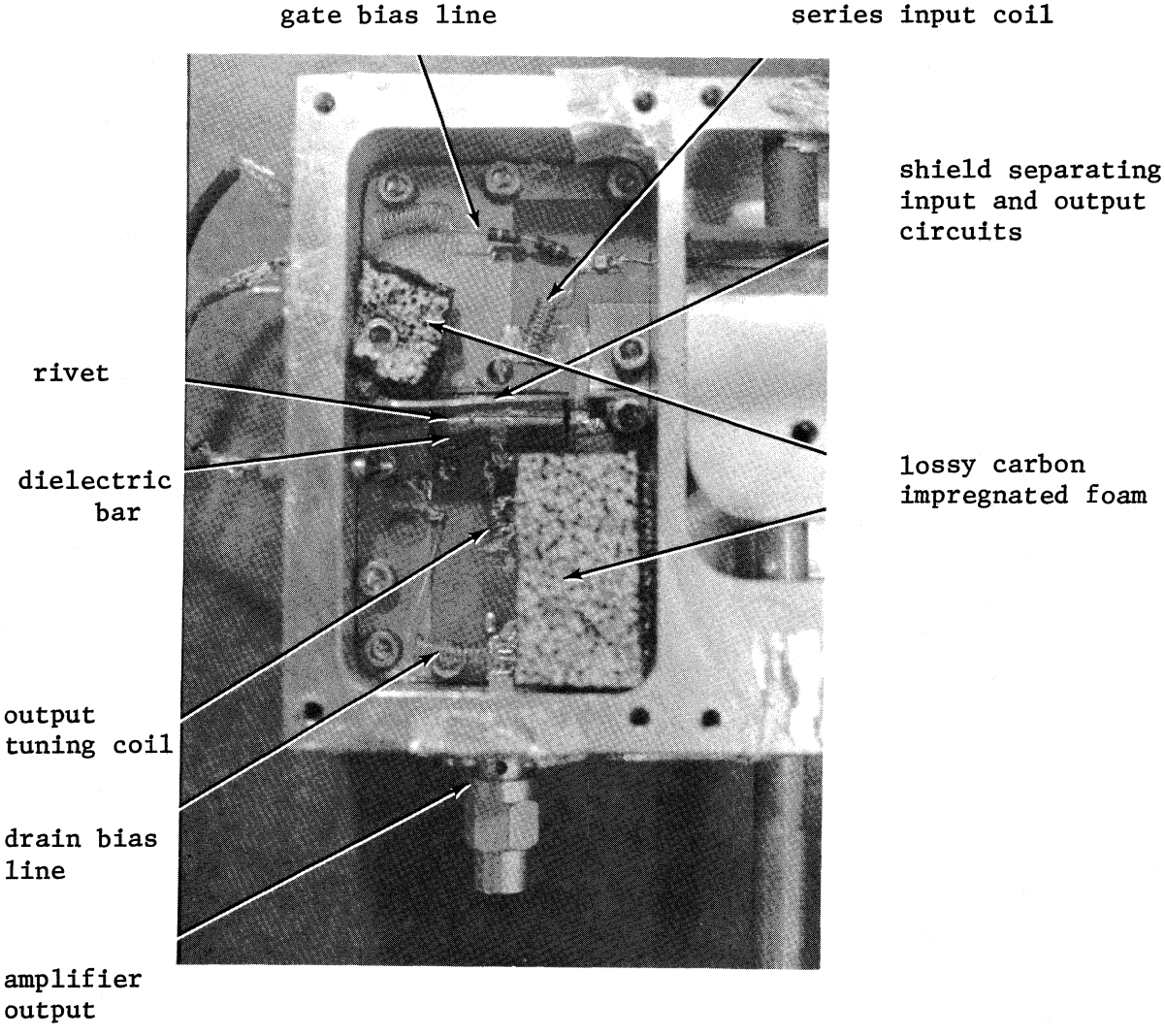


Figure 29. Photograph of the amplifier cavity of the 600 MHz amplifier.

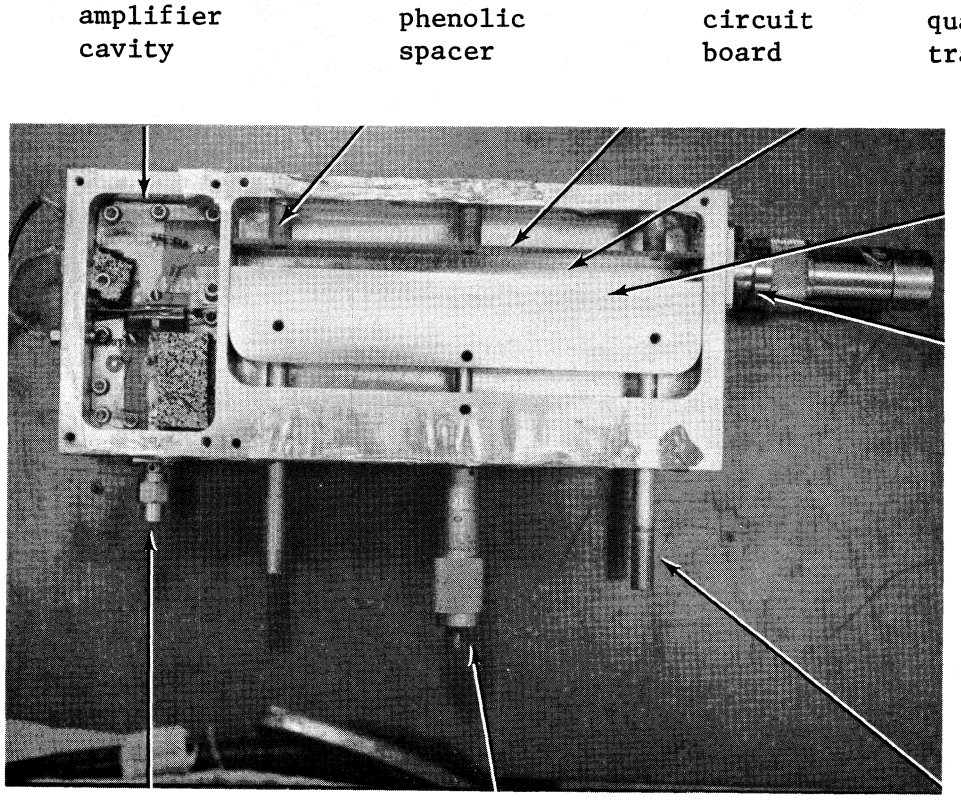


Figure 30. Photograph of the 600 MHz amplifier.

series coil resonates C_{gs}, a loaded Q of 5.2 is obtained. Finally, if source inductive feedback is optimized such that Re ($Z_{FET\ INPUT}$) = R_{opt} = 75 Ω, then the loaded Q becomes 2.9. Approximate values for the circuit elements in the output matching network were obtained by theoretical calculations. Final circuit element values were chosen by making small deviations about these theoretical values and measuring the output return loss. Using this method, optimization was achieved. The output of the HFET-1000 including rivet shunt capacity has an unloaded Q of .45. The addition of the shunt 1.3 pF capacitor increases the quality factor and a loaded value of 1.9 is calculated. One sees that the power-gain bandwidth of the system is limited by the input circuit; however, fairly wide band operation is obtainable.

$$\{BW\}_{max} = \frac{f_{center}}{Q} = \frac{600\ MHz}{2.9} = 207\ MHz \qquad \text{Eq. (35)}$$

Using the circuit simulation program BAMP, it has been found that an inductance close to 1 nH is necessary to provide a real input impedance to the FET of 70 Ω over a wide frequency range.

4.3 Cryogenic Operation

Not only must the amplifier work at room temperature, but also at cryogenic temperatures. To obtain temperature flexibility, the amplifier is cooled in a cryogenic refrigerator rather than in a liquid nitrogen bath. Since the dewar is evacuated while cold, all heat must flow away from the chip via the circuit board and case. We have already calculated the thermal resistance of the FET in section 2.8 and found θ_{FET} = 4.14 °K/W. During actual operation, a diode temperature sensor will be attached to the copper rivet. Therefore, if

the thermal resistance between FET and rivet is calculated, the temperature of the FET will be known.

Conductive epoxy can no longer be used to bond the FET because its thermal resistance is too high. The FET must be soldered and the solder with lowest thermal resistance is pure indium (Indalloy #4 [40]). At 20°K, the thermal resistivity of this solder is $K = 1.8 \frac{W}{cm\ °K}$ [26].

$$\theta_{solder} = \frac{t_{solder}}{K\ A} \qquad \text{Eq. (36)}$$

Equation 36 determines the thermal resistivity of a rectangular block.

t_{solder} = average solder thicknesss = 1 mil.

A = solder area = chip area.

The result is $\theta_{solder} = .74$ °K/W. This value is an order of magnitude better than most solders will provide.

Finally, we calculate the thermal resistivity of the copper rib on the rivet. Oxygen free hard copper was provided for the rivet construction because other less pure types of copper have a higher thermal resistance. Using the value of $K_{copper} = 10 \frac{W}{cm\ °K}$ [26] at 20°K and the averaged area of the FET and the rib in equation 36, we find $\theta_{rivet} = 1.25$ °K/W. Another approximation to the rib thermal resistance can be made by assuming the heat source to be hemispherical with radius, a, such that πa^2 = chip area. The rib is assumed to be infinite in all directions and most of the thermal resistance occurs very near to the heat source. The equation for the thermal resistance is

$$\theta_{riv} = \frac{1}{2\pi a\ K} \qquad \text{Eq. (37)}$$

and we obtain $\theta_{riv} = .66 \frac{°K}{W}$. We will use the value of $1.25 \frac{°K}{W}$ as a worst case thermal resistance for the rivet. The total thermal resistance is then $\theta_{tot} = \theta_{rivet} + \theta_{solder} + \theta_{chip} = 6.13°K/W$. Normal low noise bias conditions are $V_d = 2V$, $I_d = 20$ mA; power = $V_D I_D = 40$ mW. $\Delta T = \theta P = .25°K$. Therefore, we can conclude that the temperature sensor on the rivet reads the temperature of the channel to within one quarter of a degree Kelvin.

The refrigerator itself is a model 350 Cryodyne made by Cryogenic Technology Incorporated. It is a continuous-duty, closed cycle system that can provide up to 3 watts of refrigeration at 20°K. The refrigerator has two stages. The upper stage is cooled to a temperature of 77°K while the lower stage can reach 15°K or less. This is the stage to which the 600 MHz amplifier is bracketed.

To obtain temperature control, four high power resistors are clamped to the 15°K stage. A Lake Shore Cryogenics temperature meter with a servo-loop controller can apply up to 50 watts of heating power into the resistors. Power is supplied to the heaters until the desired temperature is reached. Measurements can be made at any temperature between 298°K and 20°K.

The dewar can has 12" of room below the 20°K stage and is 13.5" in diameter, thus providing a large amount of room for experimetal devices. A good vacuum is necessary within the dewar to prevent heat convection by gas molecules. A crude vacuum is obtained using a roughing pump (pressure = 10 μm Hg). At this point a Varian vac-ion pump is activated to improve the vacuum. The refrigerator itself acts as a pump because as the temperature decreases, gaseous impurities freeze out. This causes a problem when warming the amplifier, because as the temperature increases, impurities boil off and it becomes difficult to maintain a good vacuum. At 15°K, a vacuum of 10^{-7} torr was the best obtained.

The quarter-wave transformer is controlled by a speedometer cable which is connected to the micrometer drive. It is impossible to vary the imaginary source impedance by changing coils while the amplifier is within the dewar. However, a value of X_{opt} can be found by comparing the noise temperature versus frequency data at low temperatures to that at room temperature. $X_s = j\omega L_{series}$, therefore, if the minimum noise temperature occurs at a higher frequency when cold, this would be evidence that X_{opt} has increased to

$$\left(X_{opt,\ room\ temp} \right) \left(\frac{\omega_{min,\ cold}}{\omega_{min,\ room\ temp.}} \right) .$$

Design of a variable quarter-wave transformer which operates at cryogenic temperatures requires some consideration. The block and the slide are both made from aluminum; therefore, there will be no binding due to material contraction. There is a material difference between the brass rods and the aluminum housing. However, their coefficients of thermal expansion are very close at room temperature and are given below.

$C_1 = 1.244 \times 10^{-5}$ (unit length $\cdot$ °F)$^{-1}$ for aluminum

$C_2 = 1 \times 10^{-5}$ (unit length $\cdot$ °F)$^{-1}$ for brass [41]

at 298°K.

$\Delta C = 4.39 \times 10^{-6}$ (unit length $\cdot$ °K)$^{-1}$

$\Delta T = (300-20)$°K = 280°K

$\Delta \ell = 1.23 \times 10^{-3}$ (unit length)$^{-1}$

Diameter of rods = .25"

Δd = .31 mils.

Unfortunately, data on how the thermal expansion coefficient varies with temperature is not readily available. The actual brass rods used were made 1 mil smaller in diameter than the aluminum holes. The amount of canter in the slide depends on this difference in diameter as well as upon the ratio of the length of the aluminum guiding holes to their width. This ratio was chosen to be 3 in our design and we found very little canter in the movement of the slide.

Before cooling the amplifier, the micrometer, brass rods, and aluminum block must be cleansed of all grease and oils. Upon cooling, these materials will freeze and restrict motion. The block is rinsed with acetone. The micrometer and brass rods are placed in an ultrasonic acetone bath. Then they are placed in an oven at 100°C for 20 minutes to remove all moisture. Moving or bearing parts must not be touched by human hands.

Bonding wires to the FET must have enough slack in order to withstand the shrinkage due to cooling. A few samples of packaged FET's have indicated that the bonding wires are drawn very tight to minimize lead inductance for good high frequency performance. Upon cooling, high failure rates are observed, presumably due to shrinkage and breaking of the bonds [22]. Dielectrics typically have a shrinkage of 1% when cooled to 20°K. This means a difference of 50 mils in the quarter-wave transformer and 25 mils in the amplifier board. Enough slack must be provided to allow for such shrinkage or one will find capacitors breaking in two, etc. Hence, flexible connections must be made between various large elements.

The amplifier is bolted to a soft aluminum bracket (good thermal conductivity) which is bolted to the 15°K stage of the refrigerator. This bracket acts as the top lid of the amplifier. Indium foil is placed between all

surfaces where a good thermal contact is desired, i.e., between rivet and circuit board, circuit board and amplifier block, amplifier and bracket, bracket and refrigerator, etc.

The input line is an air dielectric, stainless steel, 50 Ω coaxial line. The output line is a semi-rigid, dielectric filled coax. Temperature sensors are attached to the rivet, the amplifier block, and the 15°K stage. This enables one to study where the most thermal resistance is present.

During the first cool down, the 15°K stage reached 16°K; however, the rivet only reached 35°K. This difference was attributed to radiation loss rather than to thermal resistance because when power was applied to the FET, the rivet temperature only changed 4°K. This implies a thermal resistance of $100 \frac{°K}{W}$ and nearly 200 mW of power would be necessary to provide the 19°K difference in temperatures. The extraneous heating power is thermal radiation whose source is the dewar can which is at room temperature. A radiation shield made from aluminum foil was used during this cool down but did not cover the bottom of the amplifier. Also, the surface of this shield was very rough. The equation describing thermal power radiated from one object to another is:

$$\text{power} \propto \left(T_1^4 - T_2^4\right) \varepsilon_1 \varepsilon_2 A \qquad \text{Eq. (38)}$$

We have assumed two parallel planes of area A, temperatures T_1 and T_2 and emissivities ε_1 and ε_2. To decrease this power, we want to decrease the temperature difference between the amplifier and the shield surrounding it. Also, a shield with a low emissivity is desired. Therefore, a new shield made from copper sheeting was constructed. It was a polished cylindrical structure which bolted to the 77°K stage. Now the radiation from the 298°K dewar can

is largely reflected by the shield and the amplifier is being radiated at by a polished 77°K object. And since a poor absorbing material is also a poor radiator, the radiation from the shield will be small (ϵ is small in equation 38). During the next cool down, a rivet temperature of 13.4°K and a 15°K stage temperature of 11°K were achieved. This indicates that only 24 mW of power is radiated at the amplifier which is almost an order of magnitude reduction.

A photograph of the amplifier in the refrigerator system is shown in Figure 31.

4.4 Amplifier Stability

One of the major difficulties encountered during the 600 MHz amplifier experiments was the prevention of oscillation. The oscillations can be caused by several different feedback mechanisms in the amplifier and the chip. Far from center band frequency, these feedback mechanisms which provide negative feedback at 600 MHz may exhibit a 180 degree phase shift such that positive feedback is provided. The parallel feedback capacitor C_{dg} (see Figure 4) is a feedback element intrinsic to the FET chip. The source lead series inductive feedback helps improve the input power match but it decreases stability at high frequencies. Electromagnetic field coupling between elements in the input and the output circuits produces feedback. Finally, the amplifier box looks like a resonant cavity at high frequencies.

Experimentally, it was observed that all oscillation occurred at frequencies between 6 and 10 GHz. This was far more curable than oscillation near the center band of the amplifier because changes can be made in the amplifier which affect the high frequency performance and damp out the oscillation, yet leave the 600 MHz performance unchanged.

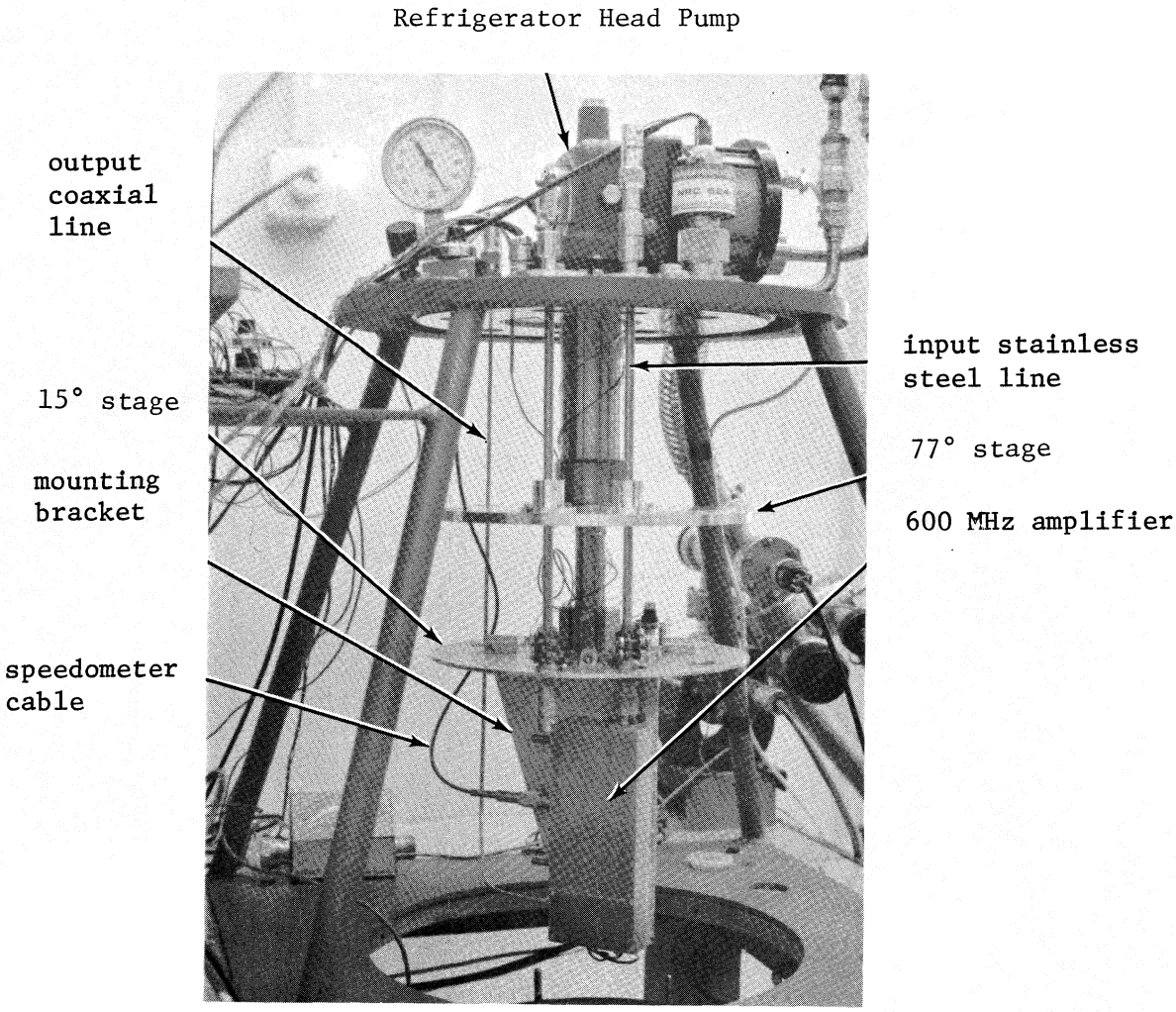


Figure 31. Photograph of the 600 MHz amplifier mounted in the cryogenic refrigerator system.

Before looking at the amplifier as a whole, we wish to check FET stability parameters. K is the transistor stability factor defined as:

$$K = \frac{1 + |S_{11}\ S_{22} - S_{12}\ S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2\ |S_{21}\ S_{12}|} \qquad \text{Eq. (39)}$$

If K is greater than unity and positive at a particular frequency, then the two-port described by the S-parameters is unconditionally stable and cannot oscillate for any input and output loads that have a positive real impedance. If K is less than one, then oscillation is dependent upon load impedance. Another interesting quantity is G_{max}, the maximum two-port power gain obtained when both input and output are conjugately matched.

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \left|K \pm \sqrt{K^2 - 1}\right| \qquad \text{Eq. (40)}$$

(The + sign is used if $1 + |S_{11}|^2 - |S_{22}|^2 - |S_{11}\ S_{22} - S_{12}\ S_{21}|^2$ is negative.)

These two quantities are calculated for frequencies of 2 GHz and 8 GHz for the HFET-1000. The results are K = .348, G_{max} = 17.7 dB at 2 GHz and K = 1.05, G_{max} = 10.6 dB at 8 GHz. The results indicate that stability increases but gain decreases as the frequency is raised. The HFET-1000 as a two port is unconditionally stable at 8 GHz. This is true for any input or output load. However, if loads are connected from input to output (i.e., if any of the feedback mechanisms previously described are present) then the amplifier becomes conditionally stable.

A principal reason for the oscillation problem in FET's is illustrated in the previous paragraph. The amplifier may be designed to work at 600 MHz

but the active device has 10 dB of gain all the way up to 8 GHz. A difficult problem exists in trying to theoretically analyze the high frequency oscillation because the circuit elements no longer behave as lumped elements but instead as distributed networks. For instance, an input series inductor probably looks more capacitive than inductive at 8 GHz. Hence, the oscillation analysis becomes a field theory problem and soon becomes extremely difficult.

Solutions to the problem were, therefore, made on an experimental basis. The oscillation was most dependent upon drain voltage. Regardless of current or gate voltage (except for very low currents where the transconductance falls off rapidly) oscillation would begin for $V_d > V_{osc}$. The value of V_{osc} was a measure of the stability of the circuit. The higher V_{osc}, the more stable the circuit.

The first attempt was to provide as low an impedance as possible at high frequency at both input and output connections to the FET. We could not achieve this goal on the input circuit because it would involve adding shunt capacity (something which has been carefully avoided!). However, the output matching network was changed from the high pass structure that was used in the 500 MHz amplifier, to a low pass structure consisting of a shunt capacitance followed by a series inductance (see Figure 27). However, the oscillation remained due to the inductance of the bonding wire to the drain plus other series parasitic inductances.

It was found that reduction of the source inductive feedback led to greater stability but it also decreases the input matching performance of the amplifier. Therefore, this solution was not acceptable. A copper shield was built, separating the input circuit from the output circuit in an attempt to reduce electromagnetic coupling. This improved the stability of the circuit

but it did not remove the oscillation altogether. It only increased the drain voltage necessary to produce oscillation a few tenths of a volt.

Finally, an optimum solution was found which totally removed all high frequency oscillation without any degradation of amplifier performance. Pieces of Eccosorb AN-72 were placed in the input and the output of the circuit. This lossy material consists of carbon impregnated in a foam structure. The effect of this lossy foam is to drastically reduce the quality factor of the amplifier box as a high frequency resonant cavity. High frequency oscillations were prevented for all values of drain bias. The lossy foam is not located close enough to the input coil to add any loss to this coil or noise to the amplifier. The lossy foam was not so successful at temperatures below 100°K. In this range, oscillations appeared at high values of drain voltage. The probable cause is that the carbon increases in resistivity at low temperatures, decreasing the loss of the foam and its usefulness.

4.5 Transmission Line Noise

The losses in the quarter wave transformer are small but finite and therefore they contribute noise to the amplifier. The simplest and most physically intuitive calculation of this noise increase can be made by using the noise temperature cascade formula for an ideal attenuator followed by an amplifier. The attenuator is assumed to be matched at the input. See Figure 32.

$$T_{12} = (L - 1)\, T_{atten} + L\, T_2 \qquad \text{Eq. (41)}$$

T_{atten} = physical temperature of attenuator = 298°K.

L = attenuator loss = $\frac{P_{in}}{P_{out}}$ = 1.00423.

T_2 = FET noise temperature = 60°K.

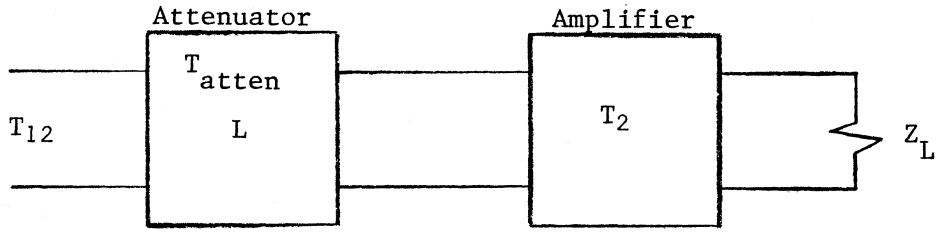


Figure 32. Cascaded attenuator and amplifier.

Equation 41 determines the cascaded noise temperature. The attenuator is assumed to be at room temperature with 2.11×10^{-3} nepers (.0183 dB) of attenuation calculated for the characteristic impedance of the line set to 50 Ω (see Table 4). Substituting these numbers into equation 41, and assuming the amplifier to be a 60°K FET, we approximate a noise temperature increase of 1.5°K.

J. Granlund [28] has analyzed this problem in more detail. He has calculated the available gain of the transmission line to be

$$G_A = \frac{R_1 \, |Z_0|^2}{R_0\left[\frac{1}{2}\left(|Z_0|^2 + |R_1|^2\right) \sinh(2\alpha\ell) + R_0 R_1 \cosh(2\alpha\ell)\right] - X_0^2 \, R_1} \qquad \text{Eq. (42)}$$

where R_1 = source impedance driving 600 MHz amplifier = 50 Ω.

$Z_0 = R_0 + jX_0$ = characteristic impedance of transmission line.

$\alpha\ell$ = total attenuation along the line in nepers.

The line is assumed to be exactly a quarter wavelength in length. The assumption is then made that the available gain of the transmission line, G_A, is not affected by changing the characteristic impedance of the line. This is obviously not correct since copper losses along the line are a function of the separation between the copper line and the ground plane (as is shown in Table 4). However, this approximation simplifies the analysis and we obtain four corrected noise parameters for the FET: T_{min} , Z_{opt} , and G_N .

$$T_{min}' = G_A T_{min} - (1 - G_A) T_{atten} \qquad \text{Eq. (43)}$$

$$Z_{opt}' = Z_{opt} \qquad \text{Eq. (44)}$$

$$G_N' = G_A G_N \qquad \text{Eq. (45)}$$

The unprimed noise parameters are those obtained directly from measurement before correction. Equation 43 is just equation 41 solved for T_2. For the numerical values mentioned previously, we obtain $G_A = .9958 \simeq e^{-2\alpha\ell}$, $T_{min} - T_{min}' \simeq 1.5°K$, and $G_N' \simeq G_N$. Only the change in noise temperature is noticeable and we find that the simple approximation of equation 41 is sufficient.

The analysis of this problem taking into account the variation in G_A as Z changes has been studied [28] but arriving at an analytic solution involves solving a fourth power equation which is impossible. However, an exact noise characterization of the FET can be obtained if the available gain, G_A, is calculated at every measured point. Then each measured noise temperature can be corrected to the FET noise temperature using equation 43 with T_N replacing T_{min}. Hence T_{min}, R_{opt}, X_{opt}, and G_N can be obtained from these corrected curves. This process was not performed for the FET data because the corrections were too

small to necessitate so much work. In our case, the corrections using equations 43, 44, and 45 were sufficient.

Granlund also has calculated the four noise parameters of the quarter-wave transformer as shown in the equivalent circuit of Figure 33.

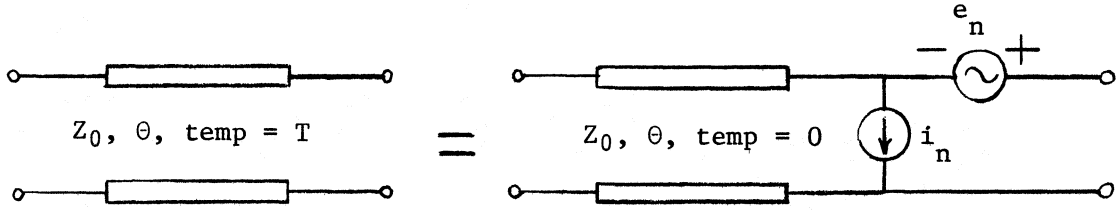


Figure 33. Equivalent noise circuit for a lossy transmission line. The lossy hot line is equivalent to a lossy cold line followed by noise sources.

The equations for the four noise parameters of this equivalent network are

$$R_N = \frac{R_0}{2} \sinh(2\alpha\ell) \simeq R_0\,\alpha\ell \qquad \text{Eq. (46)}$$

$$G_N = \frac{\sinh(2\alpha\ell)}{2R_0} \simeq \frac{\alpha\ell}{R_0} \qquad \text{Eq. (47)}$$

$$\rho = \frac{2}{\sinh(2\alpha\ell)} \left\{ \sinh^2(\alpha\ell) - \frac{(\alpha\ell)^2}{\left(\frac{\pi}{2}\right)^2} \cosh^2(\alpha\ell) + \frac{j\alpha\ell}{\frac{\pi}{2}} \cosh^2(\alpha\ell) \right\}$$

$$\simeq \alpha\ell \left\{ 1 - \left(\frac{2}{\pi}\right)^2 \right\} + j\,\frac{2}{\pi} \qquad \text{Eq. (48)}$$

Parameter definitions are the same as those previously given and the line is a quarter wavelength long ($\beta\ell = \pi/2$). We have also assumed that the dielectric loss is zero which gives G = 0 for the transmission line. This leads to an equation for the ratio of the imaginary and real parts of the characteristic impedance of the transmission line.

$$-\frac{X_0}{R_0} = \frac{\alpha}{\beta} \qquad \text{Eq. (49)}$$

The use of these transmission line noise parameters to correct the measured noise parameters is very difficult and has not yet been formulated. The fact that the noise is measured at the front end of the transmission line but the optimum source impedance is determined at the back end creates problems that have not been solved.

In conclusion, much effort has been spent in determining that the effect of the transmission line loss on the measured noise parameters is very small.

4.6 Room Temperature Results

Complete room temperature data was taken for three different HFET-1000 chips from three separate batches. Two of these (we shall call them #1 and #2) were chips mounted on rivets, whereas the third was an HFET-1102 (an HFET-1000 in a package). The measurement results used to find R_{opt} and X_{opt} are shown in Figure 34. In this graph and in the rest of the graphs of section 4.6, the circles represent chip #1, the triangles represent chip #2, and the crosses are used for the HFET-1102 package. From Figure 34 one notes that the 1102 has the lowest R_{opt} and the highest G_N of all three FET's. X_{opt} for the three FET's is very close to 300 Ω.

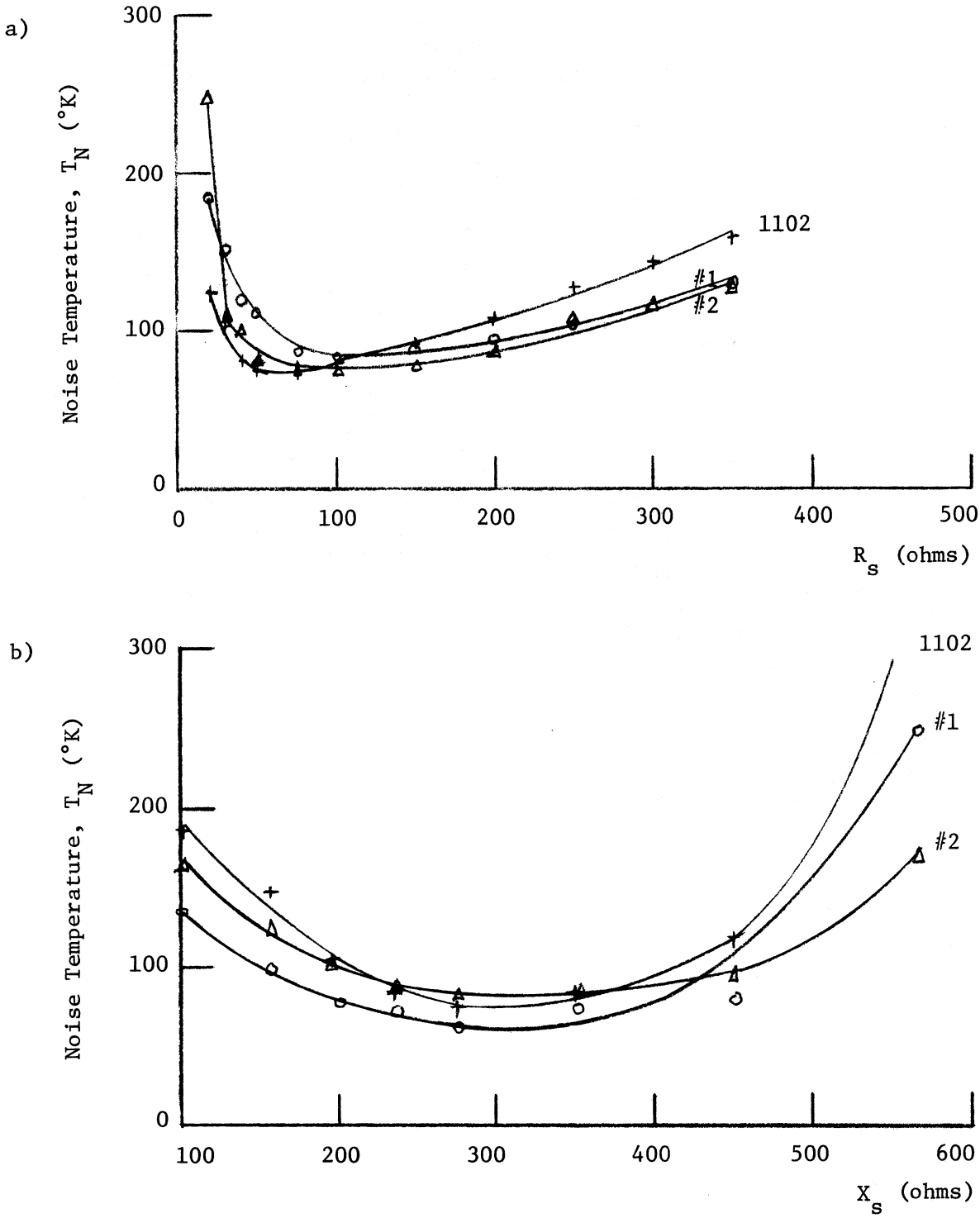


Figure 34. Measured values of noise temperature versus real source impedance (a) and imaginary source impedance (b) for the three HFET-1000's.

The graphs of Figure 34 bear a very close resemblance to the theoretical predictions of equation 29 and Figure 22. However, one must ask whether the rise in T_N at low values of R_s is due to the FET or to input circuit losses. Both the FET and the circuit losses contribute noise in this region and our calculations indicate that losses add only a small contribution (= 7°K at R_s = 50 Ω. The series coil adds approximately 6°K of noise (see section 3.3). Certainly, one can claim that regardless of how much noise is being added by the input circuit, the R_{opt} found in Figure 34a is an upper limit for the R_{opt} of the FET. Table 5 provides several noise parameters measured and calculated (using program 2 of Appendix C) for the three HFET-1000's.

TABLE 5

Measured noise parameters for three FET's using the 600 MHz amplifier.

FET	T_{min} (°K)	Z_{opt} (ohms)	G_N (mhos)	R_N (ohms)	ρ
#1	60	100 + j280	7.5×10^{-4}	62.1	.132+j.938
#2	60	85 + j325	7.5×10^{-4}	84.6	.157+j.967
1102	68	75 + j280	1.08×10^{-3}	90.7	.116+j.966

Figure 35 shows the frequency response of the noise temperature and the r.f. gain for the three FET's. These measurements are made at optimum source impedance and optimum bias for each FET. We see that very broadband noise and gain performance are obtained for all three FET's. FET #1 demonstrates an almost flat noise temperature of 70°K from 450 MHz to 700 MHz while gain was greater than 15 dB from 300 MHz to 700 MHz. Gain reached an 18 dB peak near 550 MHz. The noise and gain performance of the HFET-1102 was less broadband than the two chips. This is caused by the added shunt capacity at the input of the package which increases the Q and decreases the bandwidth. All three FET's reach nearly the same noise minimum and gain maximum. This is assurance of good reproducibility of the HFET-1000 material and geometry. As in the 500 MHz measurments, we again see that the noise minimum occurs at a higher frequency than the gain maximum indicating that $X_{opt,noise} > X_{opt,power}$.

The measured input and output return loss when $Z_s = Z_{opt}$ is given in Figure 36. We see that a great deal of variation exists in the input return loss between FET's. This is due to different lengths of the source inductance used as well as the FET parameters g_m and Y_2 as described in equation 25. FET chip #2 was matched very well to the noise optimum source impedance. This good match is attributed to an increased amount of source inductance used once the oscillation problem was solved with the carbon impregnated foam. The amount of source inductance used is near 2 nH which produces a real FET input impedance of 100 Ω. The chip #1 measurements were made prior to the use of the lossy foam; hence feedback had to be reduced to obtain a stable amplifier. About 1 nH is used and an input return loss of 10 dB maximum is obtained when $R_s = R_{opt}$. A 10 dB return loss indicates a 2:1 impedance mismatch; therefore, $R_{IN,FET} \simeq$ 40 to 50 Ω if $R_{opt} \simeq 100$ Ω. No source inductive feedback could be added to the packaged FET using a long bonding wire since all bonds are sealed within the

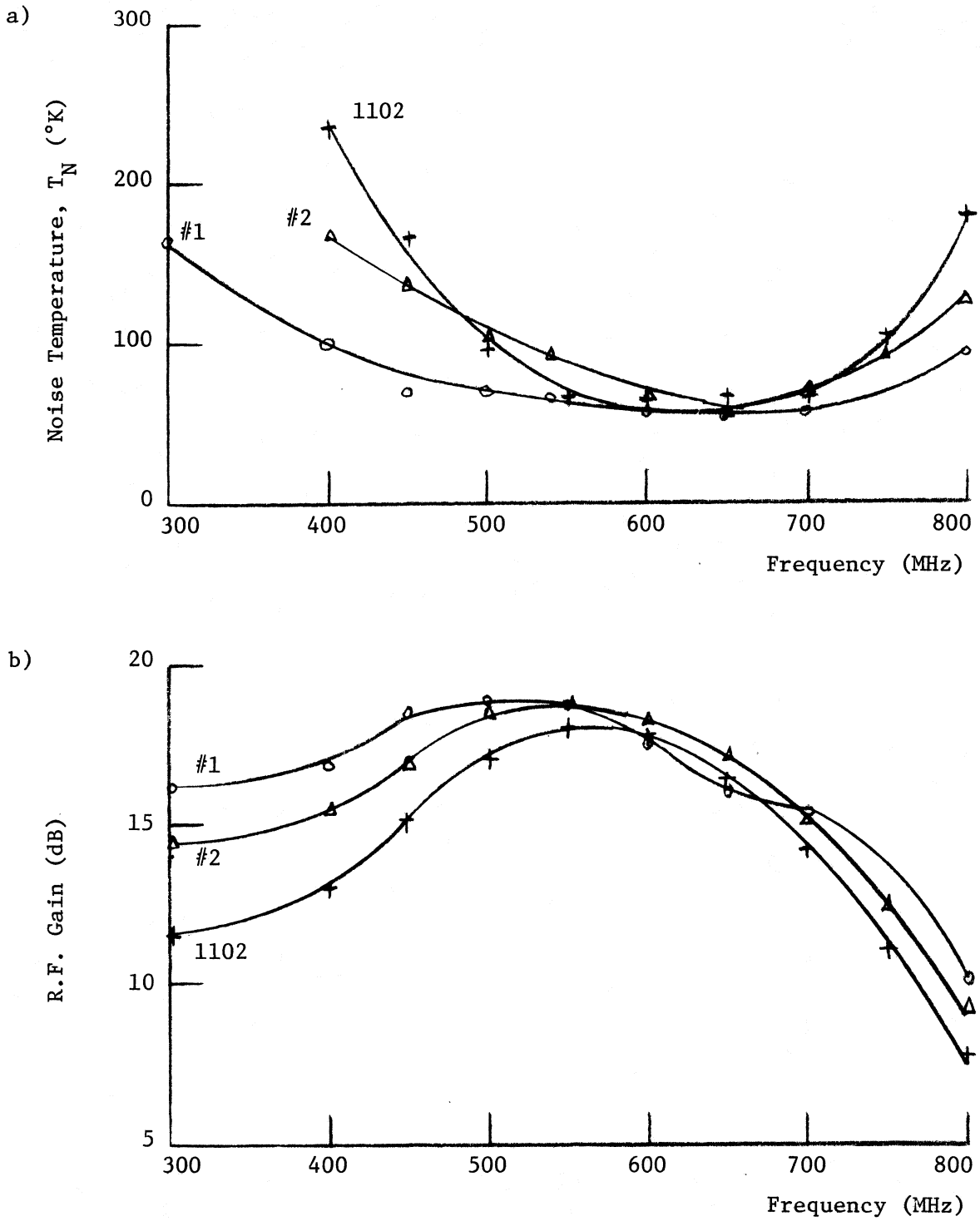


Figure 35. Noise temperature (a) and r.f. gain (b) versus frequency for three HFET-1000's ($Z_s = Z_{opt}$, optimum noise bias).

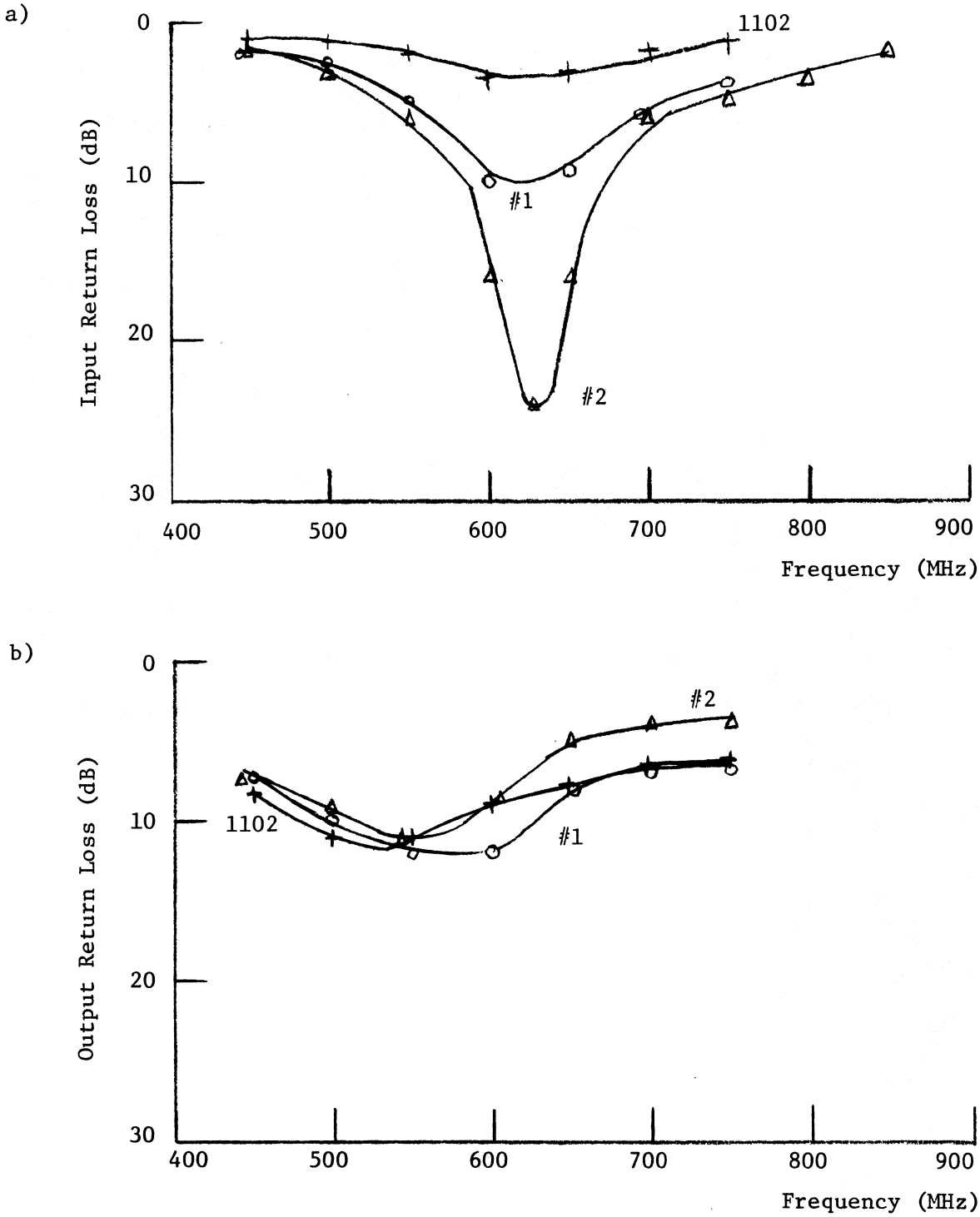


Figure 36. Input (a) and output (b) return loss of the three HFET-1000's as a function of frequency ($Z_s = Z_{opt}$, optimum noise bias).

package. Therefore, the source tab is soldered directly to ground and the lack of feedback shows up in the input return loss measurements. A maximum of 4 dB return loss was achieved. The input return loss measurements of Figure 36a exhibit the implementation and usefulness of source inductive feedback. Once the oscillation problem was solved, an input return loss of 24 dB, which is equivalent to a VSWR of 1.13, was measured. Hence, one of the most crucial objectives of a radio astronomy front end design has been met: a good input match at optimum noise source impedance.

Output return loss peaked at 10 dB near 550 MHz for all three FET's. The output return loss curves for the FET's are very similar being dependent upon the output shunt impedance of the FET and the output matching network. Figure 36b is proof that the output shunt impedance varies little between HFET-1000 chips. The 10 dB return loss indicates a 2:1 real impedance mismatch in the output circuit at resonance. Further tuning can improve this match; however, 10 dB is fine for noise measurements.

Figure 37a illustrates the noise temperature dependence upon drain bias current, whereas Figure 37b shows how transconductance and linear r.f. gain change with current. The transconductance drops off rapidly at low current because the depletion layer forces most of this current to flow near the active region-substrate boundary where chromium impurities degrade the electron mobility. The r.f. gain decreases at the same rate as g_m (being directly proportional to g_m) and at very low current the gain decreases even more rapidly. This is caused by the change in R_{ds} and the output match with bias. The noise temperature is flat for currents above 10 mA. However, below 10 mA, the noise increases as g_m decreases. This suggests that the dominant noise source is drain circuit noise which must be divided by g_m when it is referred back to the

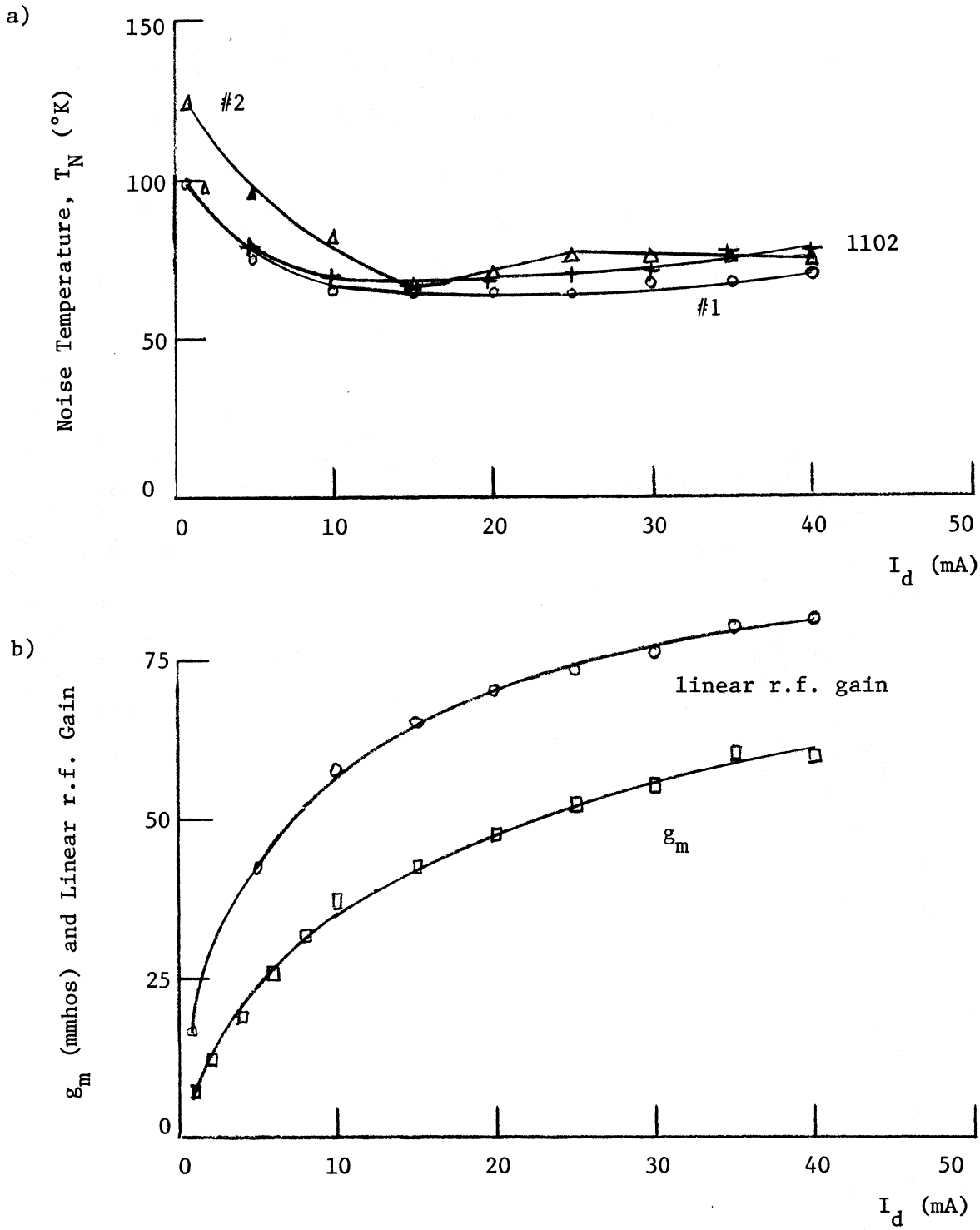


Figure 37. (a) Noise temperature vs. drain current for all three FET's.
(b) Transconductance and linear r.f. gain as a function of drain current for chip #1.

input. If g_m decreases, the noise temperature increases. This effect is not noticed at high current although g_m is changing. Perhaps a source of noise which increases with drain current (e.g., dipole diffusion noise) keeps the noise temperature from dropping any further at large currents. Figure 38a shows the current dependence of transconductance for all three FET's. All three curves have the same shape, but chip 1 exhibits substantially larger values of g_m.

The current-voltage characteristics of FET #2 are given in Figure 38b. These experimental values are typical for HFET-1000's measured during this project. This chip possesses a shorted gate saturation current of 65 mA and a pinch-off voltage of 1.7 volts.

Figure 39 shows measurements of the input return loss as the real source impedance facing the FET is changed for chip #1. With 15 mA of drain current passing through the source feedback inductor, an optimum match occurs when R_s = 40 Ω. However, when the drain bias current is removed and no source inductive feedback exists, the optimum match occurs at R_s = 12 Ω. We can conclude that the feedback increases the real input impedance of the FET by 28 Ω. Since R_{opt} = 100 Ω for this chip, a two to one impedance mismatch at resonance should occur and we would expect a 10 dB maximum return loss which is exactly what was observed in Figure 36a.

Figure 40a more clearly illustrates the change in R_{ds} with bias. This is a graph of output return loss versus frequency as we change the drain current. The output matching network was designed assuming operation near 20 mA. When one changes the current drastically, the associated change in R_{ds} will either improve or degrade the output match. From the graph, we see that an increase in current improves the impedance match, but only 6 dB of return loss is obtainable when the current drops to 1 mA.

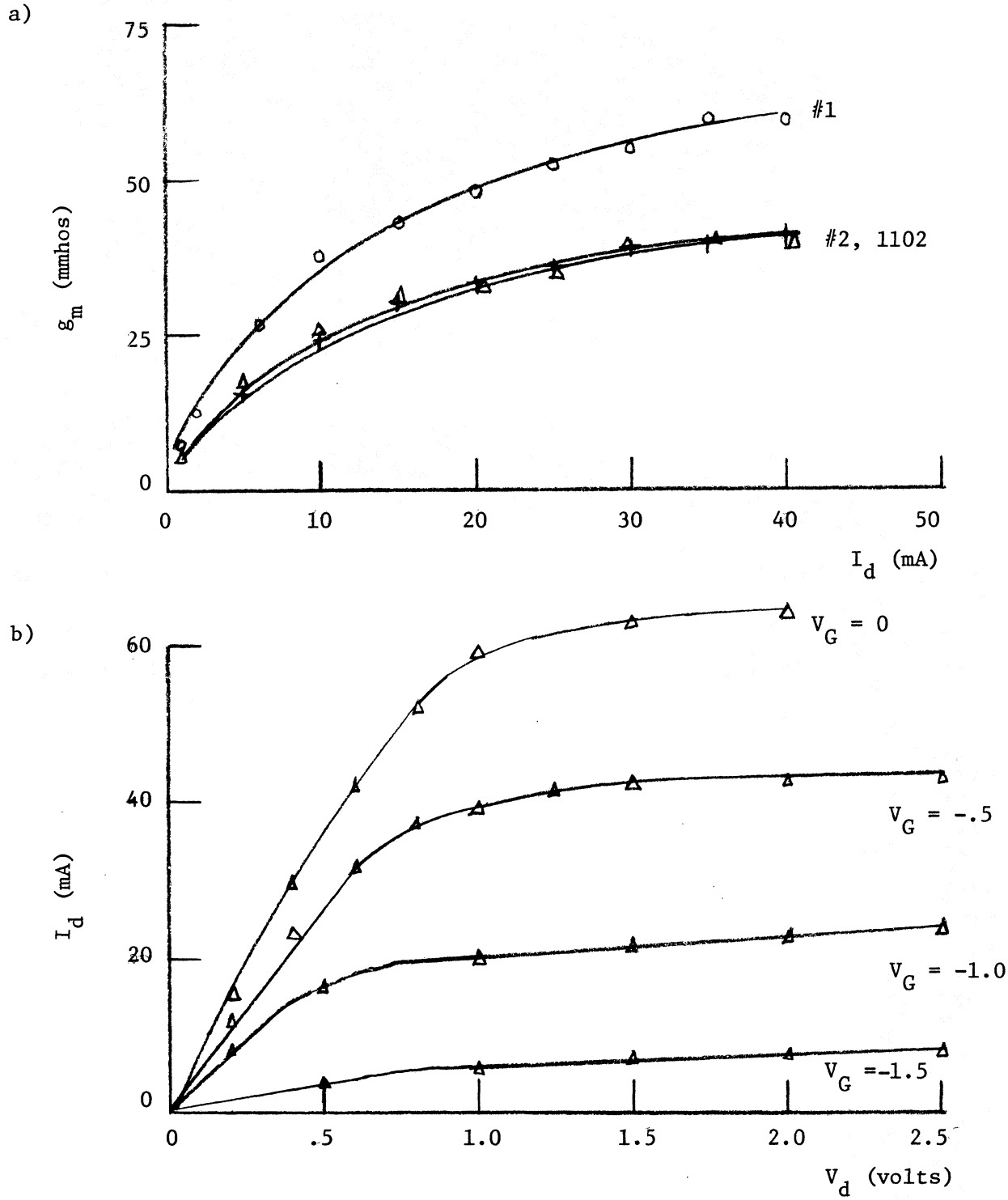


Figure 38. (a) The dependence of transconductance upon drain current for all three FET's.
(b) Current-voltage characteristics of FET chip #2.

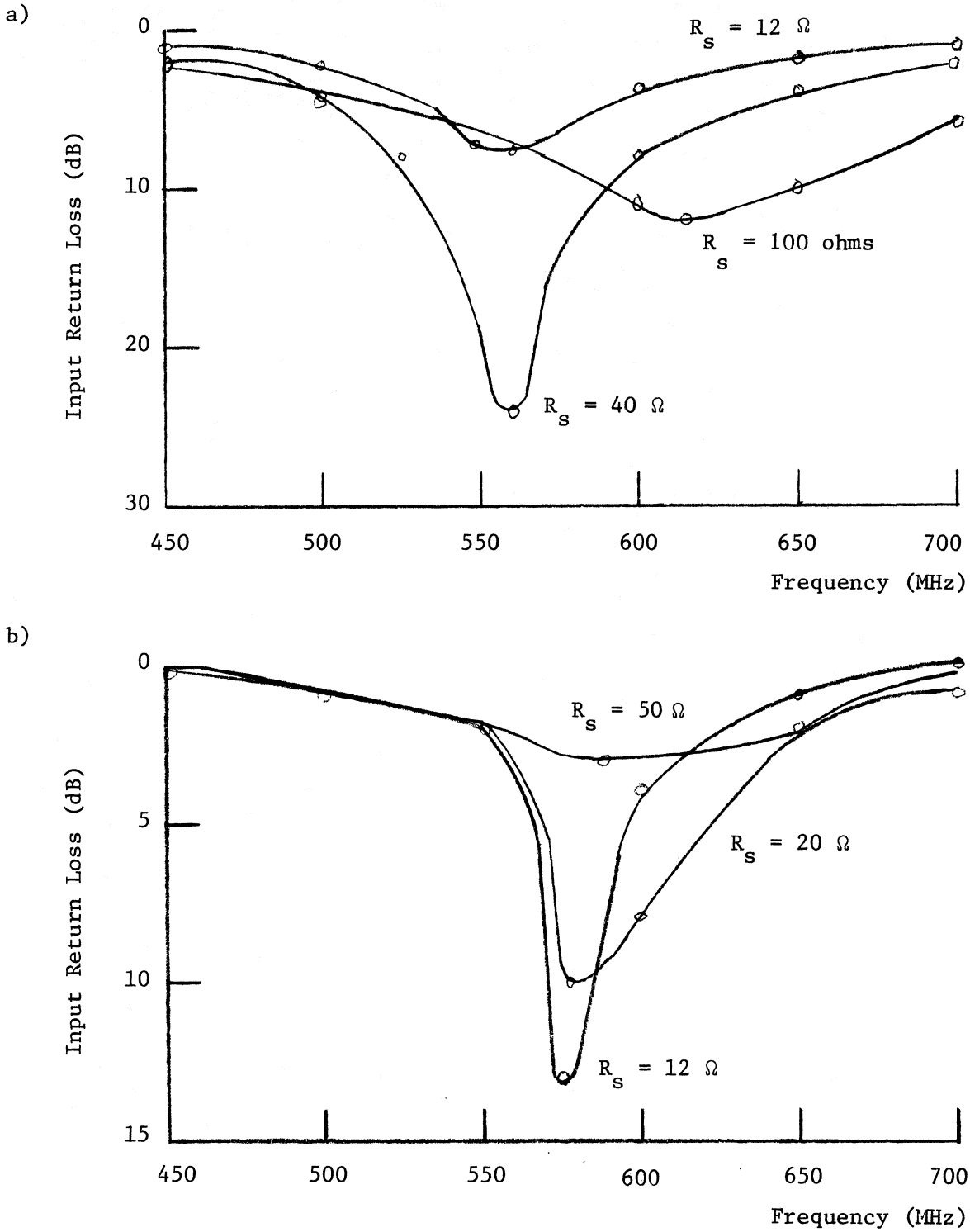
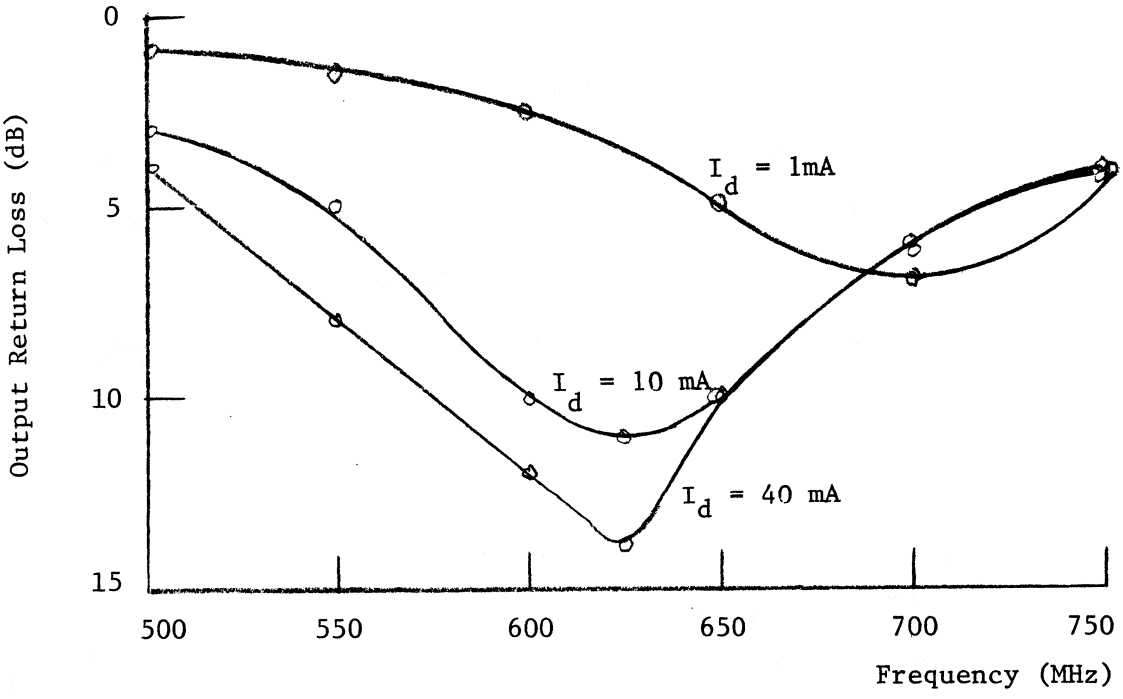


Figure 39. Measurement of the input return loss versus frequency as the real source impedance is changed for chip #1. In (a), drain current is 15 mA but in (b) there is no drain current and therefore no feedback effect.

a)



b)

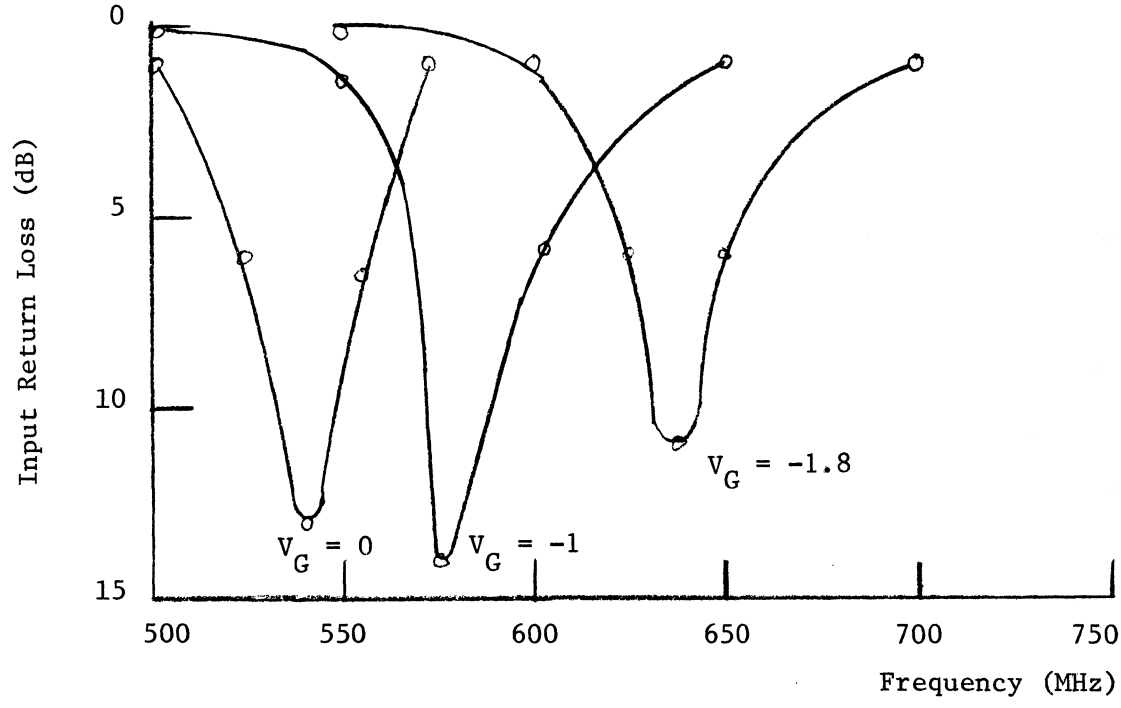


Figure 40. (a) Output return loss vs. frequency as drain current is changed for chip #1.
(b) Input return loss of the amplifier vs. frequency as the gate bias varies and using chip #1. There is no drain current, hence no feedback.

The input circuit is also bias dependent as is shown in Figure 40b. The depletion capacitance of the Schottky junction is dependent upon the reverse bias. Figure 40b shows the measured input return loss versus frequency for chip #1 and with no drain current. There is no feedback and the quarter-wave transformer is set to a source impedance value of 12 Ω to obtain a good input match. Measurements for three values of gate bias are performed. The resonant frequency for the series inductor and capacitor is

$$f_{res} = \frac{1}{2\pi} [LC]^{-1/2} \qquad \text{Eq. (50)}$$

As the reverse bias of the junction is increased, the depletion region widens and the capacitance decreases. This capacitance decrease causes a corresponding resonant frequency increase as is seen in the graph. Using this data and a value for the built-in potential of the Schottky junction, one can estimate values for the input capacitance of the FET and the shunt capacity of the input of the amplifier. A simpler method of measuring this capacity is to use an a.c. bridge.

A set of measurements made on these FET's at room temperature involved d.c. resistance measurements of the gate and the channel. Forward bias was applied to the FET gate while the drain was open circuited. The diode characteristic was plotted in Figure 41a. Forward current must be limited to 1 mA to protect the gate. A semi-log plot is shown in Figure 41b. The linear portion of this plot provides the ideality factor, η, of the FET Schottky-diode gate junction.

$$\eta = 38.6 \frac{\left(V_1 - V_2\right)}{\ln\left(\frac{I_1}{I_2}\right)} \qquad \text{Eq. (51)}$$

Points 1 and 2 are two points along the linear portion of the semi-log curve.

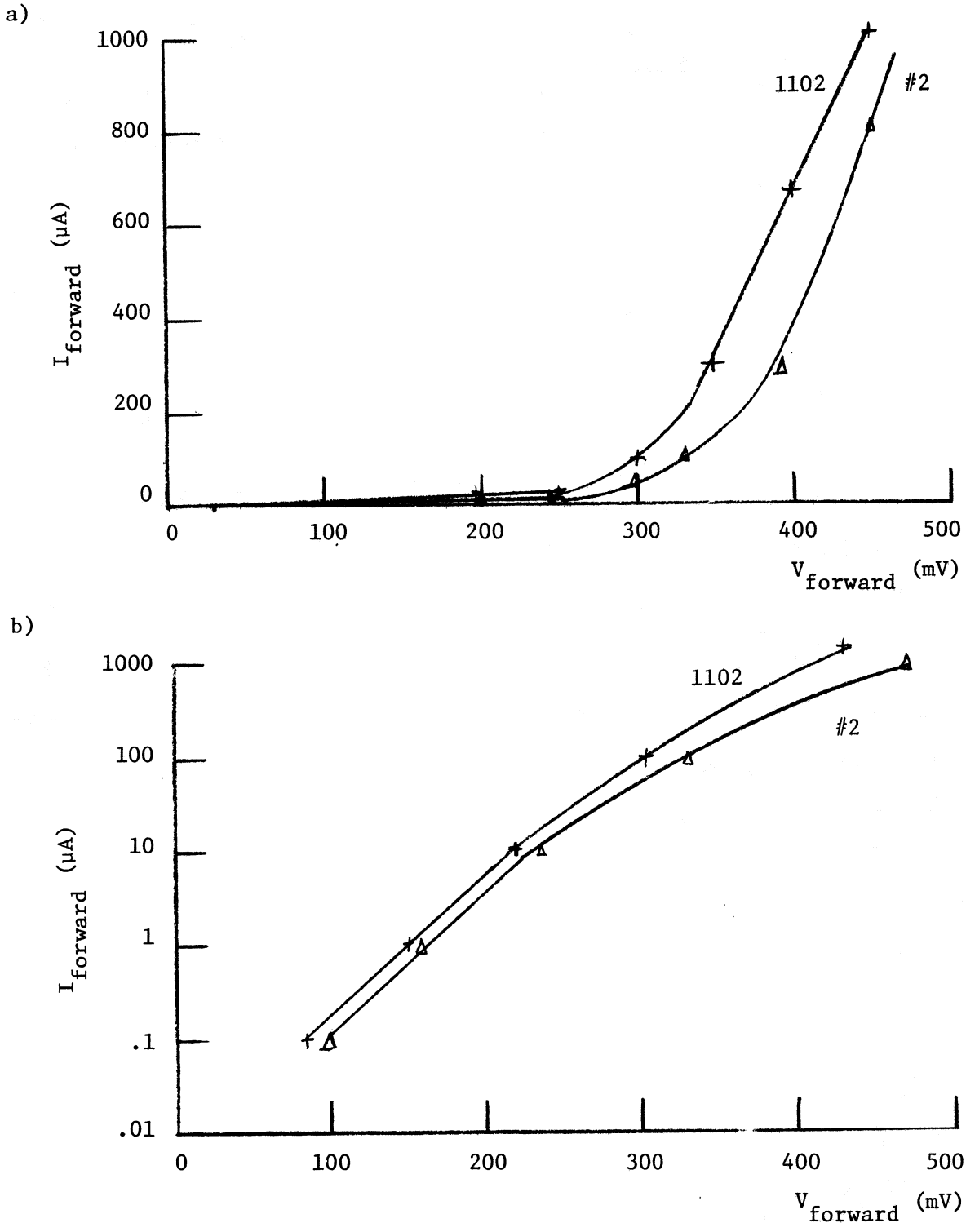


Figure 41. The forward bias characteristic of the Schottky gate (with open drain) is plotted in (a). (b) is a semi-log plot of the same data to aid calculations of η and the series resistance.

The curve deviates from linearity at higher current due to the intrinsic series resistance in the gate to source circuit of the FET. This resistance can be calculated using the equation:

$$V_{f\omega d} = IR + \frac{\eta KT}{q} \ln \frac{I}{I_0} \qquad \text{Eq. (52)}$$

I_0 = the saturation current of the diode.

For chip #2, we measured $\eta = 1.18$ and $R = 95\,\Omega$. For the HFET-1102, $\eta = 1.15$ and $R = 82\,\Omega$ were found. The values for η are quite reasonable and agree with GaAs Schottky barrier theory. However, the high values of series resistance are questionable since we expect to find $R_{FET} \simeq 12\,\Omega$ and in fact we have measured $\simeq 12\ \Omega$ using other techniques. The reason for this contradiction is not yet understood. The diodes are leaky in the reverse direction with 60 nA to 230 nA being measured at a reverse voltage of 2 volts. I_0 was measured to be 5.96 nA and 4.3 nA for the two diodes.

The resistance of the entire channel, r_{ch}, as well as the resistance of the active layer between gate and source were also measured. See Figure 42.

A constant forward current of 10 μA is applied to the gate. The depletion region of the forward biased gate maintains a constant width. Current is then passed through the drain and the channel resistance is measured. Then r_{gs} is found by measuring the increase in V_g as drain current increases. Assuming that the voltage across the junction remains constant (for a constant forward current) a value of r_{gs} is calculated. These measurements provide a look at the GaAs mobility especially when the FET is cooled. Two effects become apparent from experiments. As current increases, drain voltage increases and the depletion region near the drain becomes less forward biased.

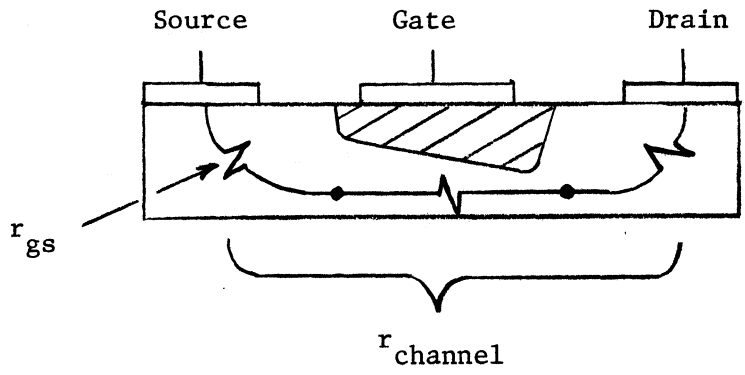


Figure 42. Illustration of the channel resistance and the gate-to-source resistance, r_{gs}, which is one component of r_{ch}.

It increases in width, thus the channel resistance increases. Also, as current increases, the same effect described above will cause most of the gate current to crowd towards the source end of the depletion region. Therefore, the effective gate to source resistance seen is smaller than before and we measure a decrease in r_{gs}.

The final room temperature tests made were designed to look for drain circuit trap noise. Section 2.5 predicts that the noise power spectrum of this type of noise should be proportional to $I_D V_{DS}$ if the FET is biased in the triode region. Measurements were made on chip #1 when it was biased in the triode region. The measured room temperature was multiplied by the measured transconductance in order to refer this noise to the output circuit. Upon analysis, no correlation between this output circuit noise and the dissipated power could be found. Hence, either drain circuit trap noise is not a major contribution at this frequency, or the measurement techniques used were not valid.

4.7 Cooled Amplifier Results

A dramatic improvement in noise performance is measured when the FET ambient temperature is reduced. A noise temperature of 17°K was measured with the FET at liquid nitrogen temperature. This is the lowest noise 600 MHz amplifier reported to this date. Table 6 provides noise parameters for chip #2 at temperatures of 16°K, 77°K, 150°K, and 300°K.

TABLE 6

Measured noise parameters for chip #2 at four different physical temperatures.

$T_{Ambient}$ (°K)	T_{min} (°K)	Z_{opt} (ohms)	G_N (mhos)	R_N (ohms)	ρ
298	60	85 + j325	7.5×10^{-4}	84.6	.157+j.967
150	26	85 + j325	4.0×10^{-4}	45.1	.081+j.967
77	17	75 + j325	2.0×10^{-4}	22.2	.215+j.974
16	17	40 + j325	2.0×10^{-4}	21.4	.325+j.992

Note that the 16°K measurement provides an absolute value of ρ slightly greater than 1 which is theoretically impossible. This is due to experimental error in the measurement process. Measured data at several temperatures is provided in Figure 43a. At each temperature, the bias and source impedance is optimized for low noise. Two curves are shown in Figure 43a. The top curve gives the actual noise temperature measured at the input connector of the refrigerator.

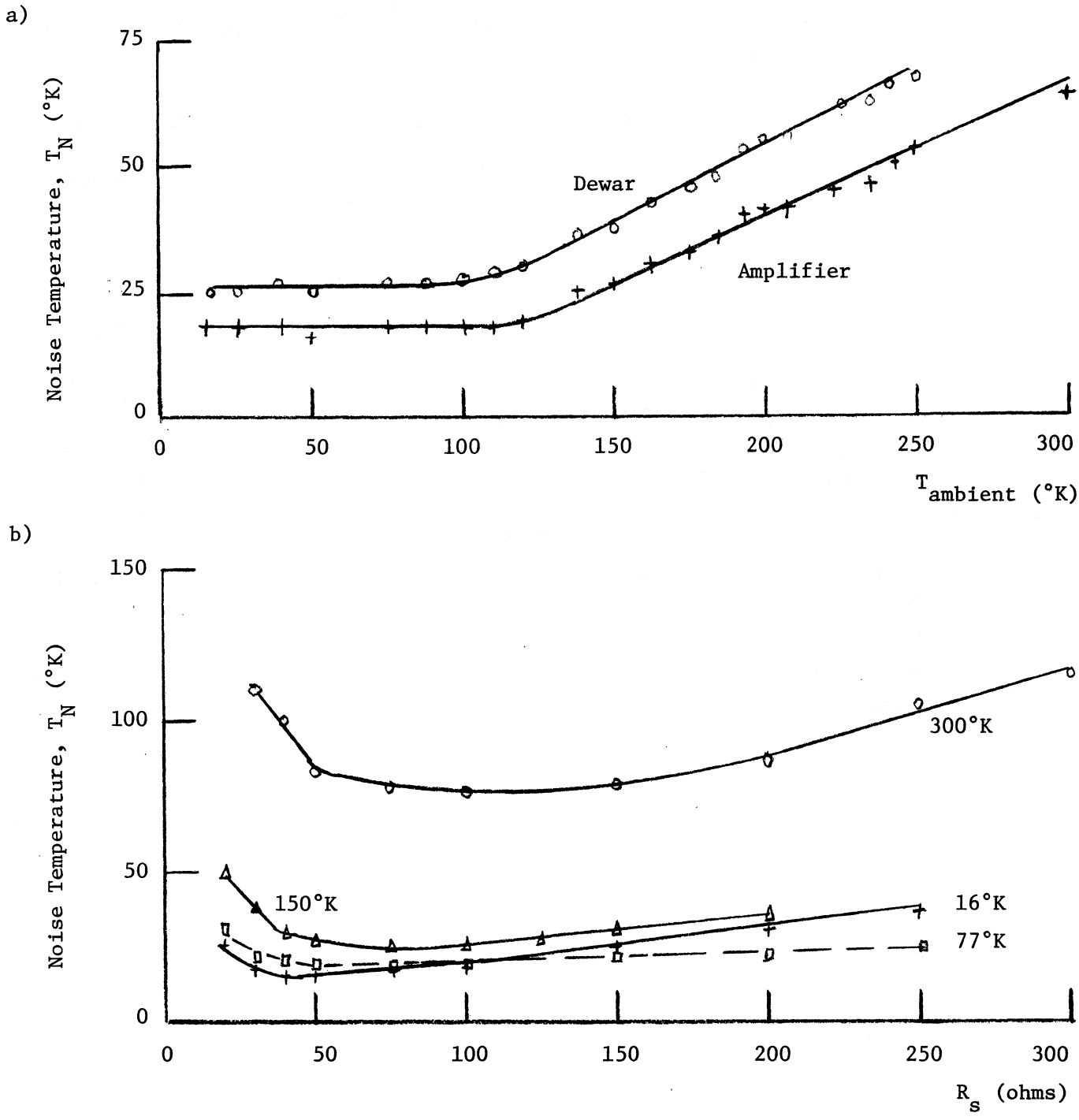


Figure 43. (a) Noise temperature vs. ambient temperature for chip #2 measured at the dewar input and corrected to the amplifier input.
(b) Noise temperature as a function of real source impedance for 300°K, 150°K, 77°K, and 16°K.

However, the stainless steel line which connects the input of the amplifier to the outside world has .20 dB of measured loss. This loss measurement was made at room temperature; however, a similar measurement proved that the loss of this line does not change upon cooling. The correction for this loss is derived in Appendix E assuming the loss is distributed uniformly along the line and that the temperature of the line varies linearly from 298°K to T_{cold}. The bottom curve is the corrected curve for the FET noise temperature. At low temperature, thermal noise added from input circuit loss is less than 1°K and can be neglected.

The results shown in Figure 43a are remarkable. The noise decreases linearly as the ambient temerature drops from 300°K to 100°K. However, below 100°K, further decrease of the physical temperature has no effect upon the FET noise temperature. We expected a noise temperature composed of a non-thermal gate circuit noise, A_{gate}, plus a thermal gate circuit noise, $B_{gate}\ T_{Amb}$, plus drain thermal and non-thermal components, $\frac{A_{drain}}{g_m} + \frac{B_{drain}\ T_{Amb}}{g_m}$. The total minimum noise temperature dependence would be,

$$T_{min} = A_{gate} + B_{gate}\ T_{Amb} + \frac{A_{drain}}{g_m} + \frac{B_{drain}\ T_{Amb}}{g_m} \qquad \text{Eq. (53)}$$

If we assume g_m is constant with temperature for simplicity, then the above expression is the equation of a straight line. There should be no bend in the curve at 100°K. The above prediction of the noise dependence upon temperature does not take the temperature dependence of trap noise into account. In conclusion, the noise mechanism which determines the shape of this curve is not yet well understood. It should be noted that the measurements of Liechti and Larrick [24] at 12 GHz also exhibit a large decrease in noise temperature

between the physical temperatures of 300°K and 130°K and a much slower noise decrease between 130°K and 77°K.

The dependence of noise temperature upon real source impedance is demonstrated in Figure 43b. The large decrease in minimum noise temperature between ambient temperatures of 300°K and 150°K is apparent while only a small decrease occurs upon further cooling to 16°K. R_{opt} decreases from 75 Ω at 77°K to 40 Ω at 16°K.

The frequency dependence of the noise temperature and the gain at 300°, 77°, and 16°K is given in Figure 44. The noise vs. frequency curves for all three temperatures have their minimum at the same frequency. This signifies that X_{opt} is the same at all three temperatures. The measured noise data at 16°K and 77°K are almost identical. A 3 dB decrease in gain is suffered when the temperature drops to 16°K and 77°K from 298°K. The cause of this gain degradation should either be (1) a decrease in FET transconductance; (2) a worse input match; or (3) a worse output match. However, measurements of all of these quantities do not account for a 3 dB loss of gain. The measured input and output return loss for four different temperatures are shown in Figure 45. The input return loss decreases at lower temperature but not enough to account for the gain decrease. The change in input and output return loss is probably due to the change in output conductance with temperature. The return loss measurements, and the noise and gain measurements of Figure 44, were taken at the optimum noise source impedance and bias. The optimum bias change and the corresponding change in transconductance are small as temperature changes.

Figure 46a exhibits the change of transconductance with drain current at four temperatures. The transconductance increases as physical temperature decreases and all four curves display a decrease at low current (due to mobility degradation at the active layer-substrate boundary as discussed in section 4.6).

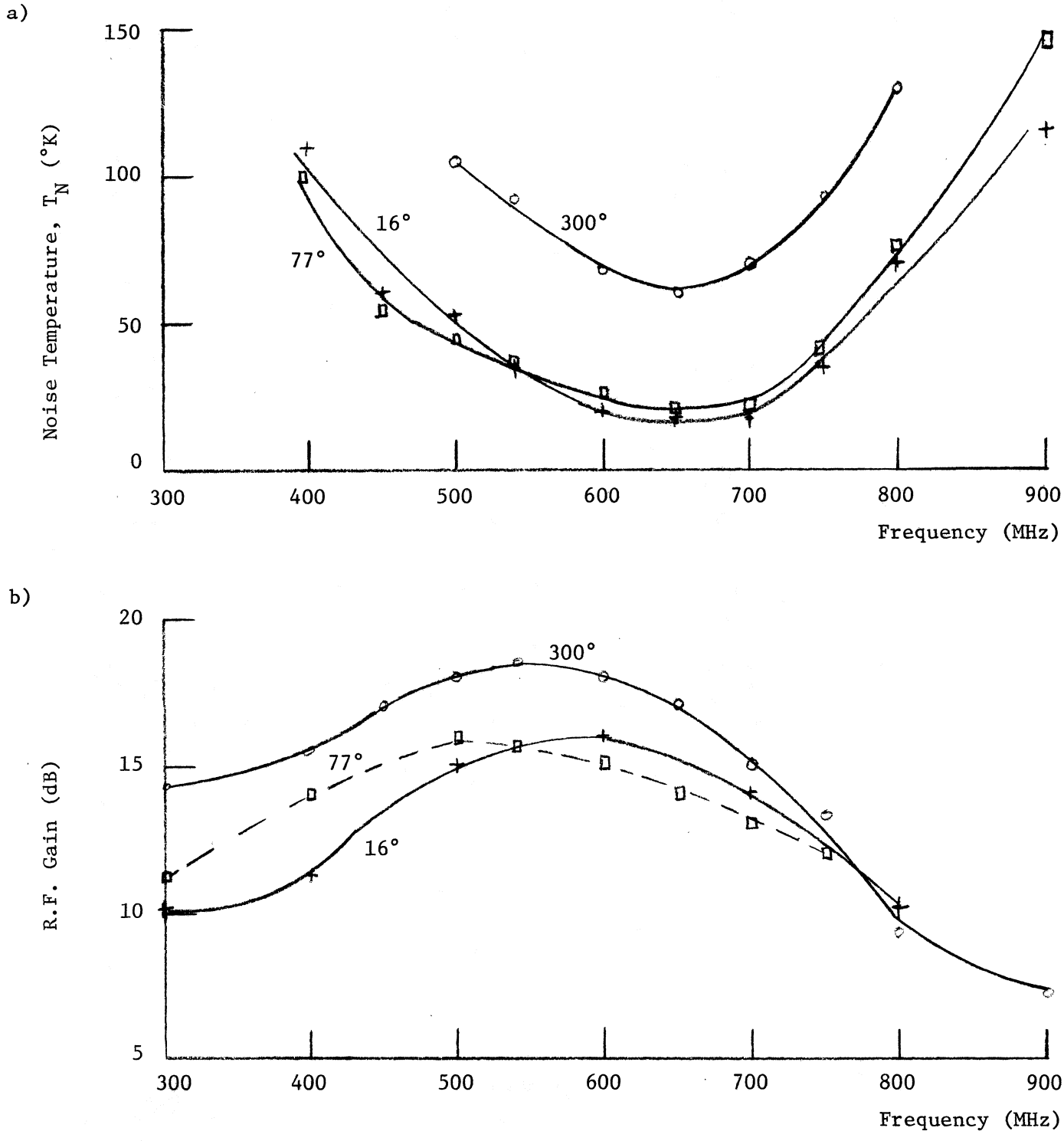
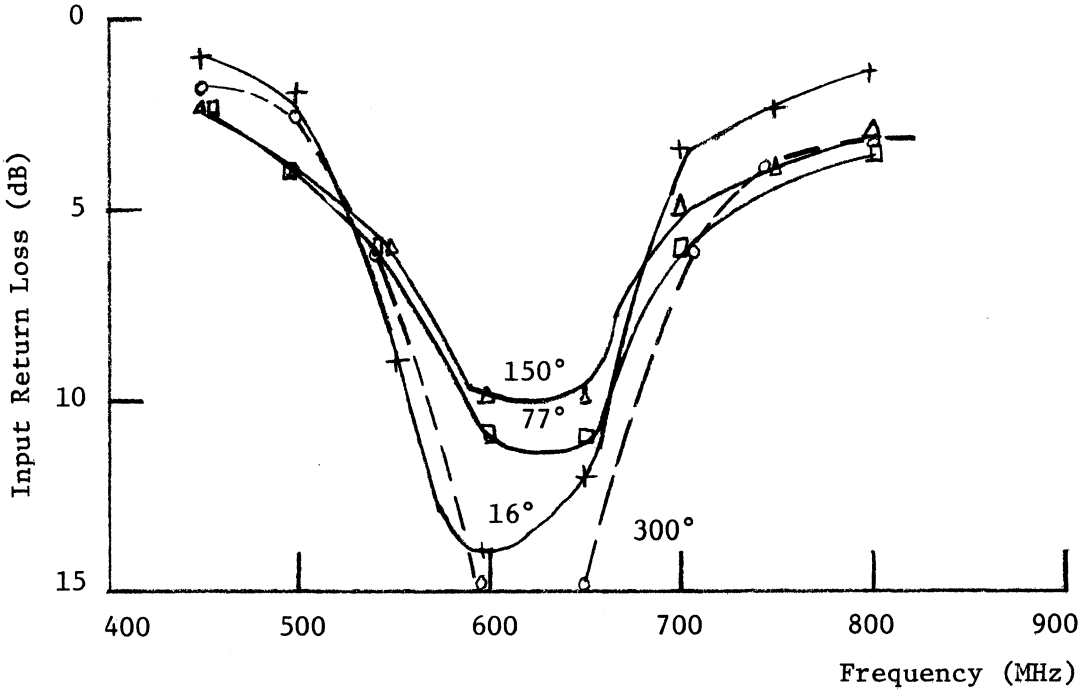


Figure 44. Noise temperature (a) and r.f. gain (b) versus frequency for chip #2 at room temperature, 77°, and 16°K.

a)



b)

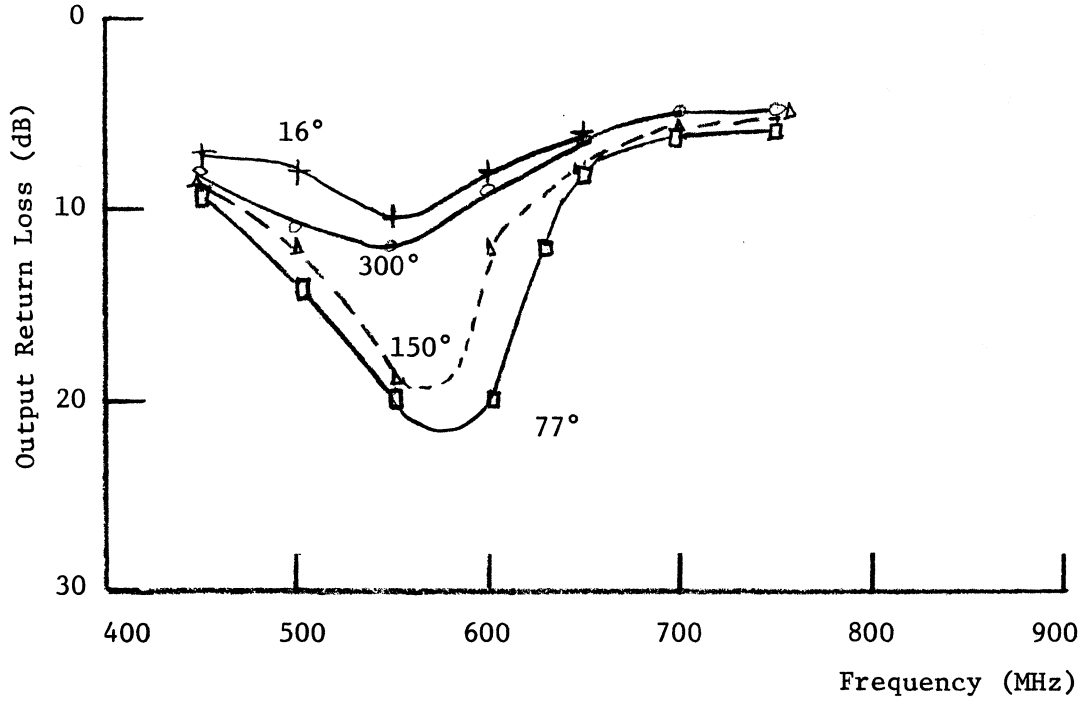


Figure 45. Input (a) and output (b) return loss versus frequency for chip #2 at temperatures of 16°, 77°, 150°, and 300°K.

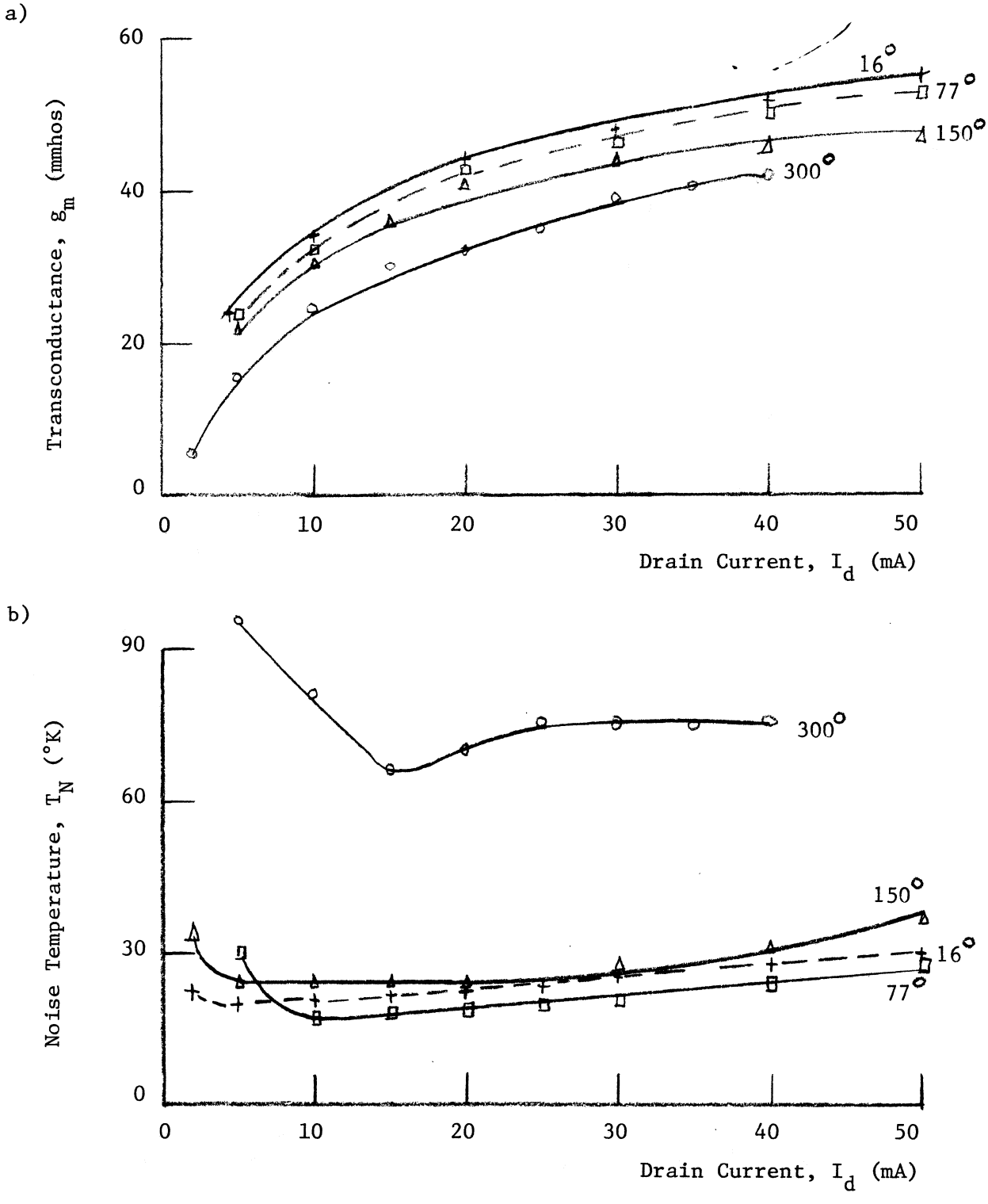


Figure 46. The above graphs demonstrate the drain current dependence of the transconductance (a) and the noise temperature (b) at 16°, 77°, 150°, and 300°K.

The corresponding increase in noise temperature (Figure 46b) at low drain current is not nearly as large at lowtemperature as it was at room temperature. This indicates that drain circuit noise being referred back to the input is no longer the dominant noise mechanism at temperatures below 150°K. The dominant noise generation has moved to the gate circuit at low physical temperatures.

Figure 47a shows how the d.c. current-voltage characteristics of the FET change with temperature. The d.c. saturation current at zero gate bias, I_{DSS}, increases by 50% (from 60 mA to 90 mA) when the FET is cooled to 16°K. This is partially due to the mobility increase at low temperature. One can observe that the output conductance of the FET (which is proportional to the I_d vs. V_D slope in the saturation region) increases as temperature decreases therefore causing the input and output matches to change (as seen in Figure 45). The current vs. temperature dependence at the typical low noise bias conditions for the FET is shown in Figure 47b. At this bias, the current increases by only 5 mA when the FET is cooled from 300°K to 37°K.

D.C. measurements of transconductance are plotted versus ambient temperature in Figure 48a for drain current held constant (15 mA) and for constant gate voltage (-1.2 V). Drain voltage is held constant and at room temperature $V_G = -1.2$ causes 15 mA of drain current. If gate voltage is held constant and temperature decreases, then the drain current increases above 15 mA. Therefore, the transconductance curve at constant gate bias is above the g_m curve at constant drain current since the transconductance increases with drain current. The transconductance curves can be compared with the theoretical mobility vs. temperature curves of Figure 48b. Two curves are given for n-type GaAs doped to $N_d = 5 \times 10^{16}$ cm^{-3} and $N_d = 4.5 \times 10^{17}$ cm^{-3}. The HFET-1000 has a dopant concentration of $N_d = 10^{17}$ cm^{-3}; therefore, the FET's mobility curve should lie somewhere between the two theoretical curves given. The curve with

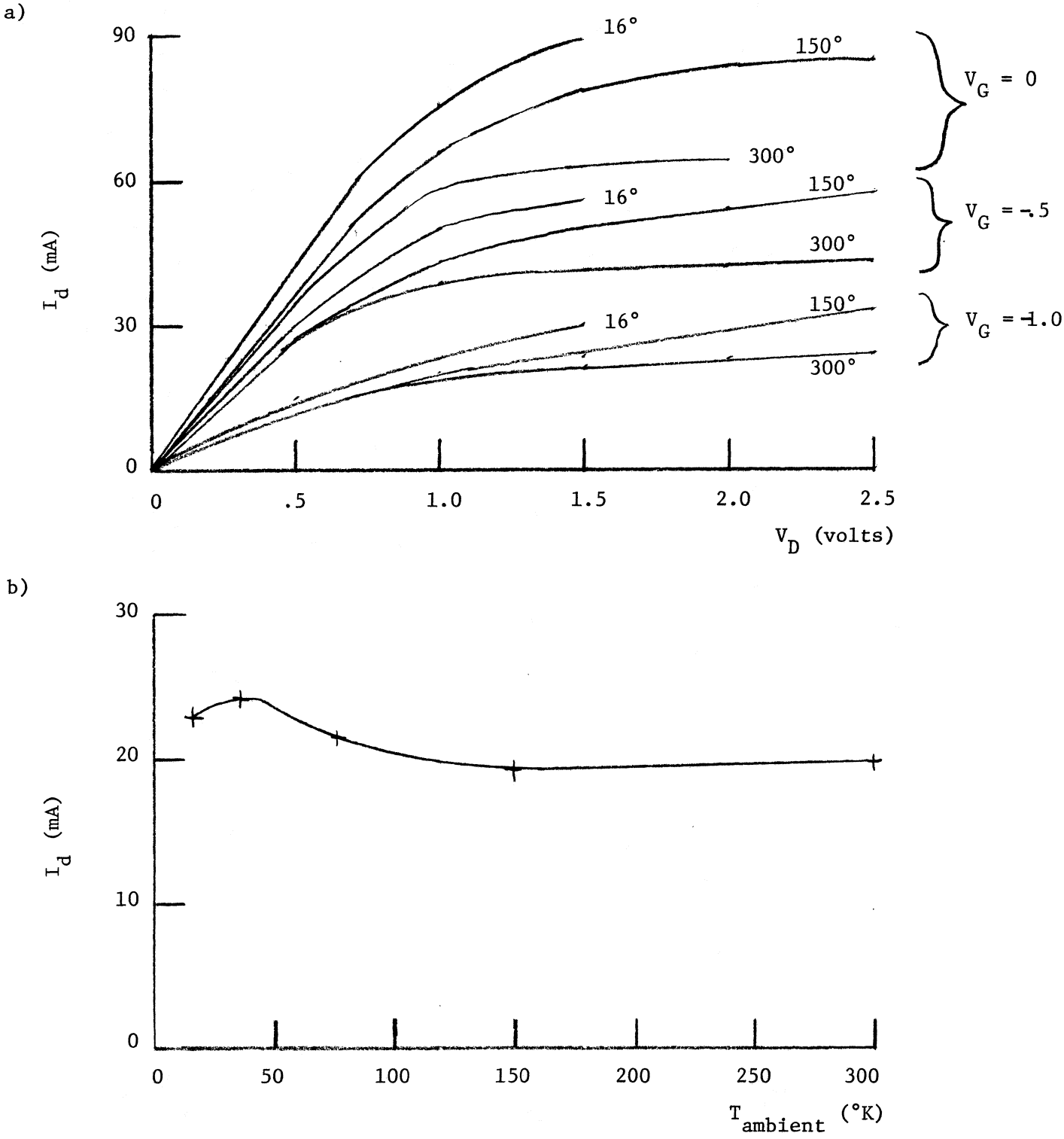


Figure 47. (a) The current-voltage characteristics of the FET change as temperature is decreased.
(b) Illustrates the increase in drain current at a typical low noise FET bias (V_d = 1.0 V, V_g = -1.0) as temperature decreases.

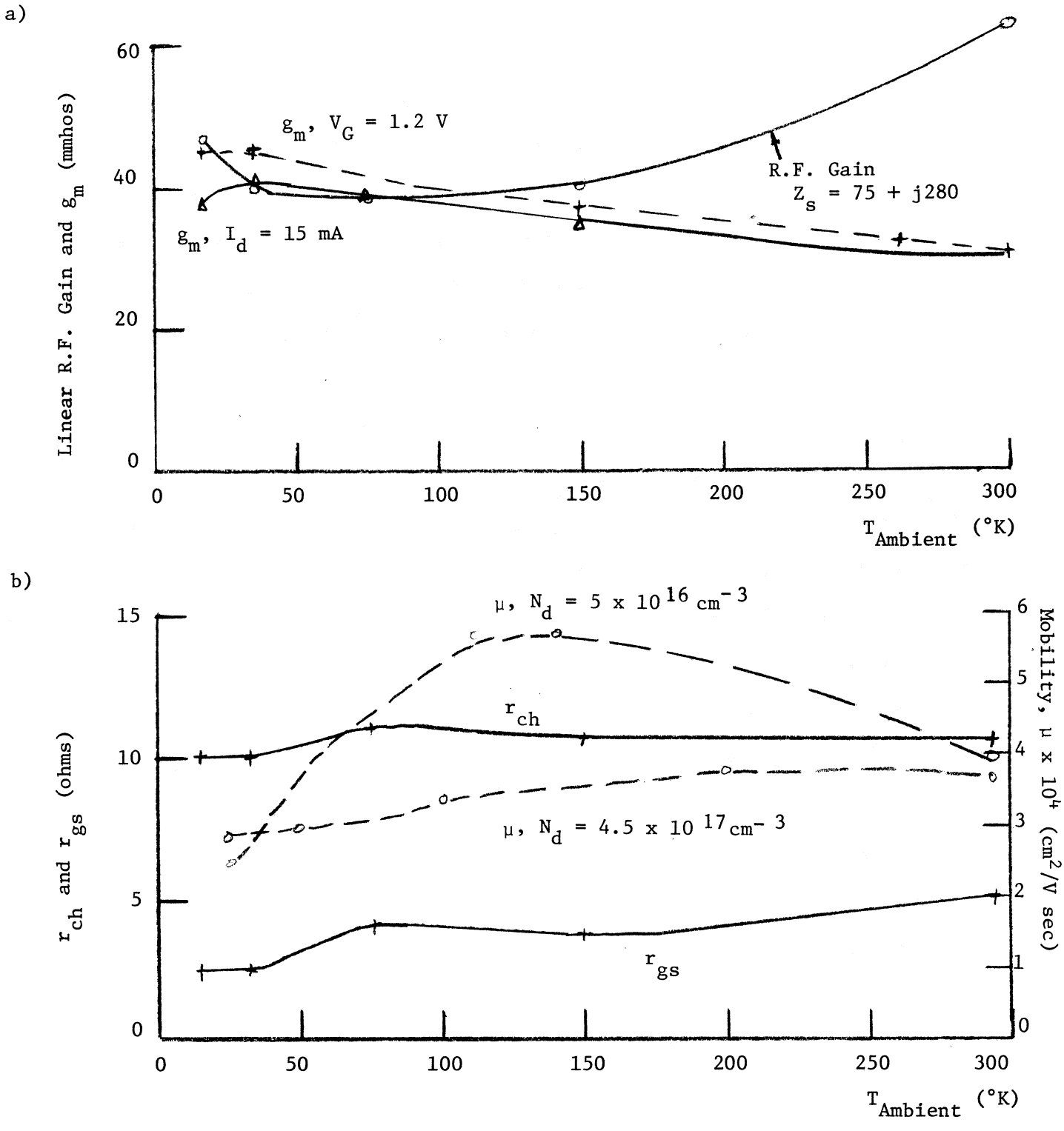


Figure 48. (a) The FET transconductance, g_m, is measured vs. temperature at constant gate voltage and drain current. Linear r.f. gain is also shown.
(b) Theoretical mobility at two doping levels and the channel and gate-to-source resistances are plotted vs. temperature.

$N_d = 5 \times 10^{16}$ cm^{-3} exhibits lattice scattering at higher temperatures ($\mu \propto T^{-3/2}$) and impurity scattering at low temperatures ($\mu \propto T^{3/2}$) but the curve with $N_d = 4.5 \times 10^{17}$ cm^{-3} shows very little temperature dependence. At this doping level the GaAs is almost degenerate. Comparing g_m and mobility, we find that the measured transconductance increases as temperature decreases similar to the more lightly doped theoretical curve. However, g_m does not start to decrease until T = 37°K, whereas the theoretical mobility decreases for T < 100°K.

Also shown in Figure 48a is the linear r.f. gain which is measured vs. temperature at a constant value of source impedance. Bias is optimized for noise performance, but this bias varies little with temperature. Again, we note the anamolous decrease in gain at low temperature although the transconductance is seen to increase.

The final temperature data to be reported are measurements of the channel and gate-to-source resistances (see Figure 42) vs. temperature given in Figure 48b. We had hoped to obtain information about the GaAs mobility from these measurements. The curves obtained show relatively little variation with temperature. Since g_m increases at low temperature, we expected r_{ch} and r_{gs} to decrease at low temperature. We conclude with the fact that all the temperature measurements made indicate that only small changes in mobility occur. Therefore, the FET mobility dependence upon temperature more closely resembles the $N_d = 4.5 \times 10^{17}$ cm^{-3} theoretical curve than the 5×10^{16} cm^{-3} data.

4.8 Conclusion

The goals of this research have been successfully reached. A method of FET parameter measurement at 600 MHz has been demonstrated and several GaAs FET chips have been analyzed. The test structure for noise parameter

measurement also meets the requirements of a radio astronomy front end amplifier. Noise temperatures for the amplifier of 60°K at room temperature and 17°K for T ≤ 100°K have been demonstrated at a frequency of 600 MHz. Using source inductive feedback, the input VSWR of the amplifier has been reduced to a value of 1.13. The amplifier output VSWR is less than 2.0 and could easily be reduced below 1.25 by further tuning. In this report, we have tried to consider all of the difficulties and engineering trade-offs associated with measuring the noise parameters of a GaAs MESFET at relatively low frequencies and building a 600 MHz low noise, well matched amplifier. Hopefully, this work will serve as a basis for further investigation of the GaAs FET's potential usefulness at frequencies below 1 GHz.

Acknowledgements

The author would like to thank the following people whose assistance made this work possible. Special thanks and gratitude is extended to Dr. Sander Weinreb of the National Radio Astronomy Observatory without whose direction and advice this research would not have been possible. I would also like to thank Dr. D. R. Decker, Dr. J. Granlund, Charles Pace and Dr. M. Pospieszalski of the National Radio Astronomy Observatory as well as Tim Forester, William Lum, and Dr. D. R. Williams of the University of California Radio Astronomy-Astronomy Department. Finally, I would like to express my appreciation to Carolyn Dunkle who typed this report.

APPENDIX A

REPRESENTATION OF NOISE

The noise characteristics of any noisy network can be completey described by four parameters. Any two port can be represented by several different equivalent circuits. The equivalent circuit of Rothe and Dahlke [11] uses the set of parameters R_N, G_N, and ρ where ρ is complex. This model states that any noisy two port can be represented by a series noise voltage source and a shunt noise current source followed by the same two port with all noise sources set equal to zero. See Figure 49.

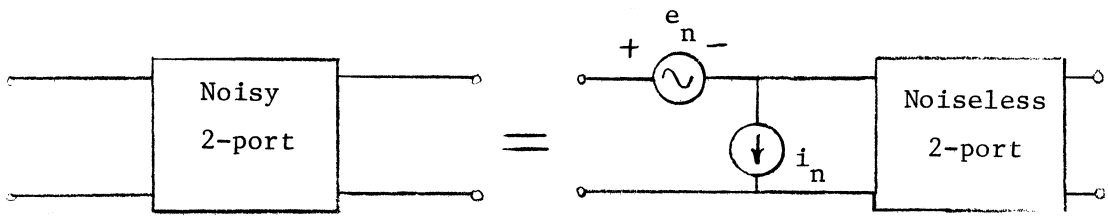


Figure 49. Rothe-Dahlke noise equivalent circuit for a noisy two-port.

In general, the noise voltage and current sources, e_n and i_n, are partially correlated, this correlation being described by the parameter ρ

$$\rho = \frac{\overline{e_n^* i_n}}{\left[\overline{|e_n|^2}\ \overline{|i_n|^2}\right]^{1/2}} \qquad \text{Eq. (54)}$$

Often the noise generators in the equivalent circuit are described by the equivalent noise resistance, R_N, and the equivalent noise conductance, G_N, which are described by:

$$R_N = \frac{\overline{|e_n|^2}}{4K\ T_0\ \Delta f} \qquad G_N = \frac{\overline{|i_n|^2}}{4K\ T_0\ \Delta f} \qquad \text{Eq. (55)}$$

Therefore, a resistor of value R_N and temperature T_0 would generate a voltage noise equivalent to $\overline{|e_n|^2}$. Likewise, a resistor with conductance G_N will generate a current noise equivalent to $\overline{|i_n|^2}$ (mean squared values).

A more convenient set of noise parameters to obtain from measurements are T_{min}, the minimum noise temperature of the two port, Z_{opt}, the complex source impedance at which the noise temperature of the device is equal to T_{min}, and either R_N or G_N as previously described. In this report, G_N is usually used. The dependence of the amplifier's noise temperature, T_N, upon the source impedance seen at the input of the two port, Z_s, was given in equation 29 and is repeated below.

$$T_N = T_{min} + \frac{G_N\ T_0}{R_s} \left|Z_s - Z_{opt}\right|^2$$

$$= T_{min} + \frac{G_N\ T_0}{R_s} \left[(R_s - R_{opt})^2 + (X_s - X_{opt})^2\right]$$

where $Z_s = R_s + jX_s$

$Z_{opt} = R_{opt} + jX_{opt}$

$T_0 = 290°K$

One may obtain T_{min} and Z_{opt} by varying the source impedance until a minimum is obtained. The noise temperature at this minimum will be equal to T_{min} and the source impedance is equal to Z_{opt}. The fourth parameter, G_N, must be obtained from a measurement of T_N at a source impedance different from Z_{opt}. Then, using equation 29, one can calculate a value for G_N since all the other elements in the equation are known.

The parameters R_N and ρ ($\rho = \rho_r + j\rho_i$) can be calculated using

$$R_N = G_N \left|Z_{opt}\right|^2 \qquad \text{Eq. (56)}$$

$$\rho_i = \frac{X_{opt}}{\left|Z_{opt}\right|} \qquad \text{Eq. (57)}$$

$$\rho_r = \frac{T_{min}}{2T_0 \sqrt{R_N G_N}} - \sqrt{1 - \left(\frac{X_{opt}}{\left|Z_{opt}\right|}\right)^2} \qquad \text{Eq. (58)}$$

Once the above measurements and calculations are performed, two complete noise descriptions of the two port have been obtained.

APPENDIX B

MEASUREMENT TECHNIQUES

The measurement techniques described in this appendix will be those used during the 600 MHz amplifier tests.

B.1 Noise Measurements

Noise temperature measurements are made by terminating the input of the device under test with a hot load and a cold load. Following the device under test is a second stage which boosts the noise signal to a detectable level. This signal is detected by a receiver which displays a number of proportional to the input power. Figure 50 illustrates the measurement setup.

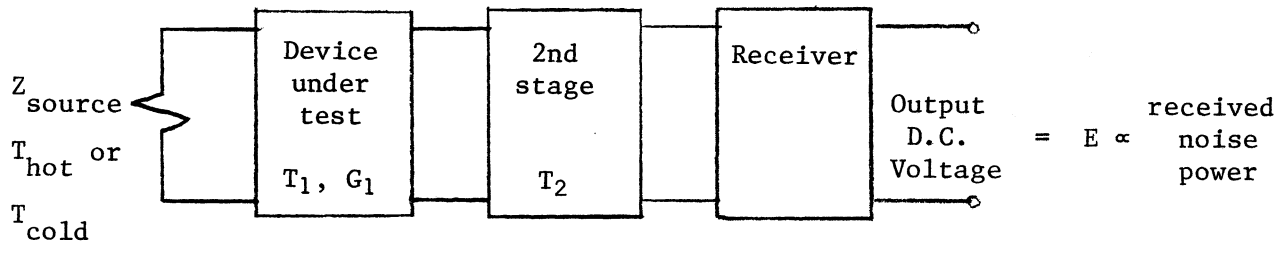


Figure 50. Hot-cold load noise measurement block diagram.

The hot load is normally a 50 Ω termination at room temperature. The cold load is a 50 Ω termination in a styrofoam bucket into which liquid nitrogen is poured. Hence $T_H = 298°K$, $T_c = 80°K$. A cold temperature of 80°K is used although the actual physical temperature of the load is 77°K. This is because small but finite losses exist in the stainless steel transmission line which connects to the load within the styrofoam bucket. From previous measurements and experience, we know that these losses increase the effective noise temperature of the cold load to 80°K. Appendix E provides a derivation of this added noise caused by an attenuator following the cold load.

E_{H1} = receiver output for hot load

E_{C1} = receiver output for cold load

$$E_{H1} = G(T_H + T_{12}) \qquad \text{Eq. (59)}$$

$$E_{C1} = G(T_C + T_{12}) \qquad \text{Eq. (60)}$$

G = total system gain from input to output

T_{12} = cascaded noise temperature of system

$$T_{12} = T_1 + \frac{T_2}{G_1} \qquad \text{Friis' formula} \qquad \text{Eq. (61)}$$

T_1 = noise temperature of device under test

G_1 = gain of device under test

T_2 = cascaded noise temperature of second stage and receiver

$$G = \frac{E_{H1} - E_{C1}}{T_H - T_C} \qquad \text{Eq. (62)}$$

$$T_{12} = \frac{E_{C1}}{G} - T_C = E_{C1}\left(\frac{T_H - T_C}{E_{H1} - E_{C1}}\right) - T_C = \frac{T_H - Y_1 T_C}{Y_1 - 1} \qquad \text{Eq. (63)}$$

where $Y_1 = \frac{E_{H1}}{E_{C1}}$

In order to find T_1 from T_{12}, G_1 and T_2 must be known. Equations 59 and 60 can be rewritten in the form,

$$E_{H1} = [G_1(T_1 + T_H) + T_2]\, K \qquad \text{Eq. (64)}$$

$$E_{C1} = [G_1(T_1 + T_C) + T_2]\, K \qquad \text{Eq. (65)}$$

K = gain of system excluding the first stage.

If the first stage is removed, and hot and cold loads are applied to the input of the second stage, we obtain

$$E_{H2} = K\,(T_2 + T_H) \qquad \text{Eq. (66)}$$

$$E_{C2} = K\,(T_2 + T_C) \qquad \text{Eq. (67)}$$

By the same algebra which obtained equation 63

$$T_2 = \frac{T_H - Y_2 T_C}{Y_2 - 1} \qquad Y_2 = \frac{E_{H2}}{E_{C2}} \qquad \text{Eq. (68)}$$

Hence, T_2 can be found from measurement.

$$E_{H1} - E_{C1} = G_1 K (T_H - T_C) \qquad \text{Eq. (69)}$$

$$E_{H2} - E_{C2} = K (T_H - T_C) \qquad \text{Eq. (70)}$$

$$\therefore \; G_1 = \frac{E_{H1} - E_{C1}}{E_{H2} - E_{C2}} \qquad \text{Eq. (71)}$$

Therefore, T_1, T_2, and G_1 can be found from four measurements of E_{H1}, E_{C1}, E_{H2}, and E_{C2}.

The second stage used in these noise measurements was an Avantek AK-1000M-28 with a 500-1000 MHz bandwidth, 30 dB gain, and 260°K noise temperature. G_1 was generally close to 18 dB; hence the second stage provided a noise addition to T_{12} of about 5°K.

The receiver used was the automatic noise figure meter front end built by the National Radio Astronomy Observatory. It basically consists of a mixer which up-converts the 600 MHz noise input signal to 1 GHz followed by another mixer which down-converts the 1 GHz signal to an I.F. frequency of 30 MHz with a 10 MHz bandwidth. There are several stages of variable gain and attenuation followed by a square law detector. Therefore, instead of looking at exactly 600 MHz noise, we see 595 to 605 MHz noise.

Another noise measuring device was used for optimization of FET bias or source impedance. The block diagram of the measurement setup is shown in Figure 51. The noise temperature meter modulates the noise diode on and off. When off, the device under test sees the 30 dB pad which looks like a 50 Ω resistor at room temperature. When the diode is on, the effective input noise temperature is $T_{ambient} + T_{diode}$. Therefore, the power meter reads a value $S + C = G (T_{12} + T_{amb} + T_{diode})$ with the noise diode on. When the diode is

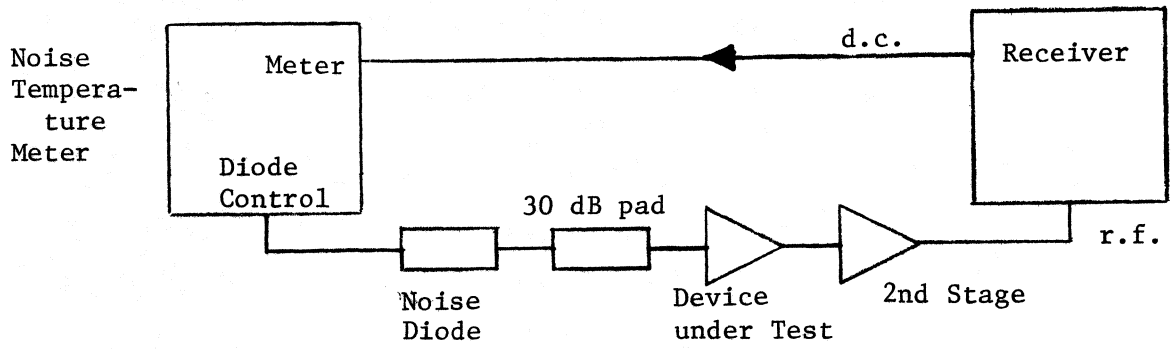


Figure 51. Block diagram for FET bias or impedance optimization using a noise diode and the noise temperature meter.

off, the meter reads $S = G\ (T_{12} + T_{amb})$. S and S + C are proportional to the noise power detected by the receiver and G is the total gain. Analog subtraction and division circuits within the meter then calculate $C = GT_{diode}$ and

$$t = \frac{S}{C} = \frac{T_{12} + T_{amb}}{T_{diode}} \qquad \text{Eq. (72)}$$

The quantity, t, varies linearly with T_{12}; therefore, optimization of FET bias and source impedance can be easily achieved by varying these parameters until t, as displayed on the noise meter, is minimized.

B.2 Gain and Return Loss

Another method of measuring gain consists of measuring the swept frequency power level before and after the device under test is inserted into the R.F. circuit path. Usually attenuation is inserted at the same time as the device under test to obtain a fairly constant power level. Too little power leads to inaccurate measurement. Too much power will cause the detector to deviate from square law operation. Less than -10 dBm of power is desirable at the detector. A typical gain measurement setup is shown in Figure 52.

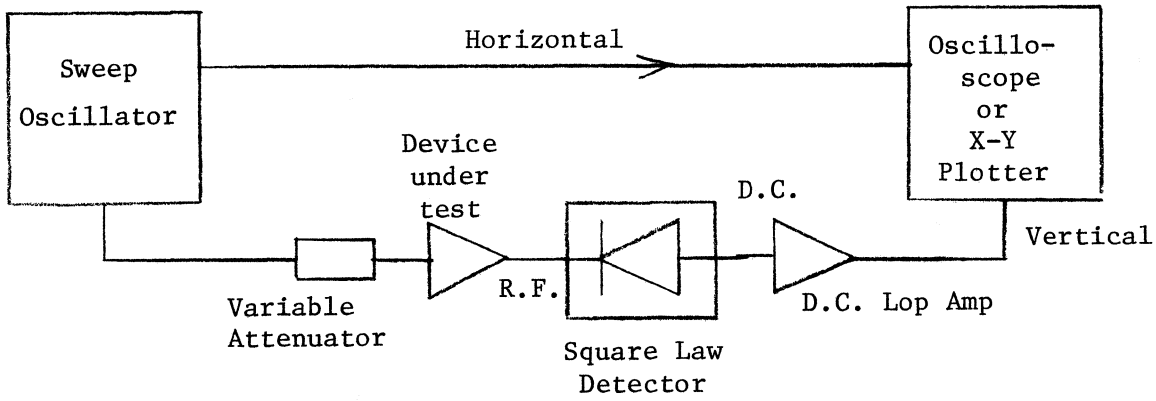


Figure 52. Block diagram for gain measurements.

Both input and output return loss are measured using a Wiltron reflectometer bridge. Return loss is defined to be

$$RL\ (dB) = 10 \log_{10} \frac{P_{out}}{P_{in}} = 20 \log_{10} (\Gamma_{in}) \qquad \text{Eq. (73)}$$

The system used to measure input return loss is illustrated below in Figure 53. To measure output return loss, the input of the device under test is terminated in 50 Ω and the output is connected to the reflectometer.

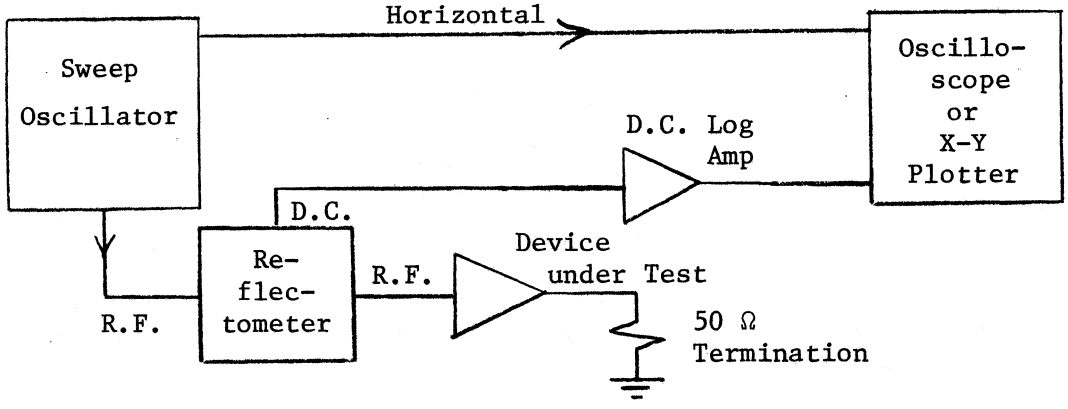


Figure 53. Block diagram for input return loss measurements.

B.3 Impedance Measurements

Measurements of inductor impedances, transmission line impedance, etc., were made using the Hewlett-Packard network analyzer test system shown in Figure 54.

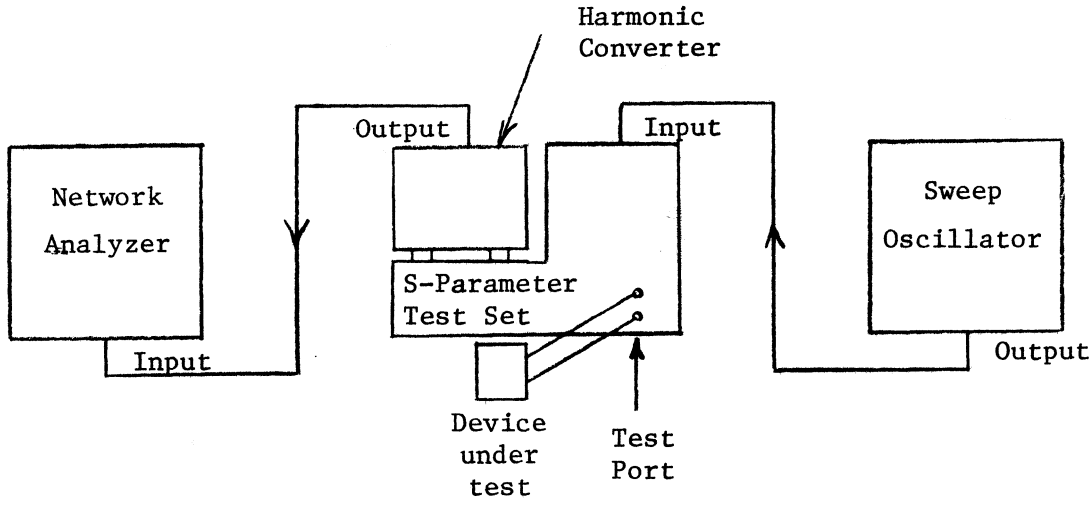


Figure 54. Block diagram of the Hewlett-Packard network analyzer system used for impedance vs. frequency measurements.

Measurements of the quarter wave transformer impedance transformation was achieved by terminating the input with 50 Ω. The amplifier circuit board is removed and a piece of semi-rigid 50 Ω coax is fitted through the hole at the amplifier end of the transmission line and the two center conductors are soldered together. The reference plane is changed until it coincides with this solder joint. Good ground contact between the amplifier block and the semi-rigid coax is essential. We are then ready to measure Z_s versus frequency at this plane.

APPENDIX C

COMPUTER PROGRAMS

The following two programs, written in BASIC, were often used during the course of this research.

Program 1 calculates the four noise parameters T_{min}, R_{opt}, X_{opt}, and G_N when four noise temperatures measured at four source impedances are used as the inputs.

```
10 REM PROGRAM TO CALCULATE FET NOISE PARAMETERS FROM MEASURED DATA.
20 DIM R[4],X[4],Q[4],A[4,4],B[4,4],T[4]
30 FOR K=1 TO 4
40 DISP "ENTER T("K")";
50 INPUT T[K]
60 DISP "ENTER R("K")";
70 INPUT R[K]
80 DISP "ENTER X("K")";
90 INPUT X[K]
100 NEXT K
110 PRINT "TEMP MATRIX EQUALS";T[1],T[2],T[3],T[4]
120 PRINT "RESISTANCE MATRIX EQUALS";R[1],R[2],R[3],R[4]
130 PRINT "REACTANCE MATRIX EQUALS";X[1],X[2],X[3],X[4]
140 FOR L=1 TO 4
150 A[L,1]=1
160 A[L,2]=290/R[L]
170 A[L,3]=(R[L]↑2+X[L]↑2)*290/R[L]
180 A[L,4]=-2*X[L]*290/R[L]
190 NEXT L
200 PRINT "A MATRIX EQUALS"
210 MAT PRINT A
220 MAT B=INV(A)
230 PRINT "B MATRIX EQUALS"
240 MAT PRINT B
250 MAT Q=B*T
260 PRINT "Q MATRIX EQUALS";Q[1],Q[2],Q[3],Q[4]
270 REM R=ROPT X=XOPT T=TMIN G=GN
280 PRINT "R=ROPT X=XOPT T=TMIN G=GN"
290 G=Q[3]
300 X=Q[4]/G
310 R=(Q[2]/G-X↑2)↑0.5
320 T=Q[1]+2*G*R*290
330 PRINT "TMIN="T,"ROPT="R,"XOPT="X,"GN="G
340 END
```

Program 2 uses the four noise parameters T_{min}, R_{opt}, X_{opt}, and G_N as inputs. They are obtained directly from experiment with the 600 MHz amplifier. The program then calculates noise parameters used in other types of noise descriptions. The noise resistance, R_N, the real and imaginary parts of the correlation coefficient, ρ, the real and imaginary parts of the correlation impedance, Z_{cor}, and the noise resistance, r_n, used by Pucel, et al. are all calculated by program 2 given below.

```
10 PRINT "FET PARAMETER CALCULATION PROGRAM"
20 DISP "TMIN EQUALS";
30 INPUT T
40 DISP "ROPT EQUALS";
50 INPUT R
60 DISP "XOPT EQUALS";
70 INPUT X
80 DISP "GN EQUALS";
90 INPUT G
100 PRINT "TMIN="T;"ROPT="R;"XOPT="X;"GN="G;
110 R1=G*(R↑2+X↑2)
120 PRINT "RN="R1
130 P1=X/(R↑2+X↑2)↑0.5
140 PRINT "PI="P1
150 P2=T/(2*(R1*G)↑0.5*290)-(1-P1↑2)↑0.5
160 PRINT "PR="P2
170 REM NOW WE HAVE CALCULATED RN, GN, PI, PR
180 R2=P2*(R1/G)↑0.5
190 PRINT "RCOR="R2
200 X1=-P1*(R1/G)↑0.5
210 PRINT "XCOR="X1
220 REM NOW COMPUTE RN FROM PUCEL THEORY ALSO USED IN ROTHE-DALKE PAPER
230 R3=R1*(1-(P1↑2+P2↑2))
240 PRINT "PUCEL RN="R3
250 END
```

APPENDIX D

HANDLING AND SOLDERING FET CHIPS

The dominant mechanism of FET destruction is due to static discharge from humans or instruments to the gate. A large negative static charge will create a strong electric field at the Schottky barrier capable of breaking down or burning out the gate. The result is usually seen as a FET with very little gate control. To prevent this from occurring, the tweezers used to manipulate the FET should always be grounded to a large metal object to prevent static buildup. Once the FET is mounted in the amplifier, it still must be protected. When the amplifier is not in use, the drain, gate, and ground leads are connected together and 50 Ω loads are placed on the input and output RF connectors.

Excessive heat will permanently damage the FET; therefore, low temperature solders (such as indium) are preferable. The FET should not experience temperatures over 320°C for more than 30 seconds.

The most successful method of soldering the FET chips to the rivets used the following technique:

1) A small chip of indium solder is cut and laid on the rivet along with a tiny amount of non-corrosive flux.
2) The rivet is current conduction heated slowly until the solder melts.
3) The chip is pressed into the solder with a micropositioner-held microscope slide.
4) Water is squirted on the rivet for rapid cooling.
5) The FET is cleaned in a solvent bath to remove flux and other contaminants.

APPENDIX E

ANALYSIS OF THE EFFECTIVE TEMPERATURE OF A 50 Ω LOAD FOLLOWED BY A LOSSY 50 Ω TRANSMISSION LINE WHOSE TEMPERATURE VARIES LINEARLY WITH LENGTH [42]

First, the simpler problem of a load followed by an attenuator is considered. Let T_L = load temperature, T_A = attenuator temperature, L = loss of attenuator = $\frac{P_{in}}{P_{out}}$. We will find the equivalence shown in Figure 55. i.e., what is the effective noise temperature of a resistor at temperature T_L followed by an attenuator at temperature T_A.

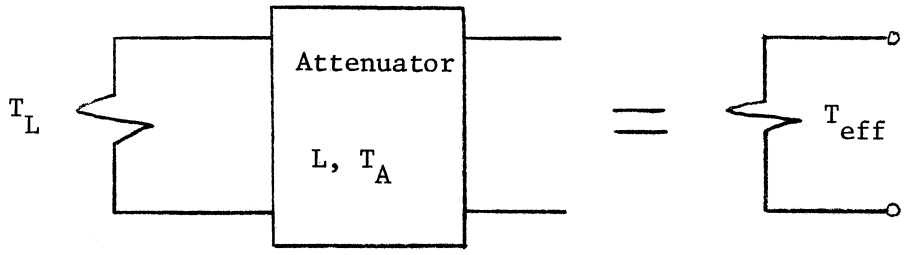


Figure 55. Noise equivalence of a resistor followed by an attenuator.

If the attenuator and load are both at temperature T_A, then the noise available power added by the attenuator equals the total available noise power of a resistive network at T_A minus the noise contributed by the load.

$$\text{Noise added by attenuator} = KT_A - KT_A \frac{1}{L} = KT_A \left(1 - \frac{1}{L}\right) \qquad \text{Eq. (74)}$$

But the noise added by the attenuator is independent of load temperature, hence

$$K\,T_{eff} = \text{total noise power} = KT_L \frac{1}{L} + KT_A \left(1 - \frac{1}{L}\right)$$

$$T_{eff} = \frac{T_L}{L} + \left(1 - \frac{1}{L}\right) T_A \qquad \text{Eq. (75)}$$

Now we must consider the problem of distributed loss along a transmission line which is cold at one end, hot at the other, and whose temperature variation is assumed to be linear. See Figure 56.

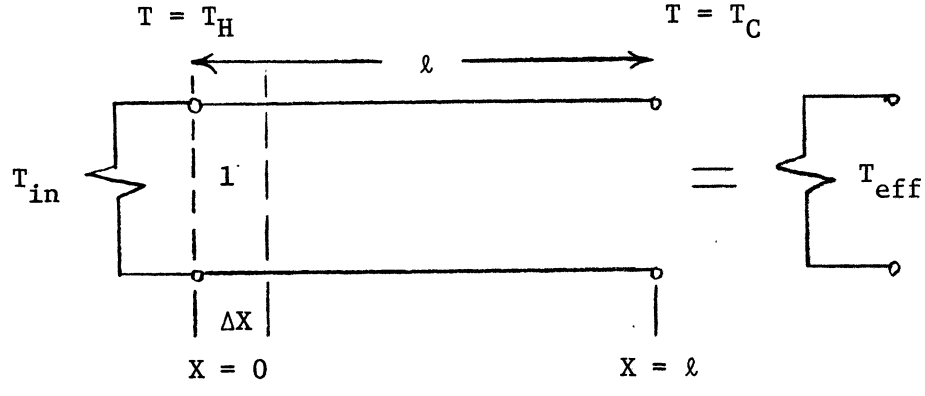


Figure 56. Noise equivalence of a resistor followed by a lossy matched transmission line whose temperature varies linearly from T_H to T_C.

It is assumed that the input load and the transmission line are at the same impedance.

ℓ = length of transmission line

L = loss per unit length in dB

L_{tot} = total loss of line in dB = $L\ell$

T_{in} = temperature of load on input of line

T_H = temperature of transmission line end closest to load

T_C = temperature of transmission line end closest to output

T_{eff} = effective noise temperature looking into output terminals of transmission line.

For the first incremental length of the transmission line as shown in Figure 56,

$$L_1 \text{ (dB)} = L\Delta x \text{ (dB)} \quad \text{or} \quad L_1 \text{ (linear)} = 10^{\frac{L\Delta x}{10}} \qquad \text{Eq. (76)}$$

$T_1(\Delta x)$ = effective noise temperature at $x = \Delta x$

$$= T_{in}\, 10^{-\frac{L\Delta x}{10}} + \left(1 - 10^{-\frac{L\Delta x}{10}}\right) T_p\left(\frac{\Delta x}{2}\right) \qquad \text{Eq. (77)}$$

$T_p(x)$ = physical temperature of transmission line at position

$$= T_H + (T_C - T_H)\frac{x}{L} \qquad \text{Eq. (78)}$$

$$T_n\,(n\Delta x) = T_{n-1}\, 10^{-\frac{L\Delta x}{10}} + \left(1 - 10^{-\frac{L\Delta x}{10}}\right) T_p\left\{(n - 1/2)\Delta x\right\} \qquad \text{Eq. (79)}$$

Expand a^x:

$$a^x = 1 + x\ell na + \ldots \qquad \text{Eq. (80)}$$

$$a = 10^{x} = {}^{-L\Delta x}_{10} \qquad 10^{-\frac{L\Delta x}{10}} = 1 - \frac{L\Delta x}{10}\,\ell n10 = 1 - L'\Delta x \qquad \text{Eq. (81)}$$

where $L' = \dfrac{L\ \ell n\ 10}{10}$

We ignore higher order terms of Δx since later on we take the limit as $\Delta x \to 0$.

$$T_n\ (n\Delta x) = T_{n-1}\ (1 - L'\Delta x) + (1 - 1 + L'\Delta x)T_p\left\{(n - 1/2)\ \Delta x\right\} \qquad \text{Eq. (82)}$$

$$\Delta T = T_n - T_{n-1} = -T_{n-1}\ L'\Delta x + L'\Delta x\ T_p\ \left\{(n - 1/2)\ \Delta x\right\} \qquad \text{Eq. (83)}$$

$$\frac{\Delta T}{\Delta x} = -T_{n-1}\ L' + L'\ T_p\ [(n - 1/2)\ \Delta x] \qquad \text{Eq. (84)}$$

$$\lim_{\Delta x \to 0} \frac{\Delta T}{\Delta X} = \frac{dT}{dx} = -T(x)\ L' + L'\ T_p(x) \qquad \text{Eq. (85)}$$

The integrating factor for a first order differential equation of the general form $\dfrac{dy(x)}{dx} + p(x)\ y(x) = q(x)$ is

$$\exp\left[\int_0^x p(x')\ dx'\right]. \qquad \text{For our problem} \quad p(x') = L'$$

$$\exp\left[\int_0^x L'\ dx'\right] = \exp L'x \qquad \text{Eq. (86)}$$

Multiplying equation 85 by exp L′x, we obtain

$$L' T_p(x) \exp (L'x) = \left[\frac{dT(x)}{dx} + T(x) L'\right] \exp (L'x)$$

$$= \frac{d}{dx} \left\{T(x) \exp (L'x)\right\} \qquad \text{Eq. (87)}$$

Integrating both sides of this perfect differential:

$$T(x) \exp (L'x) = \int_0^x L'T_p(x') \exp (L'x') dx' + \text{constant} \qquad \text{Eq. (88)}$$

Evaluate the constant using the boundard conditions at x = 0, $T(x=0) = T_{in}$.

$$T_{in} \exp (L'0) = \int_0^0 L'T_p(x') \exp (L'x') dx' + \text{constant} \qquad \text{Eq. (89)}$$

$$\text{Constant} = T_{in}$$

$$T(x) = \exp (-L'x) \int_0^x L'T_p(x') \exp (L'x') dx' + T_{in} \exp (-L'x)$$

Eq. (90)

If T_p = constant, we obtain

$$T_{eff} = T(\ell) = \exp (-L'\ell) L'T_p \frac{1}{L'} [\exp (L'\ell) - 1]$$

$$+ T_{in} \exp [-L'\ell]$$

$$T_{eff} = T_p \left[1 - \exp \left\{\frac{-\ell n\ 10}{10} L_{tot}\ (dB)\right\}\right]$$

$$+ T_{in} \exp \left[\frac{-\ell n\ 10}{10} L_{tot}\ (dB)\right] \qquad \text{Eq. (91)}$$

From numerical calculations, we find that equations 75 and 91 produce the same result for T_{eff} as expected.

Now if we let the temperature vary as in equation 78, we obtain

$$T(x) = \exp\left(-L\,\frac{\ell n\ 10}{10}x\right)\int_0^x L\,\frac{\ell n\ 10}{10}\left[T_H + (T_C - T_H)\,\frac{x'}{\ell}\right] \exp\left(L\,\frac{\ell n\ 10}{10}\,x'\right)\,dx' + T_{in}\exp\left(-L\,\frac{\ell n\ 10}{10}\,x\right) \qquad \text{Eq. (92)}$$

$$T_{eff} = T_H\left\{1 - \exp\left[-.23\ L_{tot}\ (dB)\right]\right\} + \frac{(T_C - T_H)\,e^{-.23\ L_{tot}}}{.23\ L_{tot}\ (dB)}\left\{e^{.23\ L_{tot}}(.23\ L_{tot} - 1) + 1\right\} + T_{in}\exp\left(-.23\ L_{tot}\right) \qquad \text{Eq. (93)}$$

where L_{tot} is in dB.

Calculations show that close numerical agreement is found between the value of T_{eff} obtained from equation 93 and that obtained from equation 75 using the average of the two end temperatures, $\frac{T_H + T_C}{2}$, as the attenuator temperature. This is true when only small losses in the line are present (e.g., L_{tot} = .2 dB). As the loss in the line increases, the approximate and exact analysis of T_{eff} will diverge since the loss appears in the exponential of the exact analysis.

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