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CORRECTABLE SUBREFLECTOR CONTROLLER

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1.0 INTRODUCTION

The Correctable Subreflector is a device engineered to compensate for position dependent distortion in the main reflector of the NRAO 140-foot telescope. Accurate deformation of the subreflector surface is required to achieve this correction. This report describes the electronics and electro-mechanical system used to achieve this accurate deformation. An Engineering Division report which describes the mechanical aspects of the subreflector complements this report.

First, a block diagram system description is presented. This is followed by the system specifications. Functional descriptions of each of the subsystems are then given. Loop dynamics of the position servos are discussed. Finally, a number of appendices contain further detail on various items discussed in the text of this report.

2.0 SYSTEM BLOCK DIAGRAM DESCRIPTION

Figure 1 shows a block diagram of the system covered in this report. The actuators are commanded by digital words that originate either in the H-316 computer or on digiswitches. A data acquisition system in the focus electronics informs the control room electronics of the status of various things at the focus. The block diagram is discussed in detail below.

The Mode Select Switch dictates whether position commands for the actuators originate in the H-316 computer or on the Manual Position Command Switches. In the computer mode, the H-316 outputs position data, in parallel, to the Computer Interface. The Computer Interface signals the Interface Controller when it has received a complete set of position commands. Under control of the Interface Controller, position commands are shifted from the Computer Interface

to the Interface Controller. When the Interface Controller has the complete set of position commands, it signals the Up-Link Controller which compares each command with the electronic limit. The Up-Link Controller simultaneously channels data to the Formatter which appropriately groups the commands and the results of the magnitude comparisons, and sends them to the Decoder in the Focus Box.

In manual mode, the actuator positions are controlled by digiswitches on the Correctable Subreflector Digital Interface. When the Update Enable Switch is pressed, the Up-Link Controller tests the commands against the electronic limit and senses the position of the Update Select Switch. All this information is channeled to the Formatter which groups it appropriately and sends it to the Decoder in the Focus Box.

In either computer or manual mode, the Focus Box Decoder receives data from the Control Room Formatter. For each position command, the Decoder looks at a transmitted bit which tells it whether the command should be given to the Servo. This bit depends on the magnitude comparison done by the Up-Link Controller and, in manual mode, on the Update Select Switch. If the command is to be given to the Servo, the Decoder does so. The Position Servo drives the Actuator to null the difference between the commanded position and the position sensed by the Position Transducer.

Data flow from the focus to the control room is independent of the mode of operation. It is obtained and manipulated in the following manner. The Data Acquisition Subsystem digitizes six analog quantities: the temperature, the sum of the loop errors, and the four actuator positions obtained from the position transducers. These digital words are formatted and transmitted to the Decoder for display on the Digital Interface front panel. The Data Acquisition Subsystem also detects two error conditions. The first of these is a lock error

which is flagged if the digitized value for the sum of the lock errors differs from zero by more than one bit. The second is temperature. If the digitized value of temperature is not within certain limits, or if the heater controller signals a temperature error, a temperature error is flagged. Both of these error conditions are transmitted via the Decoder to the Display where red LED's and, in the case of a temperature error, an audible alarm signal the error conditions.

The H-316 control computer receives some information from the Digital Interface, via the Computer Interface. This includes the state of the Computer/Manual Switch, the electronic limit, and the lock and temperature error status.

A heater is included in the focus box. Its function is to limit the temperature range to which the electronics are subjected, thus improving positioning accuracy. It is used when the free air temperature is less than 20°C and maintains temperature within the box at about 25°C. The heater also alerts the Data Acquisition system if it fails.

3.0 SYSTEM SPECIFICATIONS

Performance and operational specifications are presented in this section. Some of the specifications are detailed further in Appendix A.

3.1 Accuracy

Positioning Accuracy:

Stability with temperature ...	< 0.04 mm
Stability with time	< 0.0025 mm
Finite positioning time	<< 0.001 mm
Resolution:	0.02 mm/step
Operating Temperature Range, Focus Box:	-30°C to +50°C

3.2 I/O Definitions

Input Requirements from H-316 Computer:

A block of four ten-bit words. Eight bits of each word specify position and two designate one of four actuators. The commands must be given in sequence A1, A2, A3, A4.

Output to H-316 Computer:

One eleven-bit word. Eight bits specify the electronic position limit entered on the Digital Interface front panel. One bit specifies computer or manual control as specified by the Mode Select Switch on the same front panel. Two bits specify error conditions in the focus electronics: one specifies whether the Focus Box temperature is within its normal operating range; the other specifies that one or more of the actuators are not in their commanded positions.

Digital Interface Front Panel Controls and Indicators:

(See the photograph of the front panel in Figure 2.)

Power Circuit Breakers:

Local: Provides 60 Hz, 115 V power to the Digital Interface chassis only.

Focus Control: Provides 60 Hz, 115 V power to the position control and monitoring electronics in the Focus Box when local power is on.

Focus Heater: Provides 60 Hz, 115 V power to the focus heaters, associated electronics and fan when local power is on.

Temperature Alarm Switch: Enables the audible temperature alarm.

Temperature Alarm: Produces an audible signal to alert the operator that the Focus Box is not operating in its specified temperature range.

Temperature Error LED: Provides a visible indication that the Focus Box is not within its specified temperature range.

Lock Error LED: Provides a visible indication that the commanded and actual positions of one or more actuators differ.

Display Select Switch: Selects which of ten possible quantities is displayed.

Lock: The digitized sum of the commanded and actual position difference for four actuators, i.e.,

$$\sum_{\text{All Actuators}} (\text{commanded} - \text{actual}) .$$

Display Select Switch (continued):

Lock (continued):

The scale is from 0.00 to 3.20, and when all actuators are in their commanded positions, lock should read approximately mid-scale.

Temperature: Temperature within the Focus Box on a scale from 0.00 to 3.20. The conversion to °C is given in Appendix A.

Measured, A1 thru A4: The digitized actual position of the respective actuators relative to the subreflector frame in millimeters.

Computer Command A1 thru A4: When the digital interface is in the computer mode, this displays the computer commanded position, in millimeters, for the respective actuator.

Limit Digiswitches: Selects an electronic limit. Any position command greater than this limit is ignored. These switches are set, during calibration, to the greatest deflection obtainable on all four actuators without hitting a mechanical limit.

Command Mode Select Switch: Selects the source of command position data, either the H-316 computer or the Digital Interface.

Manual Position Control Digiswitches: Used to select command positions for each actuator.

Update Select Switch: Selects which actuator positions are to be updated, in manual mode only.

Update Enable: Causes the selected actuator command positions to be updated at the focus, in manual mode only.

4.0 FUNCTIONAL CIRCUIT DESCRIPTIONS

4.1 Computer Interface

The Computer Interface has the function of handling data transfers between the H-316 computer and the Correctable Subreflector Digital Interface. The electronics to implement these transfers are described in the following, and a schematic is shown in Figure 3.

Position Data present on OTB 9 to OTB 16 is buffered by 7404 gates which drive four 74165 eight-bit shift registers. OTB 6 and OTB 5 define an address for the data, i.e., they specifiy one of four actuators. These two bits

control the two least significant bits of a 7442 decoder. Input bit "C" of the 7442 is brought high when the address bus equals 152_8. Input bit "D" of the 7442 is brought low by a buffered version of the computer's output strobe signal, RRLIN-. Thus, when RRLIN- goes low and the address bus is 152_8, data on output bus lines 9 to 16 is loaded into the 74165 addressed by OTB 6 and OTB 5 via the 7442 decoder. The load signal to the 74165 used to store data for actuator 4 is buffered (CDATRDY) and sent to the Digital Interface. The Digital Interface assumes that all four command positions have been loaded when it receives the CDATRDY and it proceeds to serially clock data out of the 316 interface. Note that the inversion introduced by the 7404 input buffers is removed by extracting data from the $\overline{QH}$ output of the shift register.

Data is sent from the Digital Interface to the 316 Interface by clocking it into two 74164 shift registers. All clocking is controlled by the Digital Interface. The PDATRDY signal is also sent, to prevent the computer from reading data while it is being shifted or when the Digital Interface is not powered. When the 316 wants to read the data, it simply puts 052_8 on its address bus, enabling the 316 Interface's input bus drivers (7403, open collector NAND gates).

4.2 Correctable Subreflector Digital Interface

The Correctable Subreflector Digital Interface, or, simply, the Digital Interface, is divisible into five sections:

1. Data Flow Controller to H-316 Computer Interface.
2. Data Flow Controller from H-316 Computer Interface.
3. Data Formatter and Transmitter.
4. Data Decoder.
5. Display.

The electronics used to implement these functions are described in the following. Schematics for all these electronics comprise Figures 4 through 8.

4.2.1 Data Flow Controller to H-316 Computer Interface

The function of this controller is to send a data word to the H-316 Computer Interface. The origin of the bits of this data word are explained in the following. Also, a functional description of how this word is transferred to the Computer Interface is given.

Four sets of information are contained in the data word. The first is the COMP+ signal. It is derived from the COMPUTER/MANUAL CONTROL SWITCH as shown in Figure 4. The second is the TALRT- signal which alerts the computer of an out-of-range temperature in the focus box. It is derived from the logical OR of two status bits sent by the focus electronics (see Figures 6 and 8). The third LALRT-, which informs the computer that the servos are in or out of lock, is derived similarly. The fourth is the electronic limit L7 to LØ. It is derived from the front panel Limit Switch via a BCD to binary converter (see Figure 5).

The above described word forms the data input to a multiplexer, shown in Figure 5. The data stream to the 316 Interface comes from the output of this multiplexer. A 74193 counter and associated electronics, shown in the same figure, control the multiplexer. Operation of the counter is depicted by means of the timing diagram in Figure 5. A reset pulse, DSTRT+, starts the counter in a particular state. Subsequently, the counter steps through the desired sequence. One of three conditions may cause a reset pulse. The first is powering the Digital Interface, which causes the RST- signal at the preset input of the 7474 flip-flop to go low for about two seconds. The second is a change in command mode. (See CONTΔ+, Figures 4 and 7.) The third is the detection of a CDATRDY signal (see Figure 4). The third condition is delayed by approximately

500 milliseconds so that the LALRT- bit, when it is transmitted, represents the effect of the command just given by the computer, i.e., did the actuators go where I told them to?

4.2.2 Data Flow Controller from the H-316 Computer Interface

As described in Section 4.1, the H-316 Computer Interface signals the Digital Interface after position commands are loaded into it by the computer. The task of the controller described in this section is to fetch these position commands, store them, and signal the Data Formatter, Tester and Transmitter when it is done.

The electronics to accomplish this task include a counter and its associated control logic, and a 32-bit shift register. The sequence of operation is as follows. The CDATRDY signal from the 316 Interface passes through a multiplexer shown in Figure 4 if the Digital Interface is in computer mode. It is then stretched and synchronized by the flip-flops, 4D, in Figure 6. The stretched pulse resets the counter which then cycles through thirty-two states and allows thirty-two clock pulses, CRCR+, to the shift register in the Digital Interface and thirty-one to that in the H-316 Interface. This shifts data from the H-316 Interface to the Digital Interface. Upon completion of the shift, the signal C1CY+ goes high to signal the Formatter.

4.2.3 Data Formatter, Tester and Transmitter

The task of the Data Formatter, Tester and Transmitter is to group data into a form suitable for transmission to the focus, to test position commands to see if they are greater than the electronic limit, and to transmit the data to the focus. The implementation of this task is shown in block diagram form in Figure 9 and in schematic form in Figures 4 and 7. Details of the implementation are discussed below.

Data flow is controlled by the counter shown, along with its timing diagram, in Figure 7. The counter's clock is conditioned on the TBMT (Transmit Buffer Empty) signal from the UART. The counter outputs and the signal COMP+ (indicating computer or manual control) control the multiplexers. Thus, each time the UART's transmit buffer is empty a new data group is strobed into it. The contents of each data group is shown in the DATA FORMAT TABLE, Figure 7. Inspection of this table reveals that a position command for a given actuator is clocked into the UART in three bytes. First, the least significant four bits are sent, then the most significant four bits and, finally, the address of the actuator for which the data is intended, and a bit, UPDATEN+, to indicate whether or not the command position should be updated in the Focus Electronics. The state of UPDATEN+ depends on the magnitude comparison, and, in the manual mode, on the position of the Update Select Switch. In manual mode, each data group, 0 through E, is transmitted only once, after the update enable switch is pressed. However, in computer mode, data is continuously transmitted. The UART handles the task of serializing the data and encoding it with start, stop, and parity bits.

4.2.4 Data Decoder

The Data Decoder has the task of finding a synchronizing bit in, and storing the data received from, the Focus Electronics. This task is easily accomplished as can be seen by viewing the schematic in Figure 6 and the data format in Table 1. All that is required to detect sync is detecting a 1 in the fifth bit. Data bytes are simply stored in shift registers. When the sync bit is found, they are strobed into buffer registers.

TABLE 1

Downlink Data Format

Data Group	TD5	TD4	TD3	TD2	TD1
C	1	LST-1	LST-Ø	TST-1	TST-Ø
B	Ø	L7	L6	L5	L4
A	Ø	L3	L2	L1	LØ
9	Ø	T7	T6	T5	T4
8	Ø	T3	T2	T1	TØ
7	Ø	A4-7	A4-6	A4-5	A4-3
6	Ø	A4-3	A4-2	A4-1	A4-Ø
5	Ø	A3-7	A3-6	A3-5	A3-4
4	Ø	A3-3	A3-2	A3-1	A3-Ø
3	Ø	A2-7	A2-6	A2-5	A2-4
2	Ø	A2-3	A2-2	A2-1	A2-Ø
1	Ø	A1-7	A1-6	A1-5	A1-4
Ø	Ø	A1-3	A1-2	A1-1	A1-Ø

4.2.5 Display Electronics

Data from the Focus Electronics and computer are presented on the front panel of the Digital Interface by the Display Electronics. These electronics include multiplexers, a binary to BCD converter, a few logic gates, as well as the associated numeric display, discrete LED's, audible alarm, and switches. The definition of the displayed quantities is found in Section 3.2. A few more subtle points of the implementation of the display are discussed

below. The remainder of the description is obvious by inspection of Figure 2.

The numeric display is driven by a binary to BCD converter, which in turn is driven by multiplexers controlled by the display select switch. A multiply by two and divide by 100 are performed on the data so that the display reads subreflector motion relative to the subreflector frame, in millimeters. The multiply by two is effected by a hard-wired left shift into the binary to BCD converter. The divide by 100 is implemented by lighting the appropriate decimal point.

4.3 Focus Electronics

The principal requirements of the Focus Electronics are to position four actuators accurately and to inform the control room of its status. Other requirements of the Focus Electronics are that they not produce considerable RFI and that the communication channel be optically isolated from the control room. The implementation of these requirements is discussed below under five major headings: Data Decoder, Servo Loop, Heater Electronics, Data Acquisition Electronics, RFI Shielding and Filtering.

4.3.1 Data Decoder

The Data Decoder is shown in the schematic in Figure 10. It receives data from the control room electronics, formatted as shown on the Data Format Table of Figure 7. It then stores data bytes until it has an error free position command and address. If required, it stores the command into the latch of the appropriate servo.

Serial data is received, via the optical isolator, by the 2502 UART which transforms it into parallel data bytes. The bytes are then stored in 74174 latches along with the error status of each byte. When a one is detected in

bit five (RD5), one of five possible strobes (STRB1 through STRB5), determined by SØ, S1, and S2, is activated only if all three bytes were transmitted error-free.

4.3.2 Servo Loop

There is one servo loop for each of the four actuators. Comprising each loop are the following functional subsystems: D/A Converter, Position Sensor, Summing Amplifier, Compensation Amplifier, Voltage to Frequency Converter, Actuator, and Motor Driver. Each of these subsystems is described in the following paragraphs.

4.3.2.1 D/A Converter

The D/A Converter subsystem consists of two 74175 registers, an SSS 1508A D/A converter, a 2.5 volt reference (common to four loops), and associated resistors and capacitors, shown in Figure 11. Position commands received by the Focus Data Decoder (reference Section 4.3.1) are strobed into the 74175's. These store the position command and present it to the SSS 1508A D/A which outputs a current proportional to the command. The 2.5 volt reference source and R4 and R5 form an adjustable offset.

4.3.2.2 Position Sensor

The Position Sensor subsystem consists of an oscillator (Schaevitz PCB214, Figure 12, common to four loops) a Linear Variable Differential Transformer (LVDT, Schaevitz HCA250), and a demodulator (Schaevitz PCB433C, Figure 13). The LVDT is driven by a 2.5 kHz sinusoidal voltage produced by the oscillator. The LVDT output is a position dependent, amplitude modulated voltage. It is demodulated by the demodulator whose output is, then, a position dependent voltage. Gain and offset trimpots are provided on the demodulator. These are used for system calibration.

4.3.2.3 Summing Amplifier

The Summing Amplifier consists of A1, R6 and R7 in Figure 11. Its output voltage is proportional to the sum of the three input currents: the SSS 1508A output current, the offset current, and the current derived from the demodulator output and R8 and R9. Due to the loop's negative feedback, A1's output voltage represents the difference between the commanded and actual positions. The scale is approximately 2 volts/mm.

4.3.2.4 Compensation Amplifier

The Compensation Amplifier consists of A2 and associated components in Figure 11. It provides lead-lag as well as terminated integration compensation for the loop. The small signal transfer function is

$$\frac{V_{out}}{Vin} = 109 \underbrace{\frac{(.141\ S + 1)}{S}}_{\text{Terminated Integration}} \cdot \underbrace{\frac{(0.081\ S + 1)}{(3.11 \times 10^{-3}\ S + 1}}_{\text{Lead-Lag}}$$

The back-to-back diodes across the 0.22 μF capacitor effectively remove the integrating capacitor from the loop at larger amplitudes. This is to guanantee the stability of an otherwise conditionally stable system. The two zener diodes prevent A2 from saturating and possibly making the loop operate incorrectly.

4.3.2.5 Voltage to Frequency Converter

The Voltage to Frequency Converter is shown in Figure 14. Its input is the voltage output of the compensation amplifier. It has two outputs. One produces a varying-frequency pulse train in response to a positive input and the other does the same for a negative input. Response to a positive input is as follows. The positive voltage causes U5 to integrate down. If the input voltage is great enough (> 0.7 V) the integration rate is faster. The output of the integrator is level shifted by R11, R13, R17, and R19, and sampled by U3. When the integrator output reaches approximately -5 volts, U3 pin 8 goes high at the next sampling instant, and U4 pin 3 goes low for five milliseconds. This causes a five millisecond feedback current pulse through R18 to reset the integrator and allows the cycle to start again. The pulse at U4 pin 3 also drives one of the two motor driver inputs. Response to a negative input voltage similarly produces pulses at U4 pin 6 to drive the other motor driver input.

4.3.2.6 Actuator

The actuator is a modified version of AIRESEARCH part number 34596. It has a travel range of 0.250 inches. The schematic of the actuator is shown in Figure 15. The motor is a two-stator, series wound motor. Current in one stator causes motion in one direction and current in the other produces motion in the opposite direction. There are two mechanically activated limit switches, one for each end of travel.

4.3.2.7 Motor Driver

The Motor Driver circuit is shown in Figure 14. It consists of two saturating switches, one for each motor stator, and an overcurrent protection circuit. Each saturating switch consists of two transistors and associated components. Q2 and Q3 form one switch and Q5 and Q6 the other. C4 and C9 control the rise and fall times of the output voltage, to limit RFI. CR1 and CR8 are flyback diodes. Q1 and associated components form the overcurrent protection circuit. When they sense an overcurrent condition, the drive to the motor drivers is removed.

4.3.3 Temperature Controller

This system is intended to heat the control electronics at the focus to the 140-ft telescope to approximately 25°C during the winter, when outside temperature is expected to vary from 20°C down to -30°C. The system consists of a temperature control circuit, a failsafe circuit to prevent thermal runaway in the event that the control circuit fails, a circuit to provide a TTL level signal to notify the operator should the controller fail, and two heaters.

4.3.3.1 Controller

The temperature control circuit consists of IC-1 and its associated components, including T1 (see Figure 16). IC-1 will trigger T1 at the zero crossing of each half cycle of A.C. as long as the temperature is below that set by the 10 K pot and the thermistor (in this case, 25°C). This allows current to flow through the load so long as T2 is also triggered.

4.3.3.2 Failsafe

IC-2, T2, and their associated components, make up the failsafe circuit. IC-2 will provide trigger pulses to T2 as long as the temperature is below 30°C. IC-2 also incorporates a protection circuit to inhibit triggering T2 in the event that the thermistor opens or shorts. This circuit is not connnected in IC-1 so that, if its thermistor opens, the failsafe circuit will shut the heater down and notify the operator of a failure. This will also occur should IC-2's thermistor open; thus the operator is notified of a thermistor opening in either circuit and runaway cannot occur.

4.3.3.3 Failure Indicator

The optoisolator (IC-3) is used to isolate, invert, and make TTL compatible, the trigger pulse from IC-2. The low going pulse at pin 5 of IC-3 is used to trigger the monostable multivibrator

(IC-5). Since the period of these trigger pulses is shorter than its output pulse, pin 5 of IC-5 is kept in a low state. Here a bi-directional LED is used to indicate a failure. Normally, current flows through the LED into pin 5 and the LED is green. In the event of a failure, the monostable is not triggered, and current flows in the opposite direction, into pin 8 and the LED is red. Different valued pullup resistors are used here to equalize brightness of the LED's.

IC-4 and its associated circuitry are used to provide an active high TTL level indicating that AC line voltage is present. This is necessary since, during the summer, the AC power to the heater will be shut off (the TTL supply is on a different line). In order to avoid an erroneous failure signal, this level is gated with the output of the monostable; this insures that when the failure line is active, a component failure has indeed occurred.

4.3.3.4 Miscellaneous

Since the box containing the control electronics may be rotated or inclined at any angle, a fan is necessary to insure proper circulation of heat to guard against hot spots, and to reduce thermal lag in the system. Note that all components in the temperature control and failsafe circuits are rated to operate down to -40°C, insuring proper start up, even in hostile conditions. The TTL circuitry used, however, is only rated for use down to 0°C, so during start-up the signal on the failure line may be invalid until the box reaches proper operating temperature.

Each of the two heaters can supply up to 250 watts. Some test data, shown in Appendix C, has shown that this is more than adequate.

Because the Triacs T1 and T2 are gated on at the zero crossing of the line voltage, and because the heater units are resistive, RFI from this system is negligible.

4.3.4 Data Acquisition System

The Data Acquisition electronics have the task of monitoring the status of the focus electronics and informing the control room of that status. The quantities monitored include the position of the four actuators, the loop error, the box temperature, and an error indicator from the heater. The implementation of these functions is discussed below in five sections: Origin of Signals to be Monitored, A/D Conversion, Error Checking, Data Formatting and Transmission, and Diagnostic Hardware.

4.3.4.1 Origin of Signals to be Monitored

Four of the signals to be monitored, PACT 1, PACT 2, PACT 3, PACT 4 (Figure 17) represent the positions of the four actuators. These positions are output from the demodulators (reference Section 4.3.2.2)'. Each demodulator output drives a resistive divider, part of which (R10) is shown in Figure 11 and part (10 K and two unspecified resistors) shown in Figure 17. The unspecified resistors permit gain calibration. Offset calibration is done using R5 in Figure 11.

A fifth signal to be monitored is PERR (Figure 17). This signal is derived by resistively summing the four loop error voltages (Figure 11). This is a way of checking all error voltages at once; it is unlikely that PERR will equal zero if one or more of the loop error voltages is not zero.

The sixth signal to be digitized is the box temperature (Figure 17). A voltage proportional to temperature is provided as an output from the REF02 5-volt reference. This voltage is scaled using the OP-15 high input impedance op-amp, the five volt reference, and associated resistors.

The seventh signal to be monitored is a digital signal from the heater, FAILURE+. It is described in detail in Section 4.3.3.3.

4.3.4.2 A/D Conversion

The conversion of the six analog signals to be monitored into digital quantities is handled partly in hardware and partly in firmware. A block diagram of this subsystem is shown in Figure 18 and the schematic is shown in Figure 17. A flow chart of the firmware and the firmware are to be found in Appendix B. The digitization is done as follows.

Using a program stored in the ROM, the microprocessor loads three channel select bits into the Peripheral Interface Adapter. These three bits select one of the eight inputs of the multiplexer as one input to the Difference Amplifier. The microprocessor then goes through a Successive Approximation alogrithim (see flow chart, Appendix B) in which it puts out eight approximations to the D/A converter and observes the comparator output through the Peripheral Interface Adapter. This results in an 8-bit approximation to the analog signal. Each analog quantity is approximated to eight bits using this scheme.

4.3.4.3 Error Testing

The microprocessor tests two quantities, temperature and servo lock, in order to alert the control room of a malfunction. Temperature is tested by comparing the digitized value of temperature against minimum and maximum values stored in the ROM. The error

bit TST-Ø is set if the measured temperature is greater than the specified maximum and TST-1 if less than the specified minimum. TST-Ø is also set if the heater's FAILURE+ signal is true.

Lock is tested by comparing the digitized value of the sum of the loop errors, D_{PERR}, against the digitized value for ground, D_G. Error bit LST-Ø is set if $D_G + 1 < D_{PERR}$. Error bit LST-1 is set if $D_{PERR} < D_G - 1$. Both lock error bits are set if $D_{PERR} - D_G$ causes an overflow, indicating an error of unknown polarity.

4.3.4.4 Data Formatting and Transmission

In addition to acquiring data on the status of the focus electronics, the Data Acquisition System must inform the control room electronics of this status. This involves organizing data into a format recognizable by and transmitting the data to the control room electronics. Part of this is done by the 6802 microprocessor and part by the 2502 UART. The microprocessor organizes the data into the format shown in Table 1. When the microprocessor has a data byte ready, it monitors the "ready" line (TBMT) of the UART via the PIA until it indicates ready. Then the microprocessor loads the UART with the data byte. The data byte is then converted into a five bit, odd parity, serial format by the UART, and transmitted to a similarly configured UART in the control room.

4.3.4.5 Diagnostic Hardware

A significant amount of diagnostic hardware is included on the Data Acquisition Board. This hardware proved invaluable in the initial debugging of the system, and is still useful in pinpointing some failures. It is shown in Figure 17. A Halt/Go Switch is used to stop program execution; a Single Cycle Switch and associated hardware allow a program to be executed one step at a time. LED's and associated latches and inverters allow the state of the data and address busses to be viewed during any phase of an instruction in single cycle mode. The particular phase of the instruction is chosen by switches 6, 7, and 8 at 11B, by the shift register at 8G and by the multiplexer at 9E. Thus it is possible to follow one's program through in great detail and assure it is working properly.

4.3.5 RFI Filtering and Shielding

To prevent excessive RFI from being generated by the Focus Electronics, all wires passing through the aluminum box are filtered either by an LC network or, where higher impedance to ground is dictated by circuit constaints, by a feedthrough capacitor. Also, all slots in the box are EMI/RFI sealed with

Metex "Xecon Polastrip Gasketing". These filtering and shielding devices are visible in Figure 19. At this time there are no quantitative results indicating how well the box is shielded. However, no obvious problems were seen in the first telescope trial of this system.

4.3.6 Servo Loop Considerations

The Servo Loop used to position the actuators is, at best, quite difficult to analyze. One prime reason for this is the series wound motor in the actuator. The torque produced by such a motor is proportional to the square of the current flowing through it, resulting in a non-linear transfer function. Also the actuator's load is widely varying and a sampled, rather than continuous, system is used to drive the actuators.

To get a feel for the frequency response of the actuator, it was put into a linear, continuous loop. Phase shift was added to the loop until oscillation was achieved. Assuming unity loop gain and 180° phase shift during oscillation; it is possible to calculate the actuator's contribution to this since everything else is known. By varying the loop gain and phase it was possible to come up with the frequency response of the actuator. Compensation was designed based on this.

The widely varying load causes wide variation in damping. Depending on initial and final positions, everything from slightly underdamped to moderately damped motion can be seen. This is not very detrimental to system performance since high-speed response is not a primary requirement; the telescope does not move too fast either! For a further discussion of the effect of response time on the overall error, see Appendix A. Some photographs of the servo's response to large and small commands are also included in this Appendix. The effect of the varying load also manifests itself in the frequency and amplitude of the limit cycle.

Since speed is not one of the primary requirements of this servo it was sacrificed to reduce power requirements. The electronics are designed such that at most two of the four actuators are driven at any instant. This halves the power supply requirement.

5.0 ACKNOWLEDGEMENTS

Many people are to be thanked for their assistance in this project. Steve MacMinn did the bulk of the design of the Temperature Controller and polished up the design of the firmware for the Data Acquisition System. He is also responsible for Section 4.3.3 and Appendices B and C in this report. Ron Weimer, Rick Fisher, Dwayne Schiebel, Ray Hallman, Bill Vrable, Woon-Yin Wong, Bob Vance, and Tom Cram must be thanked for their helpful suggestions. Thanks to Dwayne Schiebel also for debugging help and to Bill Vrable, Larry Miller, and Winston Cottrell for the construction.

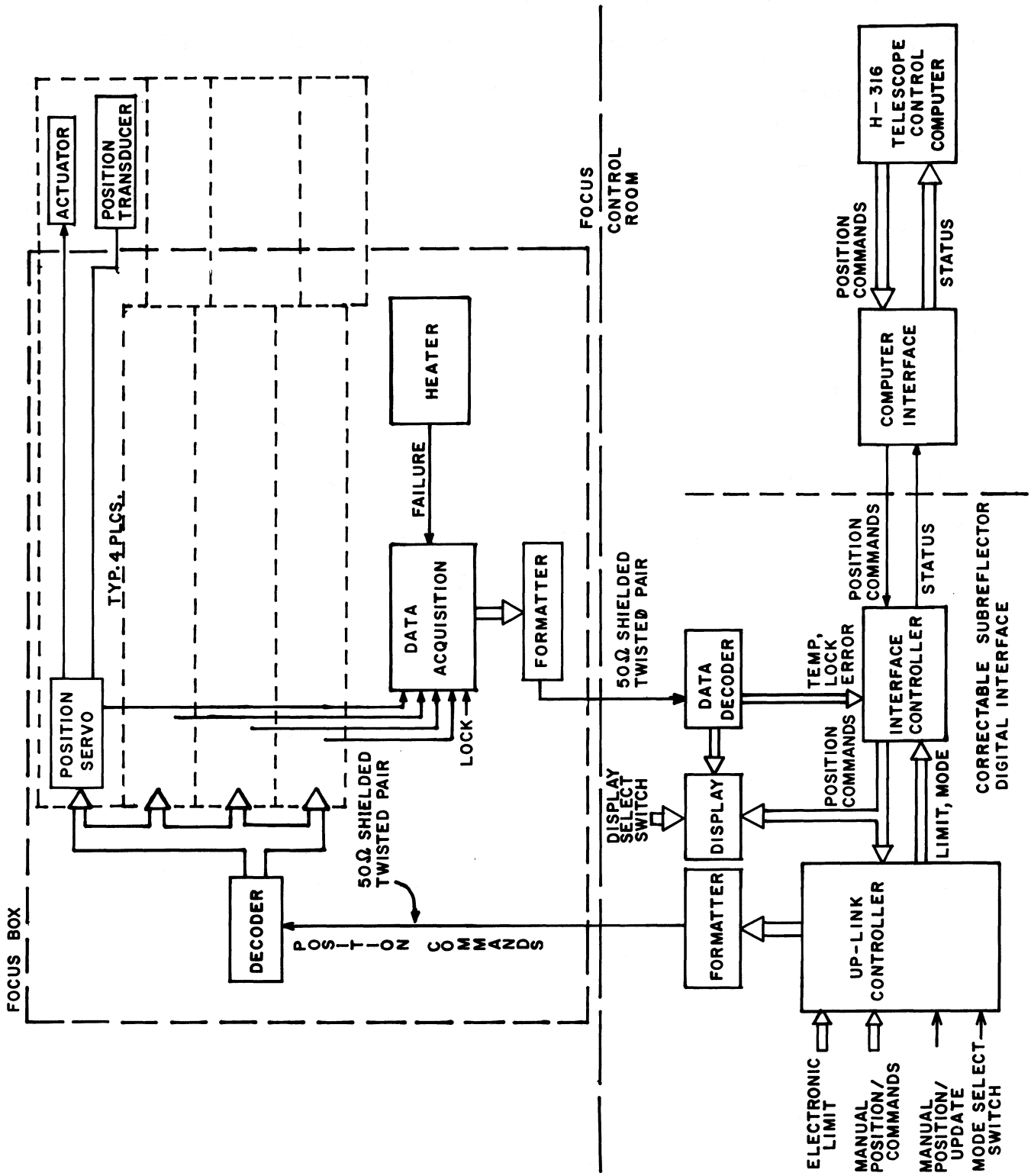


Figure 1. Correctable Subreflector Controller Block Diagram

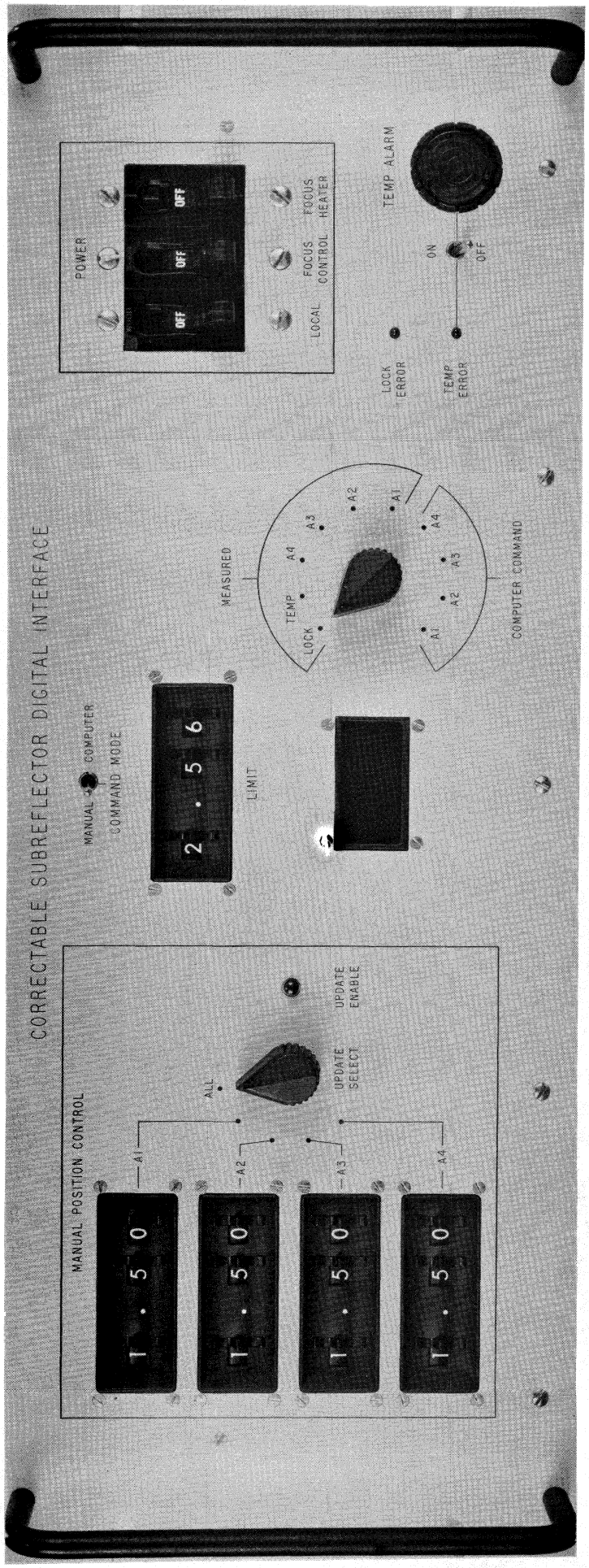


Figure 2. Correctable Subreflector Digital Interface Front Panel

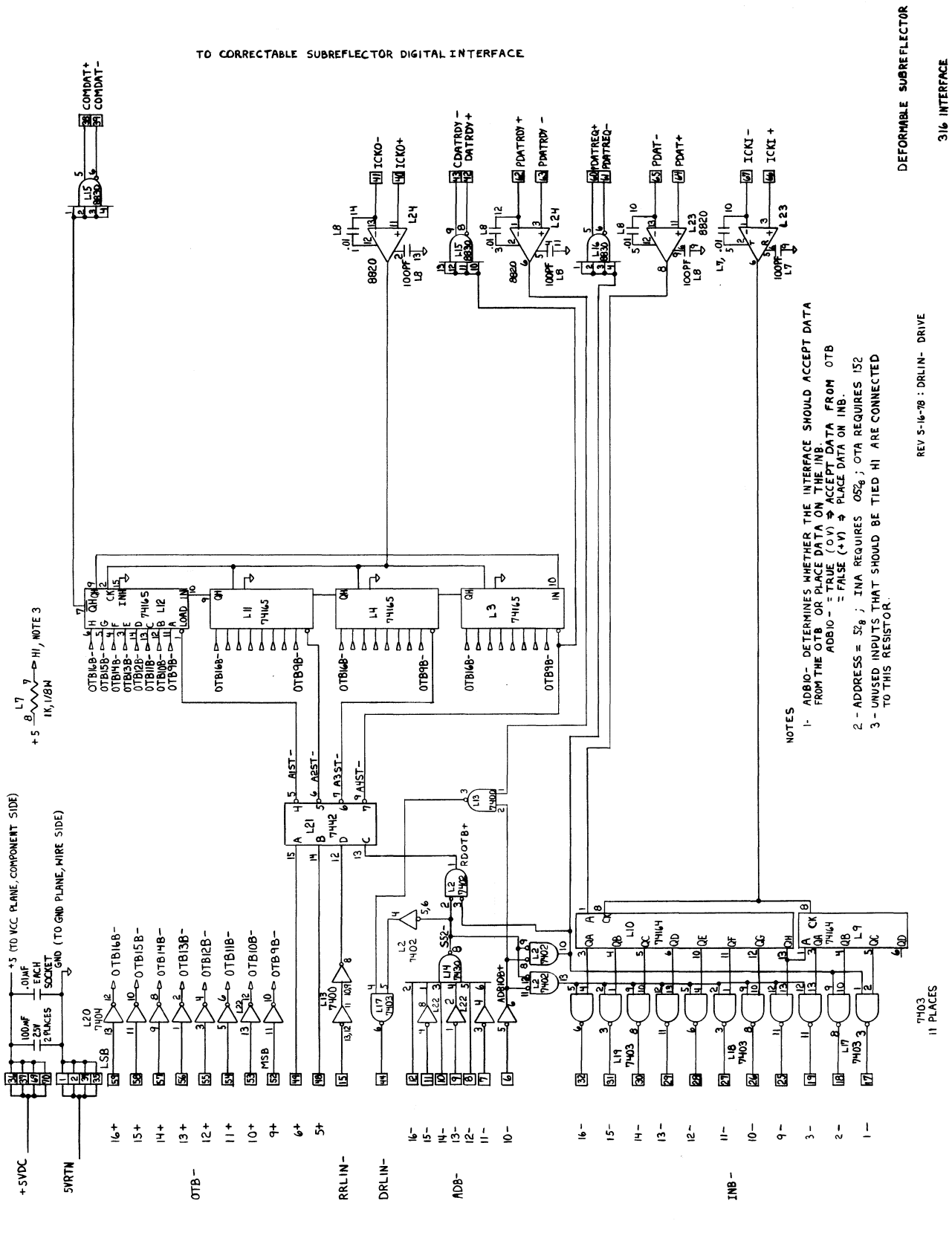


Figure 3. H-316 Interface Schematic

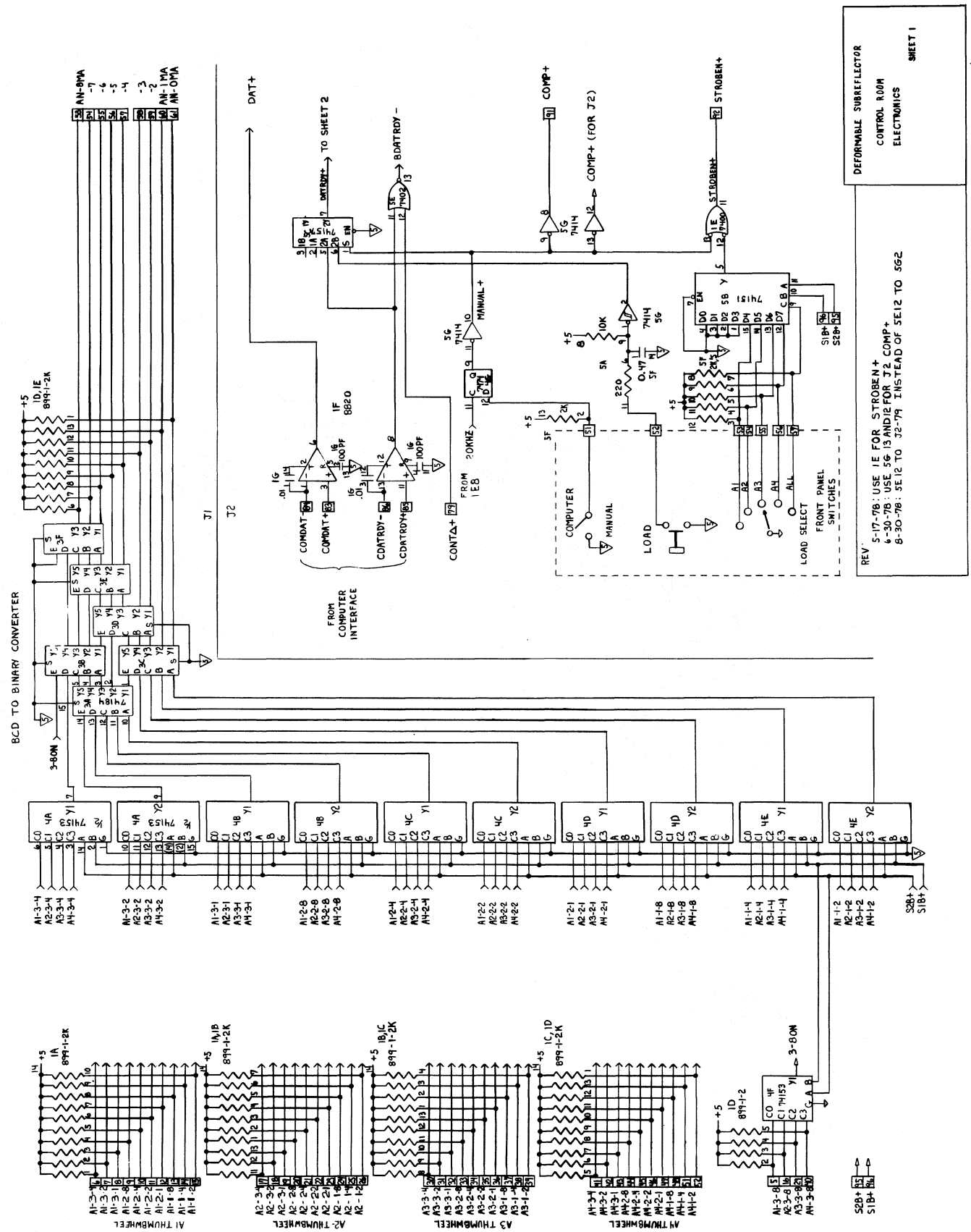


Figure 4. Correctable Subreflector Digital Interface Schematic, Sheet 1

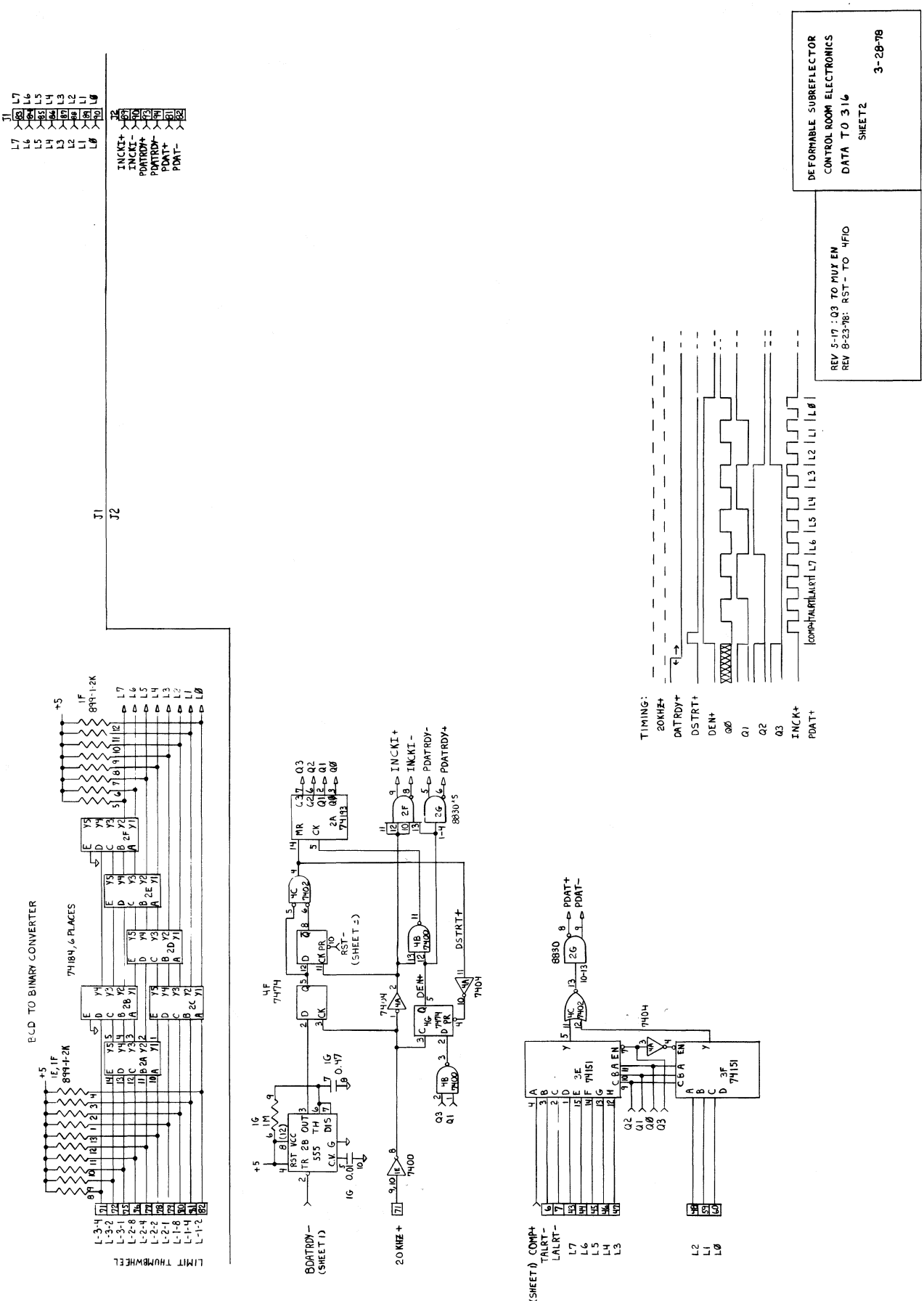


Figure 5. Correctable Subreflector Digital Interface Schematic, Sheet 2

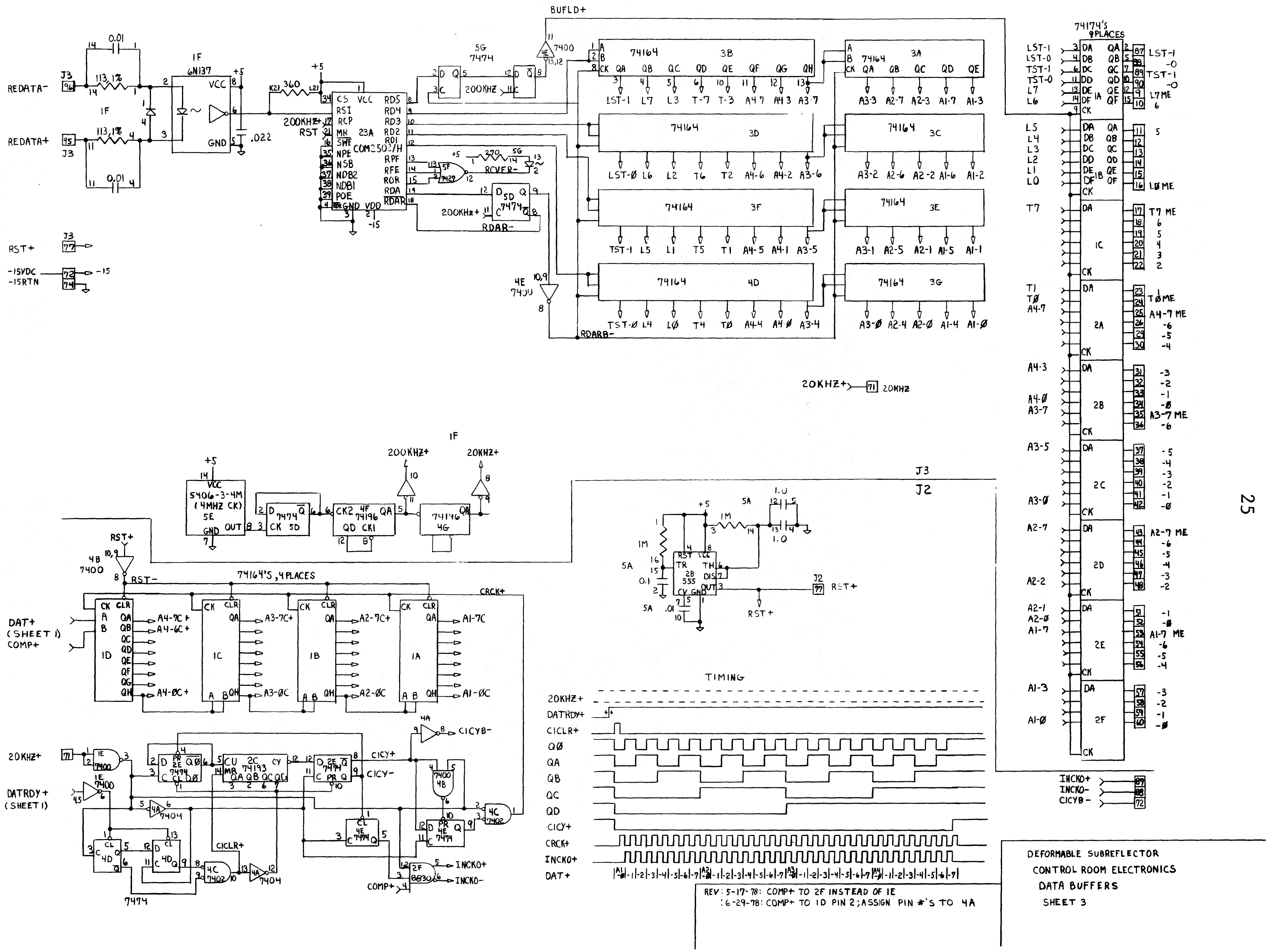


Figure 6. Correctable Subreflector Digital Interface Schematic, Sheet 3

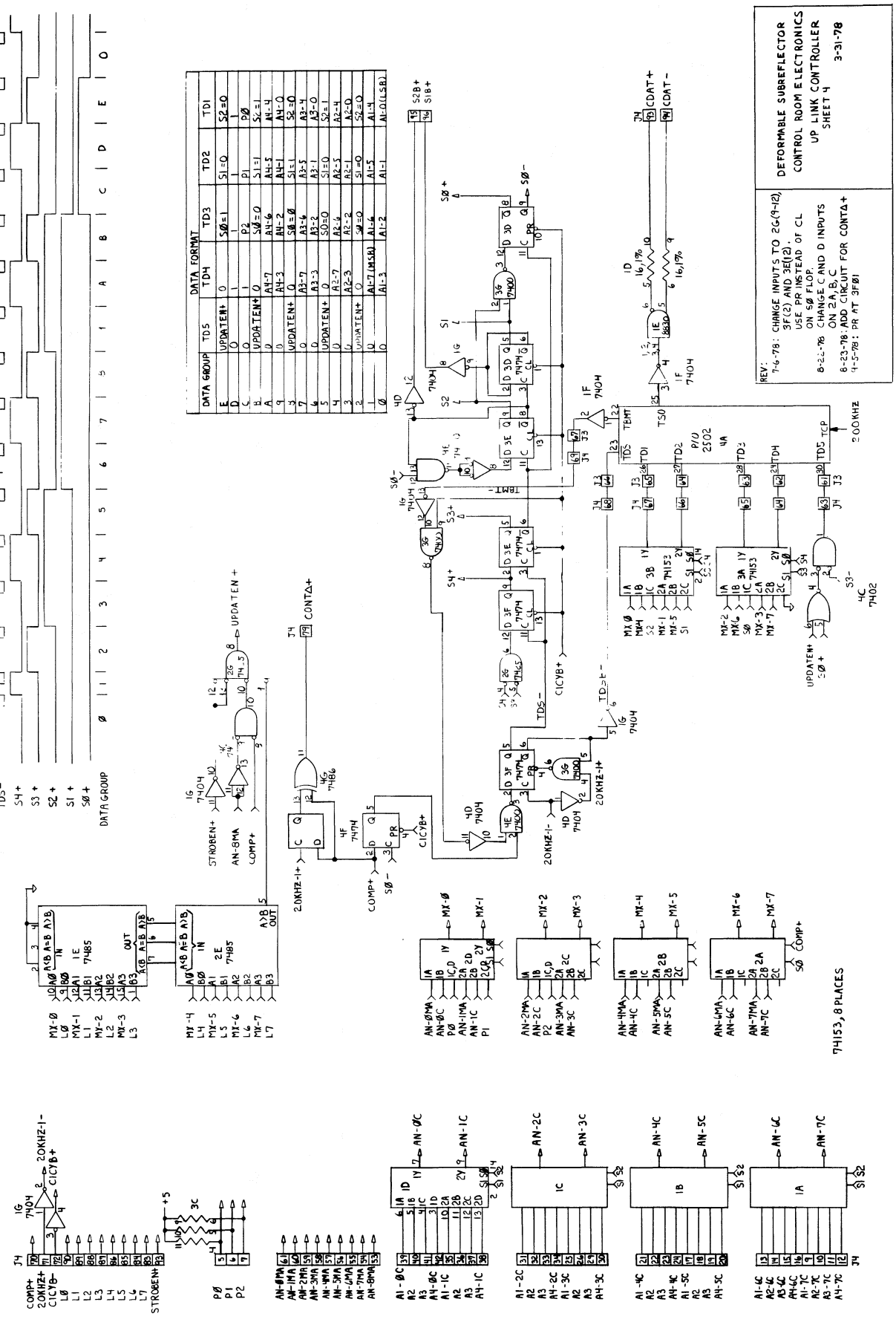


Figure 7. Correctable Subreflector Digital Interface Schematic, Sheet 4

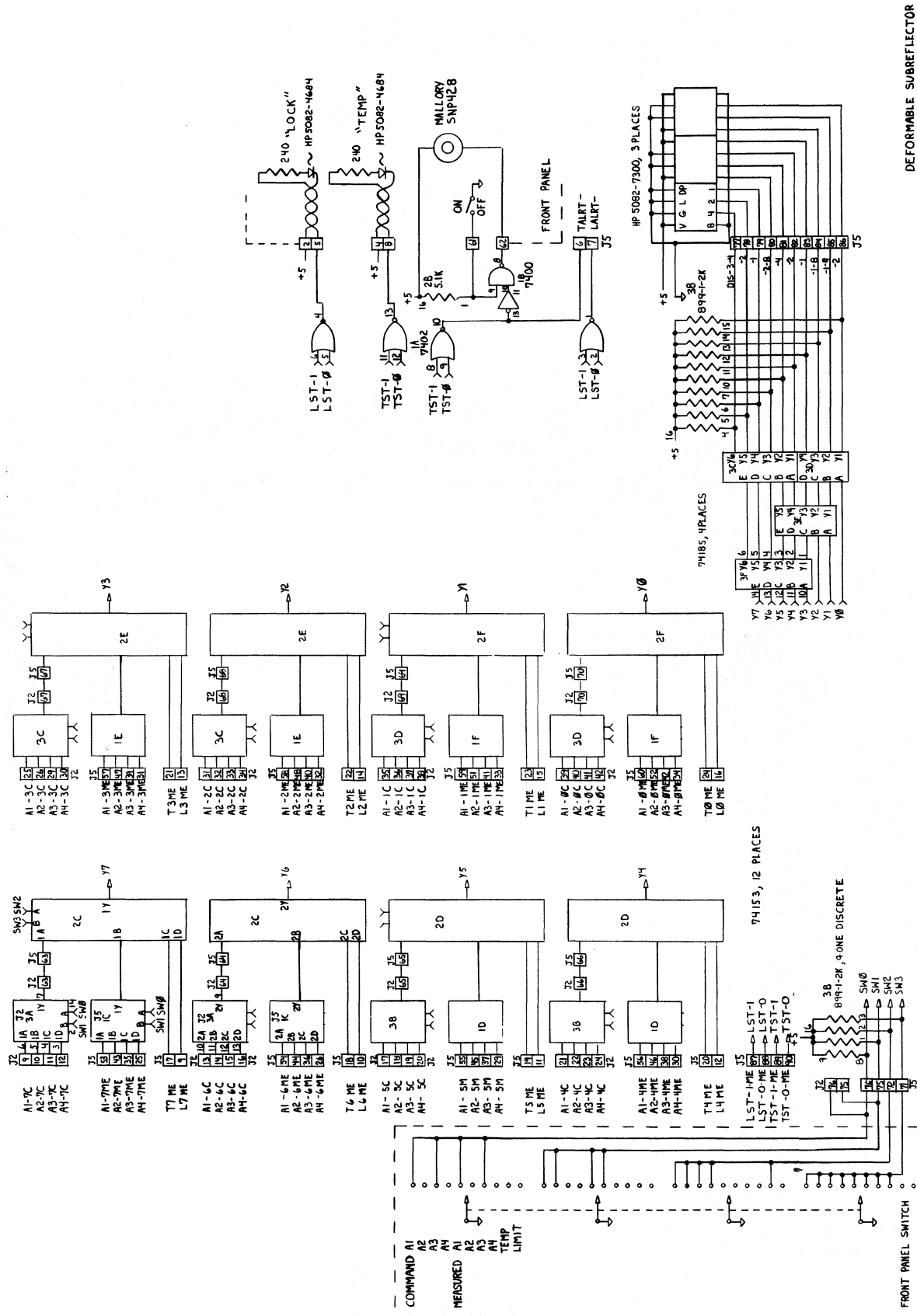


Figure 8. Correctable Subreflector Digital Interface Schematic, Sheet 5

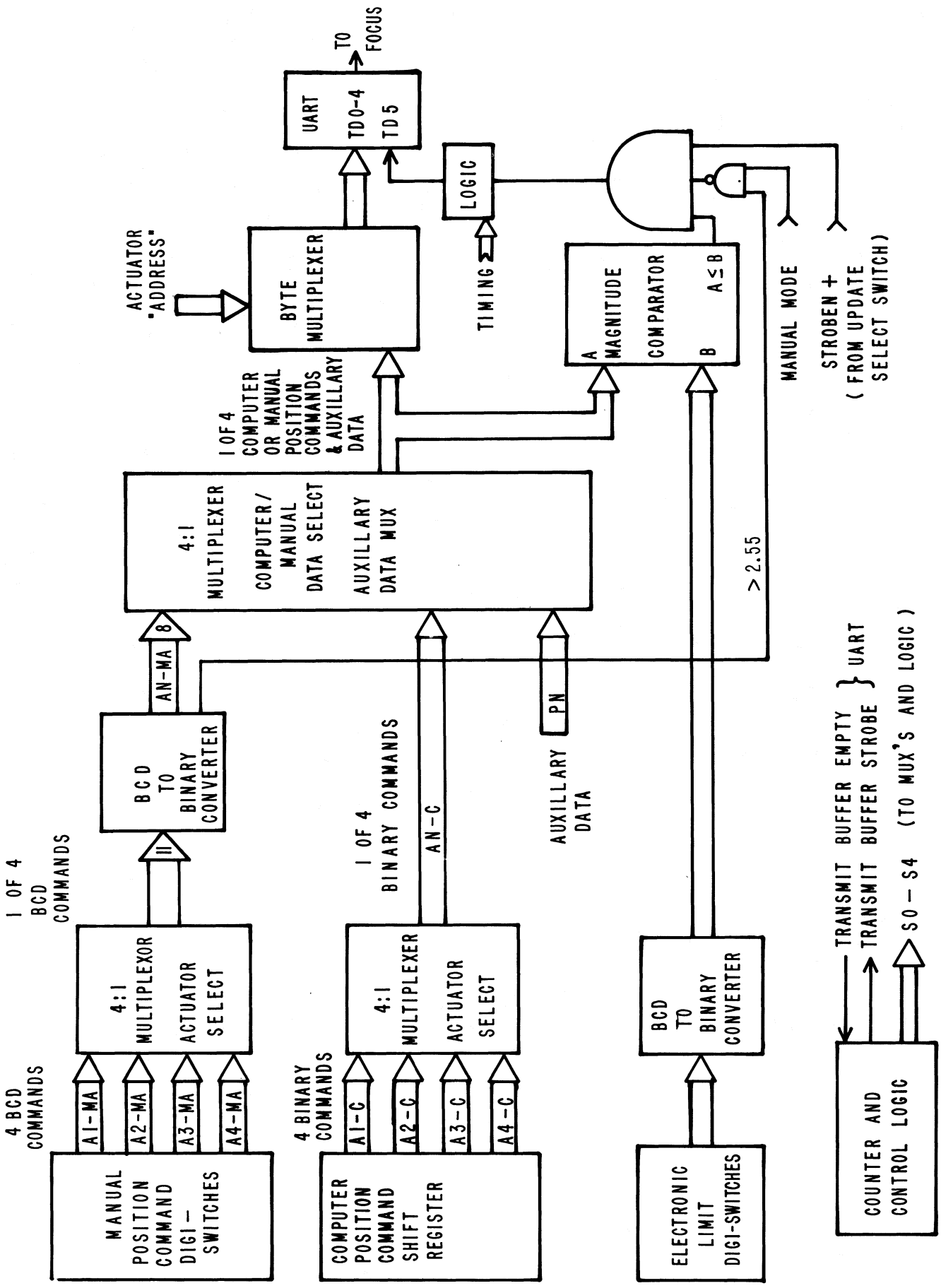


Figure 9. Data Formatter, Tester and Transmitter Block Diagram

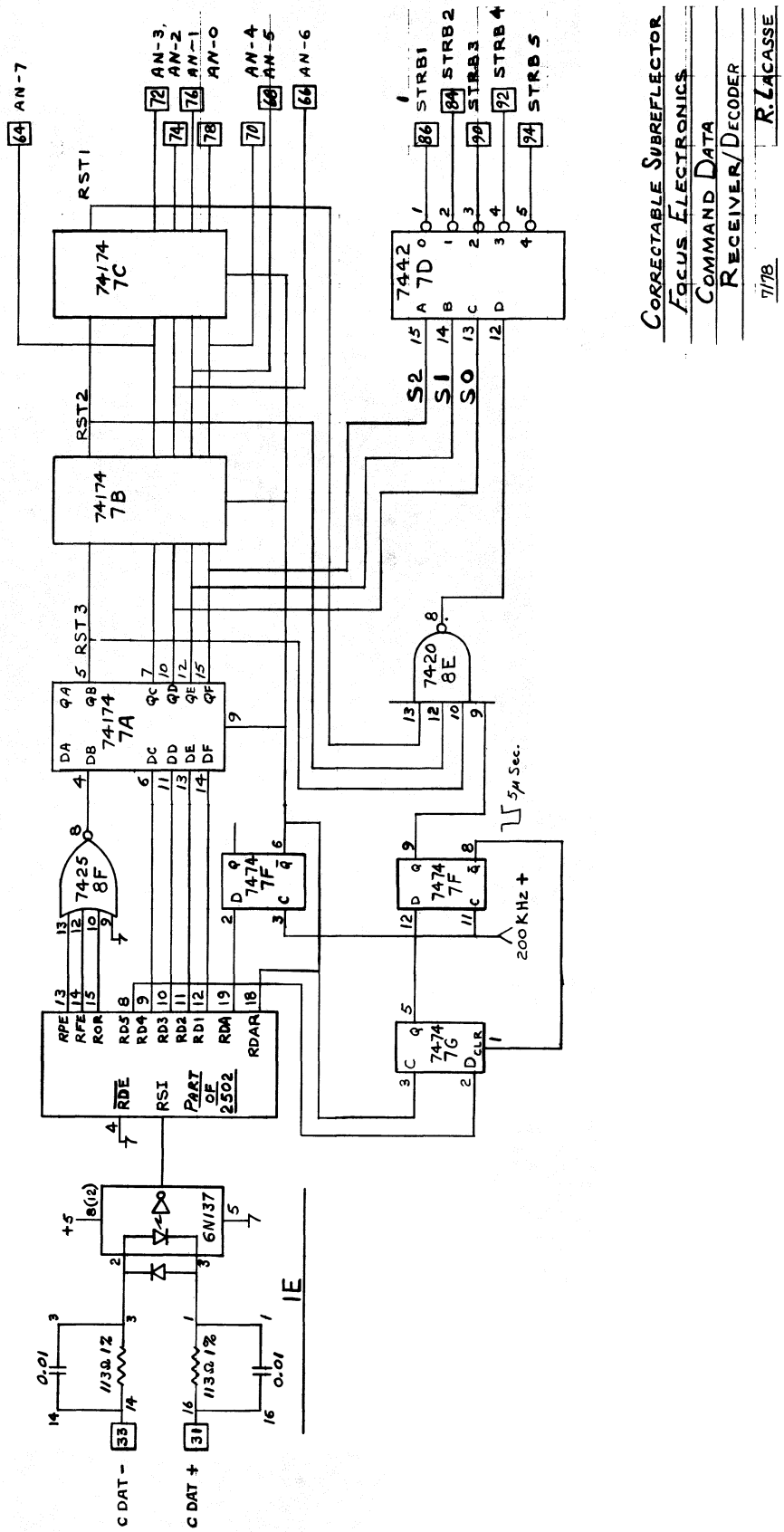


Figure 10. Focus Electronics, Command Data Receiver/Decoder Schematic

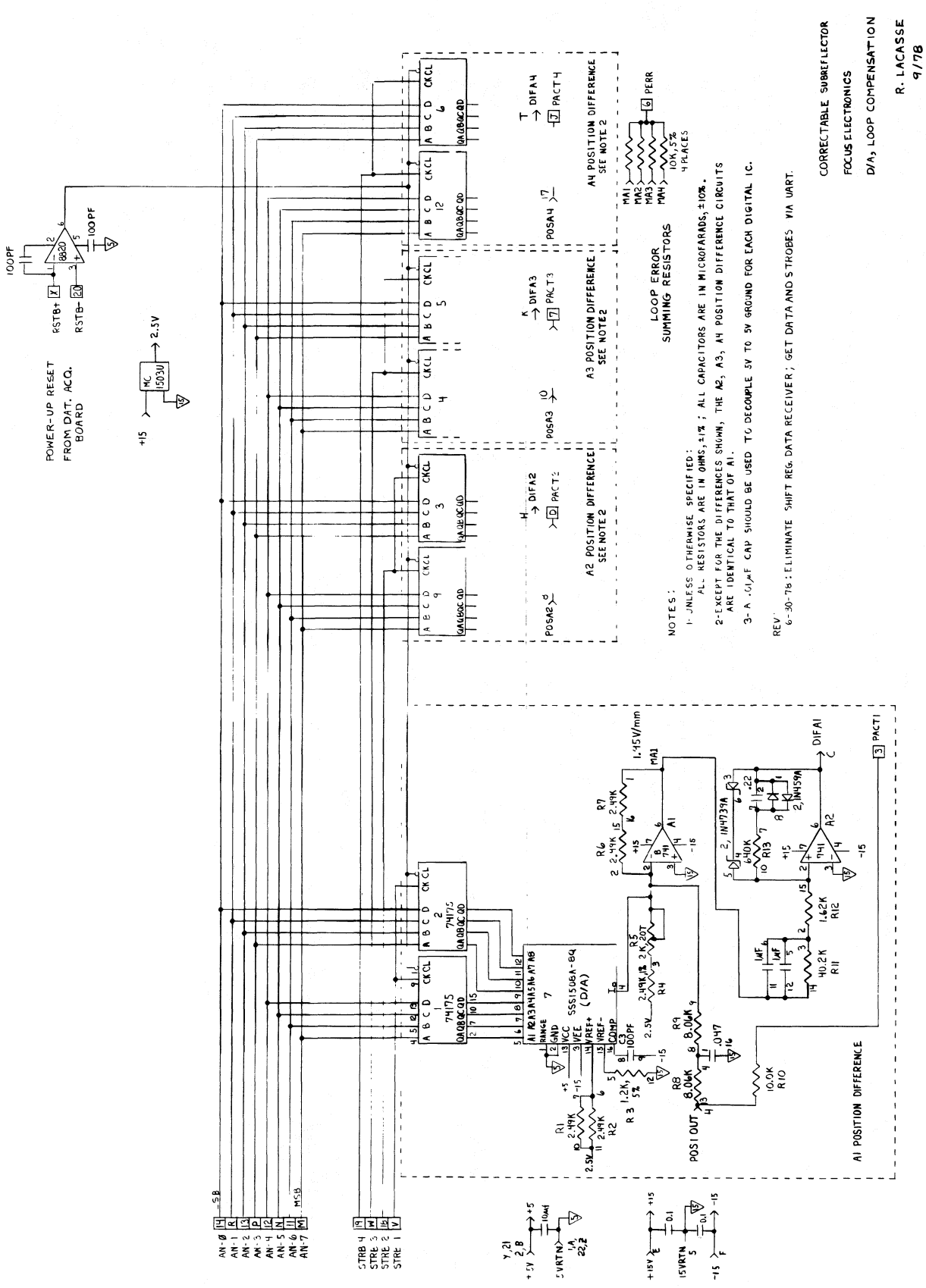


Figure 11. Focus Electronics, D/A and Loop Compensation Schematic

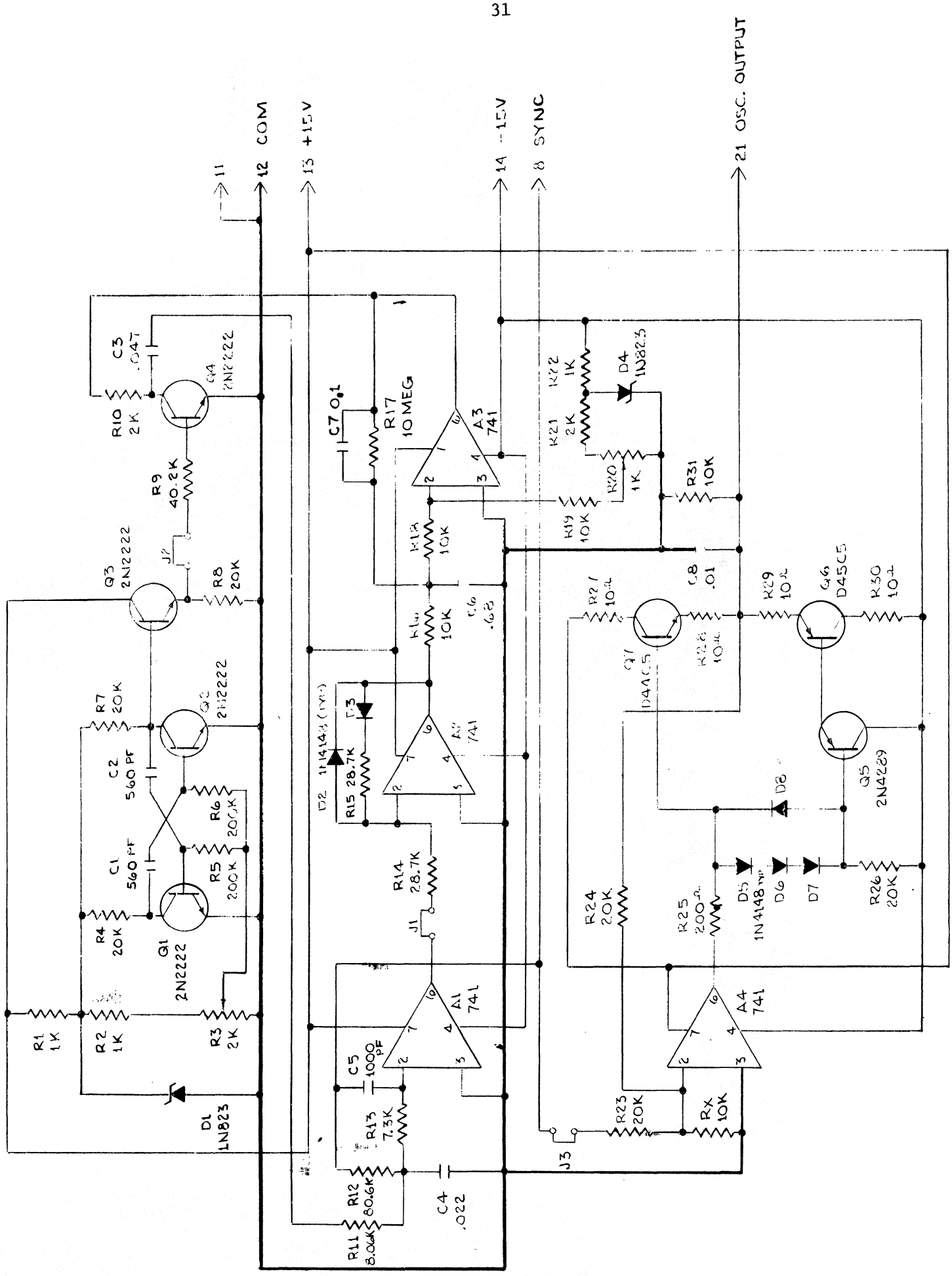


Figure 12. LVDT Oscillator Schematic

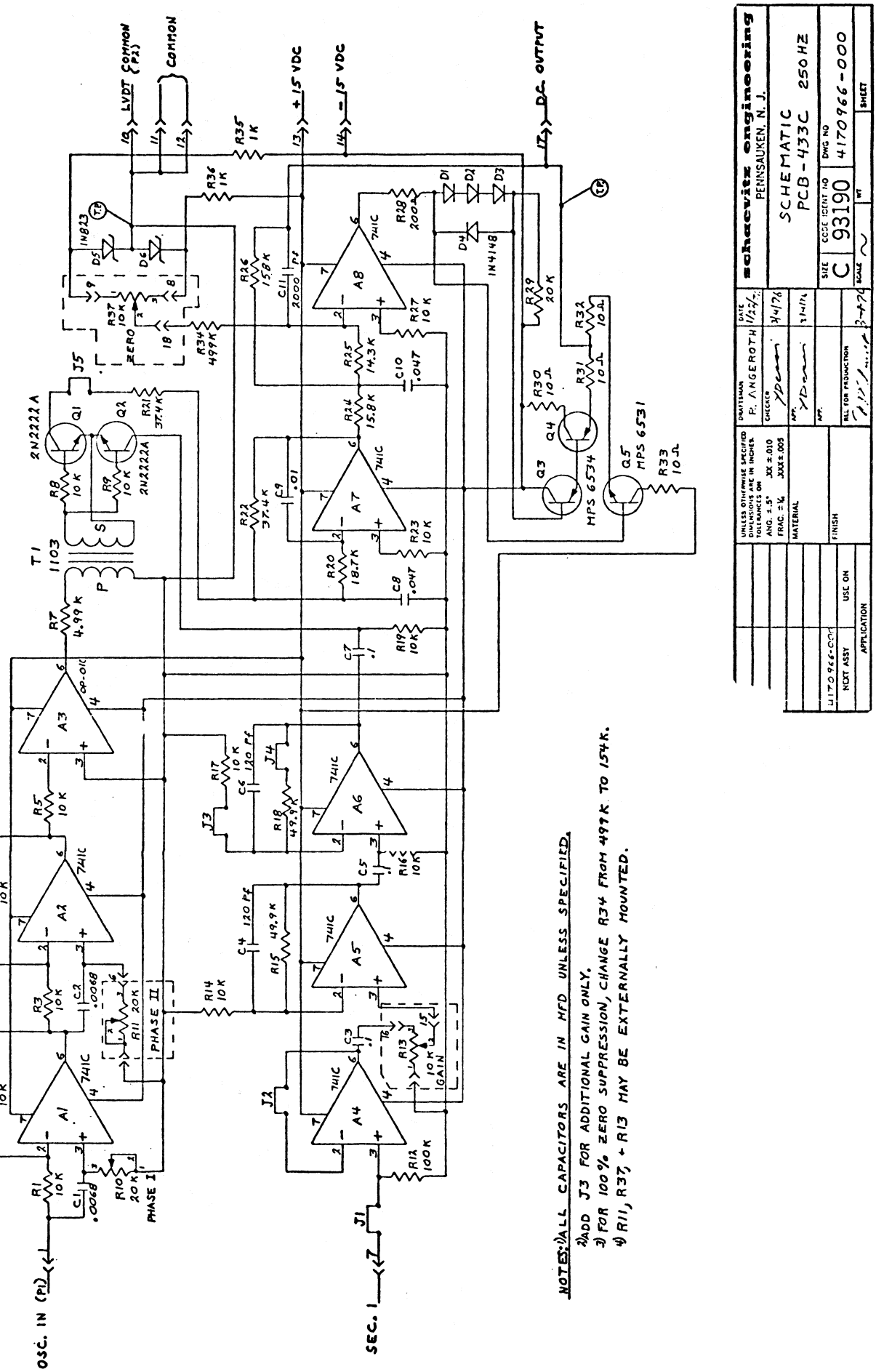
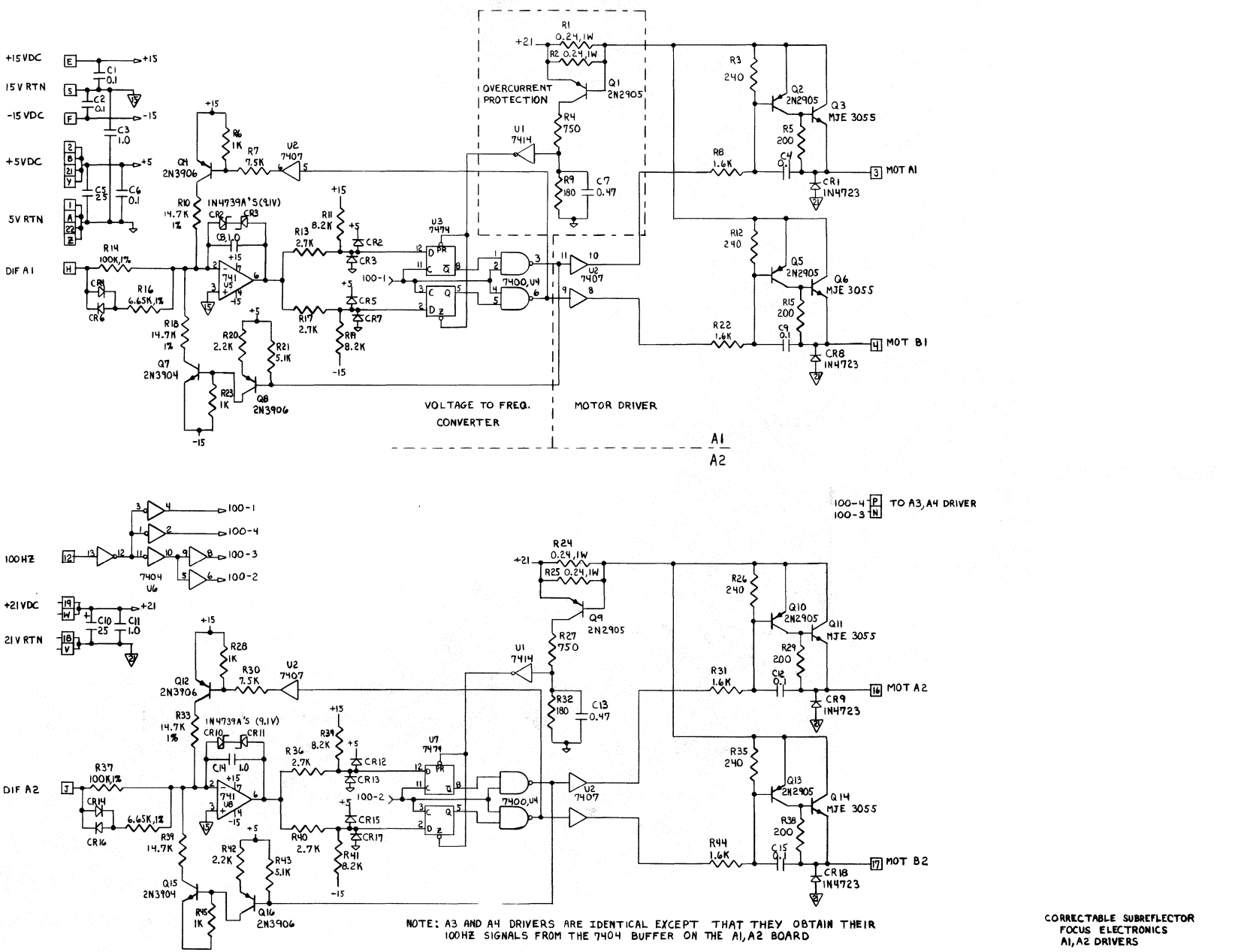


Figure 13. LVDT Demodulator Schematic



CORRECTABLE SUBREFLECTOR
FOCUS ELECTRONICS
A1,A2 DRIVERS

R.LACASSE 6-2-78

Figure 14. Focus Electronics, A1, A2 Drivers Schematic

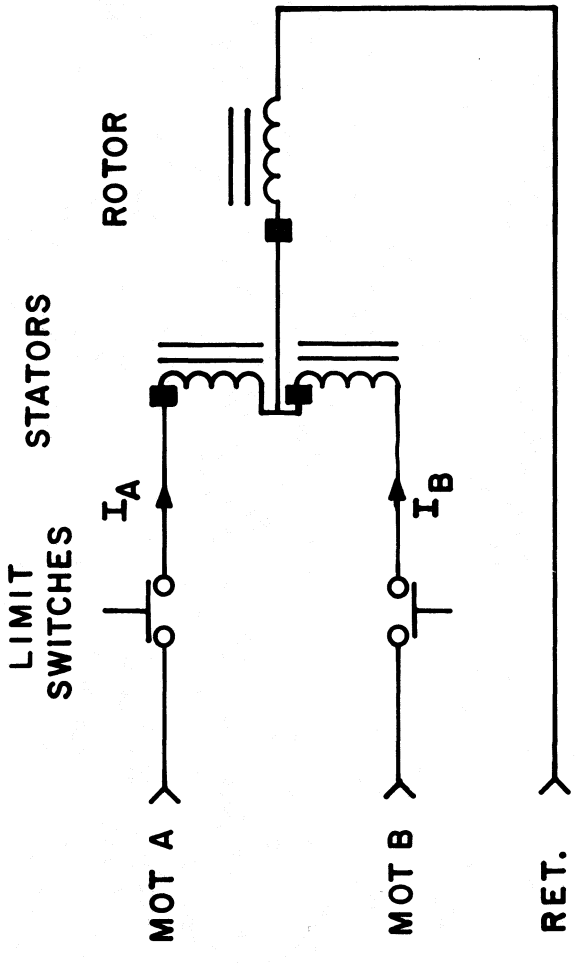


Figure 15. Actuator Motor Schematic

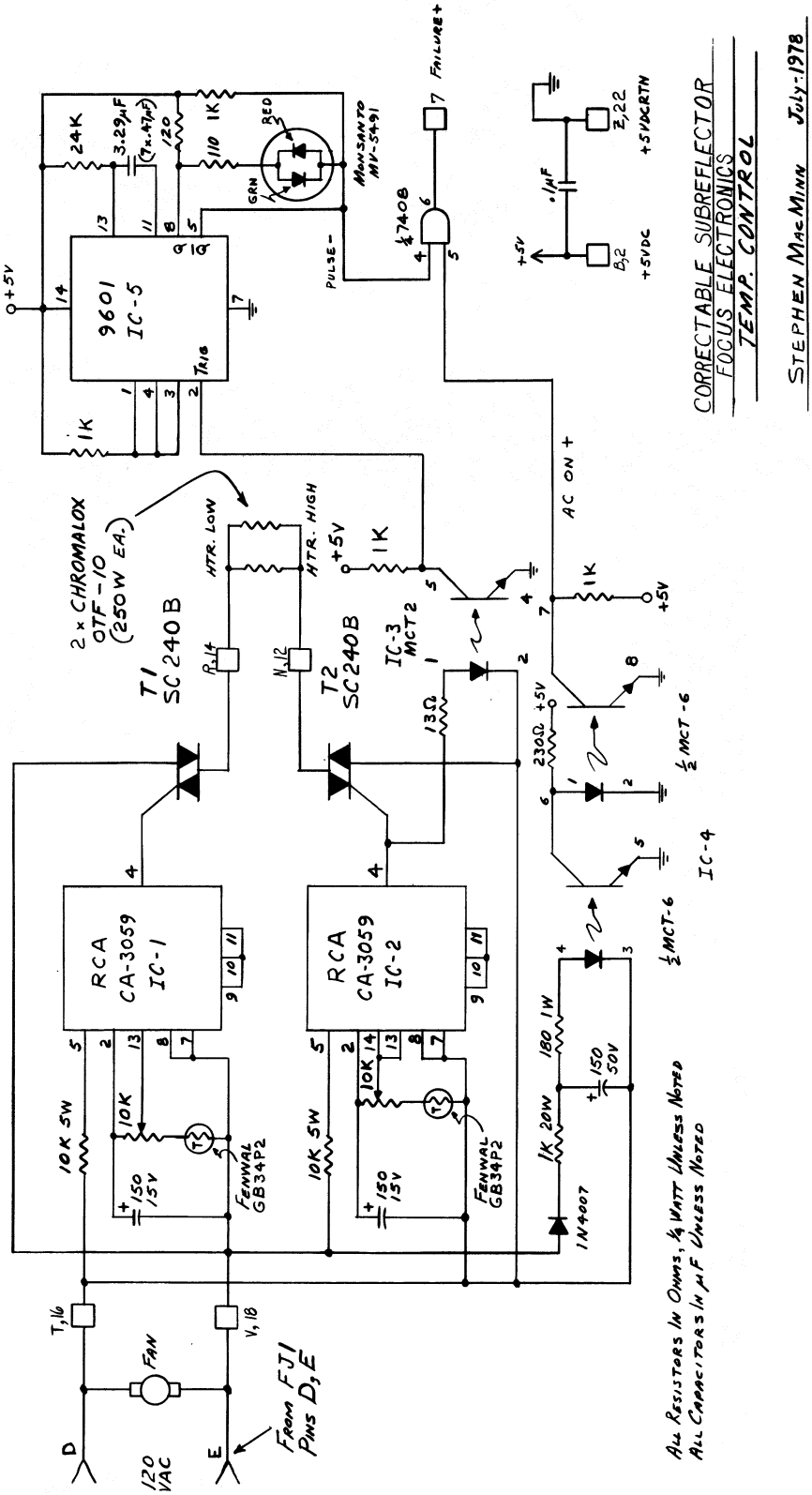


Figure 16. Focus Electronics, Temperature Controller Schematic

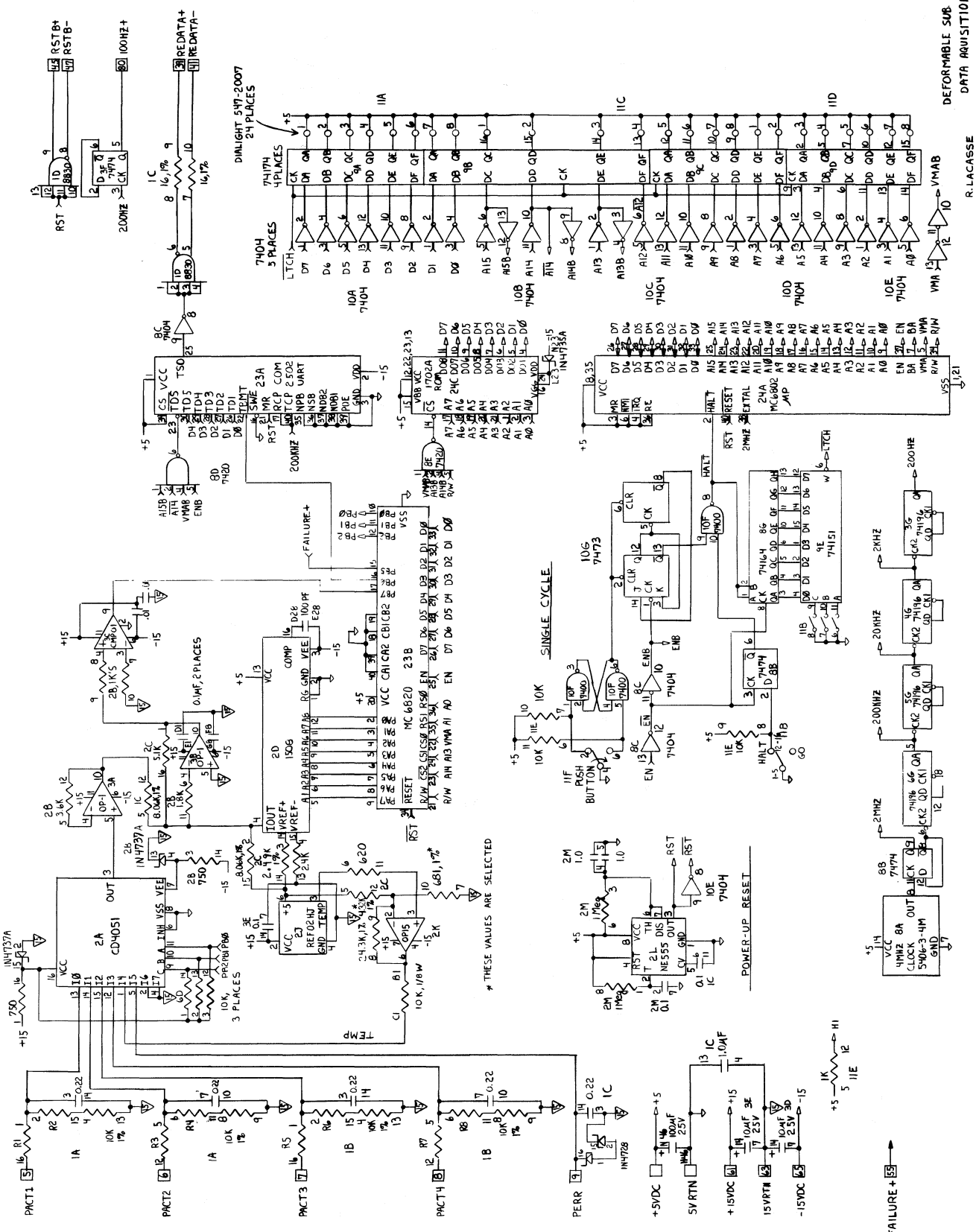


Figure 17. Focus Electronics, Data Acquisition Schematic

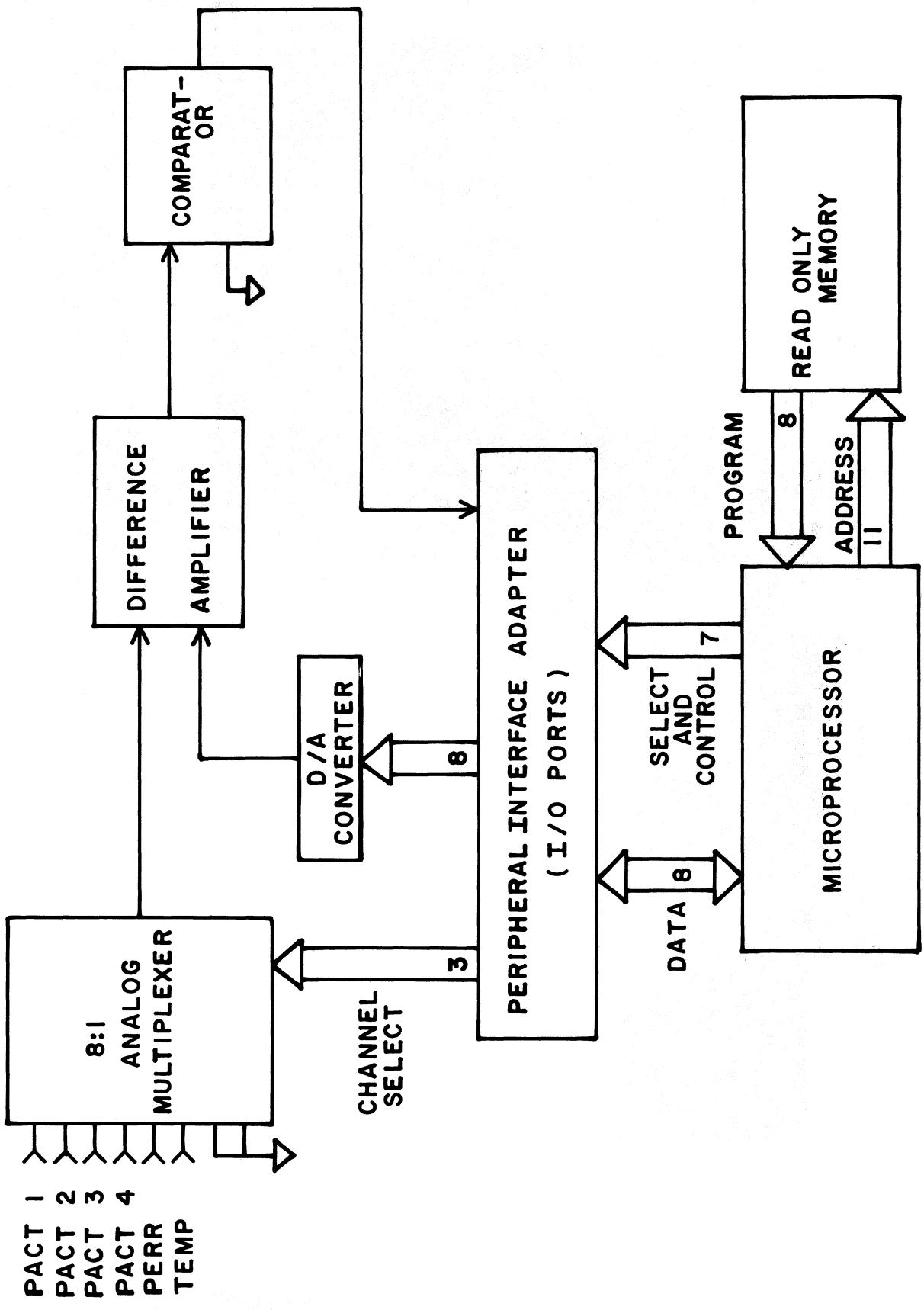


Figure 18. Data Digitizer Block Diagram

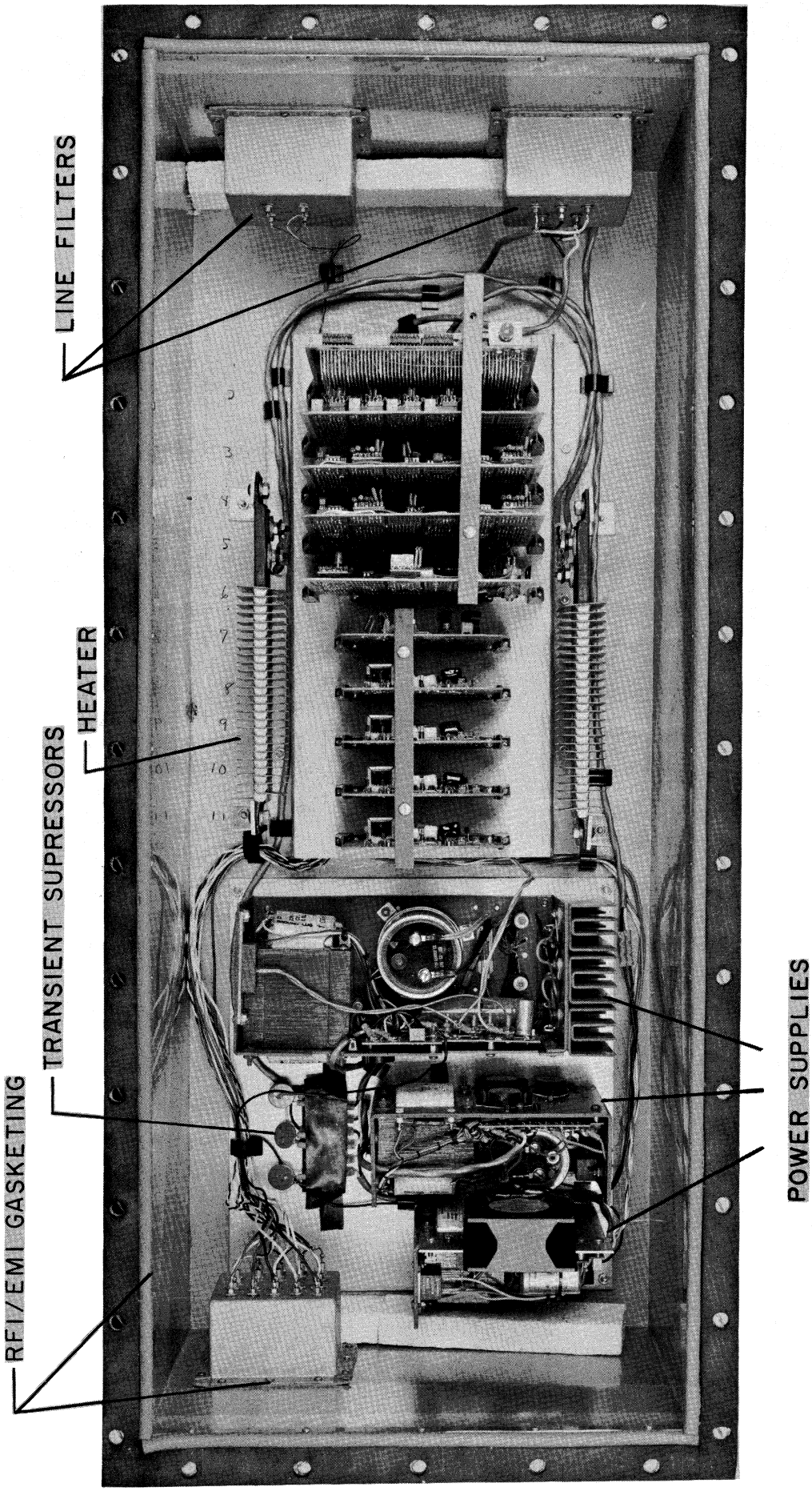


Figure 19. View of the Focus Box with Cover Removed

APPENDIX A

Additional Specifications

This appendix details some of the specifications presented in Section 3.0. Errors introduced by various subsystems due to aging and temperature variations are detailed. These numbers are based on manufacturer's specifications. The effect of servo bandwidth, or, finite positioning time is shown. The data formats for communication with the H-316 control computer are detailed. Finally, a table which converts the front panel temperature readout to Centigrade degrees is included.

Calculated Stability Errors in Electronics
[Temperature Range 25°C to 50°C]

	Percent of 3.18 mm
LVDT Non-Linearity	.175
Oscillators for LVDT's, Amplitude Temperature Dependence	.5
Oscillators for LVDT's Time Dependence	.003
Amplifier/Demodulator for LVDT's:	
Temperature	1.0
Non-Linearity	.0035
Time	.05
D/A Converter	
Non-Linearity	.19
Temperature	.05
D/A Voltage Reference, Temperature	.06
D/A Amplifier (Summing Amplifier)	
I to V, Temperature	.125
D/A Offset, Temperature	.233
Actuator Position, Temperature	.225
Op Amp Offset, Temperature	.01
Compensation Op-Amp	
Offset, Temperature	.032
Time Dependence of Above Four Elements (EST)	.05
RSS Total	1.20%
Equivalent to	.038 mm
or	1.5 mils

APPENDIX A (Continued):

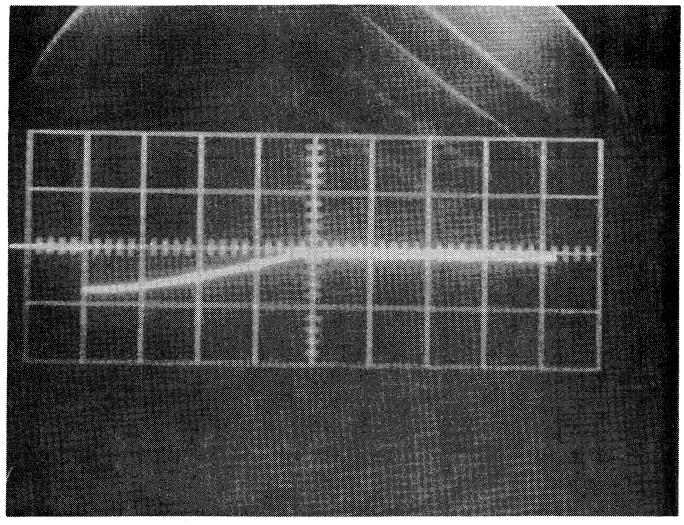
Finite Positioning Time Error Calculation

An average positioning error is introduced by the finite positioning time of the servo. This is because the servo's response to a step command change is roughly exponential. The magnitude of this error can be calculated as follows:

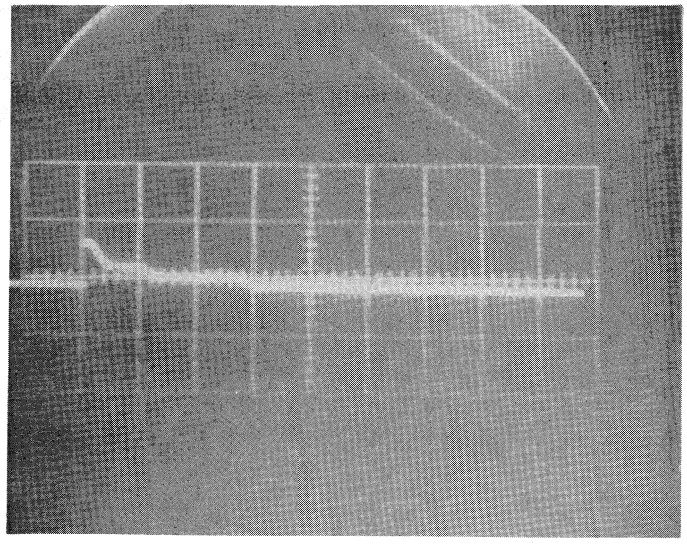
Telescope motion of 70° in elevation requires 160 position steps of the subreflector controller. Integrating the error shown in Figure A-1-a yields about .006 mm · sec. In tracking mode the telescope travels 70° in about 16,800 sec. Thus we can calculate

$$\text{Average Error} = \frac{\text{Positioning Error}}{\text{Average Time Between Steps}} = \frac{.006 \text{ mm} \cdot \text{sec}}{16{,}800/160} = 5.7 \times 10^{-5} \text{ mm}$$

(A)
COMMAND = 2 MM
HORIZONTAL = 0.2 SEC/DIV.



(B)
COMMAND = 0.02 MM
HORIZONTAL = 0.2 SEC/DIV.



(C)
COMMAND = 0.02 MM
HORIZONTAL = 0.2 SEC/DIV.
NOTE THAT THE ERROR DOES NOT RETURN TO ZERO DUE TO THE LIMIT CYCLE.

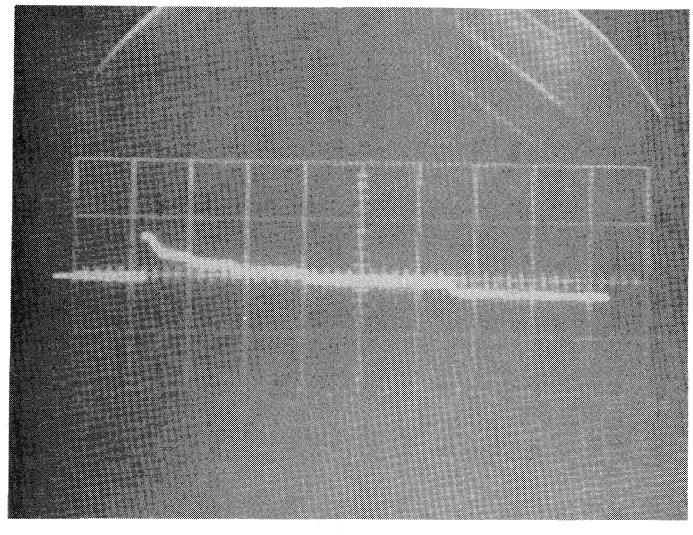


FIGURE A-1: LOOP ERROR, IN RESPONSE TO LARGE AND SMALL COMMANDS

APPENDIX A (Continued):

Formats for Data Exchanges Between the H-316 Computer and Correctable Subreflector Controller Interface

From Interface to H-316

Address Bus = $\emptyset 52_8$

Input Bus

INB-1	Computer/Manual, Computer = 1
INB-2	Temperature Error = 0
INB-3	Lock Error = 0
INB-9	MSB
	→ Electronic Limit
INB-16	LSB

From H-316 to Interface

Address Bus = 152_8

Output Bus

OTB-5	Actuator Address MSB	00 = A1, etc.
OTB-6	Actuator Address LSB	
OTB-9	MSB	
	→ Position Command	
OTB-16	LSB	

Note: The position commands should be given in sequence, i.e., A1 first and A4 last.

TABLE A-1

Temperature Conversion

(Digital Interface Readout to °C)

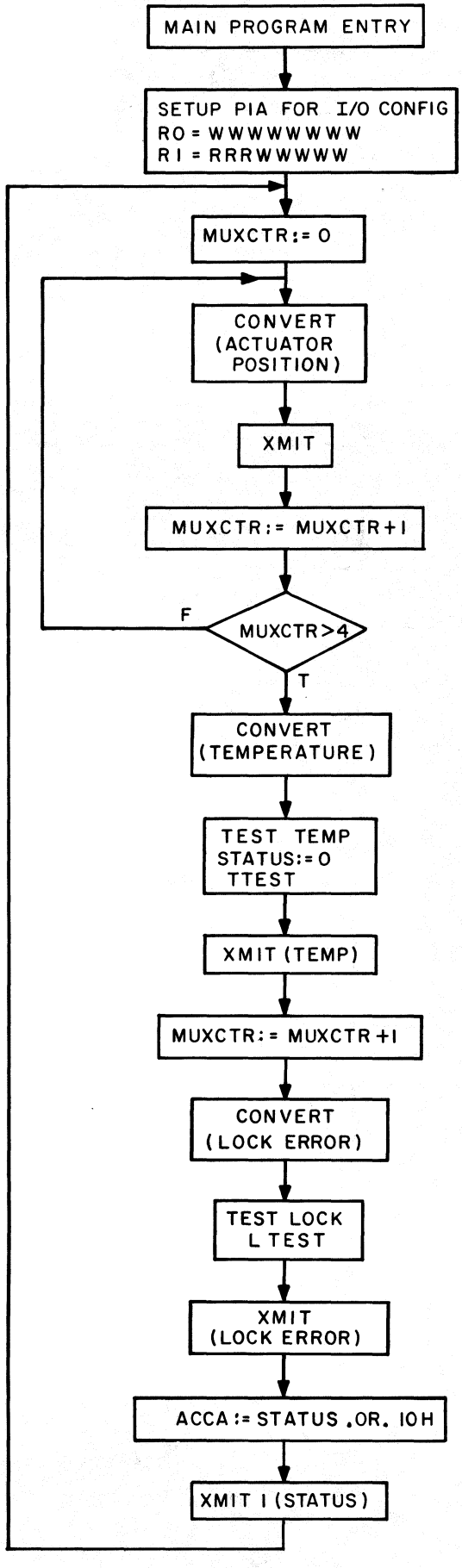
Readout	Temperature °C	Readout	Temperature °C
0.00	-40	1.70	+24
0.10	-36	1.80	28
0.20	-33	1.90	31
0.30	-29	2.00	35
0.40	-25	2.10	39
0.50	-21	2.20	43
0.60	-18	2.30	46
0.70	-14	2.40	50
0.80	-10	2.50	54
0.90	-6	2.60	58
1.00	-3	2.70	61
1.10	+1	2.80	65
1.20	5	2.90	69
1.30	9	3.00	73
1.40	13	3.10	76
1.50	16	3.20	80
1.60	20		

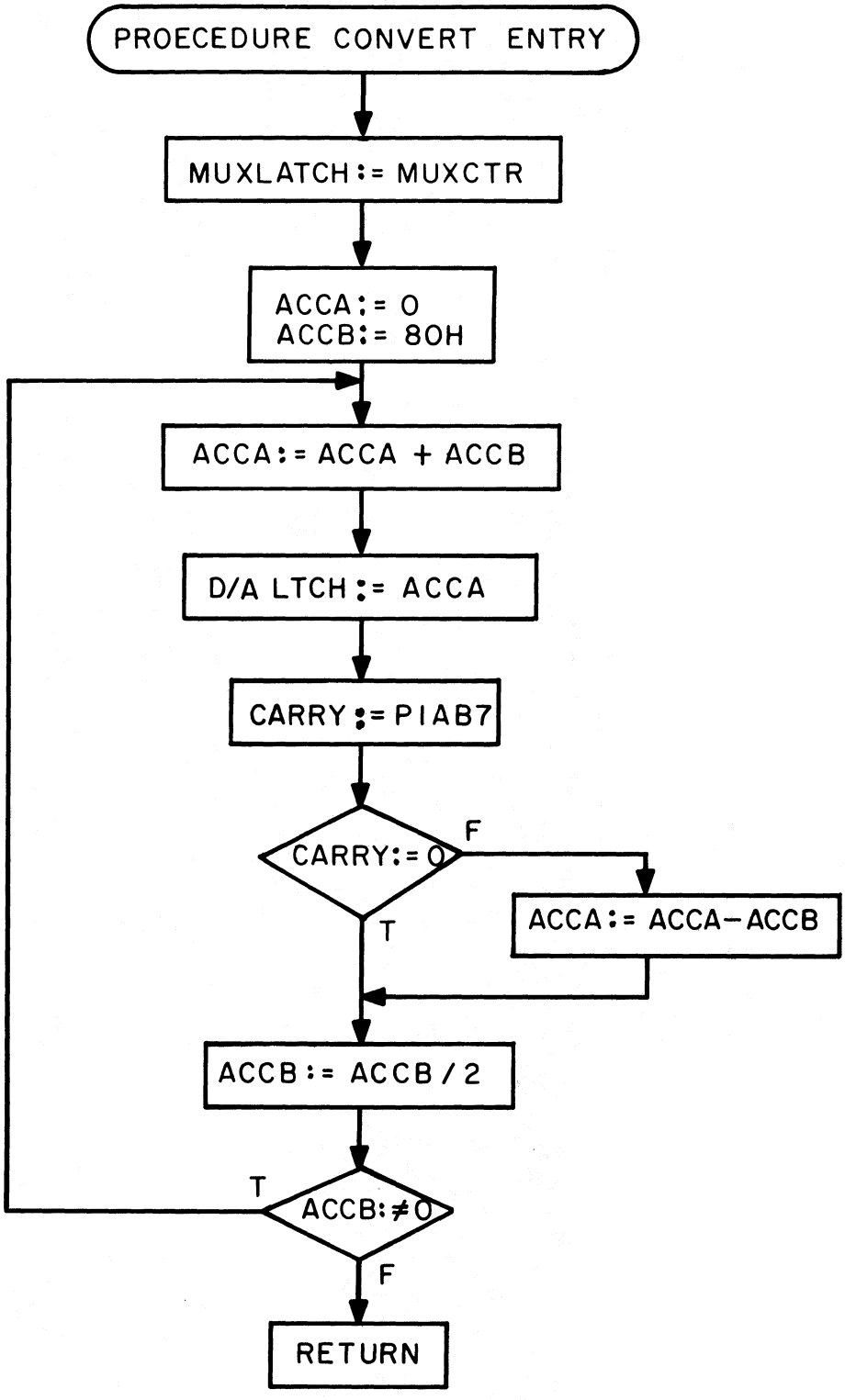
APPENDIX B

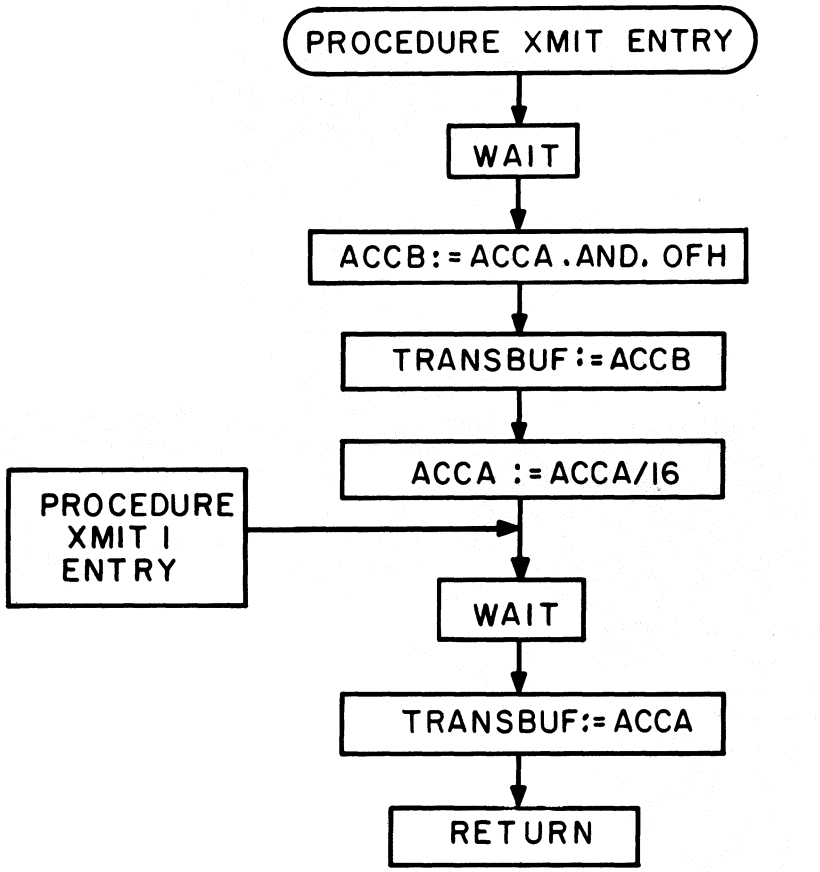
Flow Chart of Data Acquisition Firmware

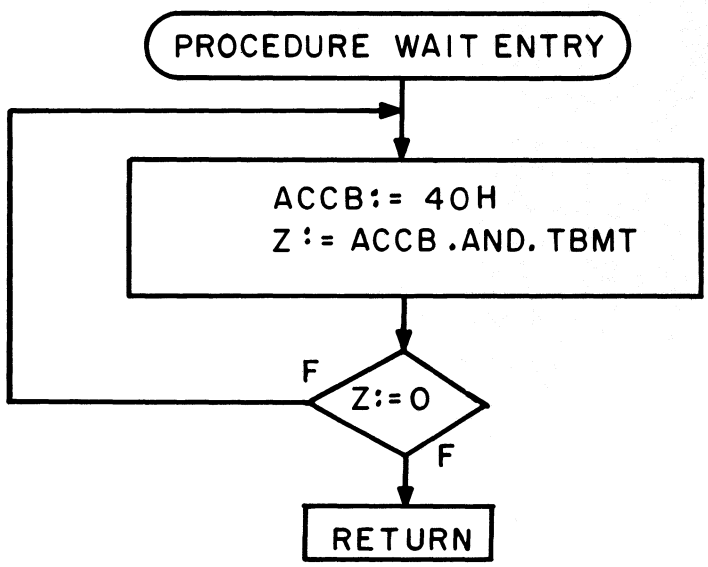
This appendix contains the flow chart description of the firmware used in the Correctable Subreflector Controller Data Acquisition firmware. The flow chart consists of five parts. First is the Main Program which does initialization and controls subroutine calls. Second is the CONVERT Subroutine which handles the A/D conversion. Third is the XMIT Subroutine which formats data and supervises its transmission. Fourth is the TTEST Subroutine which flags temperature errors. Fifth is the LTEST Subroutine which flags servo lock errors. The program listing is also included.

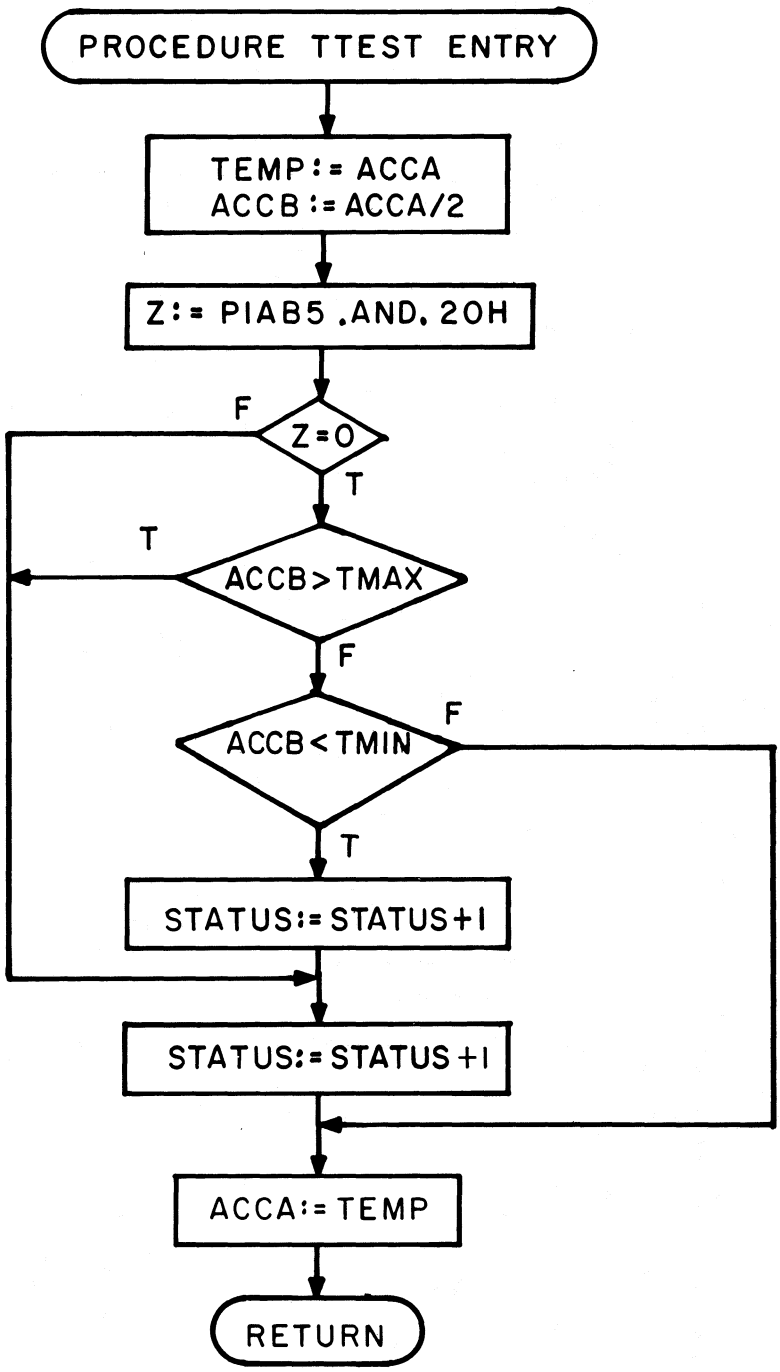
DATA ACQUISITION SYSTEM FIRMWARE

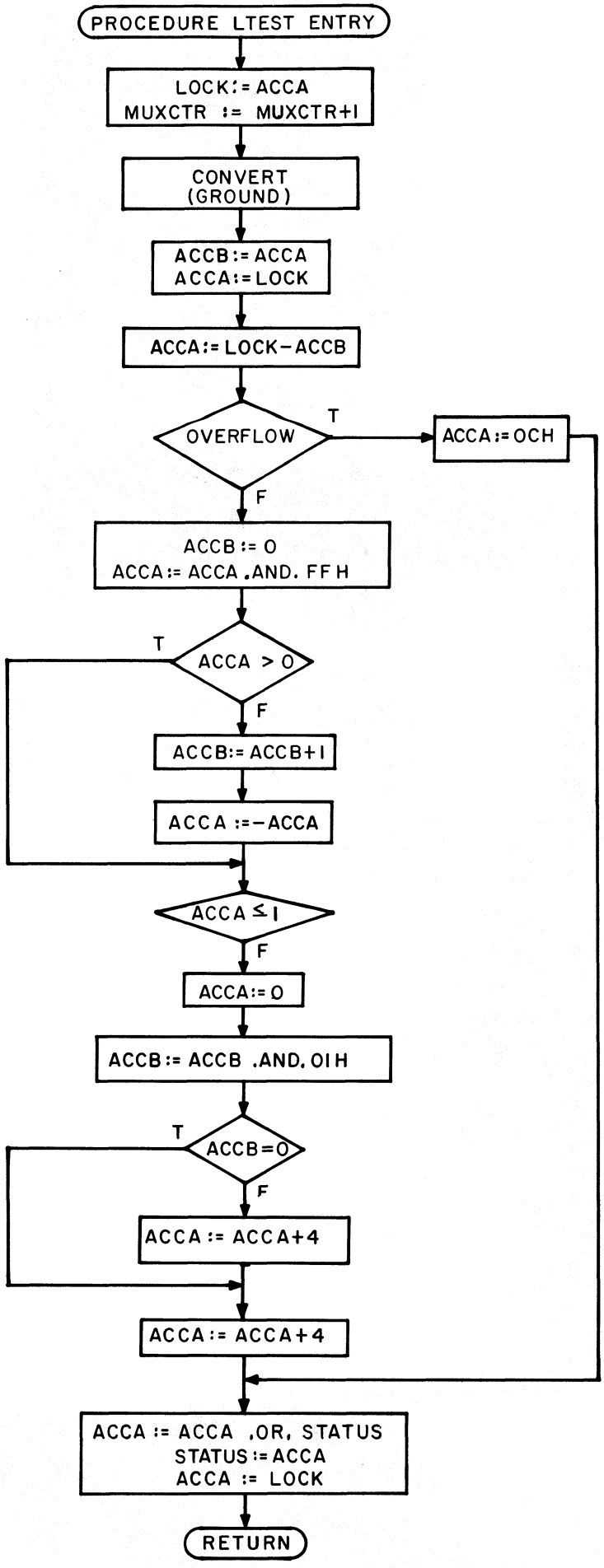



PROECEDURE CONVERT ENTRY
MUXLATCH := MUXCTR
ACCA := 0
ACCB := 80H
ACCA := ACCA + ACCB
D/A LTCH := ACCA
CARRY := PIAB7
CARRY := 0
F
T
ACCA := ACCA-ACCB
ACCB := ACCB / 2
T
ACCB := ≠0
F
RETURN


PROCEDURE XMIT ENTRY
WAIT
ACCB:=ACCA.AND. OFH
TRANSBUF:=ACCB
ACCA :=ACCA/16
PROCEDURE XMIT I ENTRY
WAIT
TRANSBUF:=ACCA
RETURN


PROCEDURE WAIT ENTRY
ACCB:= 40H
Z := ACCB .AND. TBMT
F
Z:=0
F
RETURN


PROCEDURE TTEST ENTRY
TEMP:= ACCA
ACCB:= ACCA/2
Z:= PIAB5 .AND. 20H
F
Z=0
T
T
ACCB>TMAX
F
F
ACCB<TMIN
T
STATUS:= STATUS+1
STATUS:= STATUS+1
ACCA:= TEMP
RETURN


PROCEDURE LTEST ENTRY
LOCK:=ACCA
MUXCTR := MUXCTR+1
CONVERT (GROUND)
ACCB:=ACCA
ACCA:=LOCK
ACCA:=LOCK-ACCB
OVERFLOW
T
ACCA:=0CH
F
ACCB:=0
ACCA:=ACCA .AND. FFH
T
ACCA > 0
F
ACCB:=ACCB+1
ACCA :=-ACCA
ACCA ≤ 1
F
ACCA:=0
ACCB:=ACCB .AND. 01H
T
ACCB=0
F
ACCA := ACCA+4
ACCA := ACCA+4
ACCA := ACCA .OR. STATUS
STATUS:=ACCA
ACCA := LOCK
RETURN

APPENDIX B (Continued):

```
*** $MAIN - Data Acquisition System, V2.0
*
*
*
*
*
```

ADDR	INSTR		LABEL	MNEUMONIC		COMMENTS
0000	CE 20 00		PIAINIT	LDX	2000H	POINTS TO PIA
0003	6F 01			CLR	CONREGA	SET UP FOR DATA-
0005	6F 03			CLR	CONREGB	DIRECTION WRITE.
0007	86 1F			LDAA	FFH	
0009	A7 00			STAA	DATDIRA	RØ = WWWWWWWW
000B	86 IF			LDAA	1FH	
000D	A7 02			STAA	DATDIRB	R1 = RRRWWWWW
000F	86 04			LDAA	Ø4H	NOW, SET UP TO TALK
0011	A7 01			STAA	CONREGA	TO DATA BUFFERS,
0013	A7 03			STAA	CONREGB	AND FALL INTO ...
0015	8E ØØ 7F		BEGIN	LDS	ØØ7FH	SET UP THE STACK.
0018	7F ØØ ØØ		REPEAT	CLR	MUXCTR	
001B	8D 26	X	SENDACT	BSR	CONVERT	SEND THE ACTUATOR DATA.
001D	8D 3A	X		BSR	XMIT	
001F	7C ØØ ØØ			INC	MUXCTR	
0022	C6 Ø4			LDAB	Ø4H	ALL FOUR ACTUATORS
0024	F1 ØØ ØØ			CMPB	MUXCTR	FINISHED? IF NOT, DO
0027	2E F2	X		BGT	SENDACT	IT AGAIN: IF SO, FALL
						INTO ...
0029	8D 18	X		BSR	CONVERT	GET THE TEMP.
002B	7F ØØ Ø2			CLR	STATUS	
002E	8D 42	X		BSR	TTEST	TEST TEMP.
0030	8D 27	X		BSR	XMIT	SEND TEMP.
0032	7C ØØ ØØ			INC	MUXCTR	
0035	8D ØC	X		BSR	CONVERT	GET LOCK CONDITION.
0037	8D 54	X		BSR	LTEST	TEST LOCK CONDITION.
0039	8D 1E	X		BSR	XMIT	SEND LOCK CONDITION.
003B	96 02			LDAA	STATUS	
003D	8A 1Ø			ORAA	1ØH	SEND STATUS BYTE AND
003F	8D 24	X		BSR	XMITSTA	END OF FRAME BIT.
0041	2Ø D5	X		BRA	REPEAT	DO IT ALL AGAIN.

APPENDIX B (Continued):

```
*** $CONVERT - Do a Software Successive Approximation
*
*   ENTRY    - Channel # in MUXCTR
*   EXIT     - Digitized value in A
*   CALLS    - None
*   USES     - A, B
```

ADDR	INSTR		LABEL	MNEUMONIC		COMMENTS
0043	96 ØØ		CONVERT	LDAA	MUXCTR	
0045	A7 Ø2			STAA	MUXLATCH	SELECT INPUT CHANNEL.
ØØ47	C6 80			LDAB	8ØH	
ØØ49	4F			CLRA		ACCUMULATE RESULT HERE.
ØØ4A	1B		SARLOOP	ABA		
004B	A7 ØØ			STAA	D/ALTCH	COMPARE 'EM.
004D	A6 Ø2			LDAA	PIAB7	
004F	49			ROLA		
0050	A6 ØØ			LDAA	D/ALTCH	GET VALUE BACK.
0052	24 01	X		BCC	.FWD	
0054	10			SBA		TOO BIG.
0055	54		.FWD	LSRB		NEXT BIT.
0056	24 F2	X		BCC	SARLOOP	
0058	39			RTS		GO HOME.

APPENDIX B (Continued):

```
*** $XMIT        - Transmit down to control room.
*   ENTRY POINTS - XMIT, XMITSTA
*   XMIT         - Sends a byte down to the control
*                  room thru the UART in two nibbles,
*                  low then high.
*   XMITSTA      - Sends low 5 bits of A as is (UART only
                                                  sends 5 bits)
*   ENTRY        - Byte to be sent is in A.
*   EXIT         - None.
*   CALLS        - Wait (internal, uses B).
*   USES         - A, B.
```

ADDR	INSTR		LABEL	MNEUMONIC		COMMENTS
0059	8D 10	X	XMIT	BSR	WAIT	
ØØ5B	16			TAB		
005C	C4 ØF			ANDB	ØFH	GET LOW NIBBLE.
ØØ5E	F7 80 00			STAB	TRANSBUF	SEND IT.
0061	44			LSRA		GET HIGH NIBBLE.
0062	44			LSRA		
0063	44			LSRA		
0064	44			LSRA		
0065	8D Ø4	X	XMITSTA	BSR	WAIT	WHEN UART'S READY
0067	B7 8Ø ØØ			STAA	TRANSBUF	... SEND IT
006A	39			RTS		... AND GO HOME.
006B	C6 40		WAIT	LDAB	4ØH	
006D	E5 02		.BACK	BITB	TBE	WAIT FOR TBE
006F	27 FC	X		BEQ	.BACK	
0071	39			RTS		

APPENDIX B (Continued):

```
*** $TTEST - See if temp within limits.
*
*     ENTRY - Temp in A, Status = 0.
*     EXIT  - Too high, bit Ø of status set too low;
*             Bit 1 of status set o.k.; status unchanged.
*     CALLS - None.
*     USES  - B.
```

ADDR	INSTR		LABEL	MNEUMONIC		COMMENTS
0072	16		TTEST	TAB		
0073	54			LSRB		÷2
0074	97 Ø3			STAA	TEMP	
0076	86 2Ø			LDAA	2ØH	SET FAILURE BIT FROM
0078	A5 Ø2			BITA	PIAB5	HEATER AND TEST IT.
007A	26 ØB	X		BNE	>TMAX	
007C	C1 46			CMPB	TMAX	
007E	2E Ø7	X		BGT	>TMAX	
0080	C1 1A			CMPB	TMIN	
0082	2E Ø6	X		BGT	TOK	
0084	7C ØØ Ø2			INC	STATUS	
0087	7C ØØ Ø2		>TMAX	INC	STATUS	
008A	96 Ø3		TOK	LDAA	TEMP	
008C	39			RTS		

APPENDIX B (Continued):

```
*** $LTEST - Test lock condition   V2.0
*
*   ENTRY  - Lock value in A, MUXCTR = 5.
*   EXIT   - Too high, bit 3 of status set.
*            Too low,  bit 2 of status set.
*            Indeterminate, both 2 and 3 set.
*            Locked, no change in status, neither set.
*   CALLS  - Convert.
*   USES   - A, B.
```

ADDR	INSTR		LABEL	MNEUMONIC		COMMENTS
ØØ8D	97 04		LTEST	STAA	LOCK	
ØØ8F	7C ØØ ØØ			INC	MUXCTR	
ØØ92	8D AF	X		BSR	CONVERT	
ØØ94	16			TAB		
ØØ95	96 Ø4			LDAA	LOCK	
ØØ97	10			SBA		
ØØ98	29 1E	X		BVS	TOOBIG	
ØØ9A	5F			CLRB		
ØØ9B	84 FF			ANDA	FFH	SET CONTROL BITS.
ØØ9D	2E Ø2	X		BGT	.LFWD	
ØØ9F	5C					
ØØAØ	4O			NEGA		
ØØA1	81 Ø1		.LFWD	CMPA	Ø1H	|LOCK - GND|
ØØA3	23 ØD	X		BLS	ENDL	|LOCK - GND| ≤ 1
ØØA5	4F			CLRA		
ØØA6	C4 Ø1			ANDB	Ø1H	
ØØA8	27 Ø2	X		BEQ	ADD4	
ØØAA	8B Ø4			ADDA	Ø4H	
ØØAC	8B Ø4			ADD4	ADDA Ø4H	
ØØAE	9A Ø2		.LT2	ORAA	STATUS	
ØØBØ	97 Ø2			STAA	STATUS	
ØØB2	96 Ø4		ENDL	LDAA	LOCK	
ØØB4	39			RTS		
ØØB5	86 ØC		TOOBIG	LDAA	ØCH	SET 2 AND 3.
ØØB7	20 F5	X		BRA	.LT2	

APPENDIX C

Temperature Controller Performance Data

This appendix contains a graph showing the performance of the Temperature Controller with Focus Electronics. Box temperature and heater duty cycle are plotted against time. Also included is a drawing depicting the test set-up used to obtain this graph.

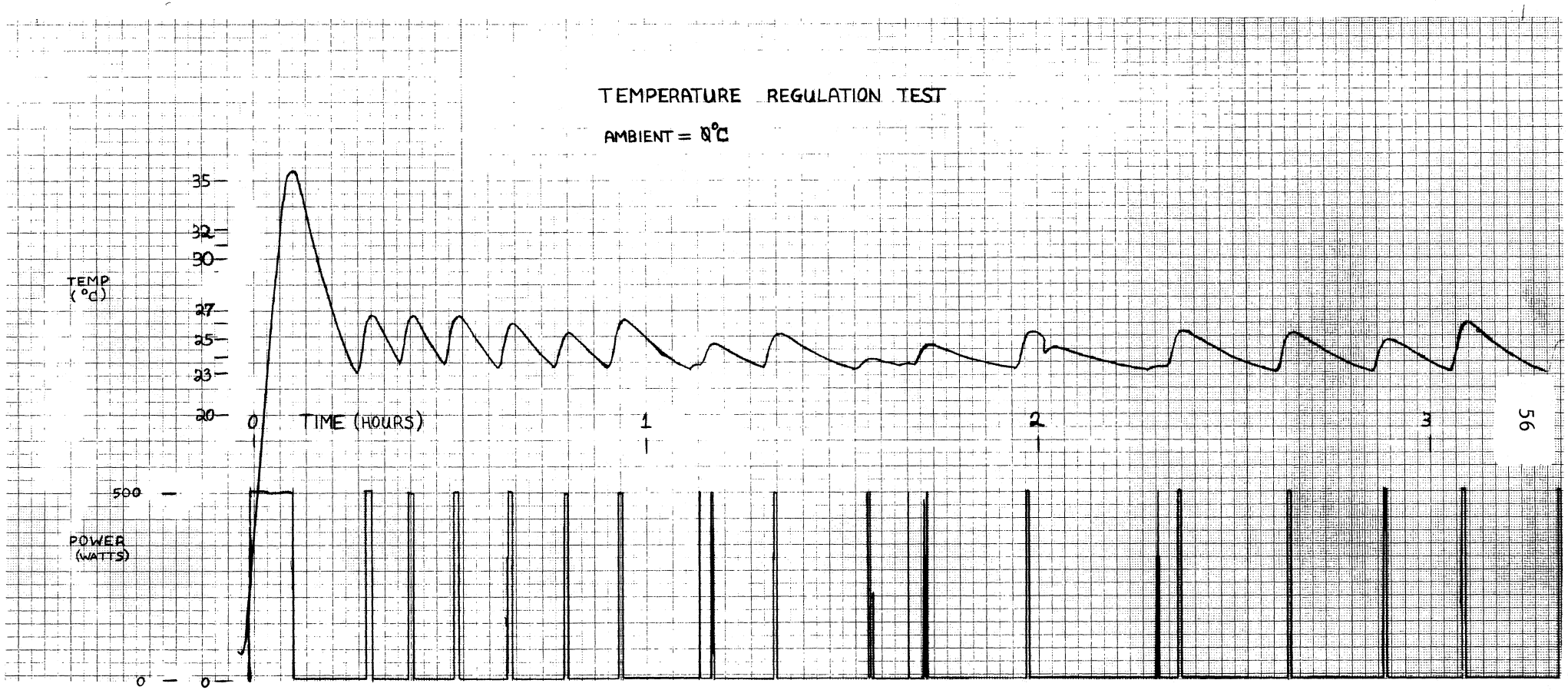


Figure C-1. Temperature Controller Test Results

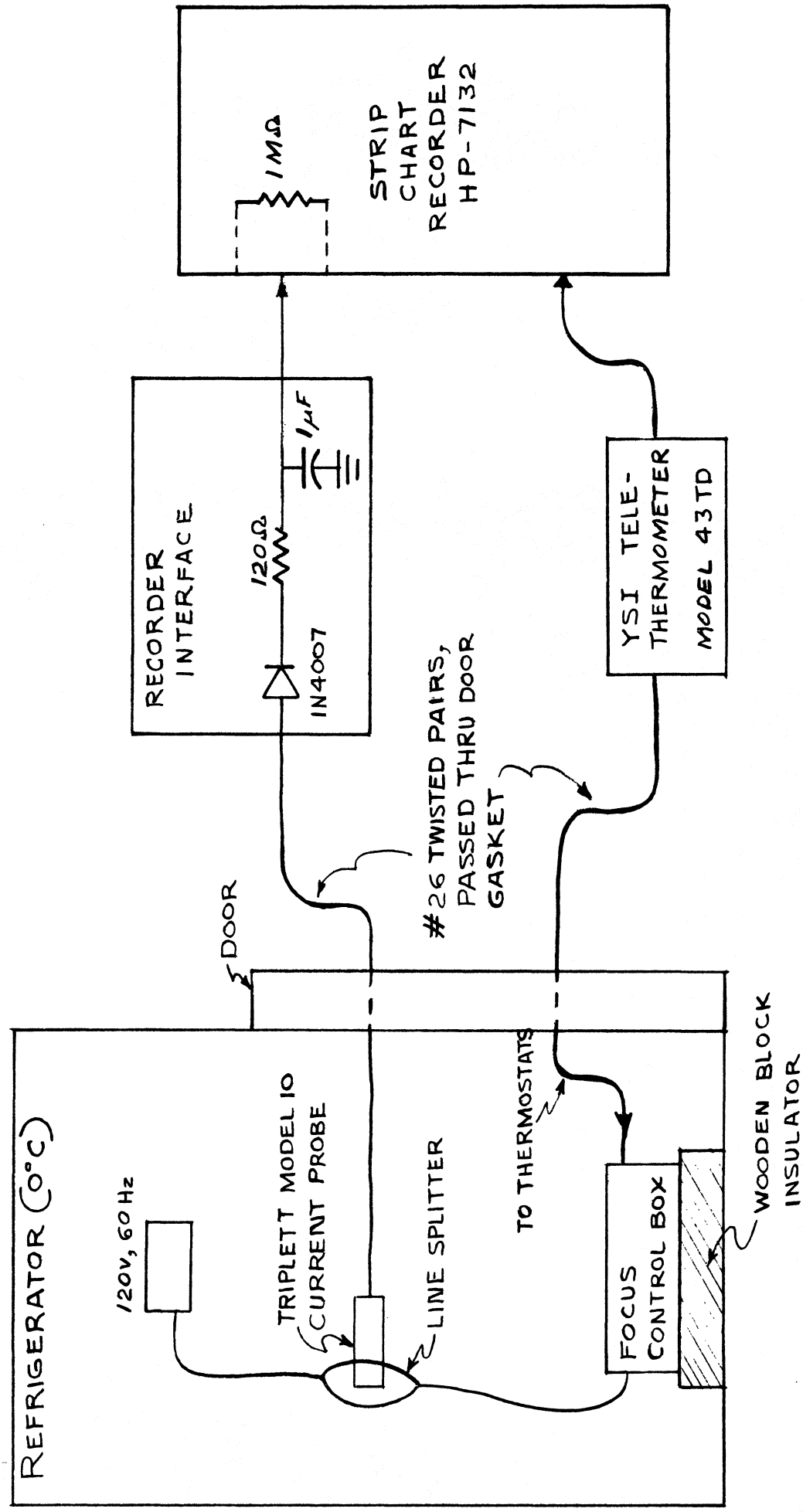


Figure C-2. Temperature Controller Test Setup