NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT No. 187

THE NRAO VLBI MARK II PROCESSOR

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JUNE 1978

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INDEX

THE NRAO VLBI MARK II PROCESSOR

CHAPTER 1: Introduction

This report describes the hardware developments of the Mark II VLBI processor during the past four years. The reader is referred to NRAO Electronics Division Internal Report #118, in which the principle of the Mark II system is described. The processor control program is described in NRAO User's Manual #26. We will limit this report to the processor and describe in detail all needed features.

Summary of changed and added hardware features (see Figures 1.2, 1.3, 1.10):

The old 190 channel correlator was replaced by a larger 576 channel correlator.

The new correlator works with eith 1, 2 or 3 stations and processes autocorrelation, cross-correlation or a combination thereof in any one of 8 modes.

A self-checking feature was added to the correlator which insures that the correlator circuitry is working properly.

Nine extra channels for total counts were added in addition to the correlator channels.

The fringe rotator was redesigned.

The two-station (Leach) buffer was replaced by a three-station buffer.

Buffers B and C were enlarged to 81,920 bits. One may add a delay from 0 to 19,456 μs under program control for source switching experiments.

The previously open head drum servo loop was closed.

The audio decoder was redesigned.

The video decoder was redesigned and accepts MK-II or MK-II-C format.

The buffer was designed so that VR-660 or IVC-825 video recorders may be connected on any of the inputs.

The buffer was designed so that when an error is detected for the 512 μs sync word the correlator is blanked during the previous 512 μs of data.

A blanking circuit was added that insures that invalid data is shifted out of the correlator before the correlator is unblanked.

A special FFT processor was added to the system to calculate spectra and correct for fractional bit shift.

Block diagram Figure 1.2 shows the overall system.

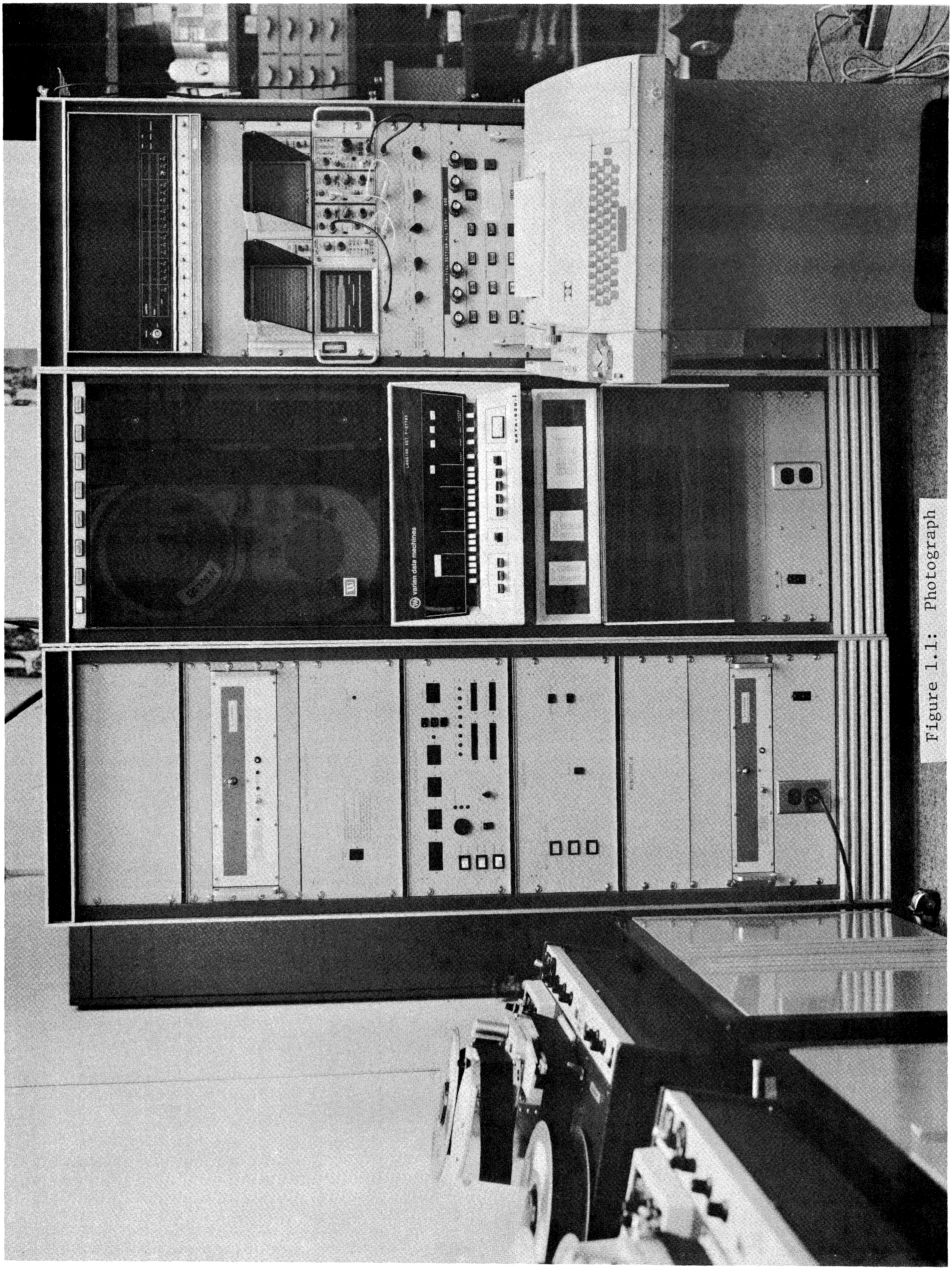

Figure 1.1: Photograph

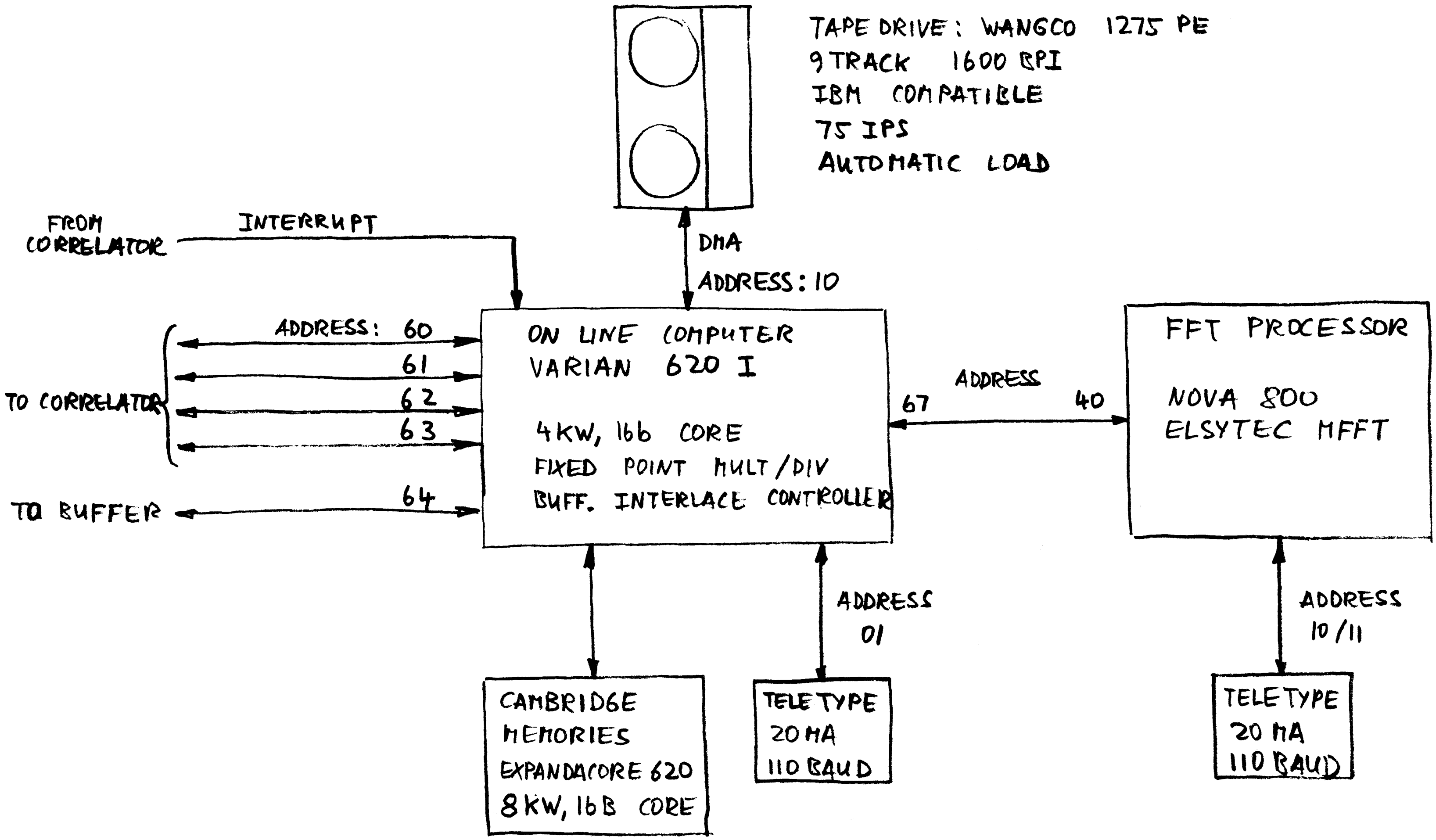

FIGURE 1.2: CONTROL COMPUTER AND FFT PROCESSOR.

Specification of Buffer:

Inputs from each of three video recorders:

- ASTRODATA: clipped diphase video signal at 4 Mb/s, 0.3-15 V_{pp} into 75Ω
- HEADSWITCH: 30 Hz square wave, 7 V_{pp}, none for MK II-C
- AUDIO 1: diphase time code at 3.84 Kb/s, 0.5-20 V_{pp}
- AUDIO 2: diphase ID code at 3.84 Kb/s, 0.5-20 V_{pp}

Outputs to each of three video recorders:

- RUN: Relay contact to start-stop recorders
- 60 Hz REFERENCE: 60 Hz TTL square wave to which the recorder motors lock.
- HEAD DRUM: Analog signal $\pm$7V with TC = 5 seconds to control phase of head drum servo. Not used for MK-II-C.

Inputs from Correlator Control:

- REFCLK: 4 MHz square wave, master reference
- UCLK B, C: 4 MHz square wave, unload clock
- MODE 2: correlator mode 2
- ALERT OFF: Disables audible error buzzer

Outputs to correlator control:

- DAT A, B, C: 4 Mb NRZ data
- FRAME A, B, C
- TCD DAT A, B, C: audio NRZ data
- TCD CLK A, B, C: audio clock
- FLERR A, B, C: error count
- DATOK A, B, C: True when data is decoded properly
- XFER: True when processor is ready to correlate

Computer I/O to 1 general purpose Varian interface as assigned in Chapter 3.

Block diagram Figure 1.3 shows the buffer.

The buffer is designed to decode MK II (VR 660) as well as MK II C (IVC 825A) formats shown in Figures 1.4, 1.5, 1.6, 1.7, and 1.8. Buffer A has a small 4,096 bit memory half of which is used to correct for time displacements (jitter) of the tape recorders and the other half is used to keep track of bad 512 μs sync patterns. At the end of every 2,048 bits a 8 bit sync pattern is decoded. If this pattern does not appear or if it is decoded at the wrong time, an error in the pattern or a bit slip has occurred during the last 512 microseconds. When this data is shifted thru the correlator the correlator is blanked by DATOK going false.

Buffer B and C each have a 81,920 bit memory, of which 4,096 bits perform the same function as Buffer A, and 77,824 bits are used for delay of 0 to 19,456 μs. This delay is under program control and may be changed rapidly. Timing and address relations for Buffer A, B and C are shown in Figure 1.9.

TO / FROM AMPEX OR IVC RECORDERS

TO / FROM CORRELATOR

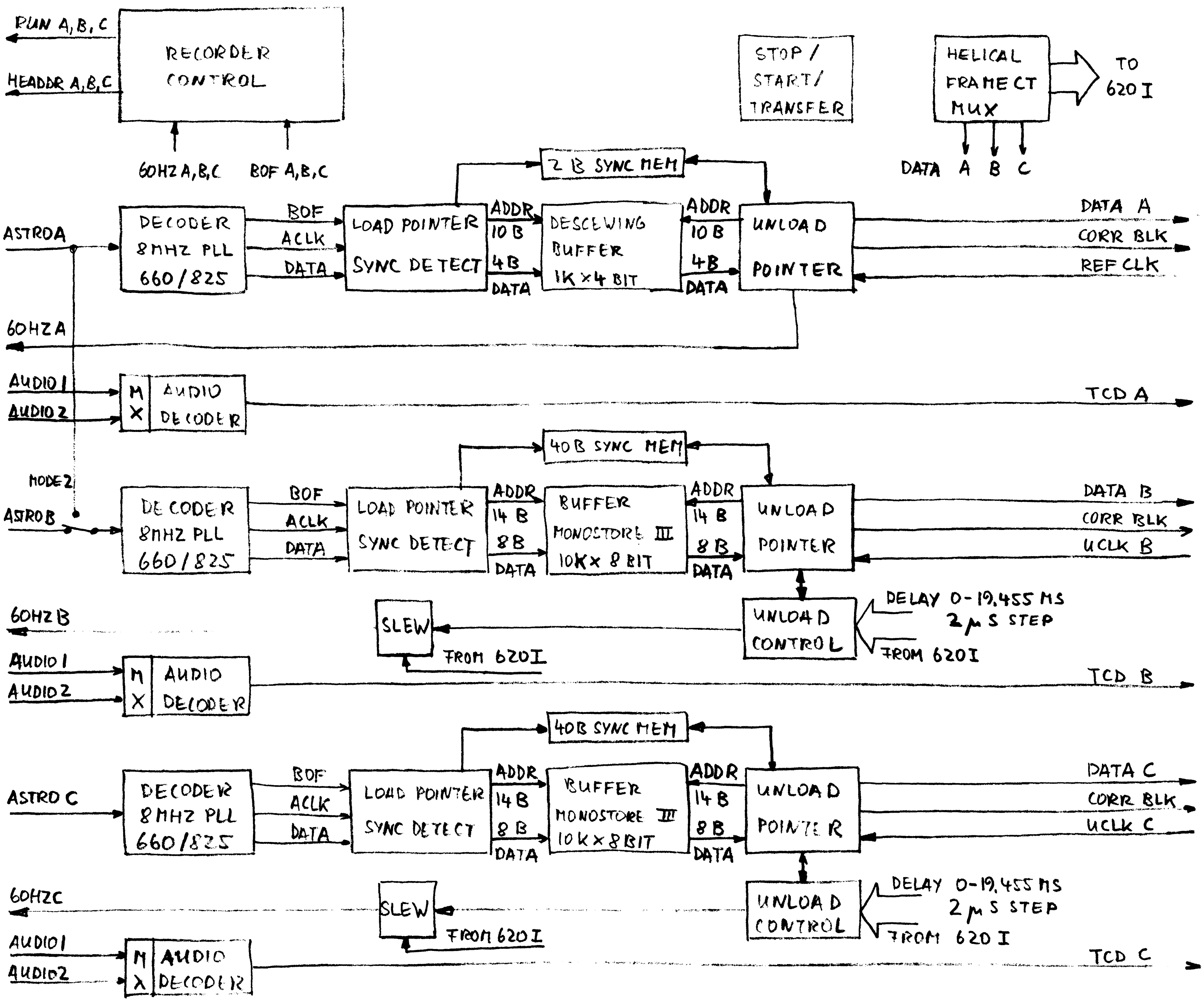

FIGURE 1.3: BUFFER

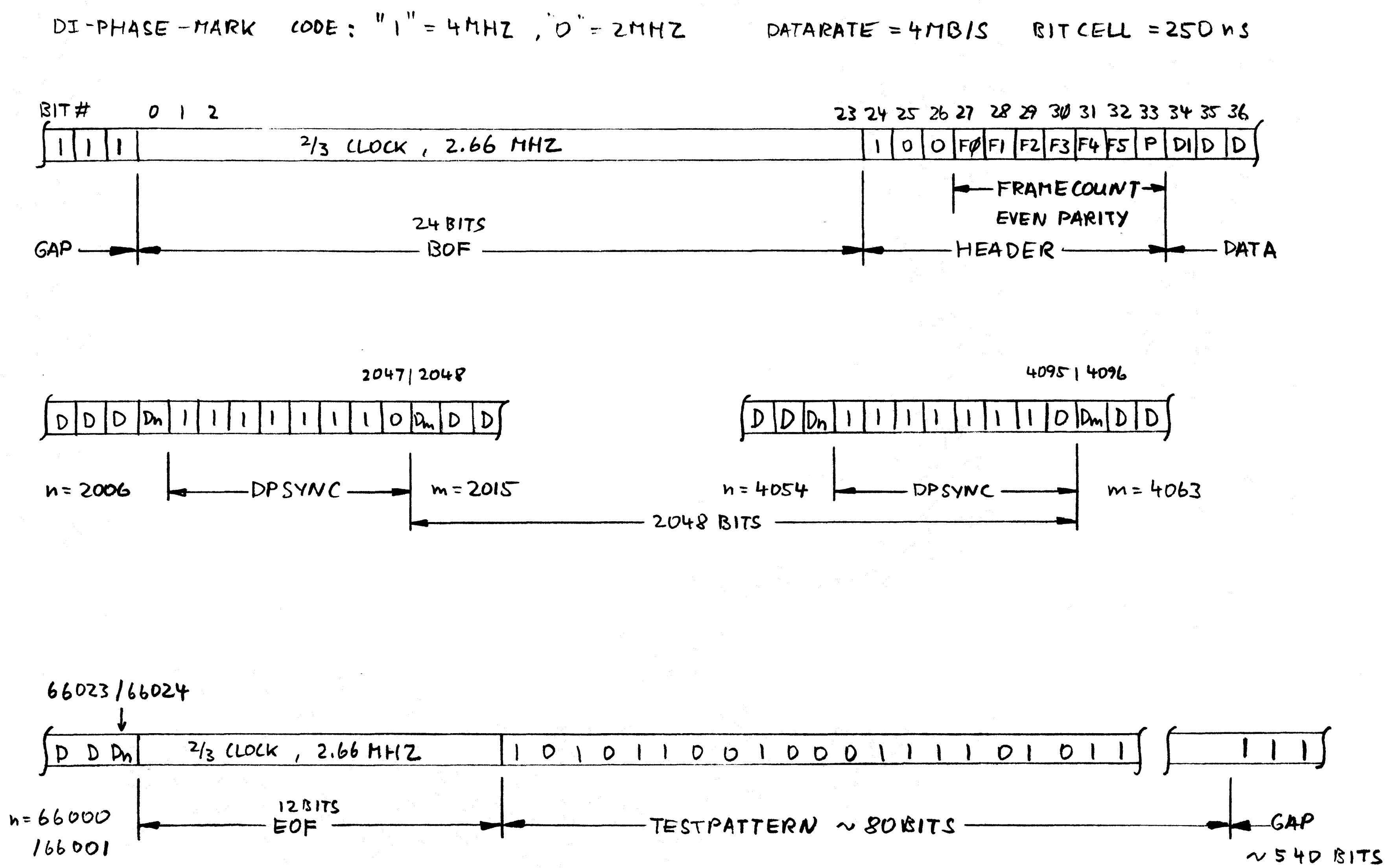

FIGURE 1.4 : MK II VIDEO FORMAT.

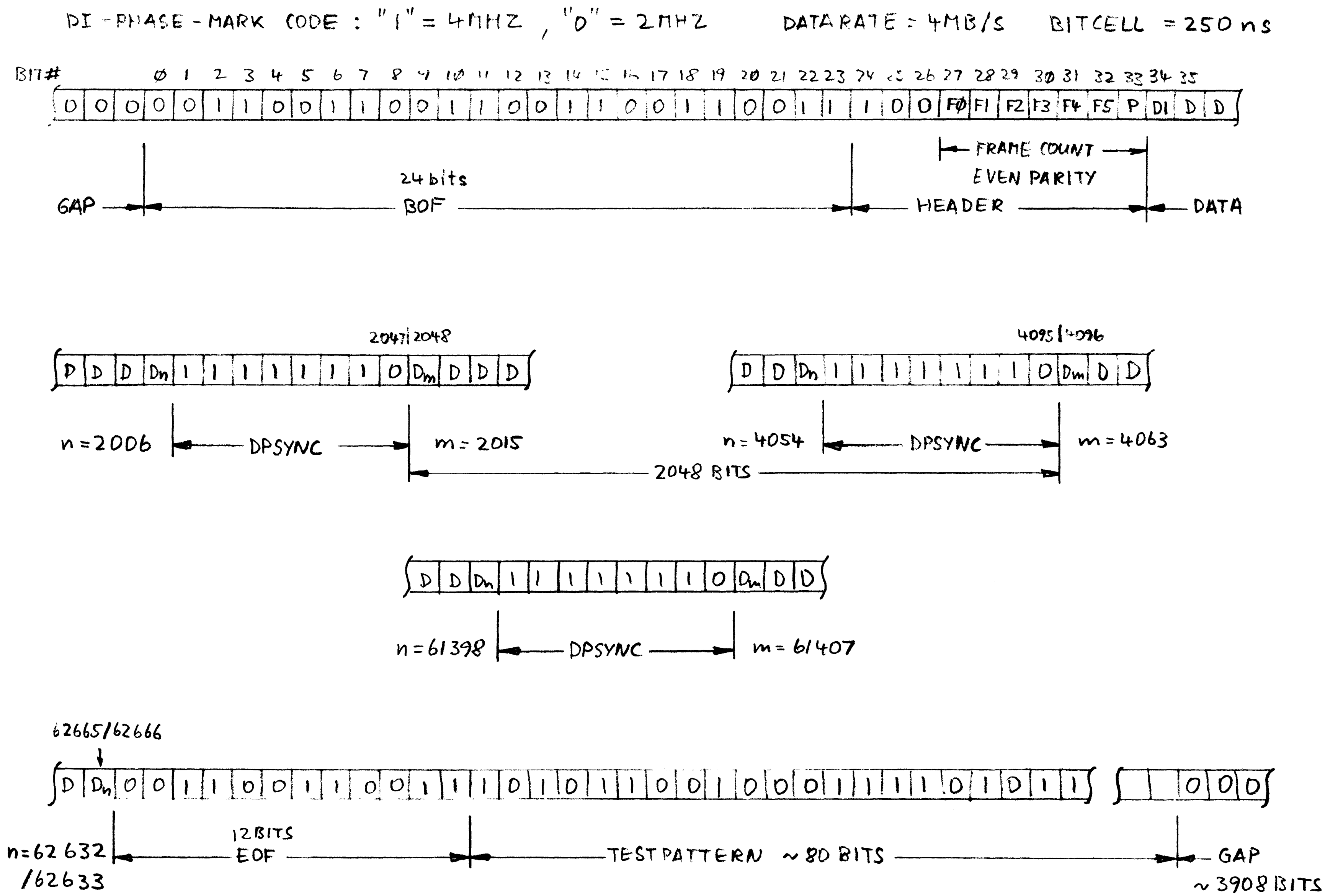

FIGURE 1.5: MKIIC VIDEO FORMAT

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

OLD FORMAT AUDIO TRACK 1

FIGURE 14

1	1	1	1	1	1	1	1	0	I	F_0	F_1	F_2	F_3	F_4	F_5	S_{00}	S_{01}	S_{02}	S_{03}	S_{10}	S_{11}	S_{12}	S_{13}	M_{00}	M_{01}	M_{02}	M_{03}	M_{10}	M_{11}	M_{12}	M_{13}
H_{00}	H_{01}	H_{02}	H_{03}	H_{10}	H_{11}	H_{12}	H_{13}	D_{00}	D_{01}	D_{02}	D_{03}	D_{10}	D_{11}	D_{12}	D_{13}	D_{20}	D_{21}	D_{22}	D_{23}	X_{00}	X_{01}	X_{02}	X_{03}	X_{10}	X_{11}	X_{12}	X_{13}	0	0	0	0

LEGEND

SYMBOL	WEIGHTING	FUNCTION
F_0	2^0	FRAME COUNT(0-59)
F_1	2^1	
F_2	2^2	
F_3	2^3	
F_4	2^4	
F_5	2^5	FRAME COUNT(0-59)
S_{00}	$10^0,2^0$	SECONDS (UNITS)
S_{01}	$10^0,2^1$	
S_{02}	$10^0,2^2$	
S_{03}	$10^0,2^3$	SECONDS (UNITS)
S_{10}	$10^1,2^0$	SECONDS (TENS)
S_{11}	$10^1,2^1$	
S_{12}	$10^1,2^2$	
S_{13}	$10^1,2^3$	SECONDS (TENS)

SYMBOL	WEIGHTING	FUNCTION
M_{00}	$10^0,2^0$	MINUTES (UNITS)
M_{01}	$10^0,2^1$	
M_{02}	$10^0,2^2$	
M_{03}	$10^0,2^3$	MINUTES (UNITS)
M_{10}	$10^1,2^0$	MINUTES (TENS)
M_{11}	$10^1,2^1$	
M_{12}	$10^1,2^2$	
M_{13}	$10^1,2^3$	MINUTES (TENS)
H_{00}	$10^0,2^0$	HOURS (UNITS)
H_{01}	$10^0,2^1$	
H_{02}	$10^0,2^2$	
H_{03}	$10^0,2^3$	HOURS (UNITS)
H_{10}	$10^1,2^0$	HOURS (TENS)
H_{11}	$10^1,2^1$	HOURS (TENS)

SYMBOL	WEIGHTING	FUNCTION
H_{12}	$10^1,2^2$	HOURS (TENS)
H_{13}	$10^1,2^3$	HOURS (TENS)
D_{00}	$10^0,2^0$	DAYS (UNITS)
D_{01}	$10^0,2^1$	
D_{02}	$10^0,2^2$	
D_{03}	$10^0,2^3$	DAYS (UNITS)
D_{10}	$10^1,2^0$	DAYS (TENS)
D_{11}	$10^1,2^1$	
D_{12}	$10^1,2^2$	
D_{13}	$10^1,2^3$	DAYS (TENS)
D_{20}	$10^2,2^0$	DAYS (HUNDREDS)
D_{21}	$10^2,2^1$	
D_{22}	$10^2,2^2$	DAYS (HUNDREDS)

SYMBOL	WEIGHTING	FUNCTION
D_{23}	$10^2,2^3$	DAYS (HUNDREDS)
X_{00}	$N_0,2^0$	AUXILIARY INPUTS
X_{01}	$N_0,2^1$	
X_{02}	$N_0,2^2$	
X_{03}	$N_0,2^3$	
X_{10}	$N_1,2^0$	
X_{11}	$N_1,2^1$	
X_{12}	$N_1,2^2$	
X_{13}	$N_1,2^3$	AUXILIARY INPUTS

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

5. ALL INPUTS ARE $\overline{\text{DATA}}$.
4. 1 BIT IS "1" FOR FRAME LENGTH OF 66.001 AND "0" FOR 66.000.
3. ALL EXTERNAL INPUTS MUST BE IN THE BCD FORMAT
2. LOGIC "0" IS A "HIGH" INPUT TO RECORD ENCODER.
1. LOGIC "1" IS A "LOW" INPUT TO RECORD ENCODER.

NOTE: [illegible]

QTY / QTY / NEXT ASSY / USED ON / APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN
CHECKED
DESIGN ENGINEER
PROJECT RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
CONTROLS DIVISION
717 NORTH CONEY AVENUE AZUSA, CALIFORNIA

LONGITUDINAL TAPE FORMAT
TIME CODE DATA
NATIONAL RADIO ASTRONOMY OBSERVATORY

SIZE	CODE IDENT NO.	DWG NO.
B	96261	FIGURE 14
SCALE		SHEET 1 of 1

1-10

FIGURE 1.6: OLD AUDIO TRACK 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

NEW FORMAT AUDIO TRACK 1

FIGURE 14

1	1	1	1	1	1	1	1	0	I	F_0	F_1	F_2	F_3	F_4	F_5	S_{00}	S_{01}	S_{02}	S_{03}	S_{10}	S_{11}	S_{12}	S_{13}	M_{00}	M_{01}	M_{02}	M_{03}	M_{10}	M_{11}	M_{12}	M_{13}

H_{00}	H_{01}	H_{02}	H_{03}	H_{10}	H_{11}	H_{12}	H_{13}	D_{00}	D_{01}	D_{02}	D_{03}	D_{10}	D_{11}	D_{12}	D_{13}	D_{20}	D_{21}	D_{22}	D_{23}	X_{00}	X_{01}	X_{02}	X_{03}	X_{10}	X_{11}	X_{12}	X_{13}	0	0	0	0

LEGEND

SYMBOL	WEIGHTING	FUNCTION
F_0	2^0	FRAME COUNT(0-59)
F_1	2^1	
F_2	2^2	
F_3	2^3	
F_4	2^4	
F_5	2^5	FRAME COUNT(0-59)
S_{00}	$10^0, 2^0$	SECONDS (UNITS)
S_{01}	$10^0, 2^1$	
S_{02}	$10^0, 2^2$	
S_{03}	$10^0, 2^3$	SECONDS (UNITS)
S_{10}	$10^1, 2^0$	SECONDS (TENS)
S_{11}	$10^1, 2^1$	
S_{12}	$10^1, 2^2$	
S_{13}	$10^1, 2^3$	SECONDS (TENS)

SYMBOL	WEIGHTING	FUNCTION
M_{00}	$10^0, 2^0$	MINUTES (UNITS)
M_{01}	$10^0, 2^1$	
M_{02}	$10^0, 2^2$	
M_{03}	$10^0, 2^3$	MINUTES (UNITS)
M_{10}	$10^1, 2^0$	MINUTES (TENS)
M_{11}	$10^1, 2^1$	
M_{12}	$10^1, 2^2$	
M_{13}	$10^1, 2^3$	MINUTES (TENS)
H_{00}	$10^0, 2^0$	HOURS (UNITS)
H_{01}	$10^0, 2^1$	
H_{02}	$10^0, 2^2$	
H_{03}	$10^0, 2^3$	HOURS (UNITS)
H_{10}	$10^1, 2^0$	HOURS (TENS)
H_{11}	$10^1, 2^1$	HOURS (TENS)

SYMBOL	WEIGHTING	FUNCTION
H_{12}	$10^1, 2^2$	HOURS (TENS)
H_{13}	$10^1, 2^3$	HOURS (TENS)
D_{00}	$10^0, 2^0$	PWR (UNITS)
D_{01}	$10^0, 2^1$	
D_{02}	$10^0, 2^2$	
D_{03}	$10^0, 2^3$	PWR (UNITS)
D_{10}	$10^1, 2^0$	PWR (TENS)
D_{11}	$10^1, 2^1$	
D_{12}	$10^1, 2^2$	
D_{13}	$10^1, 2^3$	PWR (TENS)
D_{20}	$10^2, 2^0$	PWR (HUNDREDS)
D_{21}	$10^2, 2^1$	
D_{22}	$10^2, 2^2$	PWR (HUNDREDS)

SYMBOL	WEIGHTING	FUNCTION
D_{23}	$10^2, 2^3$	PWR (HUNDREDS)
X_{00}	$N_0, 2^0$	
X_{01}	$N_0, 2^1$	
X_{02}	$N_0, 2^2$	
X_{03}	$N_0, 2^3$	
X_{10}	$N_1, 2^0$	CAL ON
X_{11}	$N_1, 2^1$	NO DATA
X_{12}	$N_1, 2^2$	NEW FORMAT
X_{13}	$N_1, 2^3$	

5. ALL INPUTS ARE DATA.
4. 1 BIT IS "1" FOR FRAME LENGTH OF 66.001 AND "0" FOR 66.000.
3. ALL EXTERNAL INPUTS MUST BE IN THE BCD FORMAT
2. LOGIC "0" IS A "HIGH" INPUT TO RECORD ENCODER.
1. LOGIC "1" IS A "LOW" INPUT TO RECORD ENCODER.

NOTES:

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRACTIONS ± XX ±
ANGLES ± XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

QTY | QTY | NEXT ASSY | USED ON
APPLICATION

CONTRACT NO.
DRAWN
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
CONTROLS DIVISION
717 NORTH CONEY AVENUE AZUSA, CALIFORNIA

LONGITUDINAL TAPE FORMAT
TIME CODE DATA
NATIONAL RADIO ASTRONOMY OBSERVATORY

SIZE	CODE IDENT NO.	DWG NO.
B	96261	F1... PI 14
SCALE		SHEET 1 of 1

1-10

FIGURE 1.7 NEW AUDIO TRACK 1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED

NEW FORMAT AUDIO TRACK 2

1	1	1	1	1	1	1	1	0	I	F_0	F_1	F_2	F_3	F_4	F_5	S_{00}	S_{01}	S_{02}	S_{03}	S_{10}	S_{11}	S_{12}	S_{13}	M_{00}	M_{01}	M_{02}	M_{03}	M_{10}	M_{11}	M_{12}	M_{13}
H_{00}	H_{01}	H_{02}	H_{03}	H_{10}	H_{11}	H_{12}	H_{13}	D_{00}	D_{01}	D_{02}	D_{03}	D_{10}	D_{11}	D_{12}	D_{13}	D_{20}	D_{21}	D_{22}	D_{23}	X_{00}	X_{01}	X_{02}	X_{03}	X_{10}	X_{11}	X_{12}	X_{13}	0	0	0	0

FIGURE 14

LEGEND

SYMBOL	WEIGHTING	FUNCTION
F_0	2^0	
F_1	2^1	
F_2	2^2	
F_3	2^3	
F_4	2^4	
F_5	2^5	
SC_{00}	$16^0, 2^0$	SOURCE CODE
SC_{01}	$16^0, 2^1$	
SC_{02}	$16^0, 2^2$	
SC_{03}	$16^0, 2^3$	
SC_{10}	$16^1, 2^0$	
SC_{11}	$16^1, 2^1$	
SC_{12}	$16^1, 2^2$	
SC_{13}	$16^1, 2^3$	SOURCE CODE

SYMBOL	WEIGHTING	FUNCTION
SC_{20}	$16^2, 2^0$	SOURCE CODE
SC_{21}	$16^2, 2^1$	
SC_{22}	$16^2, 2^2$	
SC_{23}	$16^2, 2^3$	
SC_{30}	$16^3, 2^0$	
SC_{31}	$16^3, 2^1$	
SC_{32}	$16^3, 2^2$	
SC_{33}	$16^3, 2^3$	
SC_{40}	$16^3, 2^0$	
SC_{41}	$16^4, 2^1$	
SC_{42}	$16^4, 2^2$	
SC_{43}	$16^4, 2^3$	
SC_{50}	$16^5, 2^0$	
SC_{51}	$16^5, 2^1$	SOURCE CODE

SYMBOL	WEIGHTING	FUNCTION
SC_{52}	$16^5, 2^2$	SOURCE CODE
SC_{53}	$16^5, 2^3$	SOURCE CODE
D_{00}	$10^0, 2^0$	DAYS (UNITS)
D_{01}	$10^0, 2^1$	
D_{02}	$10^0, 2^2$	
D_{03}	$10^0, 2^3$	DAYS (UNITS)
D_{10}	$10^1, 2^0$	DAYS (TENS)
D_{11}	$10^1, 2^1$	
D_{12}	$10^1, 2^2$	
D_{13}	$10^1, 2^3$	DAYS (TENS)
D_{20}	$10^2, 2^0$	DAYS (HUNDREDS)
D_{21}	$10^2, 2^1$	
D_{22}	$10^2, 2^2$	DAYS (HUNDREDS)

SYMBOL	WEIGHTING	FUNCTION
D_{23}	$10^2, 2^3$	DAYS (HUNDREDS)
X_{00}	$N_0, 2^0$	TERMINAL ID
X_{01}	$N_0, 2^1$	
X_{02}	$N_0, 2^2$	
X_{03}	$N_0, 2^3$	
X_{10}	$N_1, 2^0$	
X_{11}	$N_1, 2^1$	
X_{12}	$N_1, 2^2$	
X_{13}	$N_1, 2^3$	TERMINAL ID

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

5. ALL INPUTS ARE DATA.
4. 1 BIT IS "1" FOR FRAME LENGTH OF 66.001 AND "0" FOR 66.000.
3. ALL EXTERNAL INPUTS MUST BE IN THE BCD FORMAT
2. LOGIC "[illegible]" IS A "[illegible]" INPUT TO RECORD ENCODER.
1. [illegible] IS A "[illegible]" INPUT TO RECORD ENCODER.

NOTES [illegible]

QTY | QTY | NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRACTIONS ± | XX ±
ANGLES ± | XXX ±
MATERIAL
FINISH

CONTRACT NO.
DRAWN
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
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717 NORTH CONEY AVENUE AZUSA, CALIFORNIA

LONGITUDINAL TAPE FORMAT
TIME CODE DATA
NATIONAL RADIO ASTRONOMY OBSERVATORY

SIZE	CODE IDENT NO.	DWG NO.
B	96261	FI[illegible]PI 14

SCALE | SHEET 1 of 1

1-10

FIGURE 1.8: AUDIO TRACK 2

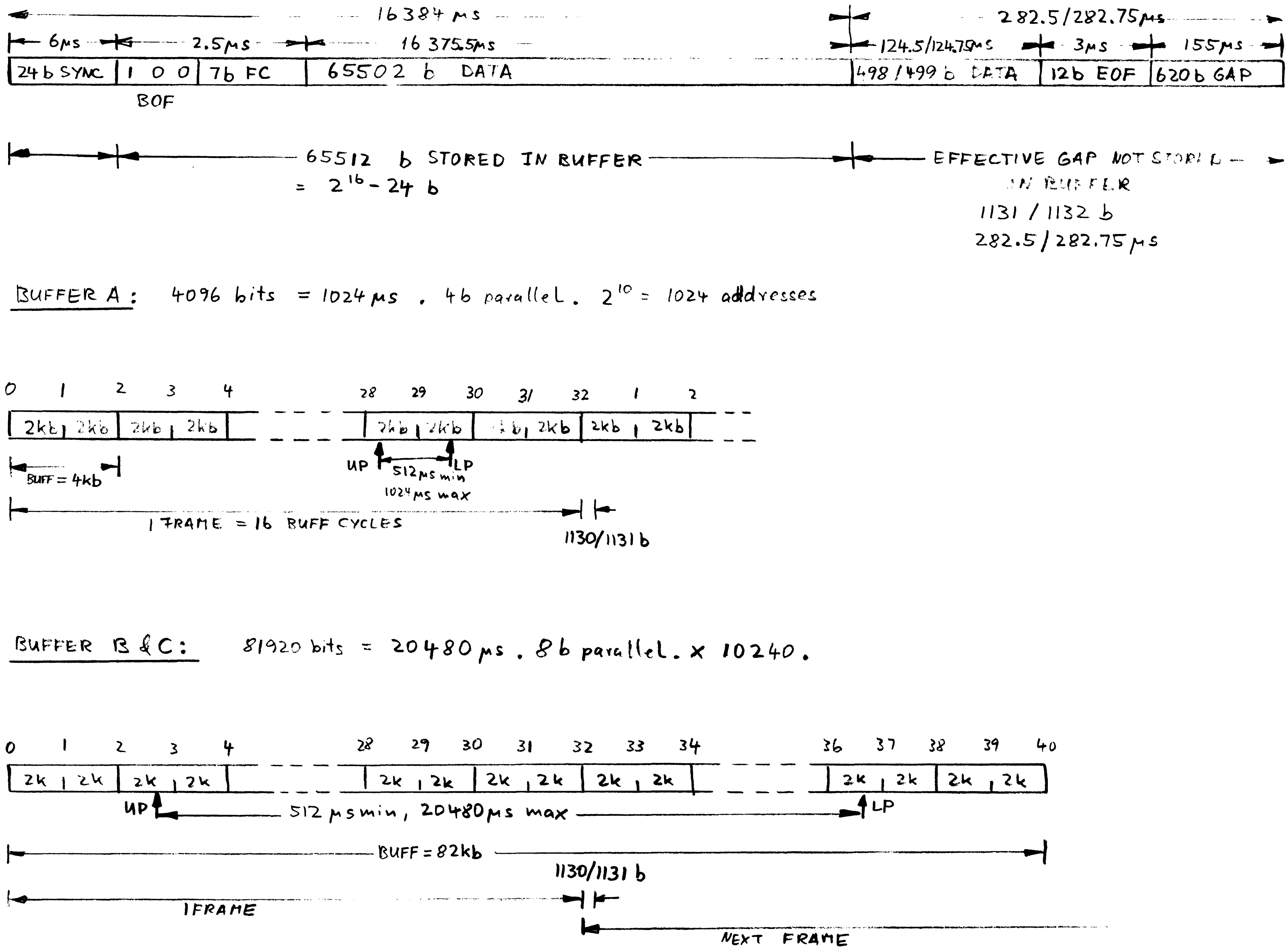


FIGURE 1.9: BUFFER ORGANIZATION

Specification of Correlator:

A block diagram of the correlator is shown in Figure 1.10. There is one cable to the buffer and a description of the signals is given above. There are four cables interfacing to the computers thru four general purpose interfaces. Their description is given in Chapter 3. One additional cable connects to the computer I/O bus to handle the 60 Hz interrupt. The correlator has a total of 576 channels which are arranged in one of 8 modes as shown in Figure 1.11. In addition to those channels there are 9 total count channels plus 16 channels which may be placed in parallel with any of the others under program control.

MODE		CORRELATOR
0	-	96 CH AUTO A, 96 CH AUTO B, 192 CH CROSS A-B
1	-	288 CH AUTO A, 288 CH AUTO B
2	-	576 CH AUTO A
3	-	192 CH AUTO A, 192 CH AUTO B, 192 CH AUTO C
4	-	288 CH CROSS A-B
5	-	128 CH AUTO A, 128 CH AUTO B, 128 CH CROSS A-B
6	-	96 CH CROSS A-B, 96 CH CROSS A-C, 96 CH CROSS B-C
7	<	64 CH AUTO A, 64 CH AUTO B, 64 CH AUTO C 64 CH CROSS A-B, 64 CH CROSS A-C, 64 CH CROSS B-C

Figure 1.11 Correlator Modes

There are three 3-level fringe rotators similar to the one described in EDIR #118. Fringe rotator A-B and A-C are independently controlled by the program whereas fringe rotator B-C takes the phase difference of A-C minus A-B.

Sample rates are controlled by the program and correspond to the bandwidths: 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz, 31.25 kHz and 15.625 kHz.

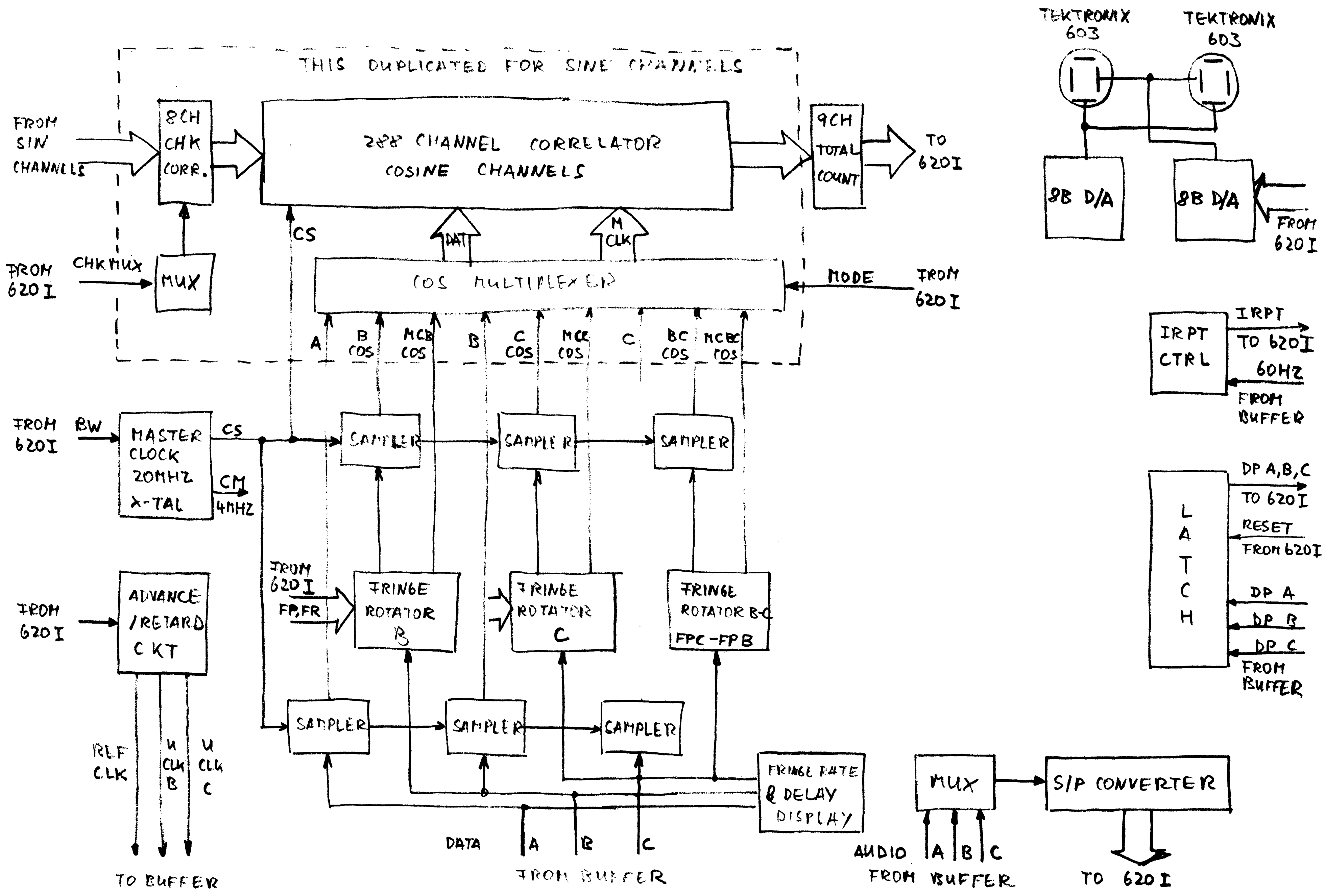


FIGURE 1.10: CORRELATOR

Specification of FFT Processor

The FFT consists of a Nova 820 CPU, an Elsytec 306/MFFT plug-in array processor and a program library supplied by Elsytec. It is a medium speed FFT processor with the following basic specification:

No. Real Points	32	64	128	256	512*	1024	2048	4098	8192	16384
Time/ms	8.8	14.5	23	39	75	139	280	600	1300	2850
No. Core Locations	58	114	226	450	898	1794	3586	7170	14338	28674

*Used by NRAO

These times are without I/O transfers and without set-up by a master program. NRAO has added fractional bit shift corrections to the master program. For further details see Chapter 2.

CHAPTER 2: Software

Introduction

The present configuration for VLBI processing consists of a Varian 620-I minicomputer and a Data General Nova 820 minicomputer. The Nova contains an Elsytec array processor hardware board which permits it to fast Fourier transform the cross-correlation function sent by the Varian and to return the resultant spectrum back to the Varian where it is written on 9 track magnetic tape.

The Varian is, in general, the same software which has been around since the processor has been in operation. There have been extensive modifications, however. These modifications add to, rather than alter the original philosophy.

The first task for the Varian program is to read into memory the PREPTAPE information. This consists of up to 20 scans. The video tapes should be positioned to within one second of time relative to each other. When the start button is pushed on the correlator chassis, the program starts the video tape players (either 2 or 3), insists on 30 consecutive good frames, then aligns the tapes to the same frame number.

The delay between station A and B is calculated and strobed in. If there is a third station the A-C delay is calculated and strobed in. A built in delay of 5 seconds must elapse before data are recorded on 9 track tape. If mode 0 or 4 is in effect, the correlator data are sent to the Nova computer to be transformed, then sent back to the Varian to be written on tape.

A CRT display of fringe amplitude for 12 channels of A-B data and 12 channels of A-C data is created by the Varian. In case of two station processing, 24 channels of A-B data are displayed.

The source statements for both the Varian and Nova computers contain many comments which make the programs self-documenting.

NOVAEDIT and VAREDIT

As an on-line aid to debugging, simple editing programs have been written for the Varian and Nova computers. These are very similar in use. They allow a programmer to assemble, set and clear break points, type out in various formats selected portions of core, move selected portions of core, and to begin executing a program at a given location. The editing instructions are slightly different for the two systems.

NOVA	VARIAN	
A	A	(ASSEMBLE)
B	SBP	(SET BREAK POINT)
C	CBP	(CLEAR BREAK POINT)
D	(NA)	(DECIMAL FRACTION TYPE-OUT)
F	(NA)	(FRACTIONAL FRACTION TYPE-OUT)
I	TSD	(INTEGER DECIMAL TYPE-OUT)
O	TSO	(INTEGER OCTAL TYPE-OUT)
T	TUO	(TYPE-OUT 2'S COMPLEMENT OCTAL)
(NA)	TUD	(TYPE-OUT UNSIGNED DECIMAL (16 BITS))
J	JMP	(JUMP-TO (BEGIN EXECUTING))
M	MOV	(MOVE CONTENTS OF SELECTED LOCATIONS)
Z	ZBR	(ZAP BREAK POINT (CBP, NO ADDRESS RESTORATION))

The assembler mimics the cross assemblers but does not permit the use of labels. All addresses must be relative to the P register or must be absolute.

The instructions to the EDIT programs are in the form of function, Address 1, Address 2, and in the case of MOVE, N. Some examples follow.

A 1000,1020	Assemble from locations 1000 through 1020.
T 12345 or TUO 12345	Types out in 2's complement octal location 12345 (Type unsigned octal)
I 15,20 or TSD 15,20	Types out in integer decimal locations 15 through 20 (Type signed decimal)
F 17000	Accepts fractional decimal in the form + or - .DDDDD where DDDDD refers to decimal digits
M 100,200,20 or MOV 100,200,20	Will move locations 100 through 117 to locations 200 through 217
B 1025 or SBP 1025	Will set a break point at location 1025. Location 1026 will be used also
C 1025 or CBP 1025	Will restore locations 1025 and 1026 to original values
Z 1025 or ZBP 1025	Will clear the break point switch without restoring locations 1025 and 1026
O 1777,2001 or TSO 1777,2001	Types out in signed octal locations 1777 through 2001 (type signed octal)
D 20000	Types out in signed decimal fraction location 20000
J 2040 or JMP 2040	Will jump to location 2040

N locations of core may be set to a constant value (including zero) by assembling the constant into the first location of the array then moving N-1 values from the first location to the second location.

EX. A 1000 (Enter constant into location 1000)

M 1000,1001,077 (Will propagate the constant from 1001 through 1077)

All instruction to the EDIT programs are terminated by a carriage return.

NOVAEDIT restricts mnemonics to three characters. Changes from cross-assembler follow:

ORIGINAL	NOVAEDIT
INTEN	INE
INTDS	IND
SKPBN	SBN
SKPBZ	SBZ
SKPDN	SDN
SKPDZ	SDZ
READS	RDS
INTA	INA
MSKO	MKO
IORST	IOR
HALT	HLT

Nova Subroutines

1. AGET — Accepts a character from input device.
2. APUT — Outputs a character on the output device.
3. ATYPE — Types the value in R0 in 2's complement octal.
4. TNCR — Types message in address following call
   - Entry ATNCR — No LF-CR
   - Entry ATLCR — LF-CR before typing
   - Entry ATFCR — LF-CR after typing
5. AWLIM — Compares value of R0 with limits directly following call. Lower limit is first, then upper. Return is to next location if outside limits; and to the next + one if within limits.
6. ASHFT — Logically left shifts R0 by amount following call.
7. ASRA — Arithmetically right shifts R0 amount following call.

Nova Subroutines (cont.)

8. ASLA — Arithmetically left shifts R0 by amount following call
9. ASRL — Logically right shifts R0 by amount following call.
10. ASLL — Logically left shifts R0 by amount following call.
11. ADSLA — Arithmetically shifts left the contents of the double precision value as addressed by the next location.
12. ADSLL — Logical left shift version.
13. ADSRA — Arithmetic right version.
14. ADSRL — Logical right shift version.
15. AFSUB — Double precision subtract of next address from next plus one. If overflow, return is with carry set.
16. AFADD — Double precision add.
17. AFMUL — Single precision multiply with double precision result. Address following call is multiplied by address following that. DP product is placed in following address.
18. AFDIV — A double precision dividend is divided by a single precision divisor resulting in a single precision quotient. Divisor follows call, then dividend, then quotient. Quotient+1 contains remainder. Return is with carry set if overflow.
19. FSCAL — Arithmetically shifts right the value in R0. The result is rounded rather than truncated. Accepts positive or negative numbers.
20. AMOVE — Moves one or more contiguous words from one location to another. 'FROM' address follows call, then 'TO' address, then 'N' words to move. 'N' is octal.
21. ANORM — Normalizes a binary fraction with contiguous exponent. Address of fraction, exponent follows call.
22. AFN1 — Calls MFFT routines. Function to do follows call, then PSI 1, then PSI 2, then PSI 3. MWDCT (page zero) must contain the negative number of elements to do. Before call, R0 contains address of operator, R1 contains address of operatee, R2 contains address of result.
23. AFMTH — Calls meet arithmetic routines. Following call, the address contains the function code, next is address of operand 1, next is address of operand 2, then address of result. Operand 1 is performed on operand 2.
24. LCARG — Computes cosine of value in R2, expressed in binary angle measurement (BAM). Upon return R0 contains result.
25. LSARG — Computes sine of value in R2.
26. LBARG — Computes sine and cosine of value in R2.
27. For more subroutines see the Elystec MFFT User's Guide.

Nova Program

The Nova's sole purpose is to transform the cross-correlation functions into complex spectra. The Varian reads the correlators every 200 msec., and sends the correlation functions to the Nova following each read. Modes zero and four are the only modes available to the spectral line user. Mode zero has 192 channels of A X B or a total of 384 sines and cosines. Mode four has 288 channels of A X B or a total of 576 sines and cosines. A 512 real point transform is taken, so in Mode 4, 64 points are ignored, and in Mode 0, 128 points are cleared to zero before the FFT.

The Nova is a complete slave to the Varian; that is, all tasks are initiated by the Varian. During idle moments, the Nova is in a tight wait loop, with its interrupts enabled, waiting on an interrupt from the Varian. There are three expected commands from the Varian. The first is an initialization command which is generated by the Varian at Varian set-up time. This occurs when the Varian is syncing the tapes as during scan changes. The cosine table for the FFT is computed at this time and some minor initialization is done. The other two expected interrupts are when the Varian is ready to send data and receive data.

When data transfer occurs, it is done one word at a time. One computer sends a word to the other, then waits until the other has received it before another word is sent. When the Varian is sending, it is in interrupt enable state and will be interrupted out of this 'SEND' mode before all data have been sent. This is no problem, except the actual time required to send data is somewhat greater than if the Varian could devote its undivided attention to the task. As soon as the Nova has received all the data, it immediately begins to work on it. There are four tasks to be performed:

1. Normalize the data by total counts and scale them.
2. Arrange the data in the proper mode, including inserting zeros or discarding data, as necessary.
3. Perform the FFT.
4. Perform the fractional bit shift (FBS) correction.

The cosine and sine total counts are divided by PI, then all cosine values are divided by cosine TC/PI and sine values are divided by sine TC/PI. Prior to this division, cos TC/PI and sin TC/PI are normalized, that is, they are shifted left until the most significant bit (MSB) is set (since they are all positive). Actually, they are both shifted the same number of bits, the greater of them making the decision of how many bits to shift. This assures no overflow during the normalization divide step, there being no overflow indication on the Nova.

The data arrangement consists mainly of dividing the input array down the middle, moving the first half to the latter half of the array to be transformed, and likewise moving the latter half of the original array to the first half of the array to be transformed. In mode zero, zeros are inserted into the middle of the new array, and in mode four, the last 64 points of the original array do not participate in any portion of the task.

The third task is simply the forward or inverse fast Fourier transform of the data. The Elystec FFT subroutine is called, and the resulting spectrum occupies the space where the cross-correlation function originally was stored.

The complex spectrum can be written as:

S(K)=SR(K)+I*SI(K)   where SR is the real and SI the imaginary parts.

The FBS correction transforms S(K) into S'(K)

S'(K)=(SR(K)+I*SI(K)*(cos P(K)+I*sin P(K)) or

S'(K)+(SR(K)*cos P(K)-SI(K)*sin P(K))+I*(SI(K)*cos P(K)+SR(K)*sin P(K))

cos P(K) and sin P(K) are generated recursively as:

cos P(1) = 1

sin P(1) = 0

cos P(K) = cos P(K-1)*cos DELTA-sin P(K-1)*sin DELTA

sin P(K) = sin P(K-1)*cos DELTA+cos P(K-1)*sin DELTA

DELTA = PI*FBS

FBS = (TRUNC DELAY-TRUE DELAY)*BAND WIDTH/2000/N

N = SAMPLING INTERVAL = 0.25 micro seconds

Only the first 128 complex points of the spectrum are kept. The remainder are set to zero.

The actual beginning of the program is at entry 'DWAIT'. The first thing there is to disable the interrupts. 'DLOOP' busy switch is set not busy, the interrupts are enabled, and the computer stays in a jump to itself instruction.

When an interrupt occurs, 'DSERV' routine is reached. Here, all registers and the status of the carry bit are saved. If the Varian interrupted with code '0', 'DINIT' routine is called. If this entry is the first since the program was loaded, a cosine table for the FFT is calculated. Several counters are zeroed, and a table of cosines is calculated for possible Hanning weighting. The program then returns to 'DWAIT'.

If the Varian interrupts with code '2', 'DSEND' routine is called. This is the routine which sends the computed spectrum to the Varian. The spectrum has been placed in a buffer array and is safe from other routines. The data are sent, one word at a time, to the Varian. The Nova sends a word, then repeatedly asks if the Varian has received it. If more than a predetermined number of 'ASKS' occurs, the Nova gives up and goes back to 'DWAIT'. This probably means the Varian got into trouble and interrupted itself and had to resync. If the Nova successfully sends the complete spectrum to the Varian, it calls 'DOVER' routine. Here, the registers and carry bit are restored to values they contained before interruption, then return is back to location where the interrupt occurred.

Code '1' interrupt is where the real work is done. This is when the Varian wants to send a correlation function to be transformed. The Nova reads each word, tells the Varian it has read the word, then waits for the next word. The Nova's interrupts are disabled during this time, but each word is checked for a command word, so if the varian has gotten itself lost and has to restart, the Nova will be prepared for it.

Following successful data transfer, the Nova re-enables its interrupts, then enters 'DLOOP' routine. A busy switch is checked to see if the Nova had been interrupted out of this routine. This is a catastropic situation if it happens, so the Nova just stops. Operator intervention is necessary to restart the system. Normally, 'DLOOP' will not be busy and processing will continue. The first 53 words are moved from the input array to the working array for safekeeping. These are not the correlation function, but are parameters necessary to the Nova and the post-processing programs. The busy switch is set busy.

The correlation function is moved to the working array, divided in half, and the middle zeroed or portions ignored, depending on mode. Several switches are set or reset depending on sideband, Hanning weighting, and FBS correction. Delta is computed in binary angle measurement (BAM), cos and sin of total counts are divided by PI, normalized, and the reciprocal taken. The data to be transformed are checked to determine the largest absolute value. All data are shifted left by the amount needed to normalize this value. This insures maximum precision. All odd numbered values (cosines) are multiplied by the reciprocal of the cosine of total counts and all even numbered values (sines) are multiplied by the reciprocal of the sine of total counts. Exact count is kept of all scaling.

The sign on the transform is determined by which sideband is called for. As a note, the Nova's inverse FFT corresponds to the subroutine Fourg's forward FFT. The call to the Nova's FFT is straight forward. Some addresses must be inititalized, the number of points must be set, then a standard subroutine jump is used. The transform is done in place; that is, the spectrum occupies the area where the correlation function once resided.

A check is now made on whether to do the FBS correction, If it is to be done, much use is made of the Elystec's array arithmetic capability. This uses a greater amount of core, but is much faster. In fact, without using arrays, the FBS takes too long and the task cannot be completed within the allotted time. Cos and sin of delta are calculated, then a table of cos P sin P is generated.

The product arrays, cos P*RE, sin P*RE, cos P*IM, and sin P*RE are computed, 128 at a time. Then the real and imaginary parts are updated in place.

Finally, unused words in the array are set to zero. This happens even if the FBS correction is not being done. The 'DLOOP' busy switch is cleared, and the program switches back to 'DWAIT' and loops there until the next interrupt occurs.

<u>Varian Program</u>

The Varian program types out a message informing the user of the current system date, then halts. When the computer run button is pushed, the Varian reads PREPTAPE information into core, then waits for the correlator start button to be pushed. The video tapes should be aligned to the same second of time and be in remote control. When the correlator start button is pushed, the VArian starts the video tapes, waits for 30 good frame counts to come in, then synchronizes the tpaes to the same frame count. Delays are computed, strobed into the correlator and correlation begins.

The Varian enables its interrupts, then waits in a tight loop for an interrupt to come in. Interrupts occur 60 times per second, or at a 16.66666667 millisecond rate. This is the innermost loop of the program. Other loops are at 100 millisecond and 200 millisecond intervals. At the

100 millisecond interval, delays and rates are computed for the next 100 millisecond interval. The values for the 60 Hz interrupts are derived by linearly interpolating between the values computed for 100 millisecond intervals. At the 200 millisecond interval, data are either passed to the Nova for transforming or written directly on 9 track magnetic tape.

At each 60 Hz interrupt, 'VLOOP' runs the assured clock on the frame count. This assures the program that the frame count difference between A-B and A-C will not be affected by bad frame counts that occur only rarely. A series of bad frame counts will throw the program back into re-sync condition. Audio I is read for one recorder at each 60 Hz interrupt.

Every six 60 Hz interrupts (100 milliseconds) delays and rates are computed. If the Nova is to be used to transform data, at one of these 100 millisecond intervals, data are sent to the Nova and at the next interval, the previous data are read from the Nova. The assured clock is run for complete time rather than frame counts as in the 60 Hz loop.

If the Varian finds it necessary to re-sync, it types out a condition code which describes the reason.

CONDITION CODE	REASON
01	A-B frame count difference too great
05	A-B frame count difference too great
02	A-C frame count difference too great
03	A-C frame count difference too great
25	Fringe rate too large
13	Correlator stop button pushed
26	End of scan
24	Correlator stop button pushed
50	EOF on 9 track tape
42	Read PREPTAPE
23	Stop during 9 track tape write
40	Restart, same scan
44	Skip one scan
46	Restart, first scan
52	Position 9 track tape at EOF
54	Backspace one record

CONDITION CODE	REASON
56	Type current scan number and time
17	Position 9 track tape at end of data
62	Enable channel checking
64	Disable channel checking
10	Buffer fault on recorder C
11	Buffer fault on recorder B
12	Buffer fault on recorder B
30	Program interrupted itself. If in 3 station mode and addresses typed after CC are identical, probably a parity error occurred on 9 track tape and there was not time to correct it.

If switch 1 is up, certain parameters may be entered from the teletype. These are:

B DELAY=DDD CR	ACTUAL CHARACTERS DECODED	BD
C DELAY=DDD CR	(DDD=>DECIMAL DIGITS)	CD
A CLOCK=DDD CR	(CR=>CARRIAGE RETURN)	AC
B CLOCK=DDD CR		BC
C CLOCK=DDD CR		CC
B LO=DDD CR		BL
C LO=DDD CR		CL
NOTE MESSAGE ...... CR		NO
EOF CR		EO
FIRST SCAN CR		FI
ENABLE CHECKING CR		EN
DISABLE CHECKING CR		DI
DATA END CR		DA
SKIP SCAN CR		SK
READ PREPTAPE CR		RE
TYPE SCAN NUMBER CR		TY
START STOP TYPE CR		ST
WAKE UP ALERT CR		WA

The current value of setable parameters may be displayed by typing a ? in place of the = or immediately following the =. The computer's attention must be gotten by typing an X before the commands to accept or display a value. For example:

```
X WAKE UP CR        ,OR JUST X WA CR       (CR=>CARRIAGE RETURN)
X A CLOCK?
X B LO=?
X AC=1 CR
```

Only the first two non-blanks following the X will be decoded.

Loading the System

Both the Nova and Varian object codes reside on the same system tape. The system tape is placed on the tape unit and the load button pushed. After the tape reaches the load point, both the Nova and Varian may be loaded, or the Varian only may be loaded. If both computers are to be loaded, switch 13 and only switch 13 on the Nova must be in the up position. Stop, reset, and load are pushed, in that order. The Varian must be in step mode. The U register must be clear, and the key-in loader executed at location 27765. The Nova will be loaded first with an appropriate message typed on the TTY. Then, the Varian will be loaded, with its message. If the Varian only is to be loaded, the Nova step is skipped. A message saying the Nova was not loaded will be output on the TTY, then the Varian will load itself.

CHAPTER 3: System Interconnection and Computer I/O's

This chapter describes the interface between the correlator and the Varian computer. Organization of the correlator is described as seen by the computer. The 8 correlator modes are shown including the sequence in which data is presented to the computer. All I/O control and monitor lines are shown in 3.1 to 3.6. Also, all critical timing that has to be considered by the program are detailed.

All cables that interconnect all chassis, computer and tape recorder are listed in detail in the blueprints. There are six general purpose I/O connections to the computer which have fixed assignments. They are shown in Figures 3.1 to 3.6.

Timing the decoded audio is important for the program. It takes up to 34 msec. for new data to be ready after a select command. Also, timing for memo X, Y and Z needs to be considered by the programmer. X and Y need to settle 15 μsec for full scale deflection before Z may be turned on. After Z pulse is executed it takes 30 μsec for a point to print on the screen. During that time X and Y should not be changed and no other EXC 63 should be executed. All other outputs are not critical for timing.

The correlator is read out per block and card in a fixed sequence:

TC AUTO A
TC AUTO B
TC AUTO C
TC CROSS A-B COS
TC CROSS A-B SIN
TC CROSS A-C COS
TC CROSS A-C SIN
TC CROSS B-C COS
TC CROSS B-C SIN

BLOCK 00 64 CH
BLOCK 01 32 CH
BLOCK 02 32 CH
BLOCK 03 64 CH
BLOCK 04 64 CH
BLOCK 05 32 CH

BLOCK 10   64 CH

BLOCK 11   32 CH

BLOCK 12   32 CH

BLOCK 13   64 CH

BLOCK 14   64 CH

BLOCK 15   32 CH

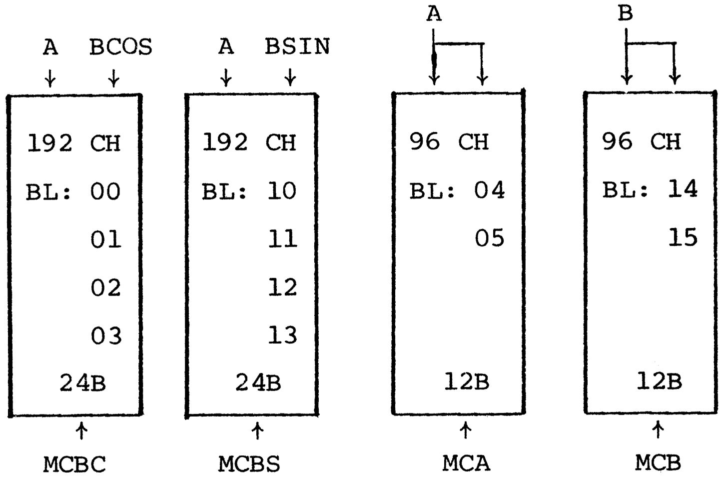
CHK 0   8 CH

CHK 1   8 CH

TERMINATOR

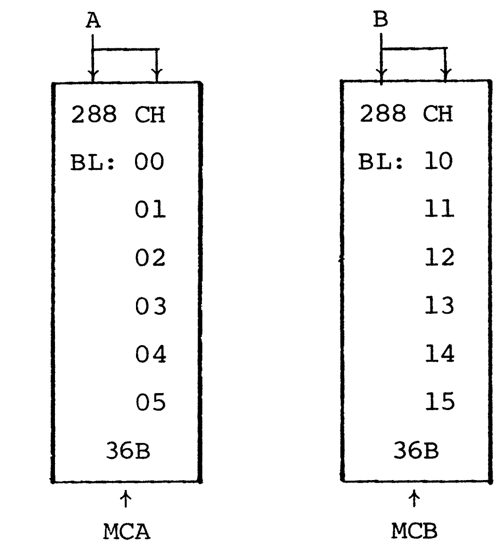
Depending upon the mode selected the blocks are arranged in the followings ways:

<u>Mode 0</u>: 96 CH Auto A, 96 CH Auto B, 192 CH Cross A-B

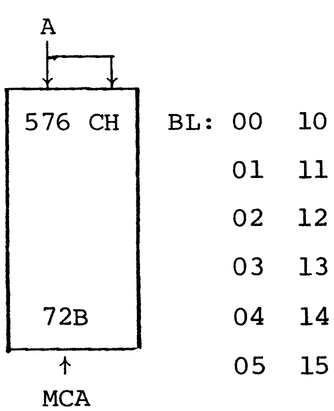


B 96 CH later than A

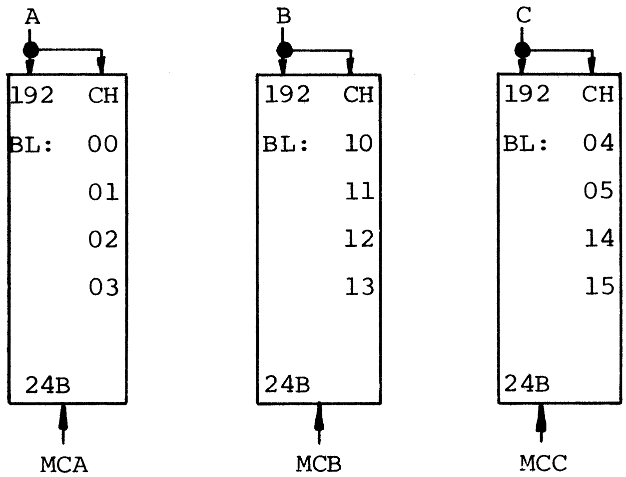
<u>Mode 1</u>: 288 CH Auto A, 288 CH Auto B



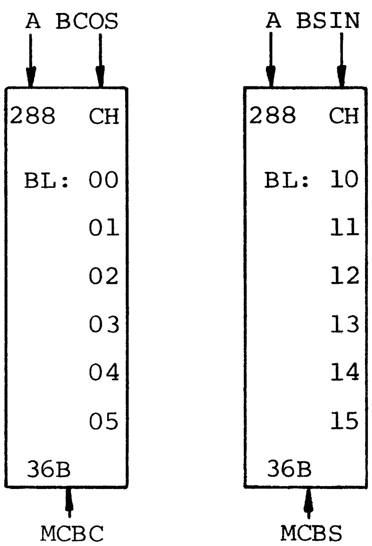
<u>Mode 2</u>: 576 CH Auto A



Mode 3: 192 CH AUTO, 192 CH AUTO B, 192 CH AUTO C

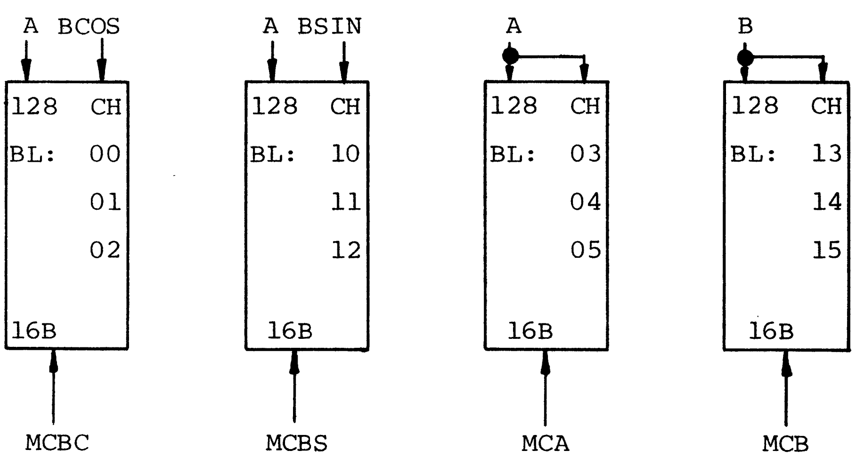


Mode 4: 288 CH CROSS A-B



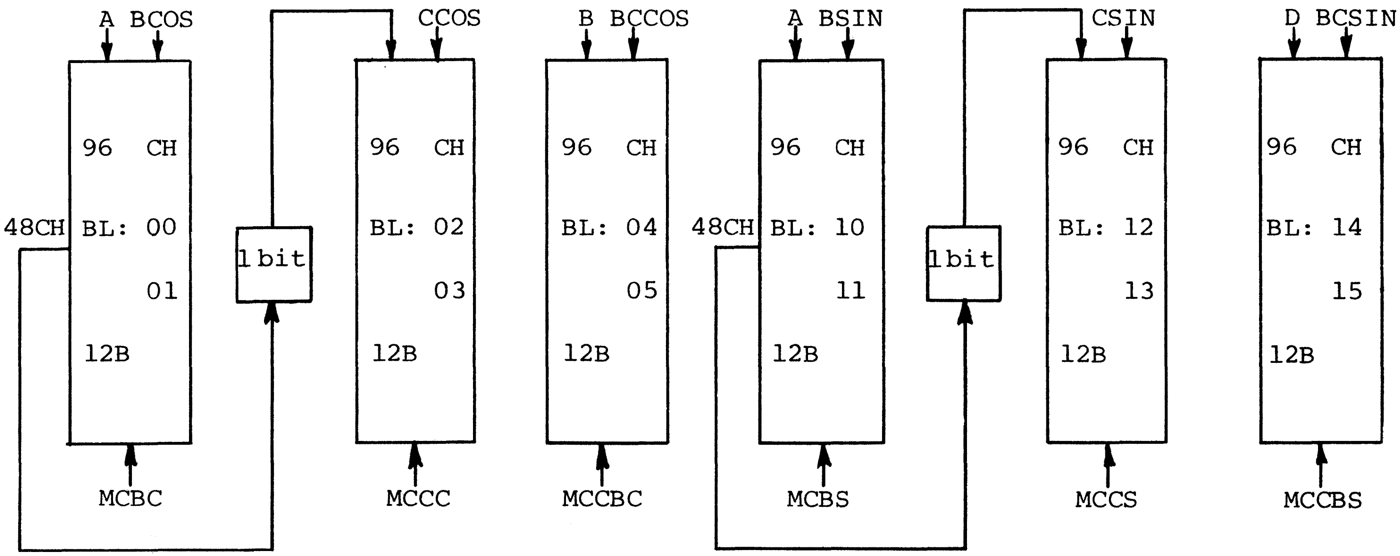
B 144 CH later than A

Mode 5: 128 CH AUTO A, 128 CH AUTO B, 128 CH CROSS A-B



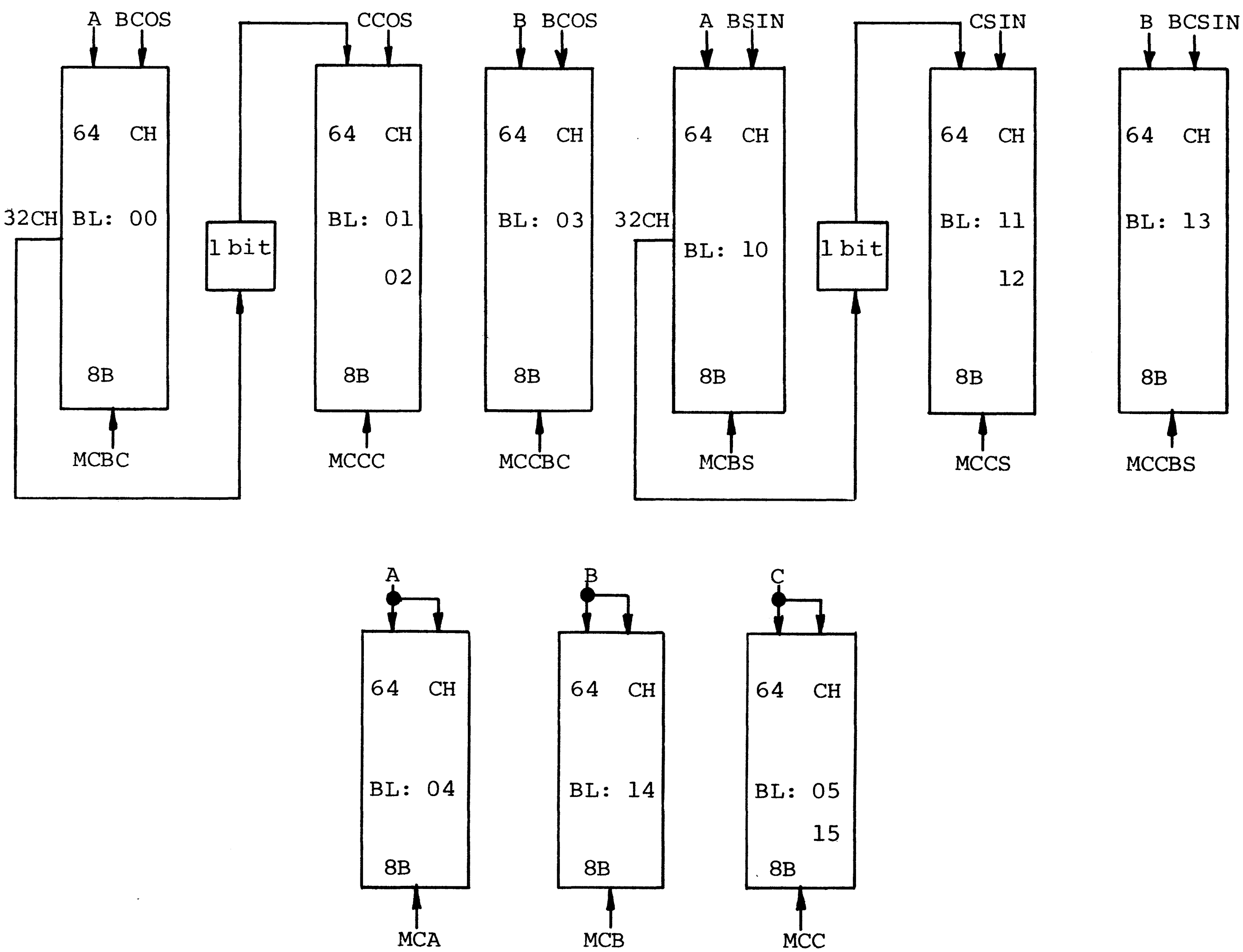
B 64 CH later than A

Mode 6: 96 CH CROSS A-B, 96 CH CROSS A-C, 96 CH CROSS B-C



B 48 CH later than A
C 96 CH later than A

Mode 7: 64 CH AUTO A, 64 CH AUTO B, 64 CH AUTO C,
64 CH CROSS A-B, 64 CH CROSS A-C, 64 CH CROSS B-C



B 32 CH later than A
C 64 CH later than A

VARIAN INTERFACE 60

OTB	
Ø	FPB Ø
1	FPB 1
2	FPB 2
3	FPB 3
4	FPB 4
5	FPB 5
6	FPB 6
7	FPB 7
8	FPC Ø
9	FPC 1
1Ø	FPC 2
11	FPC 3
12	FPC 4
13	FPC 5
14	FPC 6
15	FPC 7

BI	
Ø	COROUT Ø
1	" 1
2	" 2
3	" 3
4	" 4
5	" 5
6	" 6
7	" 7
8	" 8
9	" 9
1Ø	" 1Ø
11	" 11
12	" 12
13	" 13
14	" 14
15	COROUT 15

EXC	
Ø	CORRECOVERY
1	CORCLR
2	NXT WRD
3	RESET ERROR
4	COMP RDY
5	DELAY TRACK
6	INTRPT ENABLE
7	INTRPT DISABLE

PULSE => 1 μs

SEN	
Ø	DROPOUT A
1	DROPOUT B
2	DROPOUT C
3	XFER
4	
5	
6	INTRPT ENABLE
7	CORBSY

FIGURE 3.1

VARIAN INTERFACE 61

OTB	
Ø	
1	
2	
3	
4	FR 4
5	5
6	6
7	7
8	8
9	9
1Ø	1Ø
11	11
12	12
13	13
14	14
15	FR15

BI		
Ø	TCD1 UH1	TCD 2 SC40
1	" UH2	" SC41
2	" UH4	" SC42
3	" UH8	" SC43
4	" TH1	" SC50
5	" TH2	" SC51
6	" TH4	" SC52
7	" TH8	" SC53
8	" PØ	" UD1
9	" P1	" UD2
1Ø	" P2	" UD4
11	" P3	" UD8
12	" P4	" TD1
13	" P5	" TD2
14	" P6	" TD4
15	TCD1 P7	TCD2 TD8

EXC	
Ø	SELTCDA
1	SELTCD B
2	SELTCD C
3	SET FR B
4	SET FR C
5	ALERTOFF
6	ALERTENA
7	ALERT

ANY PULSE LENGTH

SEN	
Ø	
1	
2	
3	
4	
5	ALERTOFF
6	
7	

FIGURE 3.2

VARIAN INTERFACE 62

OTB	
Ø	FR 16 , CORMX Ø , BW Ø
1	FR 17 , CORMX 1 , BW 1
2	FR 18 , CORMX 2 , BW 2
3	FR 19
4	FR 2Ø
5	FR 21
6	FR 22
7	FR 23
8	NEG FR
9	BLKCOR
10	CHK BØ
11	CHK B1
12	CHK B2
13	CHK B3
14	CHK B4
15	CHK B5

BI				
Ø	TCD1	US1	TCD2	SCØØ
1	"	US2	"	SCØ1
2	"	US4	"	SCØ2
3	"	US8	"	SCØ3
4	"	TS1	"	SC1Ø
5	"	TS2	"	SC11
6	"	TS4	"	SC12
7	"	TS8	"	SC13
8	"	UM1	"	SC2Ø
9	"	UM2	"	SC21
1Ø	"	UM4	"	SC22
11	"	UM8	"	SC23
12	"	TM1	"	SC3Ø
13	"	TM2	"	SC31
14	"	TM4	"	SC32
15	TCD1	TM8	TCD2	SC33

EXC	
Ø	BWSTR
1	CORMXSTR
2	SET FP
3	ADVANCE B
4	RETARD B
5	ADVANCE C
6	RETARD C
7	

PULSE = > 0.3 μs

FIGURE 3.3

VARIAN INTERFACE 63

OTB	
∅	MEMOX ∅
1	1
2	2
3	3
4	4
5	5
6	6
7	MEMOX 7
8	MEMOY ∅
9	1
1∅	2
11	3
12	4
13	5
14	6
15	MEMOY 7

BI				
∅	TCD1	P8	TCD2	HD1
1	"	P9	"	HD2
2	"	P10	"	HD4
3	"	P11	"	HD8
4			"	UT1
5			"	UT2
6			"	UT4
7			"	UT8
8			"	TT1
9	"	CALON	"	TT2
1∅	"	NODATA	"	TT4
11	"	NEWCODE	TCD2	TT8
12	"	F∅		
13	"	F1		
14	"	F2		
15	TCD1	F3		

EXC	
∅	
1	MEMO1STR
2	MEMO2STR
3	MEMO1CLR
4	MEMO2CLR
5	DIM MEMO1
6	DIM MEMO2
7	DIM RESET

ANY PULSE LENGTH

SEN	
∅	
1	MEMO 1 BSY
2	MEMO 2 BSY
3	DSP TC 0.2
4	DSP TC 0.4
5	DSP TC 1
6	DSP TC 2
7	DSP TC 5

FIGURE 3.4

VARIAN INTERFACE 64

	OTB
Ø	DELAY 3 , SLEW BØ
1	" 4 , SLEW B1
2	" 5 , SLEW B2
3	" 6 , SLEW B3
4	" 7 , SLEW B4
5	" 8 , SLEW B5 (SIGN)
6	" 9 , SLEW CØ
7	" 1Ø , SLEW C1
8	" 11 , SLEW C2
9	" 12 , SLEW C3
1Ø	" 13 , SLEW C4
11	" 14 , SLEW C5 (SIGN)
12	" 15 , RUN A
13	DELAY 16 , RUN B
14	RUN C
15	AUD2

	BI
Ø	HFCA Ø , HFCA Ø , HFC B Ø
1	" 1 , " 1 , " 1
2	" 2 , " 2 , " 2
3	" 3 , " 3 , " 3
4	" 4 , " 4 , " 4
5	" 5 , " 5 , " 5
6	HFCA OK , HFCA OK , HFCB OK
7	HFCB Ø , HFCC Ø , HFCC Ø
8	" 1 , " 1 , " 1
9	" 2 , " 2 , " 2
1Ø	" 3 , " 3 , " 3
11	" 4 , " 4 , " 4
12	" 5 , " 5 , " 5
13	HFCB OK , HFCC OK , HFCC OK
14	MKIICA , MKIICB , MKIICC
15	AUD2

	EXC
Ø	RUNSTR
1	DELSTRB
2	DELSTRC
3	SELHFCAB
4	SELHFCAC
5	SELHFC BC
6	SET XFER
7	CLR XFER

PULSE = > 2μs

	SEN
Ø	STOP
1	SLEWBSY
2	BOFFLTA (16ms)
3	BOFFLTB (16ms)
4	BOFFLTC (16ms)
5	BUFFLT A (1S)
6	BUFFLT B (1S)
7	BUFFLT C (1S)

FIGURE 3.5

VARIAN INTERFACE 67.

OTB	
Ø	OUTPUT DATA OR OUTPUT CONTROL
1	
2	
3	
4	
5	
6	
7	
8	
9	
1Ø	
11	
12	
13	
14	
15	

BI	
Ø	INPUT DATA OR INPUT CONTROL
1	
2	
3	
4	
5	
6	
7	
8	
9	
1Ø	
11	
12	
13	
14	
15	

EXC	
Ø	IACK
1	ODRDY
2	OCRDY
3	SET STAT. 1
4	SET STAT. 2
5	CLR STAT
6	
7	

SEN	
Ø	OACK
1	IDRDY
2	ICRDY
3	STAT. 3
4	
5	
6	FFT RESET
7	FFT PWR ON

FIGURE 3.6

Check bits 0-5 are six control lines which set a multiplexer to select the position of the checkboard. Their assignments are given below:

CHB	BOARD	CHB	BOARD
0	00	30	40
1	01	31	41
2	02	32	42
3	03	33	43
4	04	34	44
5	05	35	45
6	06	36	46
7	07	37	47
10	10	40	50
11	11	41	51
12	12	42	52
13	13	43	53
14	20	44 … 67	No check Turns on panel indicator
15	21		
16	22		
17	23	70	TCA (TCB)
20	30	71	TCC (TCC)
21	31	72	TCBC (TCBS)
22	32	73	TCCC (TCCS)
23	33	74	TCCBC (TCCBS)
24	34	75 … 77	No check Turns on panel indicator
25	35		
26	36		
27	37		

Figure 3.7 Check Channel Assignments

Chapter 4: Circuit Description

All NRAO designed circuits are built on NRAO digital circuit boards and mounted in NRAO digital chassis. Figure 4.1 shows chassis layouts. All circuits are built on wire wrap cards with the exception of the correlator cards, which have a two-sided printed circuit card. The following sections describe function and timing of the circuits whereby the reader is referred to NRAO drawings #D2.519.

Decoder

All three decoders are identical and interchangeable. They contain decoding circuits and BOF detector for video data and decoding circuits for audio data.

Video data are first amplified and phase compensated in the recorder preamplifier and then clipped within the video recorder. This clipped video data, the "Astrodata", is the input to the decoder. Astrodata is first edge detected by a double edge detector which results in 20 ns wide pulses at 8 MHz or 4 MHz depending whether a "1" or a "0" has been recorded. A phase locked loop running at 8 MHz with a time constant of 15 μs locks to these pulses. 8 MHz is necessary because of an unfortunate choice for the video code. During the head gap a 4 MHz signal is recorded without polarity information. A 4 MHz PLL would lock with an ambiguity of 1/2 cycle. At the first "0" in the data stream this ambiguity is resolved, however the PLL cannot respond fast enough and BOF would not be decoded properly. Another unfortunate choice is the 2.66 MHz for BOF and EOF. The PLL has a narrow capture range of ±10% so that it is not upset by the 2.66 MHz BOF. Data is decoded by a fast sampler-decoder whose phase is given by the phase of the PLL and propagation thru several gates. Adjusting capacitor 8B11 effects the phase of the sampler and should be adjusted for best decoding with the front panel trimpot on half scale. This 200Ω front panel trimpot is a fine adjustment for the PLL. The operator should use it to compensate for variations in tapes and recorder performance. Detection of BOF is done with a separate circuit. At every transition of HEADSW a 45 μs 1 shot is fired. This is needed to let the video signal settle from the head-switch signal. After 45 μs gate 6C6 is enabled by BOFWDW and at the beginning of the 2/3 clock 6C6 is made and counter 6D, 6E is started. 24 clock pulses later GATE becomes true thru 5C5. When a 100 pattern is detected in 10D8 BOF becomes true for 100 ns. BOF resets counter 6D, 6E and closes GATE.

TOP VIEW

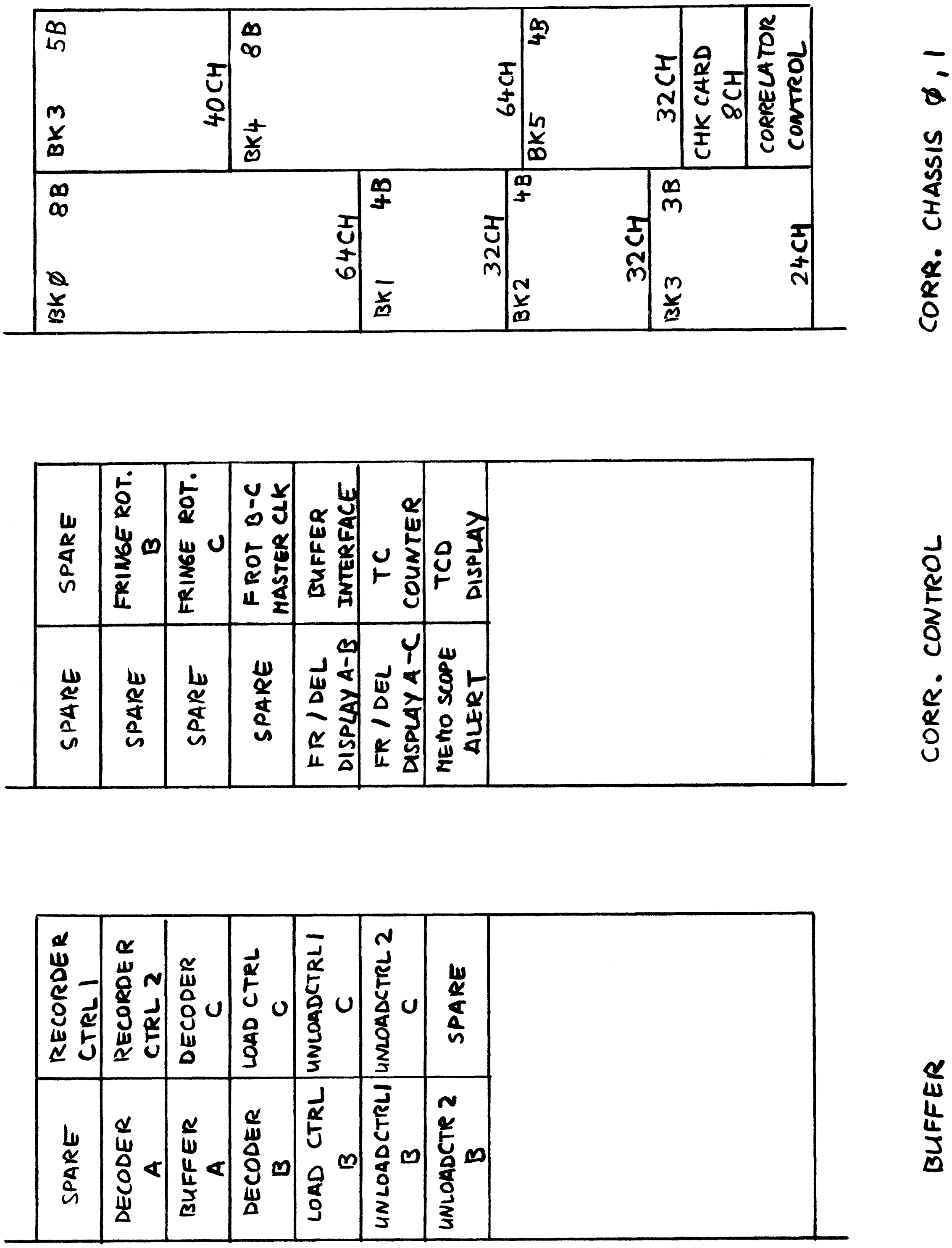


FIGURE 4.1: CHASSIS LAYOUT

If no 100 is detected GATE closes after 4 bits. EOF is not detected. MK II C format is chosen to eliminate the problem described above and therefore the BOF circuit works differently. The negative transition of 60 Hz triggers the 45 μs 1 shot. After 45 μs gate 10E1 is enabled to detect BOF. Circuit 10E6, 9F, 9E, 10E8 looks for six sequences of 0011 and opens GATE for 250 ns. During that time 10D8 should detect the 100 and BOF becomes true for 100 ns, clears 5D and disables 10E1 and closes GATE. If BOF is not detected after 1.3 ms BOFWDW is closed. BOF timing is shown in Figure 4.2.

Bit #	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
NRZO	2/3 CLK		1	0	0	F0	F1	F2	F3	F4	F5	P	D	D	D	D

$\overline{\text{BOF}}$

Figure 4.2 BOF Timing

Audio 1 and Audio 2 are decoded in the same decoder circuit. A multiplexer selects either one. Audio 1 or 2 of all three decoders A, B, C is selected simultaneously. The diphase decoder is straight forward with no critical timing circuit and experience has shown that it works without any trouble.

Buffer A

The buffer contains a 1024 word by four bit memory that works as a silo type first in - first out storage. Data is written into sequential locations at the rate at which it is decoded from the tape. After a time delay of >512 μs and <1024 μs the same data is read out at the rate of the reference clock. The timing circuit that controls read and write cycle works completely asynchronous with proper interlocks. Read and write cycle are 320 ns ±20 ns so that 2 cycles can be executed within 1 μs.

Write and read addresses are given by two counters, load pointer LP and unload pointer UP. They start addressing location 0 first, then step thru all locations to 1023. The next location is location 0 again.

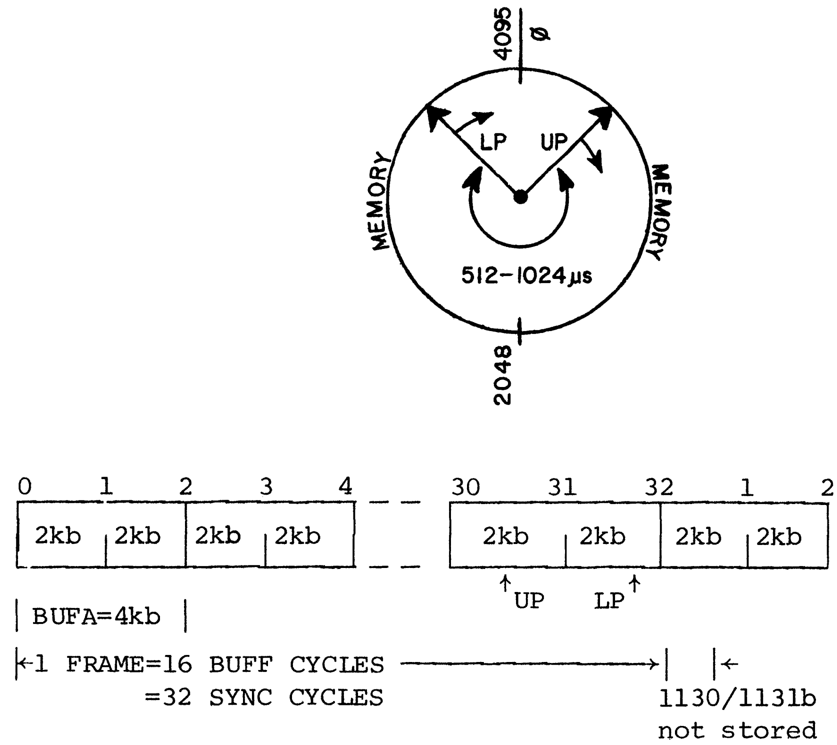


Figure 4.3 Buffer A Timing and Map

At BOF the LP is preset to 24 as it should be from Figure 4.2. BOF also sets VALFR which enables the write control circuit. LP now increments till it reaches 65536 at which time the write circuit is disabled. LP keeps counting until the next BOF. When a BOF is not detected LP is preset to 24 by BOFWDW however, the write circuit stays disabled and no data is written into memory.

Every 512 μs an 8 bit sync pattern is recorded on tape which is decoded in circuit 10B etc. The circuit searches for this pattern within a window of ±7 bits. If no sync is detected a flag is set to indicate that an error has occurred. If a sync is detected at the wrong time the flag is set as well and it is assumed that a bit slip has occurred within the preceding 512μs. LP 0-10 is then set to zero for resync. If a sync is detected at proper time no action is taken.

The UP provides the read address for the buffer memory. It also provides a 60 Hz squarewave with circuit 2E etc. This 60 Hz signal is the master 60 Hz reference which controls the entire system including channels B and C and the Varian interrupt. Since there are 66,666 2/3 bits per 60 Hz cycle there are two long frames of 66,667 bits per 1 short frame of 66,666 bits. Divide by three counter 2E keeps track of long and short frames and is initialized by detected 0 frame. At UP count = 66,665 or 66,666 SETUP becomes true and UP is set to zero at the next clock. At UP = 43 BUFFRAMEA becomes true when BOF is detected (VFME) is true. At UP = 65,536 BUFFRAMEA becomes false. BUFFRAME is the signal that blanks the correlator during head gap.

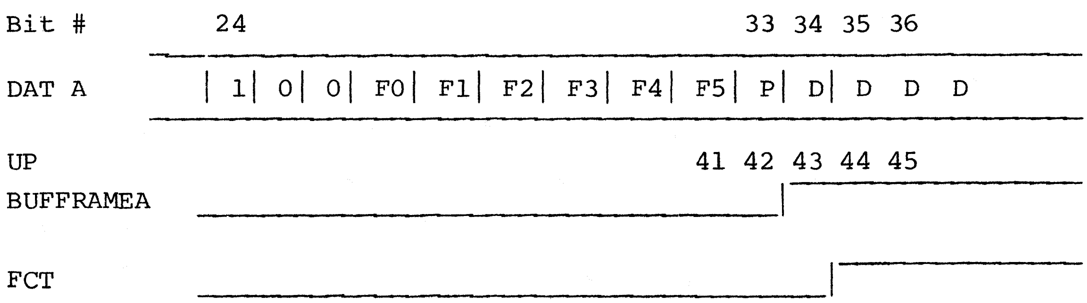


Figure 4.4 BUFFRAMEA Timing

Another signal DATOKA can also blank the correlator. Every 512 μs flag 1G is read and clocked into FF1B. Since there is a time delay of >512 μs between LP and UP we can now read the flag at the beginning of each 512 μs and therefore know whether the following 2048 bits are good or not. If the flag shows that there is an error, the correlator is blanked during an entire 512 μs period by DATOK. FLERR A is similar to DATOK and is used by the correlator to set indicator "DROPOUT".

For MK II C timing of the LP is not changed, however, 60 Hz and BUFFRAME is different. The negative transition of 60 Hz REFA is delayed and occurs now at UP = 59,648. This is the transition that the IVC 825 recorder uses to lock its head drum to. The circuits internal to the IVC recorders require this timing.

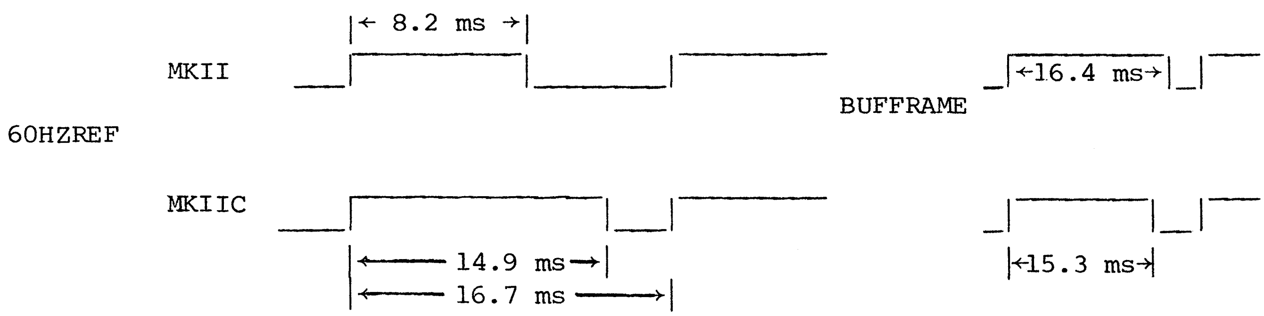


Figure 4.5 MKIIC Timing A

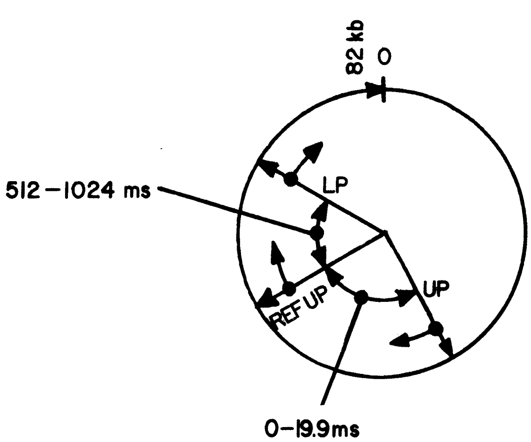
MKIIC furthermore has a shorter frame. BUFFRAME goes false at UP = 61,440. Since the frame is shorter for MKIIC format the correlator total count will be slightly smaller.

UP has to trail LP by 512 - 1024 μs. This timing is a function of the head drum servo amplifier. If phasing is adjusted incorrectly then the buffer is not working properly. Fault circuit 1B5 detects improper phasing-timing and sets BFLTA.

Buffer B(C)

Buffer B and C are identical. Each consists of a load control circuit, a memory, an unload control circuit 1 and an unload control circuit 2. Buffers B and C have a memory of 81,920 bits - 20.48 ms which handles the same deskewing task as Buffer A plus a delay of up to 79,864 bits - 19.97 ms which may be added under program control. This makes it possible to change delay rapidly (4 μs) and source switching experiments may be processed in one pass instead of two.

Since 20 ms is longer than one frame, the buffer contains a cycle of five frames. The write sequence is as follows. The BOF for the first frame, frame 0, is loaded at location 0. BOF of the next frame is written at location 65,536. Then when the address has reached 81,920 memory is looped around and location 0 is addressed. The BOF for the third frame is written at location 49,152. At the beginning of the 6th cycle we start again with writing into location 0. Figure 4.6 shows the memory map and timing. Similar to Buffer A we have a load pointer LP and an unload pointer UP but in addition we have a reference unload pointer REFUP. REFUP lags behind LP from 512 to 1024 μs. UP lags REFUP by a delay as given by the Varian computer. If that delay is zero then UP and REFUP are identical.



FRAME	1st BIT	1st DATA BIT	LAST DATA BIT	DELCT
0.5	0	34	65,535	4
1	65,536	65,570	49,151	3
2	49,152	49,186	32,767	2
3	32,768	32,802	16,383	1
4	16,384	16,418	81,919	0

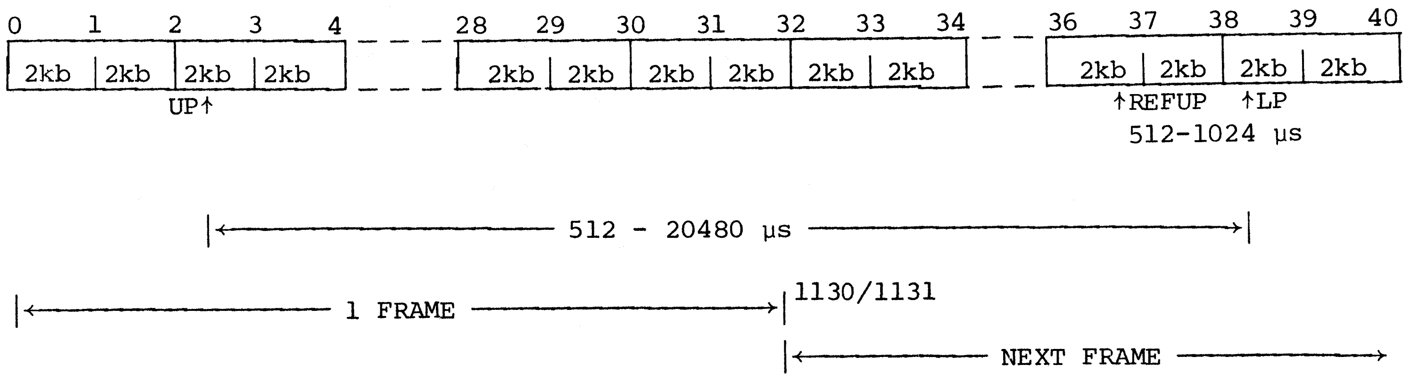


Figure 4.6 Buffer B(C) Timing and Map

UP and REFUP are counters that run normally independent from each other clocked by the same clock. Only during delay update UP is set to a new value. This new value is calculated from the present REFUP and a delay given by the Varian computer.

Load Control B(C)

The load control board contains all write logic to write into a 10240 word 8 bit/word Monostore III memory. One 8 bit word is written every 2 µs as addressed by LP. Memory address bus is time shared between LP and UP. Notice that MAI-12 and -13 are low true, all others are high true - an unfortunate feature of the Monostore III. Write control logic works asynchronously with read logic and is interlocked by WRREQ and RD signals. Every 2 µs a new 8 bit data word is latched into 2A, 2B, 2C, 2D. At the same time SETWRREQ flip flop is set. If due to a timing fault either of the Monostore III or of the write logic a request is made when SETWRREQ flip flop is still set from a previous request, WRFAIL is set indicating that data is not properly written into memory. SETWRREQ sets WRREQ flip flop if and when the previous cycle is complete and WRREQ is clear. If there is no read (RD not true) in progress a MWC pulse of 120 ns to the Monostore III is created and simultaneously VALMA becomes true placing LP on the address bus. Monostore III now executes a write cycle and after 650 ns when it is finished acknowledges with a 50 ns MCC pulse. MCC now clears WRREQ flip flop.

LP and sync detect - resync circuit are the same as for Buffer A. A divide by 5 counter 8G keeps track of the 5 frame cycle described earlier. It is initialized into proper sequence by 0FRAME. 0FRAME is a 1 per second pulse when frame count 0 is decoded. The output of counter 8G is used several ways.

First it is used to set delay counter DELCT which function is described later. The it is also used by a decoding network 7C, 7D, 7E, 7F to decode end of frame to reset VALFR. VALFR is set by BOF and therefore stays low when no BOF is detected. Another frame signal is created by 10D8 which is true even when no BOF is detected. This signal inhibits clock carries into LP11 during frame gap.

One other circuit, the write logic for a sync memory, is located on the load control board. Its function is described later with the unload circuit.

Unload Control B(C)

The unload control circuit is located on two boards: Unload Control 1 and Unload Control 2. These boards contain all necessary circuits to read the Monostore III memory. Some of the circuits are similar to Buffer A and it is necessary to know how Buffer A works in order to understand unload control B & C. The differences are:

UP is replaced by two counters: REFUP and UP.

An adder/multiplexing circuit is added to strobe a delay into UP under program control.

The 4 bit parallel data word is replaced by an 8 bit word.

The 2 bit sync memory is replaced by a 40 bit memory.

A circuit similar to load control for keeping track of the 5 frame cycle is added.

Instead of one circuit for long and short frames there are two: one for REFUP and one for UP.

The REFUP is almost identical to UP of Buffer A. It lags behind LP by 512 to 1024 µs. It is not affected by DELAY from the Varian CPU. It derives a 60 Hz reference for the video recorder. In STOP mode it is initialized by Buffer A thru SREFUPST. When the processor is in XFER mode REFUP is counting independently of Buffer A.

The unload pointer UP is a 16 bit counter which provides read address to the Monostore III memory. It is clocked by the same 4 MHz clock as REFUP but otherwise is independent, except when a new delay cycle is executed. Then starting with the current value of REFUP and a new delay, a new value for UP is calculated. This sequence is described here in detail. See Figure 4.7.

First the Varian places a new delay value DEL 3-16 on I/O lines OTB64-0-13. Then under program control a strobe DELSTR is issued. If the processor is not in STOP mode a delay cycle is initialized by placing a low level on 3A1. A sequence of 8 states, S1 to S8, is now started, each state lasting 0.5 µs.

S1: Set DELCYC, clear 3A1, load DELCT from LP circuit

Clear DATOK, disable FLERR

Set multiplexers to do $\overline{\text{DEL}}$ + REFUP + 1 (= REFUP - DEL)

Get carry if result >0 (means same frame)

Get no carry if result <0 (means skip to previous frame or frames)

Next CLK1: Clock up (Load result into UP)

Set SKPFRM1 if no carry

Set S2

Comments: If DEL=0 then we always stay within the same frame. If DEL is small then we may have to go to the previous frame depending upon the present REFUP. If DEL > 16.6 ms then we may have to go two frames back. SKPFRM 1 & 2 keep track of this.

S2: NOOP if no SKPFRM1. If SKPFRM1:

Decrement DELCT with CD

Set multiplexers to do: UP + 66666 (+1 for SHF1)

Get carry if result >1 (means same frame)

Get no carry if result <1 (means skip to next previous frame)

Next CLK1: Clock UP if SKPFRM1 (load result into UP)

Set SKPFRM2 if no carry

Set S3

Comment: UP + 66666 is calculated to make 0 < UP < 66666 for long frames. For short frames one has to calculate UP + 66667.

S3: NOOP if no SKPFRM2. If SKPFRM2:

Decrement DELCT with CD

Set multiplexers to do: UP + 66666 (+1 for SHF2)

Get carry if result >1 (means same frame)

Get no carry if result <1 (skip another frame??)

Next CLK1: Clock UP if SKPFRM2 (load result into UP)

Set $\sum$ FLT if no carry

Set S4

Comment: S3 is very similar to S2. Since DEL cannot be larger than 19965.75 μs we can never skip more than two frames. Therefore if we don't get a carry now the hardware has not worked properly and fault flip flop is set. This is a fatal error and processing should be stopped.

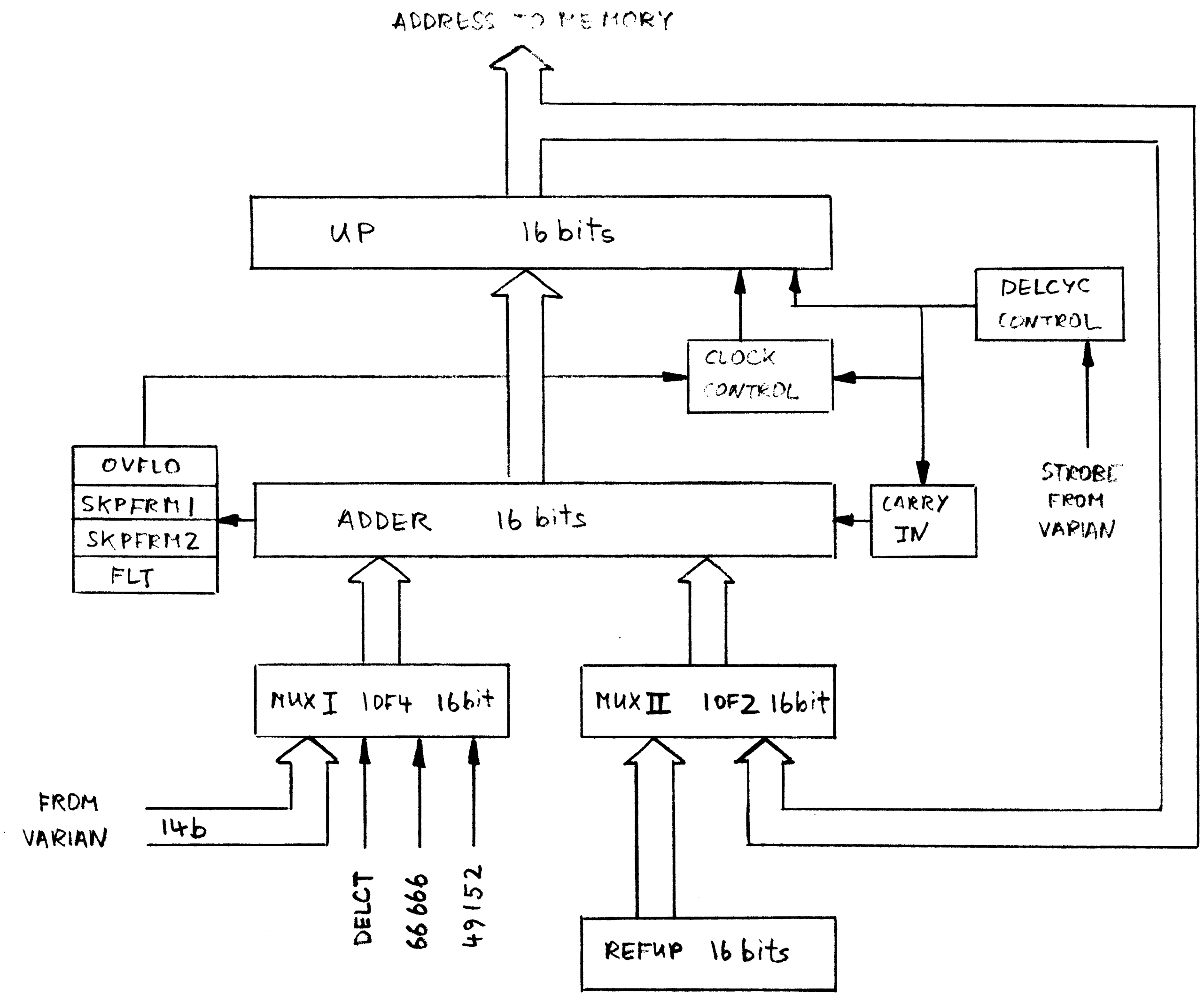


FIGURE 4.7: DELAY CYCLE, UNLOAD POINTER VB(C)

S4: Set multiplexers to do: UP + DELCT

Get carry if result >81920

Next CLK1: Clock UP (load result into UP)

Set OVFLO if carry

Set S5

Comment: During S1-S3 we have updated DELCT as we skipped frames. Now we add DELCT to UP to place UP (the read address) at right location within the sequence of 5 frames. The result may be larger than the size of the memory and overflow is set, S5 is to be executed.

S5: NOOP if no OVFLO. If OVFLO:

Set multiplexers to do: UP + 49152 (= UP -81920)

Next CLK1: Clock UP if OVFLO (load result into UP)

Set 6

Comment: +49152 is the same as -81920

We have now the final UP!

S6: Increment DELCT with CU

Next CLK1: Set S7

Comment: DELCT still had the value for the previous frame. Now it needs to be incremented so that end of current frame can be detected properly.

S7: NOOP

Next CLK1: Set S8

S8: NOOP

Next CLK1: Reset DELCYC

Enable UP clocking

Comment: During each delay cycle DELCYC normal 4 MHz clocking of UP is inhibited. At the end of DELCYC clocking is re-enabled.

At next UP0, UP1, UP2 = 0, set SRDREQ and RSREQ. Eight bits later the first good data bit appears on DATB(C) and DATOK B(C) becomes true.

DELCT is a three bit divide by five counter which keeps track of the five frame sequence. DELCT 14-16 together with UP 14-16 resets FRM flip flop 1A, 2B at UP = 65536, 49152, 32768, 16384, 0 respectively. This is the end of frame at which time the correlator is blanked and memory read cycles are inhibited. UP keeps running till it reaches 1129 or 1130 depending upon SHF0. Now FRM goes true. 1D is set and LDUP goes true. At the next clock UP is set to DELCT at 65536, 49152, 32768, 16384, 0 respectively. LDUP also starts circuit 4E, 4F which creates a double pulse CU which in turn increments DELCT. This prepares DELCT to detect the next EOF.

Every 2 μs a read cycle is executed to read one 8 bit word from the Monostore memory. It is initialized by SRDREQ if there is no DELCYC. If there is a true FRM and no RDFAIL then 6A is set which in turn sets RDREQ flip flop if no read is pending. 6A is now cleared. If there is no WRREQ then read flip flop 4E, 5A is set which inhibits any new write requests. VALMA becomes true and UP 3-16 is placed on the memory address bus for 150 ns. A 150 ns memory read command MRC is issued. After a read cycle is completed the memory returns with MCC which resets RDREQ. It should be noted that at the end of a write cycle MCC also gets true but then 6B latches the RDREQ flip flop so that it does not get reset. Now after RDREQ gets cleared by MCC the new data is on MDO and gets latched into 7B, 7C. MDO changes value as soon as the next write cycle is started. When the next SDREQ is issued data is strobed into shift register 1D and one bit later the first data bit appears on DATB(C). At UP = 35 BUFFRAMES becomes true which is one bit before F0 appears on DATB(C). At UP = 43 BUFFRAME and DATOK becomes true and the correlator is unblanked. The first data bit D1 is now on DATB(C). BUFFRAME goes false at UP = 65536 and blanks the correlator.

The sync memory is a 40 bit static write read memory at 9E, 9D, 9C. Normally it is in a read mode with WSAD low and UP 11-16 provides SYNCAD. The current data is continuously avaliable at 10E14. At UP = 9, 2057, 4105, etc. 10E is clocked and DATOK is set to the value read from memory. 10E is also clocked at the end of each DELCYC by RSREQ. When the Load Control requests a write cycle it raises WSAD and puts LP 11-16 on the SYNCAD lines. W0 and W1 now write a "0" or a "1" depending upon VALSYNC. If at that time the Unload Control attempts to clock 10E it is delayed by 9B12 which retriggers 8B and causes a 170 ns delay.

When MK II C tapes are processed 60 Hz REF is modified by REFUP = 59648. At REFUP = 0 60 Hz goes high and at 59648 60 Hz goes low. The negative transition is used for sync by the IVC recorder. Since frame length is shorter for MK II C BUFFRAME is shortened by ZDFRM. This happens at UP = 61440, 45056, 28672, 12288, 77824 respectively.

A buffer fault condition can occur several ways: If the value DEL from the CPU exceeds the capacity of the buffer memory >79864 then DELFLT becomes true. If $\sum$ FLT flip flop gets set the hardware attempts to skip three frames. A hardware malfunction has occurred in the delay cycle adder or multiplexers. If the Monostore memory has not executed a read or write cycle in time WRFAIL or RDFAIL is set. If delay between load pointer and ref-unload pointer is not within 512 and 1024 μs BFLT is set. Any of these errors are fatal and bad data is correlated.

Recorder Control 1

This board has all circuits to control motion of the video recorders. The circuits are straight forward and do not need much explanation. In the STOP mode recorders are halted and XFER is cleared. 60 Hz B and C are locked to 60 Hz A. The computer waits in an idle loop which is interrupted every 16 ms to reset the drop out error lights. When the START button is pressed the CPU can start 1, 2 or 3 recorders and wait till they are at normal speed and BOF errors, BUFFLT are off and helical frame count does increment every frame. Then the recorders B and C are slewed to line up the frames properly. The computer sets XFER, 60 Hz B and C are now independent of 60 Hz A, the CPU sets delay and the hardware is ready for data reduction.

Three identical circuits that control the head drum circuit of each recorder are located on this board. The circuits are the equivalent of the Hallman circuit for Mark II record terminals. With a timing circuit, ramp and sample-hold an error signal "HEADDRUM" is produced proportional to timing difference between BOF and 60 Hz. 60 Hz should be behind BOF by 750 μs ± 250 μs. If it is not within these limits, capacity of the buffer memory is exceeded and data is not properly correlated. "HEADDRUM" is connected to the head drum servo amplifier within recorders, biases the servo phase detector and therefore moves BOF to proper relation with respect to 60 Hz. "HEADDRUM" does now what trimpot R7 used to do with the old two station Leach hardware.

Recorder Control 2

This card contains the circuit that detects the frame counter and checks parity. DAT A, B, or C are shifted into a shift register and when BUFFRAME goes high the frame count is latched into an 8-bit latch. Frame count A is directly presented to the CPU thru a multiplexer. Frame count B and C may occur either before or after A and therefore must be latched a second time at the beginning of BUFFRAMEA. With EXC364, 464, or 564 the computer may select HFC A-B, A-C or B-C.

Two slew circuits, one for B and one for C, are located on this card, too. During slewing B or C is advanced or retarded by an integer amount of frames under computer control. The computer may command slewing from 0 to -32 or +31 frames by placing an appropriate binary number on SLEW 0-5. Following that with a RUNSTR pulse starts the slewing process. The hardware goes busy (SLEWBSY) till it is done. NOTE that slewing may be stopped by the program by setting slew 0 frames before slewing is completed. The first and last frames are slewed slowly (2 sec. per frame) and if there are more than two frames they are slewed faster (1 sec. per frame).

The number of frames to be slewed is loaded into up/down counters 5A, 5B. Gate 1G3 senses whether there is something to be slewed, gate 2E6 and FF7D6 senses whether to slew slow or fast. Circuits 3C6, 2G5, 2G9, 3A, 3B and 2F1,4 create either a count up pulse or a count down pulse every time one frame has been slewed. This process continues until a count of 0 has been slewed. The slewing is accomplished by changing the frequency of the 60 Hz reference. Gate 3E8 normally creates a reset pulse at REFUP=66680. If this reset pulse happens earlier or later the 60 Hz reference is changed accordingly and the recorders slew. Four gates 4A and 4B modify this reset pulse according to slow-fast and positive-negative slew. The circuit for slew C is identical to B.

The Correlator and Correlator Card

The correlator is located in two chassis: Chassis 0 contains all cosine channels and chassis 1 all sine channels. Each chassis has 36 correlator cards with 8 channels each and is organized in 6 blocks as shown in Figure 4.8. Each chassis has one additional card with 8 correlator channels which can be placed in parallel to any of the other cards by multiplexers under program control. An additional control card contains those multiplexers, multiplexers to select correlator modes as shown in Figure 1.11, and circuits to fan out clock signals. The correlator is read out under program control in a fixed sequence as shown in Chapter 3.

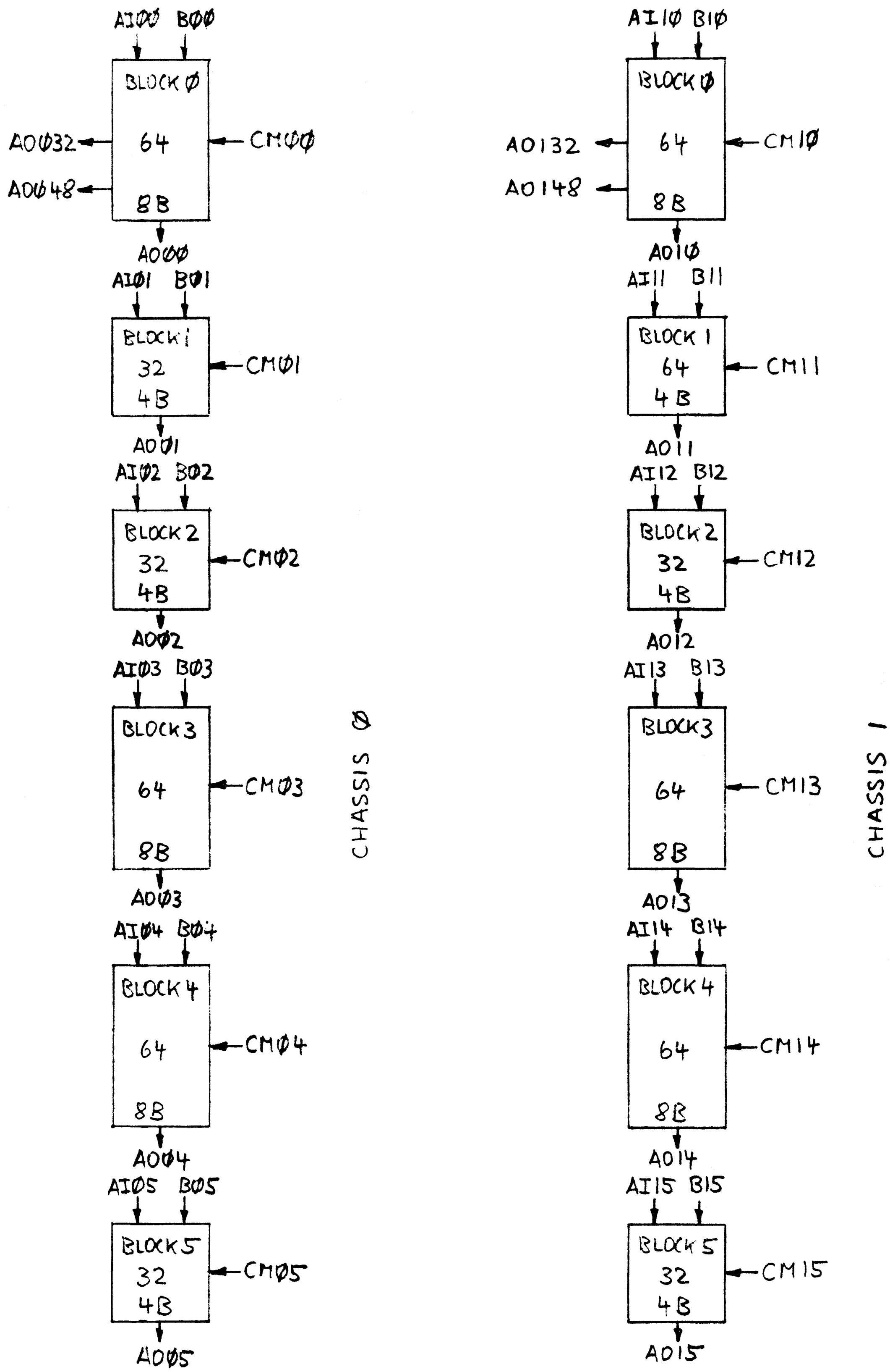


FIGURE 4.8 : CORRELATOR ORGANIZATION

The correlator card is designed straight forward using low cost 7400 series logic. It contains 8 exclusive or-gate-multipliers, one 8-bit shift register for lag, one 4-bit prescaler per channel and one 16-bit counter per channel for integration. Two 8-bit shift registers are used to read out all channels, one at a time.

When the correlator is correlating, undelayed data coming from the fringe rotator are applied on B. Delayed data are applied at AIN and come out at AOUT from where they go to the input of the next card. CS is the shift clock which is continuously clocking the "A" shift register. CS changes frequency proportional to bandwidth and is = 4 MHz at BW = 2 MHz. Multiplier clock CM is a 4 MHz clock which clocks the synchronous prescalers 74161. If a high is on the output of the exclusive or gate (bits A and B are the same) when CM goes negative the counters are incremented. If there is anti-correlation the counters are not incremented. CM is always a 4 MHz clock independent of bandwidth, however, CM is being turned off during correlator blanking. This can happen several ways. The correlator is blanked by the fringe rotator during 1/4 of each fringe cycle. It is blanked during frame gap, bad frames and bad data as detected by "DATAOK" and it is blanked under program control during read out. The carry outputs are then counted in ripple thru 16-bit counters 74177 normally for a period of 200 ms. After every 200 ms the correlator is blanked and is now ready for read out. The first channel is immediately available on the parallel output. After the computer has read the first channel a 250 ns negative pulse is applied at SRINPUT. After the next SHIFTCLOCK this low level is applied to the strobe input of the 16-bit counter of the first channel. This causes channel 2 to be loaded into channel 1 and now channel 2 is available on the output lines. At every subsequent SHIFTCLOCK this low level propagates thru the two 8-bit shift registers at a rate of 4 Mbits/s and shifts each channel up one counter. The output SROUTPUT is connected to the next card etc. It takes 4 μs to propagate thru one card and 300.5 μs to propagate thru the entire correlator. The program does not have to wait 300 μs for reading the second channel, the second channel is available in less than a CPU cycle, e.g. there may be several low bits propagating thru the correlator shift registers at one time. At the end of the correlator, e.g. the data input of the ast correlator card, a terminator is connected which grounds all input lines. As the correlator is read out "0's" are therefore shifted gradually into all counters and when all channels have been read the entire correlator is cleared except the first channel. One more "NXTWRD" command has to be executed to clear the first channel too. After this there still are several low bits propagating thru the shift registers for 300 μs and the correlator could not correlate during that time. This can be reduced to 4 μs with a "COR RECOVERY" command, which applies a low signal at SRSET of all correlator cards in parallel. It should be noted that while the correlator is read and cleared the prescalers are not affected. The four least significant bits are not erased; they are included in the counts during the next 200 ms integration. The counts of the correlator channels and check channels may differ by one bit. If a difference of three counts occurs the on-line program causes a message to be typed and turns off the correlator.

An independent command CORCLR applies a high level at CTRCLR input of the correlator cards in parallel which clears all counters and prescalers. It takes 31 μs to execute CORCLR which is followed by correlator recovery automatically.

Correlator mode multiplexers located on the correlator control board select A input, B input and multiplier clock of all six blocks and set the correlator into any one of 8 modes as shown in Figure 1.11.

A second set of multipliers 1F, 1E, 1D, 1C, 1B, 3F, and 3E control the extra check board with 8 check channels. The check board can be placed in parallel to any other card in the same chassis under program control. The check board duplicates exactly all of those 8 channels of correlation and independently of the type of data correlated should show identical counts. If a channel is not identical a hardware failure has occurred either in the particular correlator channel or in the check channel. Note that this works independently of correlator mode and it works while real data is correlated. Six control bits CHKB0-5 set the multiplexer. Octal 00 to 43 select board 00 to 53 as shown in Table 3.7. One additional multiplexer 8A is used so that the check card can also duplicate all total counts. This happens for check bits = 70 to 74. A low level is applied at AICHK by gates 8F and 2G and at BICHK by multiplexer 3F and all check channels count clock pulses. All check channels should have the same count and be equal to the total count.

TC Counter

This board contains nine 20-bit counters which count the total number of bits correlated for all modes: 3 autocorrelations and 3 complex cross correlations. The 16 most significant bits are available to the computer in similar fashion as for the correlator. This board also contains the circuitry for correlator clear and recovery which was described earlier.

Fringe Rotators

There are three three-level fringe rotators of the same type as described in Report #118. Each has one data input from the deskewing buffer and two data outputs in quadrature phase. These outputs go to the undelayed data inputs B of the correlator. Two additional MC outputs are multiplier enable lines for the cosine and sine correlators. Fringe rotator B and C is driven by independent fringe rate synthesizers which are under program control.

Fringe rotator B-C simply takes the difference of phase C - phase B. Fringe rotator B and C are built on two identical boards and rotator B-C is located on the master clock board.

The fringe rate synthesizer is different from the design in report #118. The phase is an eight bit binary number which the program sets on the FP lines. Then SETFP is executed and at the next 60 Hz interrupt precisely FP is strobed into phase registers 6F, and 4B. All less significant bits of phase registers 4C to 4F are cleared. Fringe rate registers 2C to 2G contain the current fringe rate. This fringe rate is added to the current fringe phase by adders 3B to 3F and the resulting new fringe phase is latched into the phase register every μsec. Every 1 μs the fringe phase is incremented by the amount of the fringe rate. Fringe rate register is set by 20 FR lines at the time when SETFR is executed. FR is the fringe rate in cycles per microseconds; a binary number with the binary point four places left. Maximum fringe rate is $\pm$62.5 kHz, minimum fringe rate is 0, smallest step is 62 mHz. Negative fringe rate is implemented by reversing direction of counter 6F. 6F counts down instead of up which results in a 180° phase reversal of sine channel phase PHASES and does not effect the cosine phase.

Buffer Interface

This board has most of the receiver-driver circuit to and from the buffer. Note that CS is the correlator shift clock which changes frequency with bandwidth. A, B, and C are data outputs to the correlator, FB and FC are data outputs to the fringe rotators and DATA, DATB, and DATC are outputs to a frame count detection circuit on delay display board.

This board also contains an unblanking delay circuit. As soon as data coming from deskewing buffers is good, DATOK becomes true. However, there still are invalid data bits in the correlator shift registers. The correlator has to stay blanked until they are cleared out. The time required is a function of the mode. Blanking outputs X, Y, and Z are delayed according to the table on the blueprint.

Delay and Fringe Rate Display

The fringe rate is displayed with a five digit LED panel display. When the fringe rate is >63.5 Hz then HIFR is high and PH7 is counted, which is the MSB of fringe phase, over a period of 1 second. The display is in Hz. If the fringe rate is <63.5 Hz then BTEN is counted which is 10 bits less down in the fringe phase register. The decimal point is moved three decimals left. It should be noted that an approximation is made here: 1024 = 1000 and at very low fringe rates it is possible to rotate the fringe rotator by updating the phase only; the fringe rate register may well be = 0. The display then may show 0 where in fact the rotator is rotating slowly.

The delay is measured and displayed as difference of 0 frame A and 0 frame B or C. Zero frame pulses are one pps pulses derived from decoded helical frame count 0. If data are poor, 0 frame may be decoded improperly and the display will not be stable. It typically jumps around in multiples of 16.6 ms or it may not change at all. One should recognize that the display shows the actual delay between the two data streams and not the delay which the computer has calculated and thinks it has put into the hardware.

TCD Display and Memoscope Alert

Decoded audio data are converted into parallel format by a 64 bit shift register. At the right time when a sync pattern of 11111110000 is recognized, parallel data are latched in a 52 bit latch where they are held for display and for input to the computer. Every frame the latch is updated. The circuit displays only one audio channel at a time. With multiplexer 1F any of three recorders A, B or C may be selected either under computer control when in XFER mode or by panel switches when in STOP mode. When in XFER mode and the multiplexer is changed from one recorder to another it will take between 16.6 to 33.2 ms for new data to be ready. During that time the display is blanked by TCDBLK. As data is processed and the computer scans thru the recorders rapidly one cannot read each recorder individually on the display. If one depresses one of the three select buttons, for example SWA, then during B and C the display is blanked and A may be read. The display will be dim and will flash because for over 2/3 of the time it is turned off. A retriggerable one shot circuit 10B detects if any of the 16 ms sync's are missing and turns on TCD error indicator.

The circuit for ALERT is simple and needs no further explanation. On the same board is the circuit to drive the memoscopes. Two D/A converters drive X and Y respectively of the Tektronix model 603 memoscopes. ZMEM1 and ZMEM2 turn on the beam currents to plot a point on the screen. Timing is important and needs to be considered for programming. It takes 15 μs for X and Y to settle for full scale deflection, and it takes 30 μs for Z to plot a point. Erasing a screen takes 250 ms during which time the scope goes busy. Another control is DIM which reduces the brightness of the stored image so that it may be viewed up to 1 hour and life of the CRT is extended. This function is active only when the brightness control on the front panel is completely counter-clockwise. Note that the scopes are forced dim when the computer is halted or when it goes into an unusual mode. COMPRDY and DLYTRK are both missing then and flip-flops 3G-3F are cleared.

Masterclock

This board contains 6 circuits: Masterclock, correlator-bandwidth registers, NXTWRD shaper, 60 Hz interrupt, pulsed delay and fringe-rotator B-C.

The masterclock consists of a 20 MHz crystal oscillator, a divider, multiplexer and driver circuits. The outputs are:

- MCLK: Masterclock 4 MHz squarewave for control circuits within correlator control chassis.
- SHCLK: Shift clock 4 MHz squarewave for correlator read out shift registers of correlator 0 and 1 respectively.

SHCLK QT:	1 MHz squarewave for TC counters board
1 MHz:	Squarewave for delay display
CM:	Multiplier clock 50 ns wide pulse 4 MHz for TC counters
CM0,1:	50 ns 4 MHz pulse for correlator multipliers
CS0,1:	Shift clock 50 ns wide for correlator shift registers. Frequency 4 MHz to 31.25 depending on bandwidth

Multiplier lines CM0 CM1 and shift clock lines CS0 and CS1 are long twisted pair lines terminated on both ends by 68Ω. This avoids overshoot and controls transition times accurately throughout the correlator. These lines are driven by open emitter line driver 8T13.

Next word shaper is a simple circuit which transforms the transmission of NXTWRD into a 250 ns wide pulse with precise time relation to CM.

60 Hz interrupt circuit has the necessary circuit to interrupt the CPU and interlock interrupts with DMA transfers. It connects to the computer via the I/O bus. This 60 Hz interrupt is the only interrupt of the CPU. Interrupt location is 0 since nothing is connected to the interrupt address select lines. 60 Hz from buffer sets request flip-flop 3G if interrupt enable flip-flops 2F8, 2F6 are set. At the next interrupt clock IUCK interrupt flip flop 3G sets and the CPU gets interrupted by IURX. After this interrupt is accepted by the CPU IUAX comes back and clears interrupt request flip-flop. If a DMA request is pending either TPIX or TPOX is low and interrupt flip-flop is held in the clear state by 3G13. At the next IUCK clock 3G9 will not be set. Furthermore 8E5 is held low so that request flip-flop 3G5 will not be cleared. This is necessary because an acknowledge to DMA request appears on IUAX. After DMA is serviced a waiting interrupt may then be executed at the next IUCK. Interrupts may be enabled and disabled under program control. Interrupt enable flip-flop is cleared by IUJX after each interrupt so that no interrupt is executed twice. The program needs to enable interrupts after each interrupt. When the computer is halted interrupt enable flip-flop is also cleared by SYRT when system reset is depressed.

A pulse delay circuit controls delay between tapes A-B and B-C. Every time RTD or ADV is pulsed by the program a clock pulse is deleted or inserted at UCLK. The unload counters in the buffers B and C are therefore retarded by 250 ns per pulse with respect to A. Since 60 Hz reference is derived from the unload pointer this will actually displace recorder B or C respectively. Although the advance and retard pulse are executed instantaneously in the buffer there is a limit how fast the video recorders can be slewed before head drum servo gets out of lock.

Diagnostic and Typical Failures

In our experience during the last two years problems and failures have mostly occurred in the correlator, the decoders, video tape recorders and computer 9 track tape drive.

Correlator failures are typically in the counters. If a counter counts improperly then there is a difference between that channel and the corresponding check channel. The program can correctly analyze and find the failing channel. If a counter fails in a way that parallel loading function of the chip malfunctions, then other channels than the failing channel are affected. The program will indicate failure at random channels or will indicate that the terminator is not zero. Often this happens when a totempole output is damaged so that the output voltage is between proper TTL levels. This typically causes a high being shifted into the next counter instead of a low. Note that since clearing the correlator is done by shifting in all low bits the correlator cannot be cleared. A diagnostic program READOUT tests whether the correlator shifts properly. Program CORTEST actually correlates data and compares correlator channels with check channel and detects errors by halting at particular error locations. Comments at those locations in the listing help analyze the problems. The same checking occurs while actual data is correlated by the on line program system. An error will be indicated by a TTY message if the difference is larger than two counts.

Failures of the decoder are indicated by various error lights and data cannot be decoded properly. This happens usually when the phase lock loop is maladjusted, which retrieves the lock from the BI-Ø data. Not only must the phase lock loop lock to the input data but the phase must be so that the decoder is able to sample in the middle of a bit cell. The adjustment of the trimpot capacitor for center frequency of the PLL is very critical and the circuit is somewhat temperature dependent. A front panel potentiometer is a fine control for the center frequency.

Failures of the video recorders are mostly not clear cut. Sometimes tape may work better on one tape recorder than on another. The difference may be in the video heads or the mechanical alignment or in the response of the preamplifier. These differences between recorders become less obvious when a good quality tape with good recording is played back.

Head drum servo and capstan servo are not too well designed. They are not critically damped. Head drum servo has significant temperature drift. In general however their performance is good enough for processing tapes properly. Since report #118 was written major improvements were made in the stability of the capstan servo and the head drum servo by cleaning up control track amplifier-clipper and, by closing the head drum servo loop which eliminates problems due to temperature drift, and by replacing the ± 12 internal supply with a well regulated external supply. Dramatic failures due to broken video heads, faulty components in the servos, bad switches or relays are easily spotted and repaired by replacement of a card or component. Excessive play in worn bearings, etc. can be spotted very easily and needs to be attended to by an experienced service technician.

The nine track 1/2" tape drive has given us numerous problems. Some of the gaskets of the vacuum system have failed, causing the vacuum to be unstable to the extent that tapes could not be loaded. We have had a sizable number of failures with the Molex connectors which interconnect all boards. According to Molex these connectors are not made for low voltage, low current applications as in this tape unit. Another failure we have had was in the controller timing circuit which sets record gap length. A diagnostic program "TAPE" checks for proper record gap length as well as proper recording.

Another diagnostic program "MEMO" is used to test the performance of both D/A converters and to check alignment of the memoscopes. MEMO displays three different patterns on the screen. A crossed rectangle makes visible any faulty bit of either one of the D/A converters. A checkerboard pattern checks for geometric distortion. The third pattern plots a point everywhere on the screen. Distortions in the floodgun become visible as well as burned out spot in the phosphor.

FFT Interface

Interface FFT (NOVA 820) to Varian 620

Two general purpose controllers are used to interface the Nova 820 to the Varian 620I computer. The Varian uses a buffered I/O controller mode DM 373B with device address 67. The Nova uses a general purpose interface mode 4040 and data registers mode 4041 with device address code 04 and interrupt mask bit 4. Each CPU looks to the other as a peripheral. Data transfers are in the "test and transfer" mode. The Nova 820 may also be operated in the interrupt mode. No data channels are provided.

Data transfer occurs in parallel over two independent 16 bit data lines. Transfer may occur simulataneously in both directions. Over the same lines 16 bit command words are transmitted. Handshaking is done on the ready-acknowledge principle. Five status bits are used by the Varian to transfer status information to the Nova of which two are not assigned yet. Six additional status bits are used by the Nova to indicate status to the Varian of which one is not assigned yet.

Description of Varian Interface

Device Address = 67

OTB 0 to 15:	Output of 16 bit parallel data or control data.
BI 0 to 15:	Input of 16 bit parallel data or control data.
POT 0 = IACK:	To be set after either a data or control word has been read by Varian.
POT 1 = ODRDY:	To be set after output data has been placed on OTB lines.
POT 2 = OCRDY:	To be set after output command has been placed on OTB lines.
POT 3 = STAT 1:	Sets spare status bit.
POT 4 = STAT 2:	Sets spare status bit.
POT 5 = CLRSTAT:	Clears status bit 1 and 2, FFT RESET, ODRDY, OCRDY, does not clear VARSYRT.

SEN 0 = OACK:	Set after Nova has accepted either a data or control word. Gets reset after either ODRDY or OCRDY.
SEN 1 = IDRDY:	Set after Nova has place a data word on BI. Gets reset by IACK, NOVA IORST, NOVA CLR.
SEN 2 = ICRDY:	Set after Nova has placed a command word on BI. Gets reset by IACK, NOVA IORST, NOVA CLEAR.
SEN 3 = STAT3:	Spare status bit. Gets reset by CLRSTAT, NOVA IORST, NOVA CLEAR. Gets set by NOVA IOPULSE.
SEN 6 = FFTRESET:	Set during Nova power turn on and during NOVA IDRST instruction and during Nova console reset. Cleared by CLRSTAT.
SEN 7 = FFTPWRON:	Set when power is applied to Nova.
SYRT:	Sets VARSYRT status flip-flop when Varian console master reset is depressed, VARSYRT is cleared by DATINC, NOVA IORST, NOVA CLEAR.

Description of Nova Interface

Device Address	= 04
Device Code	= 04
Interrupt Mask Bit	= 4

Output data and output command use the same output lines and therefore only one may occur at a time. DOA sets status flip-flop IDRDY for transfer of data, DOB sets status flip-flop ICRDY for transfer of command. Register C is not implemented. IDRDY and ICRDY are reset by Varian IACK, IORST, CLEAR.

Status 3 (not assigned yet) is set by the pulse output (P = 11 bit 8, 9) of control function F. Status 3 is reset by IORST or clear command code C in F. Status bit FFTWRON is set whenever power is applied to the Nova. Status bit FFTRESET is set by NOva IORST and is cleared by Varian CLRSTAT.

Input data and input command use the same input lines and therefore only one may occur at a time. DIA read a data word in and resets IDRDY status flip-flop. DIB reads a command word in and resets ICRDY status flip-flop. DIC reads a 5 bit status word in status word format:

	VAR.SYRT	IDRDY	ICRDY	SPARE1	SPARE2
BIT	11	12	13	14	15

VAR.SYRT: Is set when Varian console master reset is depressed and is reset by DIC instruction.

IDRDY: Is set by Varian ODRDY=POT67-1 and reset by DIA or Varian CLRSTAT=POT67-5 or Nova CLR instruction or Nova IORST.

ICRDY: Is set by Varian OCRDY=POT67-2 and reset by DIB or Varian CLRSTAT=POT67-5 or Nova CLR instruction or Nova IORST.

SPARE1 or 2: Is set by Varian SPARE1 or 2 = POT67-3 or 4, and is reset by CLRSTAT=POT67-5 or Nova CLR instruction or Nova IORST.

4040 OUTPUT CONTROL

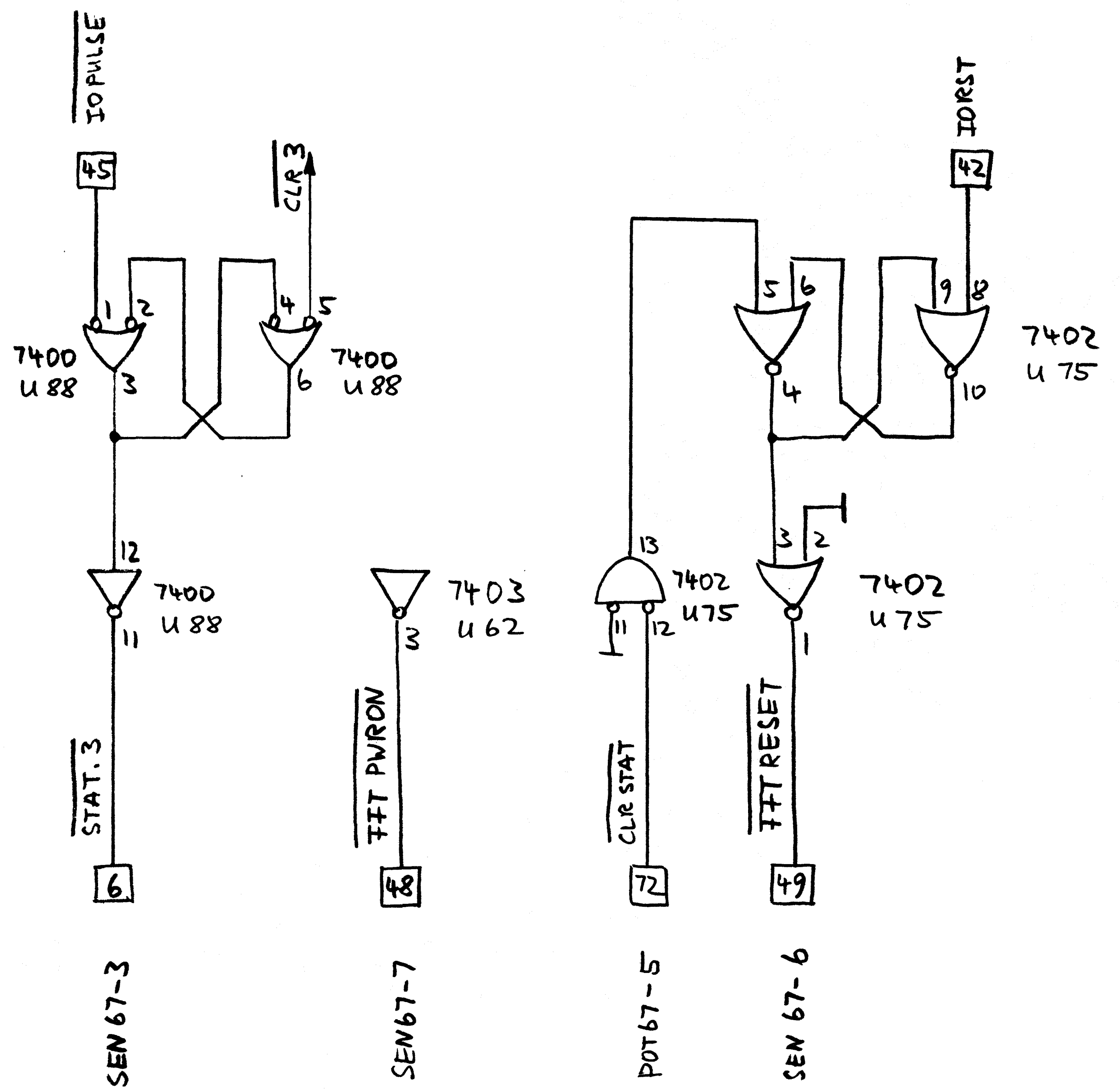


FIGURE 4.9

4040 INPUT CONTROL

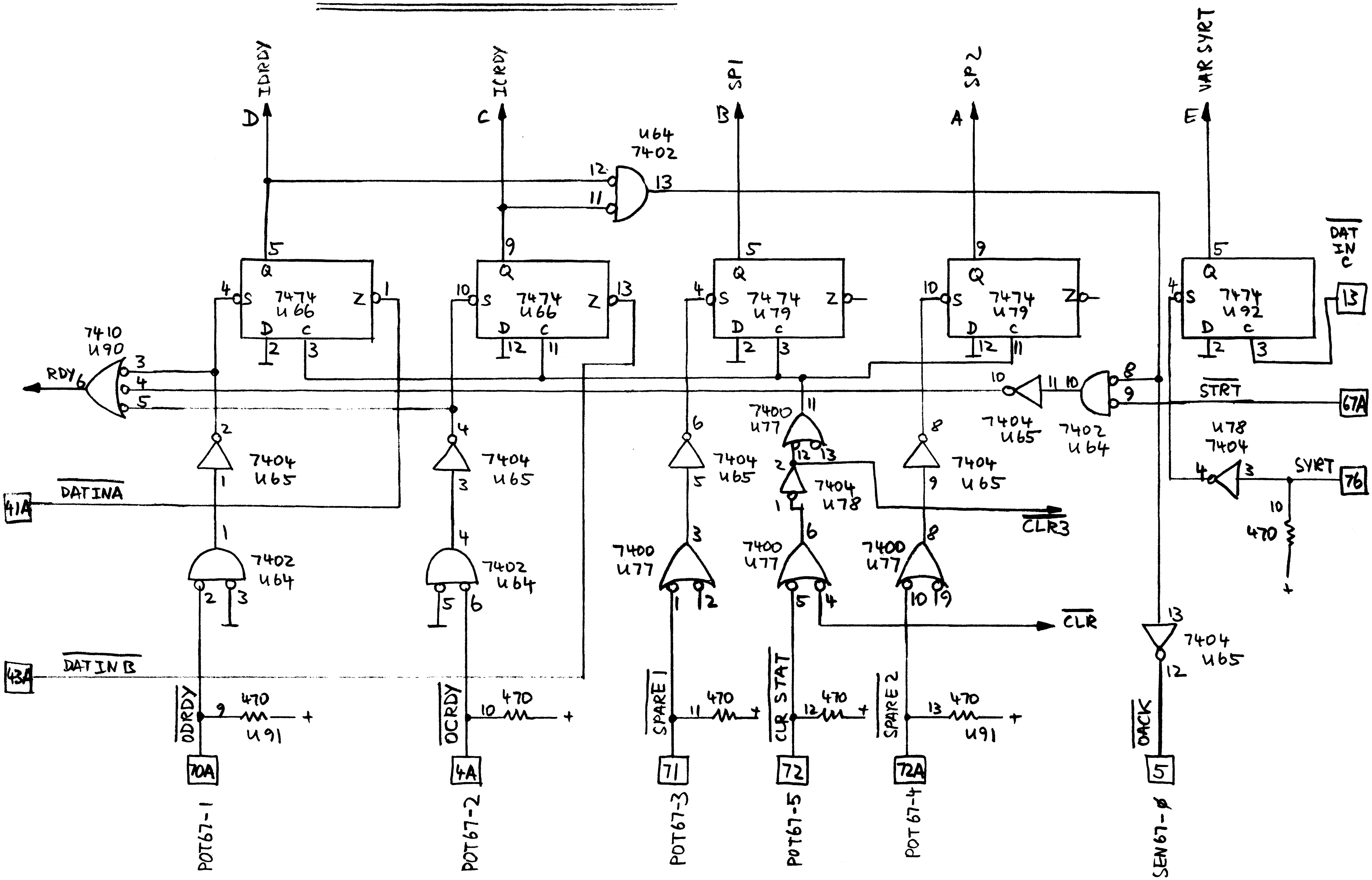


FIGURE 4.10

4040 OUTPUT CONTROL

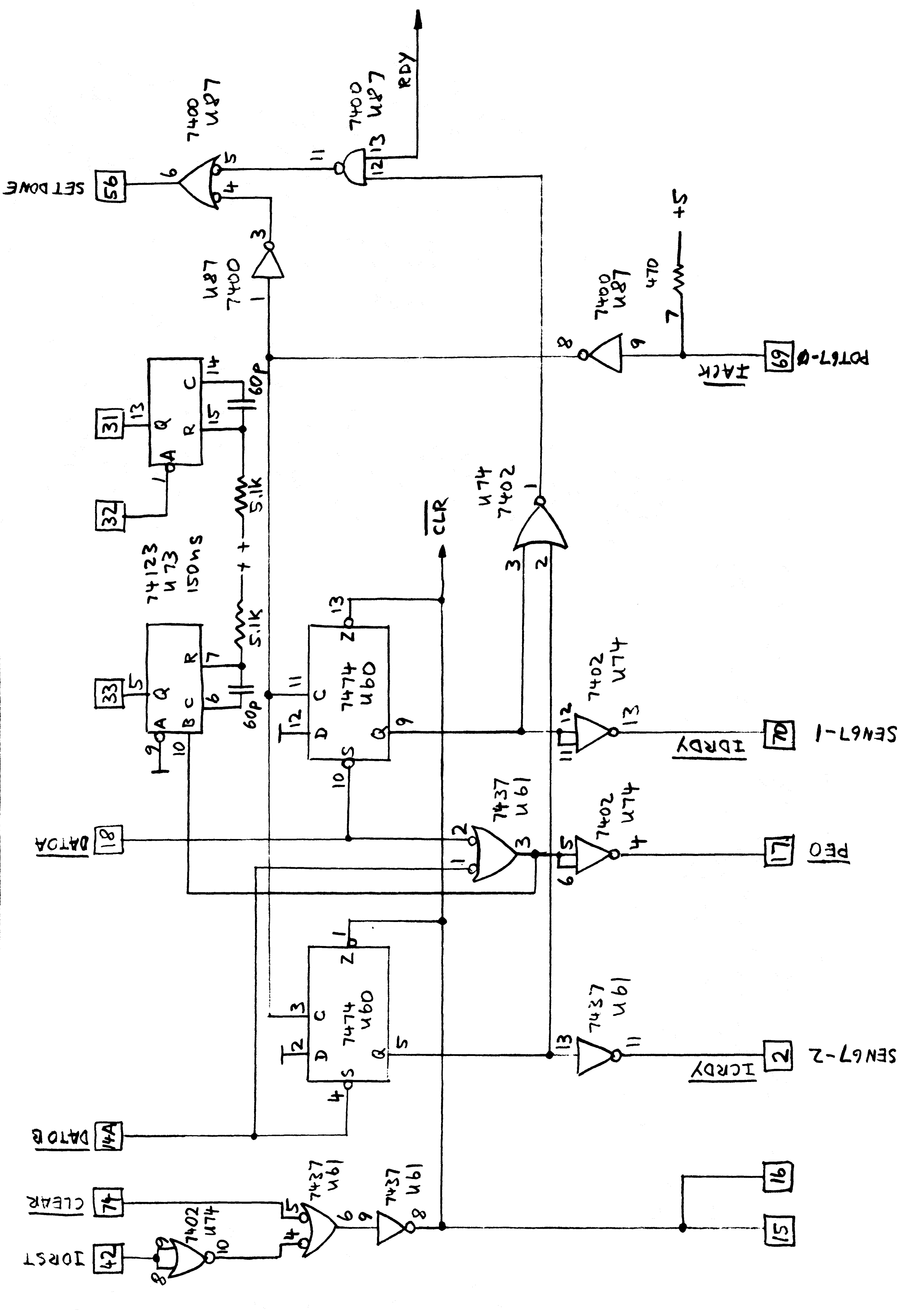


FIGURE 4.11

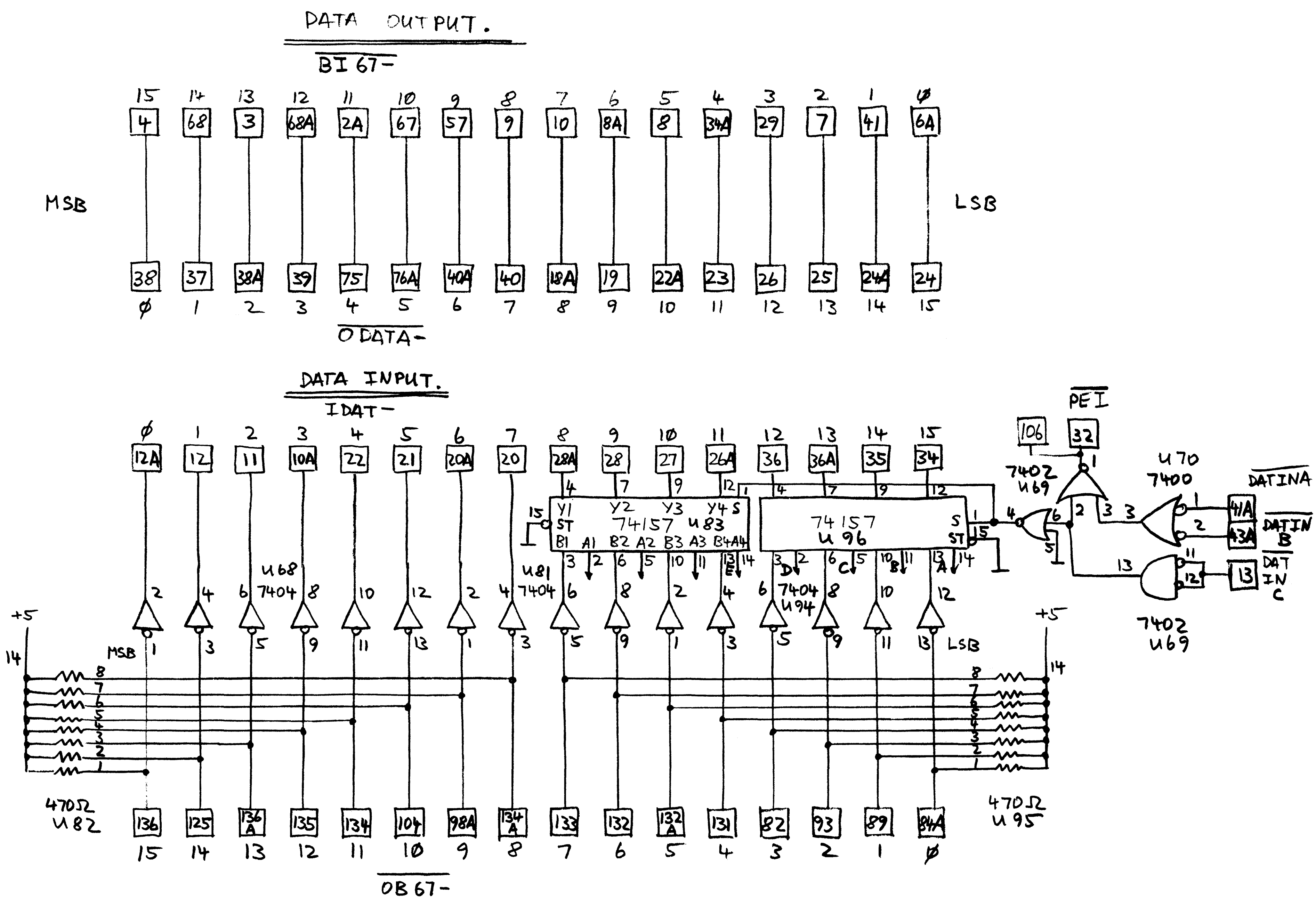

DATA OUTPUT.
BI 67-
MSB
LSB
O DATA-
DATA INPUT.
IDAT-
74157
U83
74157
U96
U68
7404
U81
7404
7404
U94
7402
U69
U70
7400
7402
U69
PEI
DATINA
DATIN B
DAT IN C
470Ω
U82
470Ω
U95
+5
OB 67-

FIGURE 4.12

VARIAN - NOVA - INTERFACE CABLE

NAME	VARIAN CD. EDGE	COLOR	PADDLE BD	NOVA BACKPLANE	4040 WW PIN
SENØ	1-1	BK	2	A92	5
Ret	1-2	GY			
SEN1	1-3	OR	3	A91	70
Ret	1-2	GY			
SEN2	1-4	BN	4	A78	2
Ret	1-5	GY			
SEN3	1-6	YE	5	A77	6
Ret	1-5	GY			
SEN4	1-7	GN	6	A76	1
Ret	1-8	GY			
SEN5	1-9	BL	7	A75	49A
Ret	1-10	BY			
SEN6	1-11	PU	8	A73	49
Ret	1-10	GY			
SEN7	1-12	WH	9	A71	48
Ret	1-10	GY			
BI Ø	1-13	BK	10	A69	6A
Ret	1-14	PU			
BI 1	1-15	RD	11	A67	41
Ret	1-14	GY			
BI 2	1-16	YE	12	A65	7
Ret	1-17	PU			
BI 3	1-18	OR	13	A63	29
Ret	1-17	PU			
BI 4	1-19	BL	14	A61	34A
Ret	1-20	PU			
BI 5	1-21	BN	15	A59	8
Ret	1-20	PU			
BI 6	1-22	WH	16	A57	8A
Ret	1-23	PU			
BI 7	1-24	RD	17	A47	10
Ret	1-23	PU			
BI 8	1-25	GN	18	A49	9
Ret	1-26	PU			
BI 9	1-27	PU	19	A79	57
Ret	1-26	WH/BK			
BI 10	1-28	YE	20	A81	67
Ret	1-29	WH/BK			
BI 11	1-30	OR	21	A84	2A
Ret	1-29	WH/BK			
BI 12	1-31	YE	22	A83	68A
Ret	1-32	WH/BK			

VARIAN - NOVA - INTERFACE CABLE

NAME	VARIAN CD. EDGE	COLOR	PADDLE BD	NOVA BACKPLANE	4040 WW PIN
OB8	2-13	WH	42	B48	134A
Ret	2-14	BK			
OB9	2-15	YE	43	B49	98A
Ret	2-14	BK			
OB10	2-16	BL	44	B51	104
Ret	2-17	BK			
OB11	2-18	BL	45	B52	134
Ret	2-17	GN			
OB12	2-19	BL	46	B53	135
Ret	2-20	WH/BK			
OB13	2-27	OR	47	B54	136A
Ret	2-26	RD			
OB14	2-25	YE	48	B67	125
Ret	2-26	RD			
OB15	2-24	WH	49	B69	136
Ret	2-23	RD			

NAME	VARIAN CD. EDGE	COLOR	PADDLE BD	NOVA BACKPLANE	4040 WW PIN
BI13	1-39	WH	23	A86	3
Ret	1-39	BL			
BI14	1-37	OR	24	A85	68
Ret	1-38	BL			
BI15	1-36	BN	25	A88	4
Ret	1-35	WH/BK			
POTØ	2-34	RD	26	A87	69
Ret	2-35	BN			
POT1	2-36	GN	27	A89	70A
Ret	2-35	BN			
POT2	2-37	BK	28	A90	4A
Ret	2-38	BN			
POT3	2-39	OR	29	B6	71
Ret	2-38	BN			
POT4	2-40	WH	30	B11	72A
Ret	2-38	BN			
POT5	2-42	YE	31	B13	72
Ret	2-41	BN			
SYRT	2-31	BL	32	B15	76
Ret	2-29	RD			
SENC	2-33	GN	33	B19	83
Ret	2-32	RD			
OBØ	2-1	YE	34	B23	84A
Ret	2-2	GN			
OB1	2-3	OR	35	B25	89
Ret	2-2	GN			
OB2	2-4	WH	36	B27	93
Ret	2-5	GN			
OB3	2-6	BK	37	B31	82
Ret	2-5	GN			
OB4	2-7	GN	38	B34	131
Ret	2-8	WH/BK			
OB5	2-9	RD	39	B36	132A
Ret	2-8	WH/BK			
OB6	2-10	RD	40	B38	132
Ret	2-11	BK			
OB7	2-12	OR	41	B40	133
Ret	2-11	BK			

A	Correlator input data from recorder A
ADV	Advance flip flop
ADVANCE	Control pulse from Varian, advances recorder 0.25 μs.
AICHK	A-input of checkboard
ALERT	Control pulse from Varian to ring beeper
ALERT ENA	Control pulse from Varian to enable beeper
ALERT OFF	Control pulse from Varian to disable beeper; also sense-bit to Varian
ASTRODATA	BI-Ø coded data from recorders
AUD 2	Control bit from Varian to select audio track 2
AUDIO	BI-phase coded time data from audio tracks
B	Correlator input data from recorder B
BCCOS	Correlator input data for B-C-cosine baseline
B COS	Correlator input data for A-B-cosine baseline
BCSIN	Correlator input data for B-C sine baseline
BI	16 bit binary input lines to Varian
BICHK	B-input of checkboard
BLKCOR	Control bit from Varian to blank the correlator
BOF	Beginning of frame
BOFFLT	Sense bit to Varian when beginning of frame is not detected. T = 16.6 msec.
BSIN	Correlator input data for A-B-baseline
BTEN	Bit 10 of fringe rotator
BUFFLT	Sense line to Varian when data is not transferred properly thru deskewing buffer
BUFFRAME	Frame signal after deskewing buffer
BW	Bandwidth
BWSTR	Bandwidth strobe pulse which strobes bandwidth on BW lines into hardware
C	Correlator input data from recorder C
CCOS	Correlator input data for A-C-cosine baseline
CD	Count down signal
CH	Chassis
CHB	Varian output lines to set checkboard multiplexer
CHK	Check

CLRSTAT	Control pulse from Varian to clear Nova status flip-flops
CLRXFER	Control pulse from Varian to clear transfer flip-flop
CM	4 MHz multiplier clock for TC counters
CMØ.1	4 MHz multiplier clock to chassis Ø and 1
COMPRDY	Control pulse from Varian to turn off 'Computer off' light
CORBSY	Sense line to Varian, goes true after CORCLR and CORRECOVERY command
CORCLR	Control pulse from Varian to clear correlator
CORMX	Control lines from Varian to set correlator mode
CORMXSTR	Control pulse from Varian which strobes correlator mode on CORMX lines into hardware
COROUT	16 parallel output lines from correlator to Varian
CORRECOVERY	Control pulse from Varian to recover correlator for next correlation after all channels are read
CORTEST	Diagnostic correlator test program
CPU	Central Processor Unit
CRT	Cathode ray tube
CS	Shift clock
CSØ,1	Shift clock to chassis Ø or 1
CSIN	Correlator input data for A-C sine baseline
CTRCLR	Counter clear input of correlator card
CU	Count up
DAT	16 bit correlator output data
DATOK	Correlator input flag, true when data has no errors
DELAY	Varian output lines to set Monostore delay
DELAYTRACK	Control pulse from Varian to clear 'Computer off' light
DELCT	Hardware counter to keep track of frame cycle 0-1-2-3-4-0
DELCYC	Hardware delay cycle flip flop is set during time when new delay is set
DELSTR	Control pulse from Varian to strobe a new DEL into the hardware
DIM	Signal to Memoscope to dim the screen
DIMMEMO	Control pulse from Varian to dim Memoscopes
DIMRESET	Control pulse from Varian to brighten Memoscope
DMA	Direct memory access
DROPOUT	Sense line to Varian, set when error in data has occurred
DSPTC	Input line to Varian, panel time constant switch

EOF	End of frame
EXC	External control, control pulse from Varian
FB	Undelayed data B
FC	Undelayed data C
FCT	Delayed frame signal
FFTRESET	Sense line to Varian, true when Nova is reset
FFTPWRON	Sense line to Varian, true when Nova power is on
FLERR	Frame lenght error, turns on dropout light
FP	Fringe phase
FPB	Varian output lines for fringe phase B
FPC	Varian output lines for fringe phase C
FR	Varian output lines for fringe rate
FRAME	Frame signal as decoded off the tape
FRM	Frame signal delayed by buffer
HD	Input to Varian, hundred days
HEADDRUM	DC signal to control phase of recorder head drum servo
HEADSWITCH	30 Hz signal from recorder tachometer
HFC	Input line to Varian, helical frame count
HFCOK	Input line to Varian, true when helical frame count parity is decoded properly
HIFR	Line for fringe rate display, true if rate >62 Hz
HZ	Hertz (cycles per second)
IACK	Control pulse from Varian to Nova after Varian has accepted data from Nova
ICRDY	Varian sense line, true when Nova has sent a control word
IDRDY	Varian sense line, true when Nova has sent a data word
INTRPT ENABLE	Control pulse from Varian to enable interrupt logic
INTRPT DISABLE	Control pulse from Varian to disable interrupt logic
IVC	International Video Corp.
IUAX	Varian I/O bus line, interrupt acknowledge
IUJX	Varian I/O bus line, interrupt jump
IUCX	Varian I/O bus line, interrupt clock
IURX	Varian I/O bus line, interrupt request
LED	Light emitting diode
LDUP	Load unload pointer
LP	Load pointer

MA	Monostore address lines
MCA	Multiplier clock for autocorrelator A
MCB	Multiplier clock for autocorrelator B
MCBC	Multiplier clock for A-B-cosine baseline
MCBS	Multiplier clock for A-B-sine baseline
MCC	Multiplier clock for autocorrelator C
MCCBC	Multiplier clock for C-B-cosine baseline
MCCBS	Multiplier clock for C-B-sine baseline
MCCC	Multiplier clock for A-C-cosine baseline
MCCS	Multiplier clock for A-C-sine baseline
MCLK	Master clock
MDO	Monostore data out
MEMOBSY	Sense line to Varian, true when Memoscope is busy
MEMOCLR	Control pulse from Varian, erases screen of Memoscope
MEMOSTR	Control pulse from Varian, turns on Memoscope beam to plot a point
MEMOX (Y)	Varian output lines to set Memoscope beam
MKIIC	Input line to Varian, set when IVC tapes are played
MODE2	Correlator mode 2 line
MRC	Monostore read command
MSB	Most significant bit
MWC	Monostore write command
NEGFR	Varian output line for negative fringe rate
NOOP	No operation
NEXTWRD	Control pulse from Varian, places the next word from correlator on COROUT lines
OACK	Sense line to Varian, set after Nova has accepted a word from Varian
OCRDY	Control pulse from Varian, tells Nova that Varian has sent a control word
ODRDY	Control pulse from Varian, tells Nova that Varian has sent a data word
OVFLO	Overflow flip flop of adder
OTB	Varian output bit
PH7	Most significant bit of fringe phase
PLL	Phase lock loop

READOUT	Diagnostic program
REFCLK	4 MHz reference clock to buffer
REFUP	Reference unload pointer
RESET ERROR	Control pulse from Varian, resets dropout
RETARD	Control pulse from Varian, retards recorder by 250 nsec.
RDFAIL	Read-fail line, set when a hardware read error is detected
RDREQ	Read request line
RTD	Retard flip flop
RUN	Varian output line, turns on recorder
RUNSTR	Control pulse from Varian, strobes RUN into hardware
SC	Shift clcok, see page 4-20
SELHFC	Control pulse from Varian, sets HFC multiplexer
SELTCD	Control pulse from Varian, sets TCD multiplexer
SEN	Varian sense lines
SETFP	Control pulse from Varian, strobes FP into hardware
SETFR	Control pulse from Varian, strobes FR into hardware
SETSTAT1,2	Control pulse from Varian, sets status flip-flop in Nova
SETWRREQ	Set write request line
SETXFER	Control pulse from Varian, sets correlator into transfer mode
SHCLK	4 MHz shift clock for readout of correlator
SHCLKQT	1 MHz clock for TC counter board
SHF	Short frame signal
SKPFRM	Skip frame
SLEW	Varian output lines to slew recorders
SLEWBSY	Varian sense line, true when recorders are slewing
SRDREQ	Set read request
SREFUPST	Set reference unload pointer in start mode
SRINPUT	Shift input of correlator to read out correlator
SROUTPUT	Shift output of correlator to read out correlator
STAT3	Varian sense line, senses Nova status 3 flip-flop
STOP	Varian sense line for stop button
SW	Switch
SYNCADD	Address lines for dropout sync

SYRT	System reset
S1-8	8 states during which new delay is strobed into hardware
TAPE	Diagnostic program
TC	Total count
TCAUTO	Total count of autocorrelator
TCCROSS	Total count of cross correlator
TCD	Time coded decimal
TCD BLK	Time code blank to blank display
TCD CLK	Time code clock
TCD DAT	Time code data
TD	Input to Varian, ten day
TH	Input to Varian, ten hour
TM	Input to Varian, ten minutes
TOTEMPOLE	Push-pull output stage
TPIX	Varian I/O bus line, trap input
TPOX	Varian I/O bus line, trap output
TS	Input to Varian, ten second
TTY	Teletype
UCLK	Unload clock
UD	Input to Varian, unit day
UH	Input to Varian, unit hour
UM	Input to Varian, unit minutes
UP	Input to Varian, unit total power
US	Input to Varian, unit seconds
UT	Input to Varian, unit terminal I.D.
VALMA	Valid monostore memory address
VALFR	Valid frame
VALSYNC	Valid dropout sync
VR	Video recorder
WØ,1	Data to be written into sync memory
WRFAIL	Write fail line, set when a hardware write error is detected
WRREQ	Write request
WSAD	Write sync at this address

X	Analog signal to Memoscope for x-deflection
XFER	Sense line to Varian, transfer
Y	Analog signal to Memoscope for Y-deflection
ZMEM	Signal to Memoscope to turn on beam
1MHZ	1 MHz squareware for delay display
60 HZ REFERENCE	Reference signal to video recorders
60 HZ REF	Internal 60 Hz signal
60 HZ	Internal 60 Hz signal
ΣFLT	Adder fault, set when hardware does not work properly during DELCYC