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THE MARK II DATA QUALITY ANALYZER/DECODER

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Richard J. Lacasse

1. Introduction

The NRAO Data Quality Analyzer/Decoder (DQA/D) is an instrument designed to give a quantitative indication of the quality of data recorded in Mark II format. Its primary purpose is to give the user an indication of the readability of his data on the Charlottesville Mark II processor while he is still at a telescope site.

This is accomplished by the logical duplication of key features of the processor's decoder and data quality analyzer circuits coupled with real-time accumulators and displays. The decoder and data quality analyzer circuits are discussed from three points of view in this report. First the specifications of the DQA/D are presented. This is a "black box" point of view; only the signals required by and produced by the DQA/D are specified. No details of the circuits internal to the unit are given. Secondly, a description of both the decoder and data quality analyzer is given based on functional block diagrams of each. Finally, the schematic drawings of all the circuits are included.

The reader who has little familarity with the Mark II recording systems is referred to NRAO Electronics Division Internal Report No. 118 by B. G. Clark, R. Weimer, and S. Weinreb. This gives a good general overview of the system, but is inaccurate in some details due to the evolution of the system. Up-to-date details, relevant to the DQA/D, are included in Appendix A. In particular, these include the formats of the Mark II and Mark IIC video and audio tracks.

Appendix B includes a variety of information useful for adding a DQA/D to a record terminal.

2. Data Quality Analyzer/Decoder Specifications

2.1 The following describes all the inputs, outputs, and switches of the DQA/D. Refer to Figures 1 and 2 for help in locating these. The figures in Appendix A, which depict the formats of Mark II and Mark IIC video and audio tracks should also be conducive to the understanding of some of the information below.

2.2 Front Panel:

Power Switch: Connects AC power to internal supplies in the up position.

Power Indicator LED: On when AC power and 5 volt supply are on.

Error Display: Indicates the number of errors accumulated in a selected counting interval. Three classes of errors are displayed: Beginning of Frame (BOF), Frame Count (FC), and Drop Out (DO). Maximum count = 999_{10} for each class.

BOF LED: Pulsed on for 8 msec each time a BOF error is found.

Parity LED: Pulsed on for 8 msec each time the parity of the frame count is wrong.

Frame Count LED: Pulsed on for 8 msec each time the present frame count does not equal the previous frame count plus one, modulo 60.

Drop Out LED: Pulsed on for 8 msec if one or more drop outs (missing or misplaced sync word) occurs in a frame.

Integration Period Selector Switch: Determines the error counting interval: 1, 10, or 60 seconds.

Integration Period Reset Switch: Begins a new integration period when released.

Playback/Read-After-Write Switch: For IVC recorders (Mark IIC format), must be in Playback when playing back and Read-after-Write when recording. For Ampex recorders, this switch has no effect.

Audio 1/Audio 2 Switch: Selects the audio track to be displayed.

Audio Track Display: Displays part of the information on Audio 1 or Audio 2 as selected by the Audio 1/Audio 2 switch. For Audio 1, Total Power, Hours, Minutes, and Seconds are displayed. For Audio 2, Days and Source Code are displayed.

2.2 Continued:

Frame Output: A TTL logic signal which is low during part of the video record gap and high otherwise.

BOF Output: A TTL logic signal which is high for approximately 100 ns when the beginning of frame code is detected.

Data Output: Decoded data stream, in TTL levels.

EOF Output: A TTL logic signal which is high near the end of the video frame.

2.3 Rear Panel:

AC Power: Power input, 47-63 Hz, 105-125 V rms, 1 A.

Fuse: 2A, Slo-Blow.

4 MHz SØM: Input from recorder. "Astrodata", or clipped diphase video signal at 4 Mb/s, 0.3 to 15 V p-p into 75 Ω.

Audio 1 SØM: Input from recorder. Diphase time code at 3.84 Kb/s, 0.5 to 20 V p-p, into 1 K Ω.

Audio 2 SØM: Input from recorder. Diphase I.D. code at 3.84 Kb/s, 0.5 to 20 V p-p, into 1 K Ω.

60 Hz: Input from Format Unit's 60 Hz, or "External Sync" output, into three TTL loads. Note that it may be necessary to buffer the output to obtain the necessary drive.

Headswitch: For Ampex recorders (Mark II format), this input is obtained from the recorder's headswitch output: 30 Hz square wave, 7 V p-p ± 100%, into 5.1 K Ω.

Ampex/IVC Switch: In Ampex position, specifies Ampex VR 660 (Mark II) input format; in IVC position, specifies IVC (Mark IIC) format.

3. Decoder Block Diagram Description

3.1 Astrodata Decoder

The primary functions of the astrodata decoder are clock recovery, data recovery, and Beginning of Frame detection. These can be broken down into a few major subdivisions, as shown in Figure 4. This figure also shows the necessary I/O interfacing. A description of the astrodata decoder, based on Figure 4, follows.

3.1 Continued:

The 4 MHz split phase modulated (SØM) astrodata is first amplified and clipped to make it compatible with the circuits that follow. The amplifier employs hysteresis as a means of noise rejection.

To decode the astrodata, it is essential to create a clock which is phase locked to the data rate. This is accomplished by the Edge Detector, Phase Locked Loop, and Frequency Divider. The edge detector produces a pulse each time the data changes state. These pulses are the input to the phase locked loop, which phase locks an 8 MHz clock to the incoming pulses. A simple frequency divider then produces the phase-locked 4 MHz clock which is used in many places in the decoder, as well as in the data quality analyzer.

The Data Recovery circuits consist of a Data Decoder, Serial to Parallel Converter, and Buffer. The Data Decoder uses the phase-locked 8 MHz clock to demodulate the split-phase modulated, amplified, clipped astrodata. The demodulated data is clocked into a serial to parallel converter for use in the data quality analyzer. One of the outputs of the Serial to Parallel Converter also goes to the BOF Detection circuits and to the scope display buffer.

To detect the beginning of frame, a search is made for a particular bit pattern in the data stream during a time window. The pattern is detected by logic gates whose inputs come from Serial to Parallel Converters. The time window is created in one of three ways, determined by the positions of the IVC/AMPEX and PLAYBACK/READ-AFTER-WRITE switches.

With the IVC/AMPEX switch in IVC position, and the PLAYBACK/READ-AFTER-WRITE switch in the PLAYBACK position, the following sequence occurs.

3.1 Continued:

The Timing Circuits detect the proper edge of the 60 Hz REFERENCE signal and open a 1.3 msec time window. During this window, the IVC BOF Window Logic circuits search for a particular sequence of twenty four bits in the data stream. If and when it is found, the BOF Window Logic produces a one bit wide time window.

With the IVC/AMPEX switch in IVC position and the PLAYBACK/R.A.W. switch in R.A.W. position, the sequence of events is identical to the one depicted above, with one exception: The 60 Hz reference signal is delayed before being applied to the Timing Circuits [1].

With the IVC/AMPEX switch in the AMPEX position and the PLAYBACK/R.A.W. switch in either position, the following sequence occurs. The HEADSWITCH signal is amplified and clipped, and edge detected similarly to the video signal. The edges start a 45 μsec interval during which noise created by the headswitch on the video signal is blanked. After this interval, the Ampex BOF Window Logic searches for the first zero bit in the data stream. (The first zero bit normally signifies the beginning of 2/3 clock of the Ampex format.) Having found the first zero bit, the logic counts 31 clock intervals, and then opens a four bit wide window.

Depending upon the position of the IVC/AMPEX switch, either the IVC or AMPEX timing window goes to the BOF Logic. If this logic finds the proper three bit pattern within the time window, a BOF pulse is produced. In IVC, PLAYBACK mode, if the BOF pulse does not occur within 1.3 msec of the 60 Hz REFERENCE, a BOF error is flagged by the BOF Error Detection

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[1] The delay is equal to the amount of time by which the read-after-write head trails the write head (about 5.6 msec).

3.1 Continued:

Logic. In the IVC, R.A.W. mode, a BOF error is flagged if the BOF pulse does not occur within 1.3 msec of the delayed 60 Hz REFERENCE signal. In Ampex mode, an error is flagged if the BOF pulse does not occur within the four bit timing window provided by the AMPEX BOF-Window Logic.

3.2 Audio Decoder (Time Code Data Decoder)

In the early days of the Mark II system, only time data was recorded on audio track. At this point in time, a variety of information is recorded on both audio tracks. For this reason, "Time-Code-Data Decoder" is now a misnomer. For lack of a better name, "Audio Decoder" is now used. Its function is to demodulate the split-phase modulated data on either audio track and to display a part of it. A functional description of the Audio Decoder, based on the block diagrams of Figure 5 follows.

A front panel switch, Audio 1/Audio 2, determines which audio track is decoded. The selected audio track signal is first amplified and clipped to make it compatible with the circuits that follow. The output of the amplifier-clipper goes to the clock recovery and data recovery circuits.

The function of the clock recovery circuit is to produce a 3.84 kHz clock for the other circuits in the decoder. This is accomplished by edge detecting the input waveform and using the detected edges to trigger a non-retriggerable one-shot. This technique produces a 3.84 kHz clock waveform with a 75% duty cycle.

The data recovery circuits consist primarily of a decoder and some shift registers. The decoder uses the recovered clock to demodulate the data stream. The demodulated data is fed through two shift registers to accomplish serial to parallel conversions. The outputs of the first

3.2 Continued:

serial to parallel converter is used by the sync extraction circuits, while the outputs of the second go to the latching display.

The sync extractor circuit produces a sync pulse which is used to latch data into the display. The sync detector produces a provisional sync when it sees a certain pattern in the data stream. The pattern can occur at two times in a frame, once at the beginning of frame and possibly a second time in the total power bits. (See Appendix A, Audio Track 1 Format.) Since a sync pulse is desired only at the beginning of frame, a sync window generator is used to produce an enabling pulse. This generator makes use of the fact that the time from the beginning of frame to the total power bits is longer than from the total power bits to the following beginning of frame, in order to get locked up in the correct sync. Once locked on the correct sync it produces a window timed such that only the beginning of frame sync passes through the AND gate to the latching display.

The latching display consists of latches and LED displays in the same mechanical assemly. The 36 outputs of the serial to parallel converter go to the latch inputs and the sync pulse to the latch clock. The latch outputs drive the appropriate LED's to produce the desired display.

4. Data Quality Analyzer, Block Diagram Description

4.1 Introduction

The Data Quality Analyzer (DQA) has the task of transforming various signals produced by the Decoder into error rates. Three types of errors, drop out, frame count, and frame count parity, are detected by the DQA, and one, beginning of frame, is detected by the decoder. Each time an error is detected, a front panel LED is pulsed on by the DQA. All errors

4.1 Continued:

are accumulated for a selectable time interval and displayed. Additionally, three signals, Frame, BOF, and EOF, useful for oscilloscope display, are produced and/or buffered by the DQA. A functional description of the DQA, based on the block diagrams of Figure 6 is given in the following paragraphs. It is divided into six major sections: Timing and Control Signal Generation, Drop Out Error Detection, Frame Count Error Detection, Accumulator Logic, Error Display, and Scope Signal Logic and Buffers.

4.2 Timing and Control Signal Generation

The central elements of the Timing and Control Generator are two counters, the Sync Interval Counter and the Frame Interval Counter. At the beginning of a frame, both counters are initialized by the BOF pulse, if one occurs. If there is no BOF pulse, the DQA creates an "assured BOF" pulse for synchronization purposes, derived from the decoder's BOF Window. After synchronization, the Sync Interval Counter counts up at the rate of one count per data bit since it is clocked by the Decoder's recovered 4 MHz clock. It is an eleven bit counter and thus overflows every 2048 bits or 512 μs, the same rate at which the sync words occur in the data stream. The carry from this counter clocks the six bit Frame Interval Counter. This counter is sufficiently long that it does not overflow during the frame. Thus, if all is working properly, it is possible to assign to each bit in the data stream a particular state of the combined Frame Interval-Sync Interval Counters. A number of these states are decoded by the Timing and Control Logic for use by various elements of the DQA.

4.3 Drop Out Error Detection

A particular pattern of eight bits, called a sync word, is inserted into the data stream every 512 μs, or 2048 bits, by the Format Unit. In a perfect recording, the data is fully recovered and this sync pattern is observed every 512 μs. However, in a real recording, temporary losses in playback amplitude, called drop outs, can occur. To the DQA/D, these can make the sync word spacing appear to be greater or less than 512 μs. It is the function of the Drop Out Error Detector to check the timing of the sync words based on timing signals from the Sync Interval Counter. Its outputs are detemined as follows. If the sync word is not found during a certain counter state, a drop out error is logged within the sync timing detector. If one or more drop outs are found within a frame, a drop out error is indicated at the output of the sync timing detector. If a sync word occurs anywhere within a 4 μs window defined by the Timing and Control Logic, the Sync Interval Counter is resynchronized with it. The resynchronization is a null operation when the sync word occurs at the correct counter state.

4.4 Frame Count Error Detector

The function of the Frame Count Error Detector is twofold. It checks the parity of the frame count and checks to see if the count increases by one, modulo 60, on successive frames. The parity check is straightforward. When the frame count is available on the data stream, it is loaded into a latch and presented to a 7 bit parallel even parity checker. If the parity is odd, the parity checker indicates a parity error. The frame count check is a bit more involved. The check consists of comparing the frame count of the present frame with that of the previous frame incremented by one,

4.4 Continued:

modulo sixty. Since the frame count cycles from zero to fifty-nine, i.e., counted up modulo sixty, threse two counts should be equal. If they are not, the comparator indicates a count error.

There are three outputs produced by the Frame Count Error Detector. Two of these, parity and count, are explained above. A third, termed "Frame Count" is simply the logical inclusive-OR of the other two.

4.5 Accumulator Logic

The basic function of the accumulator logic is to count three classes of errors, Beginning of Frame (sec. 31.), Frame Count (sec. 4.3), and Drop Out (sec. 4.2). There are a few possible variations in the counting, and these are discribed in the following.

First, the counting interval has three possible values, 1 second, 10 seconds, and 60 seconds. These intervals are derived, by a countdown and logic, from a 60 Hz Reference Signal. The Integration Period switch on the front panel selects the desired interval. Second, the accumulators and 60 Hz countdown may be cleared, starting a new counting interval, in one of two ways. The first is by pressing the reset switch located on the front panel; the second is by changing the integration period.

4.6 Error Display

The Error Display can be subdivided into two major subsections, the instantaneous error display and the cumulative error display. The functions of each are obvious by their nomenclature, and their implementation is described below.

4.6 Continued:

The instantaneous display consists of four light emitting diodes (LED's) and associated drivers. There is one LED for each of the following types of errors: Beginning of Frame (sec. 31.), Drop Out (sec. 4.2), Count and Parity (sec. 41.3). Each LED has a driver which is enabled by the appropriate error and pulsed by a signal from the Timing and Control Logic. This results in an 8 msec pulse of light for each detected error. For three of the drivers, the 8 msec pulse can be easily obtained directly from the Timing Generator. However, the logic requires a pulse stretcher in the Drop Out driver to obtain an 8 msec pulse.

The cumulative display consists of numeric displays, associated latches and control logic. There is one latch and display for each of the three error counters in the accumulator logic. The control logic includes a latch-pulse generator which produces a pulse to latch data from the accumulators at the appropriate time. Blanking logic is also included in the control logic. It blanks all three displays during certain time intervals. These intervals include the time from when the reset button is released to when new data is present in the display latches, the time from when the integration period is changed to when new data is present in the display latches, and a short interval every time the display latches are updated.

4.7 Scope Signal Logic and Buffers

It is the function of the Scope Signal Logic to create Frame and End of Frame signals. Both the data and various signals from the Timing and Control Generator are inputs required by the logic. The Frame and End of Frame (EOF) signals, along with the Beginning of Frame (BOF), are buffered and available on the front panel for scope display.

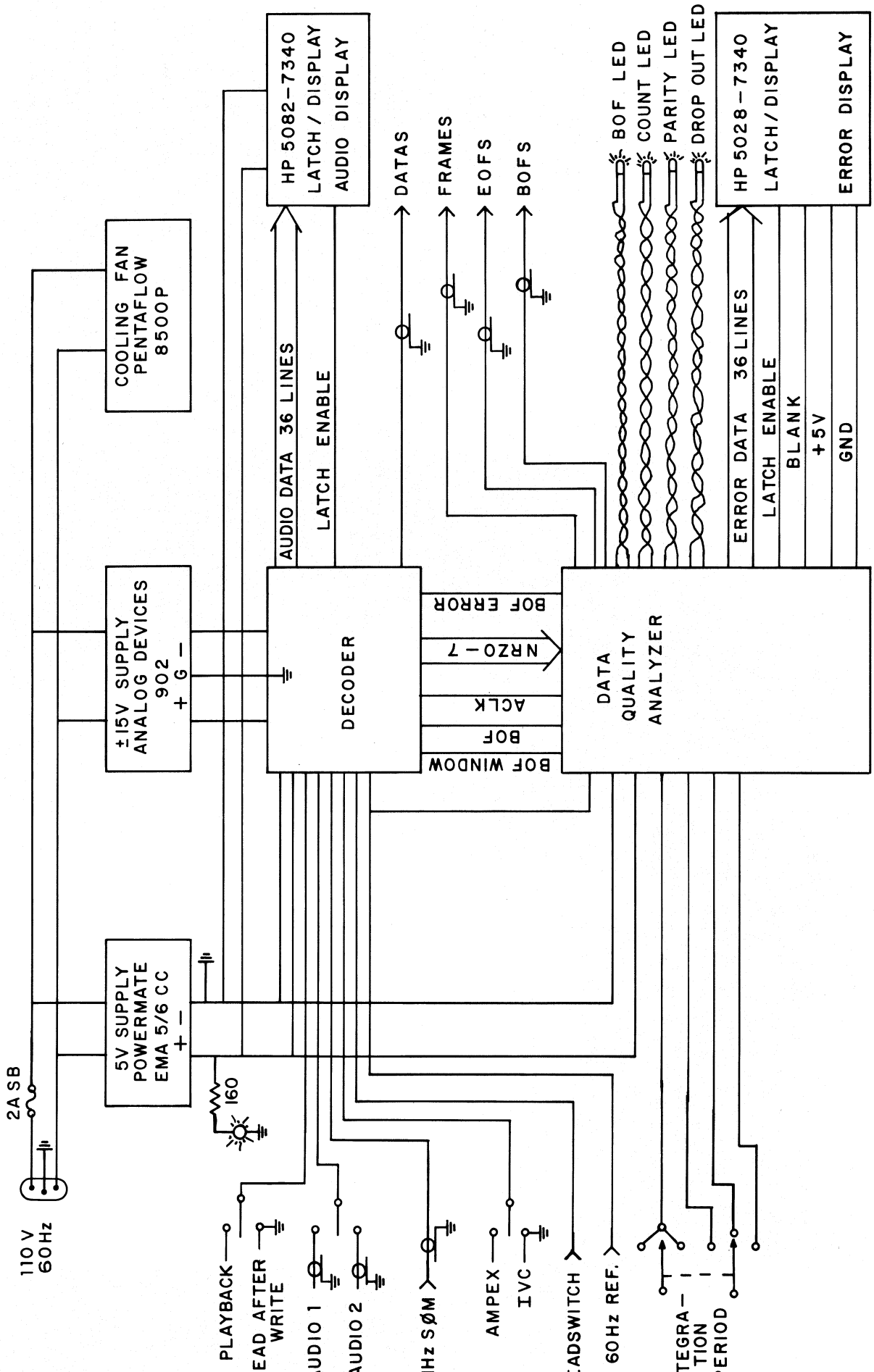
5. Circuit Schematics

5.1 Interconnection Diagram

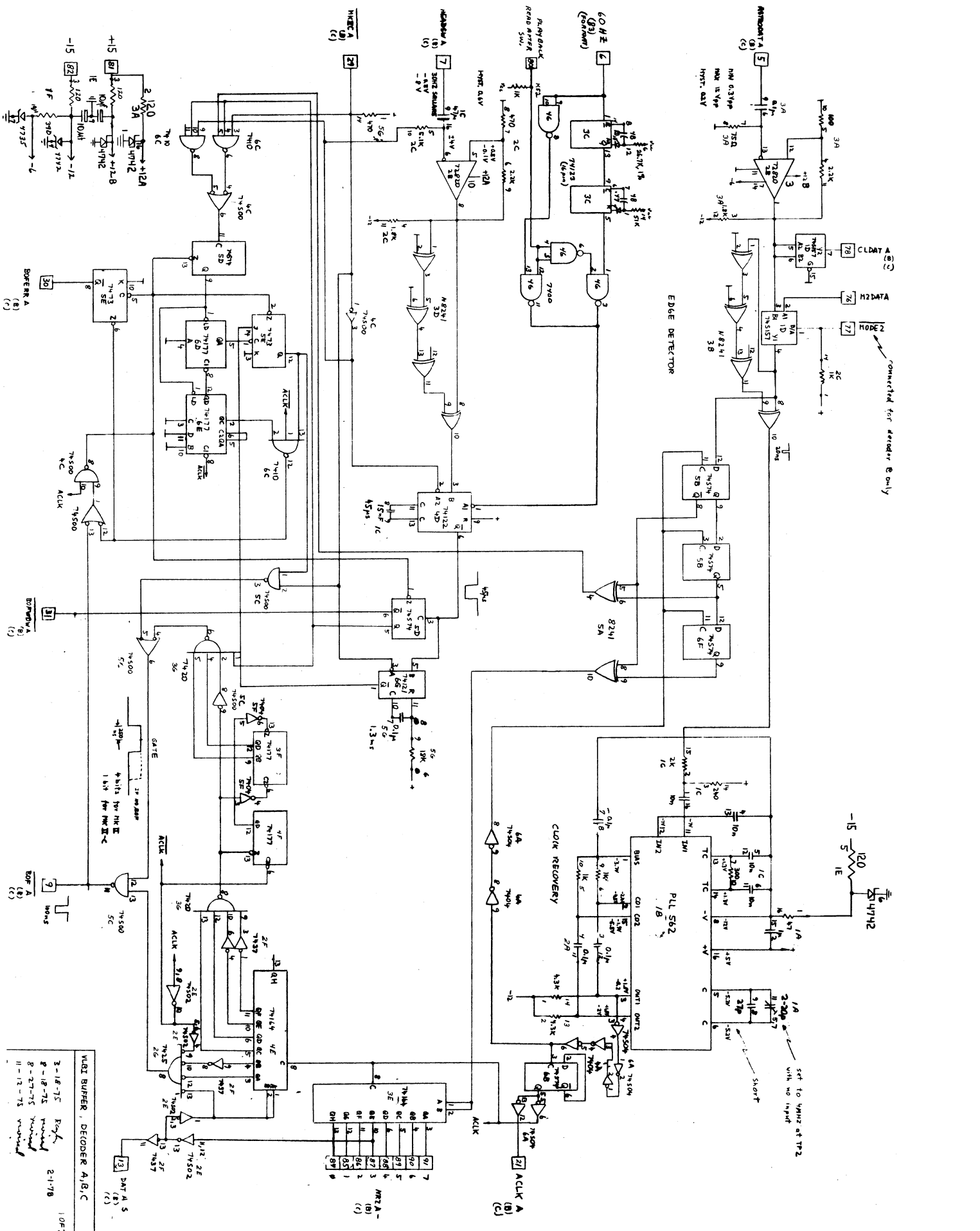
5.2 Astrodata Decoder

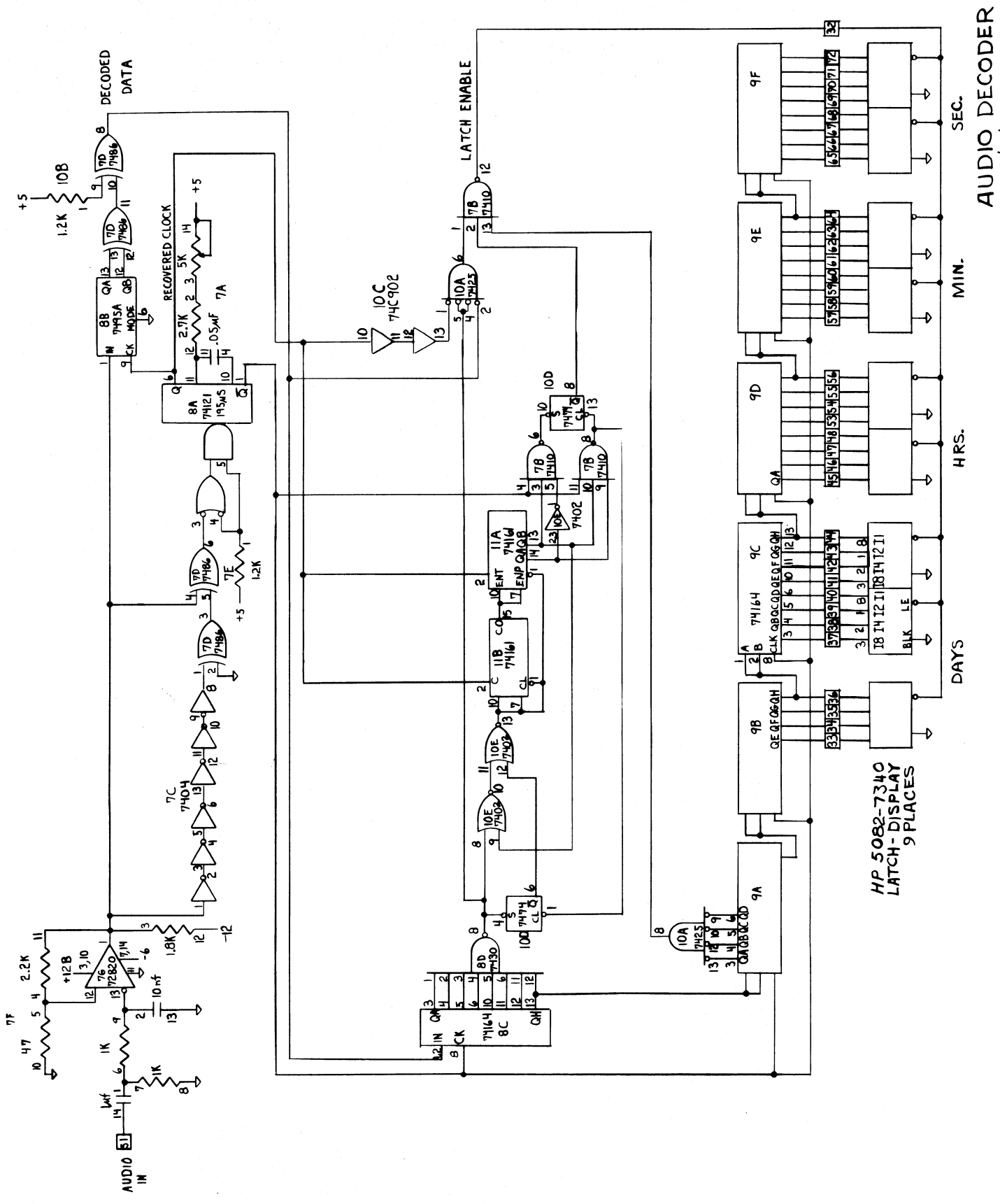
5.3 Audio Decoder

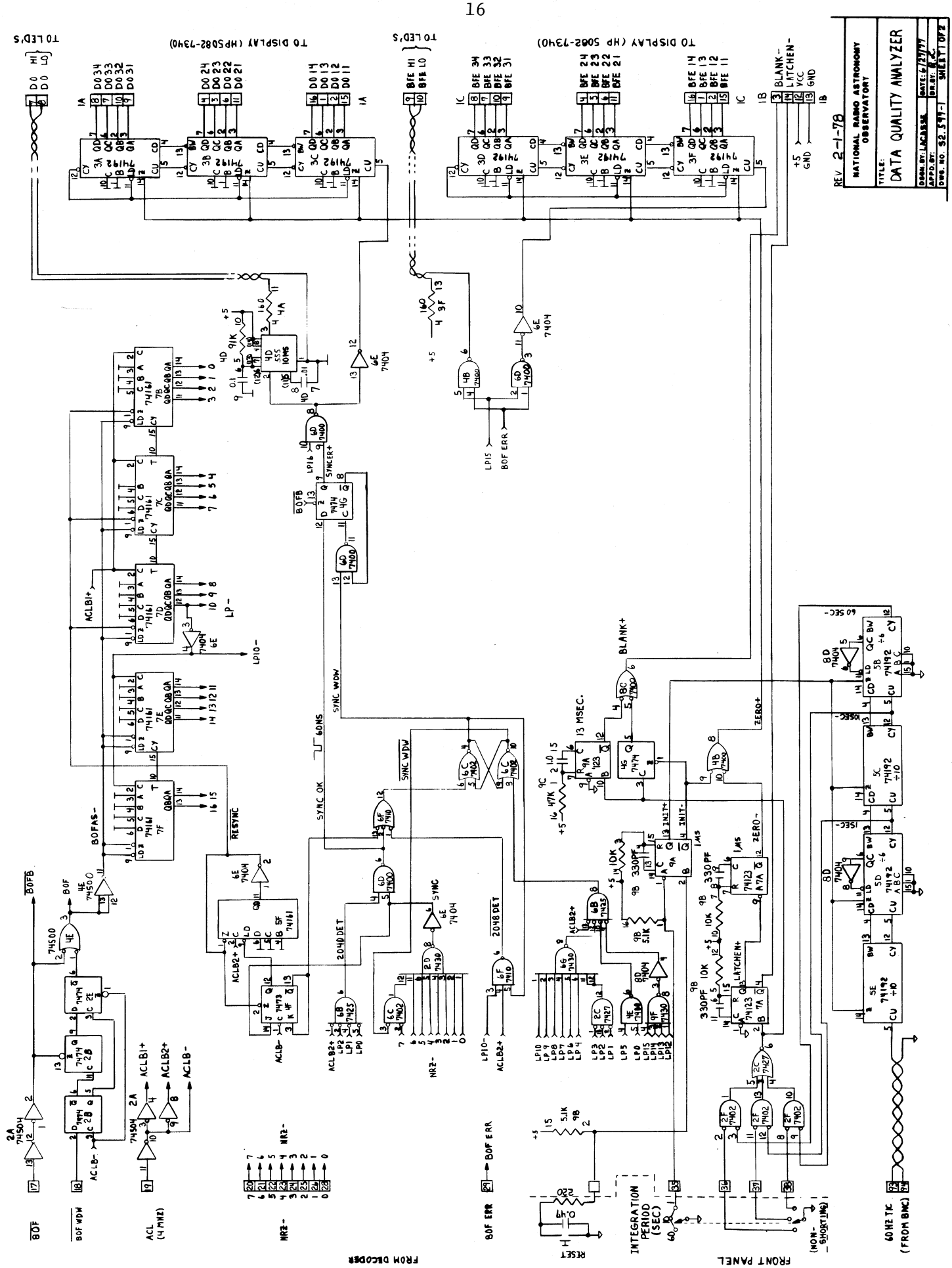
5.4 Data Quality Analyzer

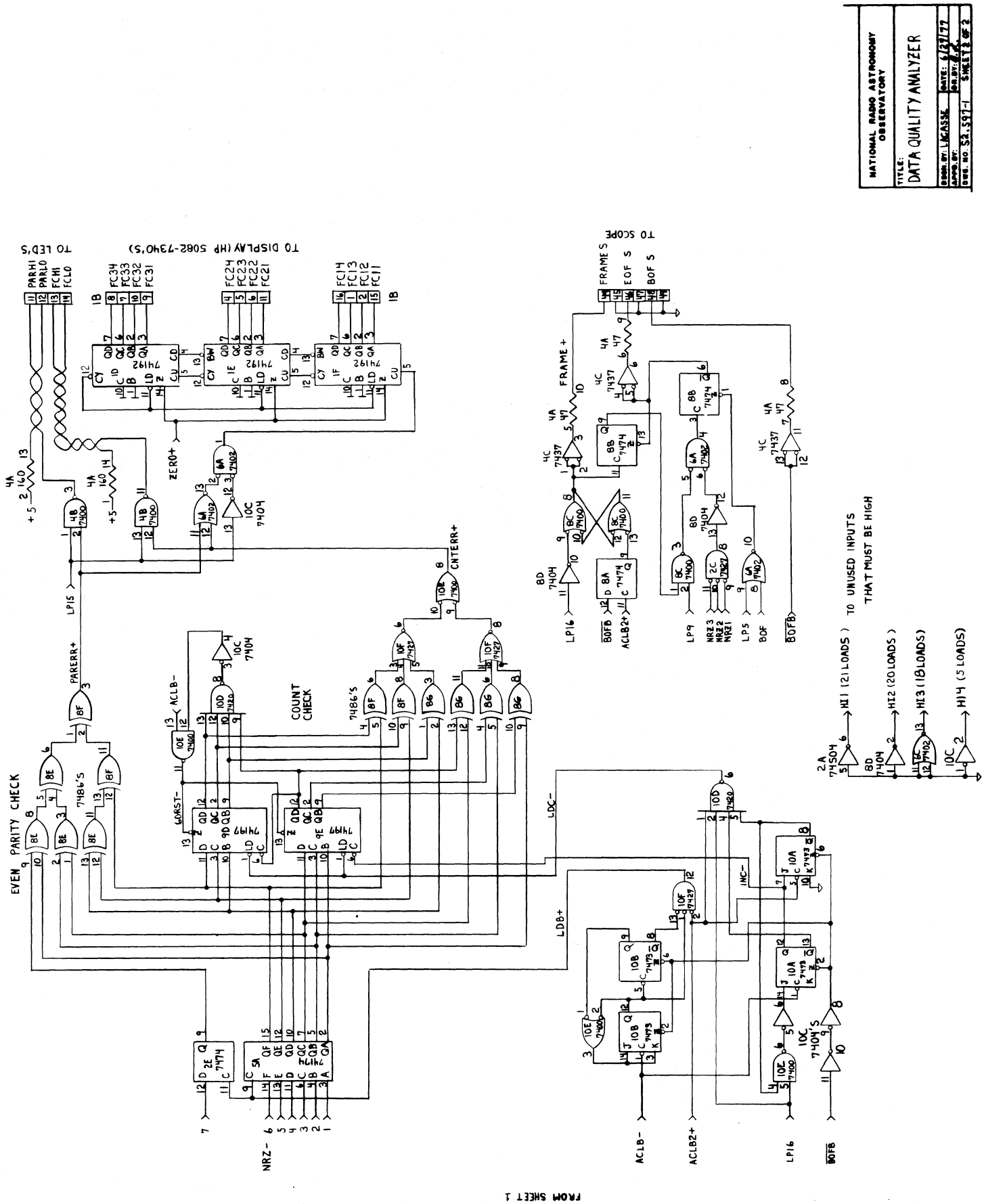


SCHEMATIC 5.1 DATA QUALITY ANALYZER/DECODER, INTERCONNECTION DIAGRAM


EDGE DETECTOR
CLOCK RECOVERY
PLL 562
VLBI BUFFER, DECODER A,B,C
1 OF 2
connected for decoder B only
set to 4MHz at TP2 with no input
short


AUDIO DECODER
1/4/78
DECODED DATA
LATCH ENABLE
RECOVERED CLOCK
AUDIO IN
SEC.
MIN.
HRS.
DAYS
HP 5082-7340
LATCH-DISPLAY
9 PLACES


TO DISPLAY (HP 5082-7340)
TO LED'S
DATA QUALITY ANALYZER
NATIONAL RADIO ASTRONOMY OBSERVATORY
REV 2-1-78
BOF
BOF WDW
ACL (4 MHz)
MR2-
BOF ERR
RESET
INTEGRATION PERIOD (SEC)
60 HZ TIC (FROM BNC)
FROM DECODER
FRONT PANEL
(NON-SHORTING)
SYNC WDW
SYNC OK
RESYNC
2048 DET
BLANK+
ZERO+
ZERO-
INIT+
INIT-
LATCHEN+
BOFAS-
LP-
LP10-
LP15
BOF ERR


NATIONAL RADIO ASTRONOMY OBSERVATORY
TITLE: DATA QUALITY ANALYZER
DRAWN BY: L. KASSE
DATE: 6/29/77
APPD. BY:
DWG. NO. 54.597-1
SHEET 1 OF 2
TO LED'S
TO DISPLAY (HP 5082-7340'S)
TO SCOPE
EVEN PARITY CHECK
COUNT CHECK
TO UNUSED INPUTS THAT MUST BE HIGH
FROM SHEET 1
PARHI
PARLO
FCHI
FCLO
FC34
FC33
FC32
FC31
FC24
FC23
FC22
FC21
FC14
FC13
FC12
FC11
FRAME S
EOF S
BOF S
FRAME+
ZERO+
LPIS
PARERR+
CNTERR+
ACLB-
CORST-
LDC-
LDB+
INC-
ACLB2+
LP16
BOFB
LP9
LP5
BOF
NRZ3
NRZ2
NRZ1
NRZ-
HI1 (21 LOADS)
HI2 (20 LOADS)
HI3 (18 LOADS)
HI4 (5 LOADS)

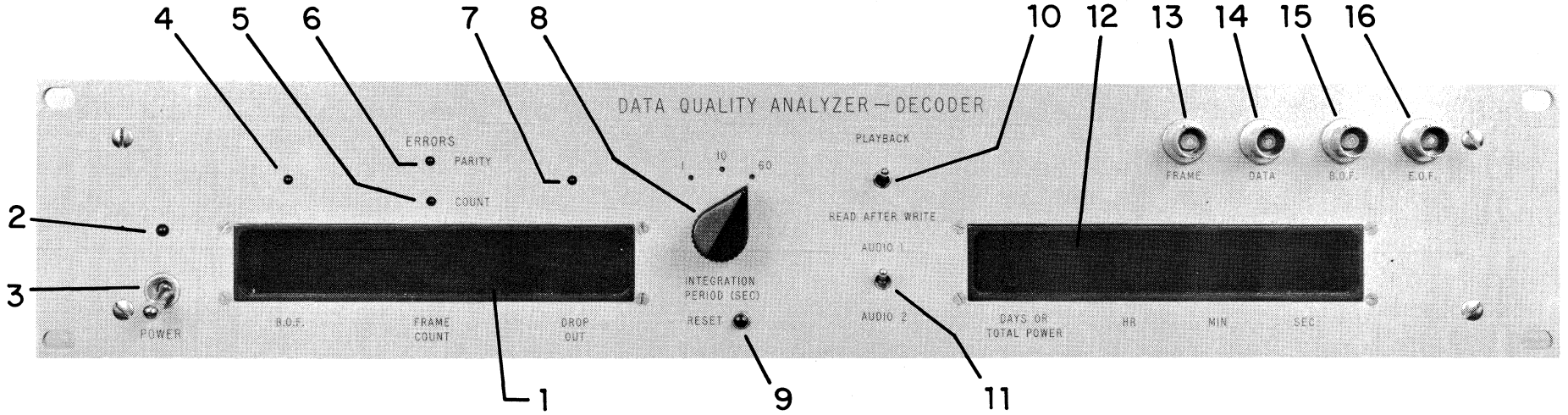
6. Acknowledgements

Credit should be given to Benno Rayhrer for most of the original decoder design, part of the data quality analyzer design, and the documentation in Appendix A.

Bill Vrable, Larry Miller and Winston Cottrell must be credited with transforming my schematics and wire lists into a working unit.

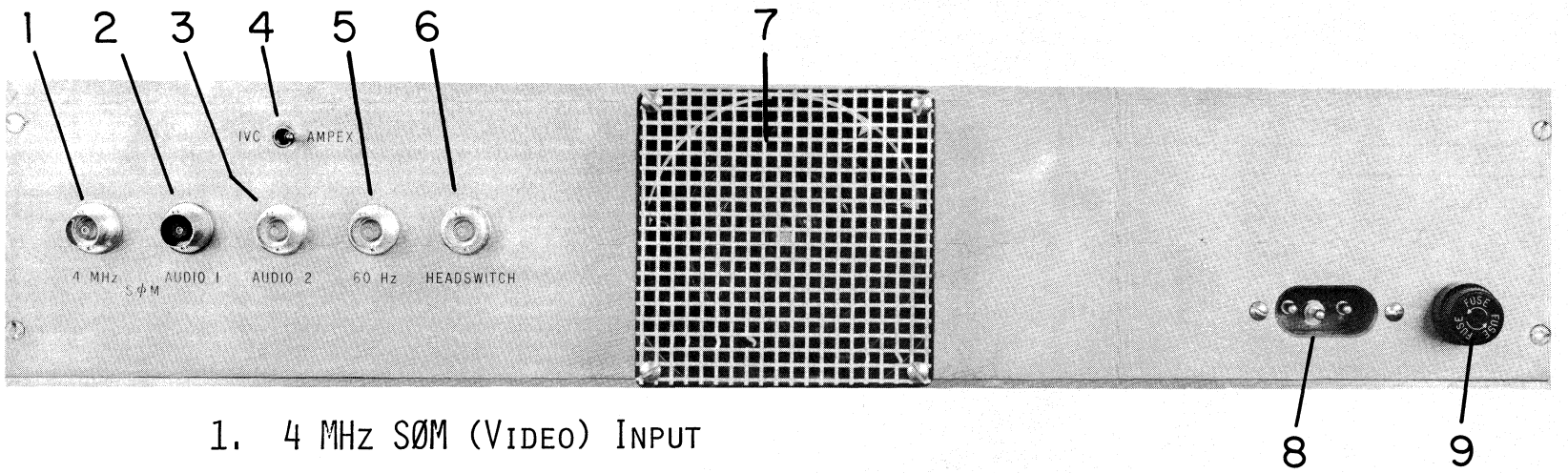
Thanks also go to a number of observers for a variety of constructive comments.

FIGURES



1. Error Display
2. Power Indicator LED
3. Power Switch
4. BOF Error LED
5. COUNT Error LED
6. PARITY Error LED
7. DROP OUT Error LED
8. Integration Period Selector Switch
9. Integration Period Reset Switch
10. Read-After-Write/Playback Switch
11. Audio 1/Audio 2 Selector Switch
12. Audio Display
13. FRAME Signal Output
14. DATA Signal Output
15. BOF Signal Output
16. EOF Signal Output

FIGURE 1. DATA QUALITY ANALYZER/DECODER (FRONT VIEW)



1. 4 MHz SØM (Video) Input
2. Audio 1 SØM Input
3. Audio 2 SØM Input
4. IVC/AMPEX Selector Switch
5. 60 Hz Reference Input (TTL)
6. HEADSWITCH Input
7. Cooling Fan
8. 60 Hz, 110 V rms Input
9. Fuse, 2A, Slo Blow

FIGURE 2. DATA QUALITY ANALYZER/DECODER (REAR VIEW).

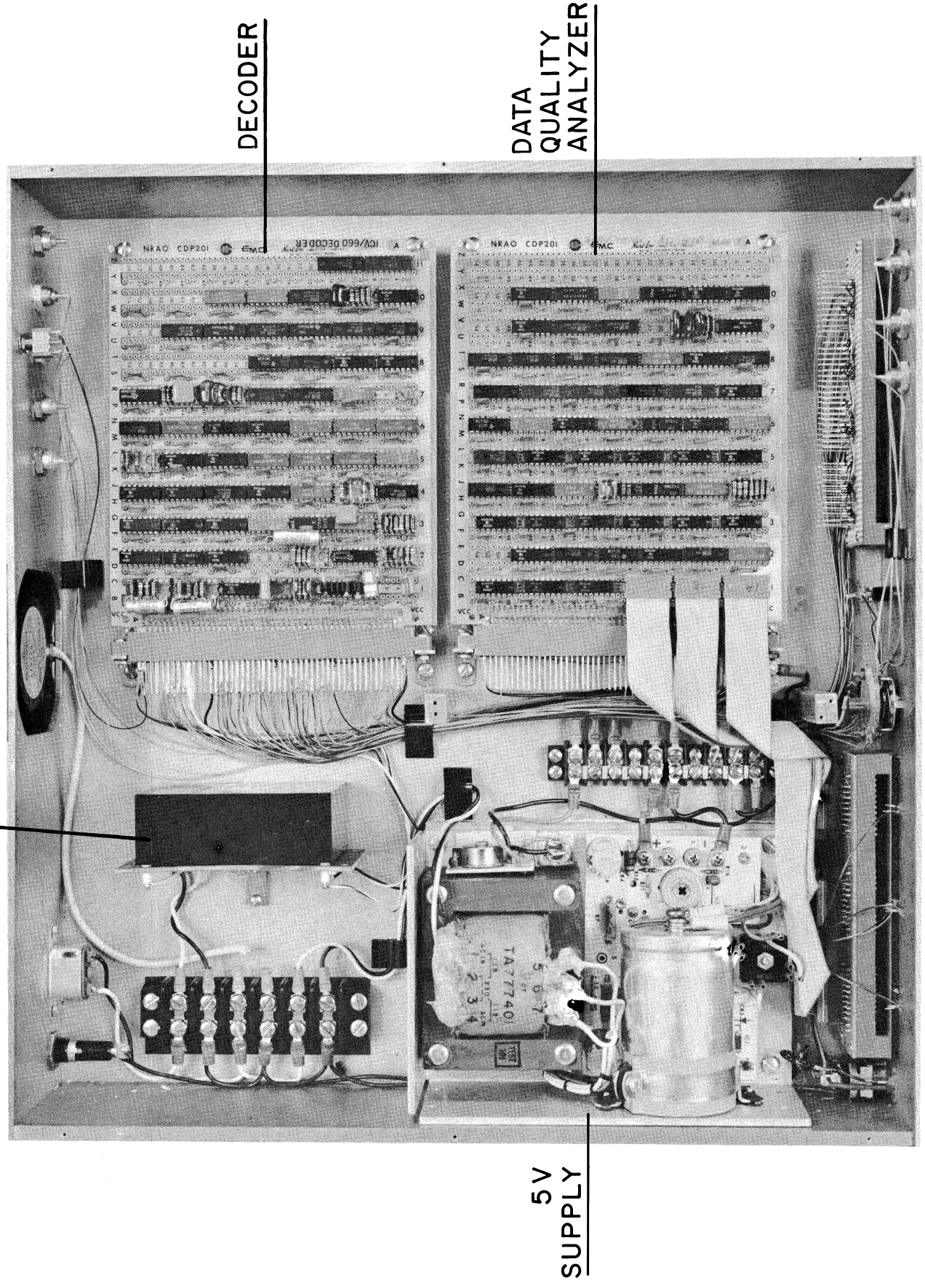


FIG. 3 DATA QUALITY ANALYZER/DECODER (Top View With Cover Removed)

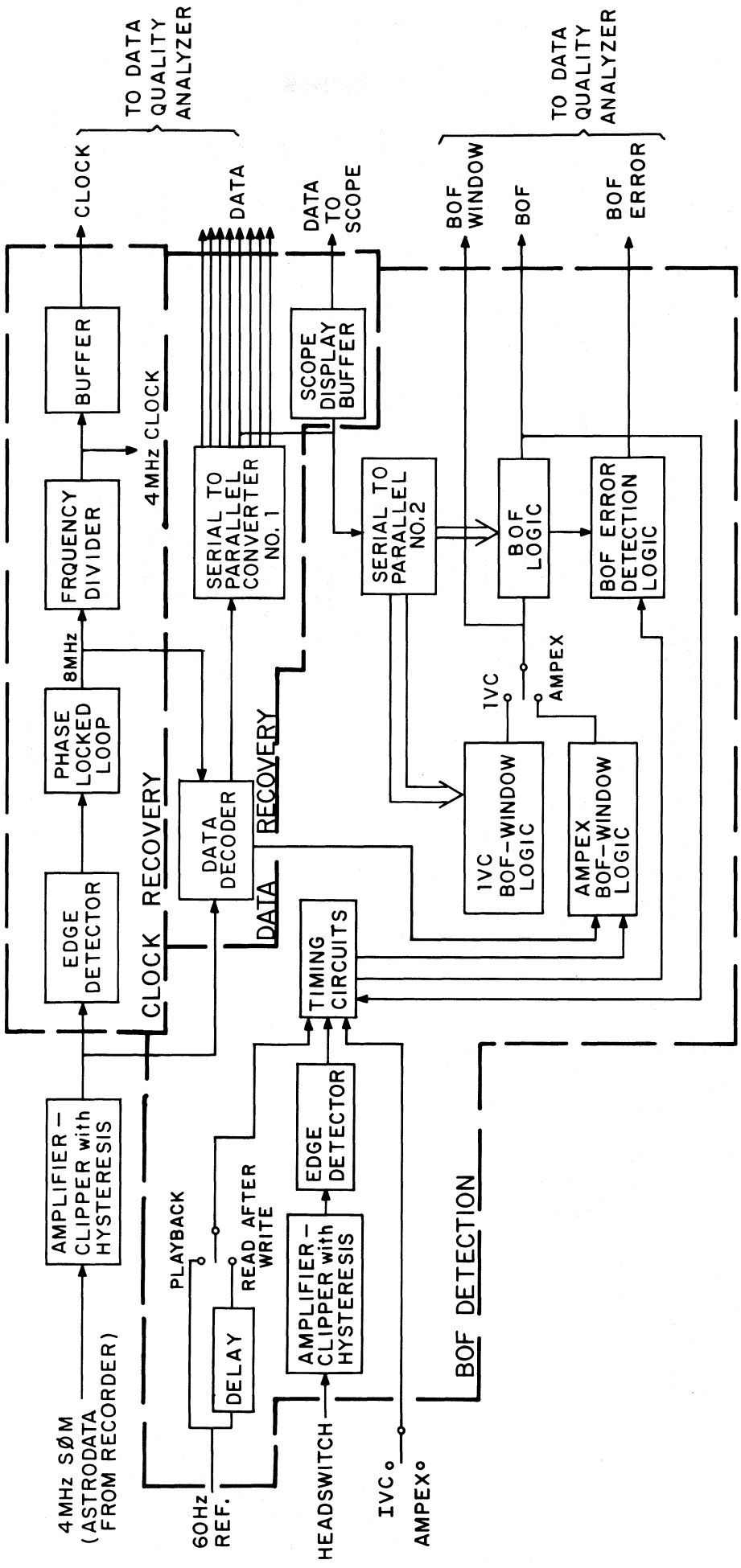


FIG. 4 VIDEO DECODER, BLOCK DIAGRAM

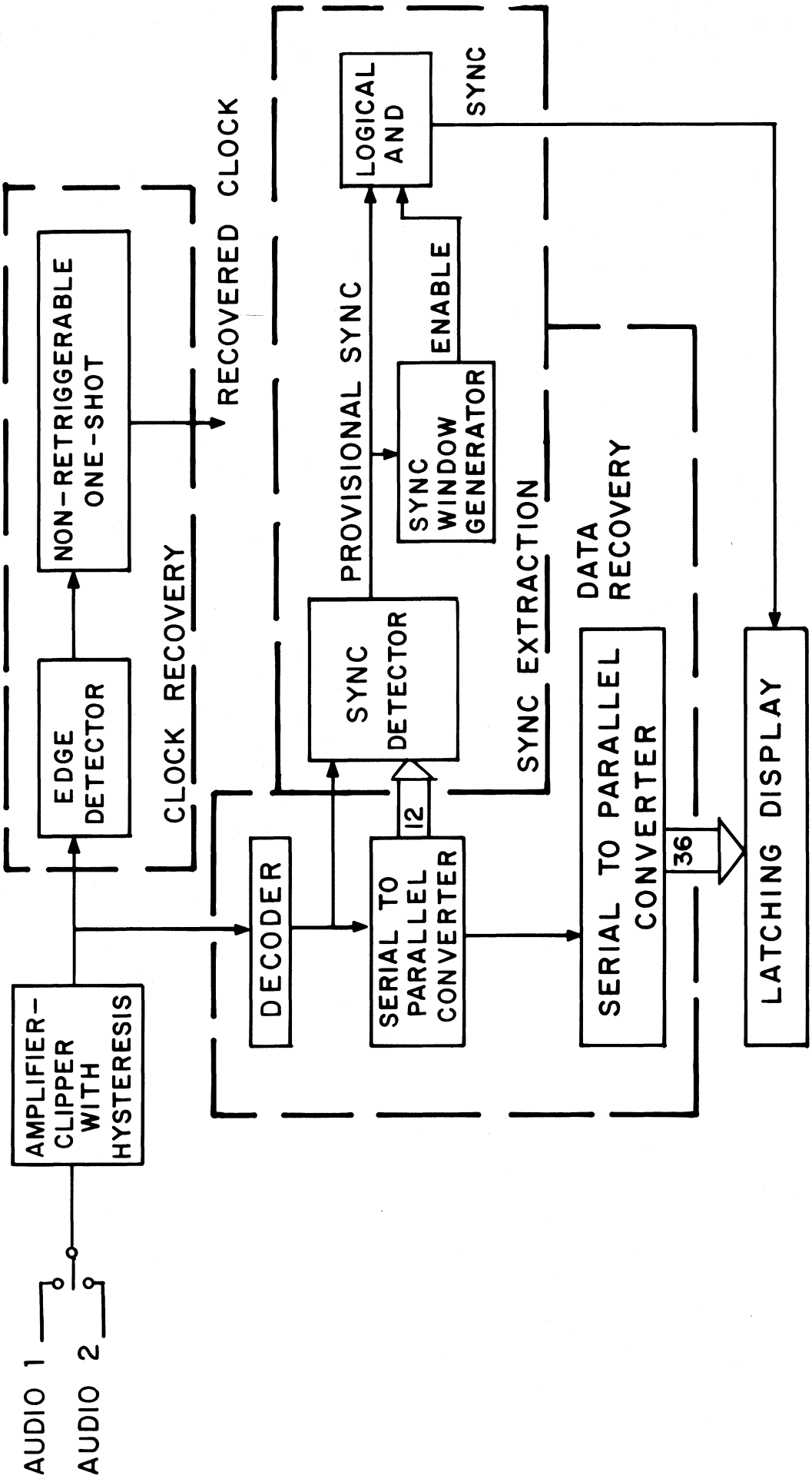


FIG. 5 AUDIO DECODER, BLOCK DIAGRAM

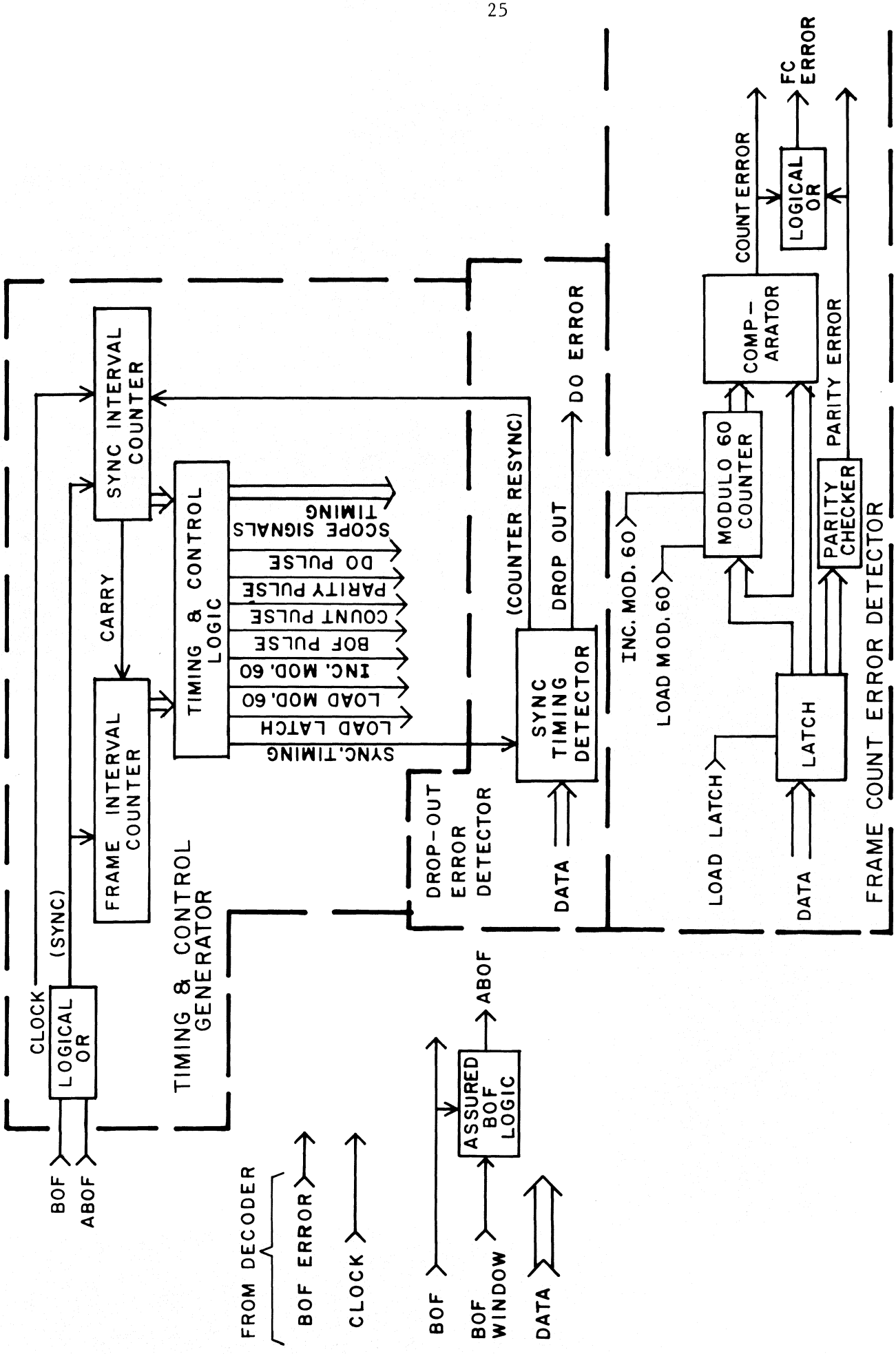


FIG. 6a DATA QUALITY ANALYZER BLOCK DIAGRAM, TIMING AND ERROR DETECTION LOGIC.

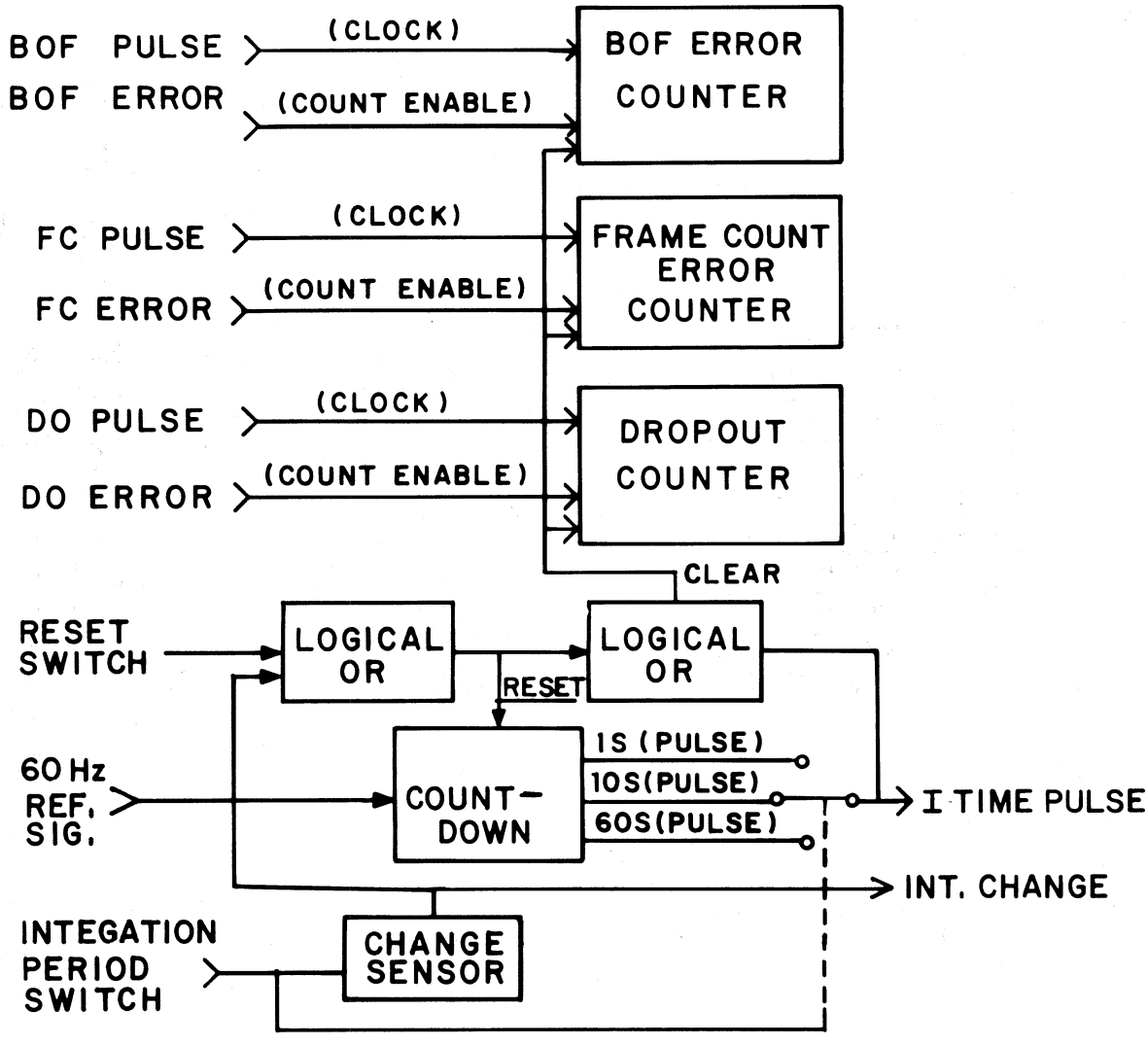


FIG. 6b DATA QUALITY ANALYZER BLOCK DIAGRAM, ACCUMULATOR LOGIC.

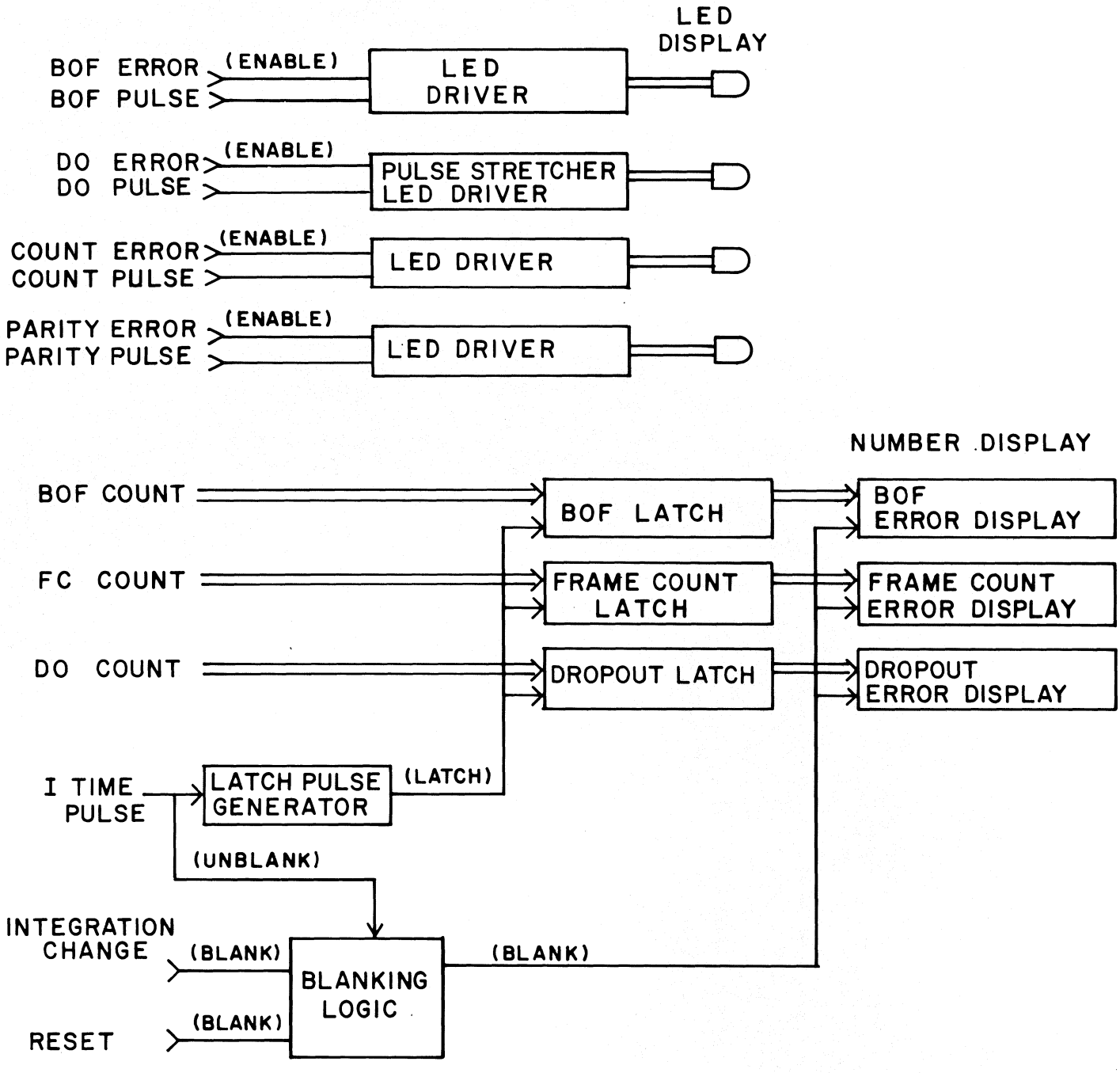


FIG. 6c DATA QUALITY ANALYZER BLOCKDIAGRAM, ERROR DISPLAY

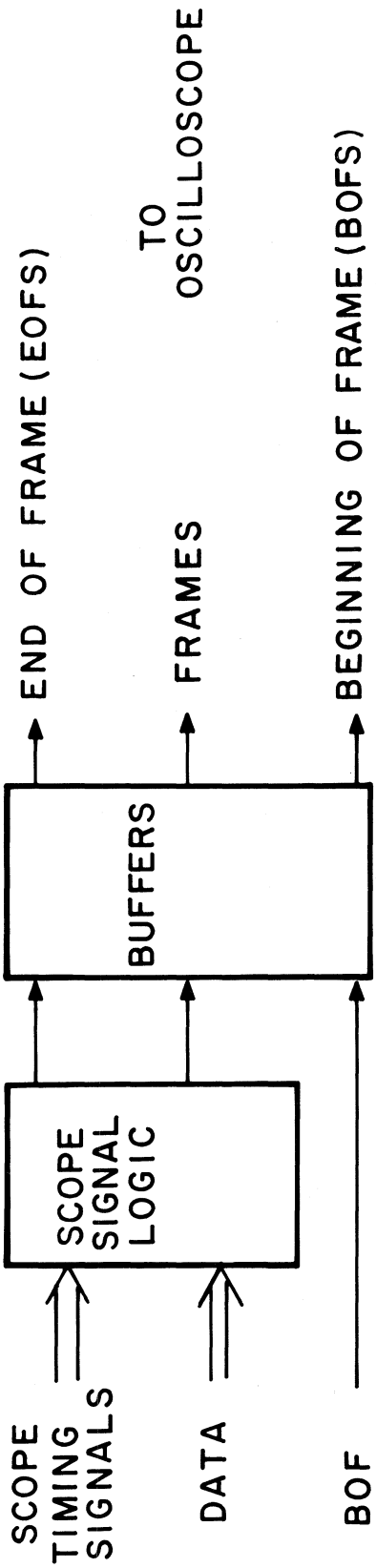


FIG. 6d DATA QUALITY ANALYZER, BLOCK DIAGRAM SCOPE SIGNAL LOGIC, & BUFFERS

APPENDIX A

MARK II FORMAT SPECIFICATIONS

This appendix includes the format specifications of the astrodata (or video) data stream and both audio data streams for Mark II and Mark IIC.

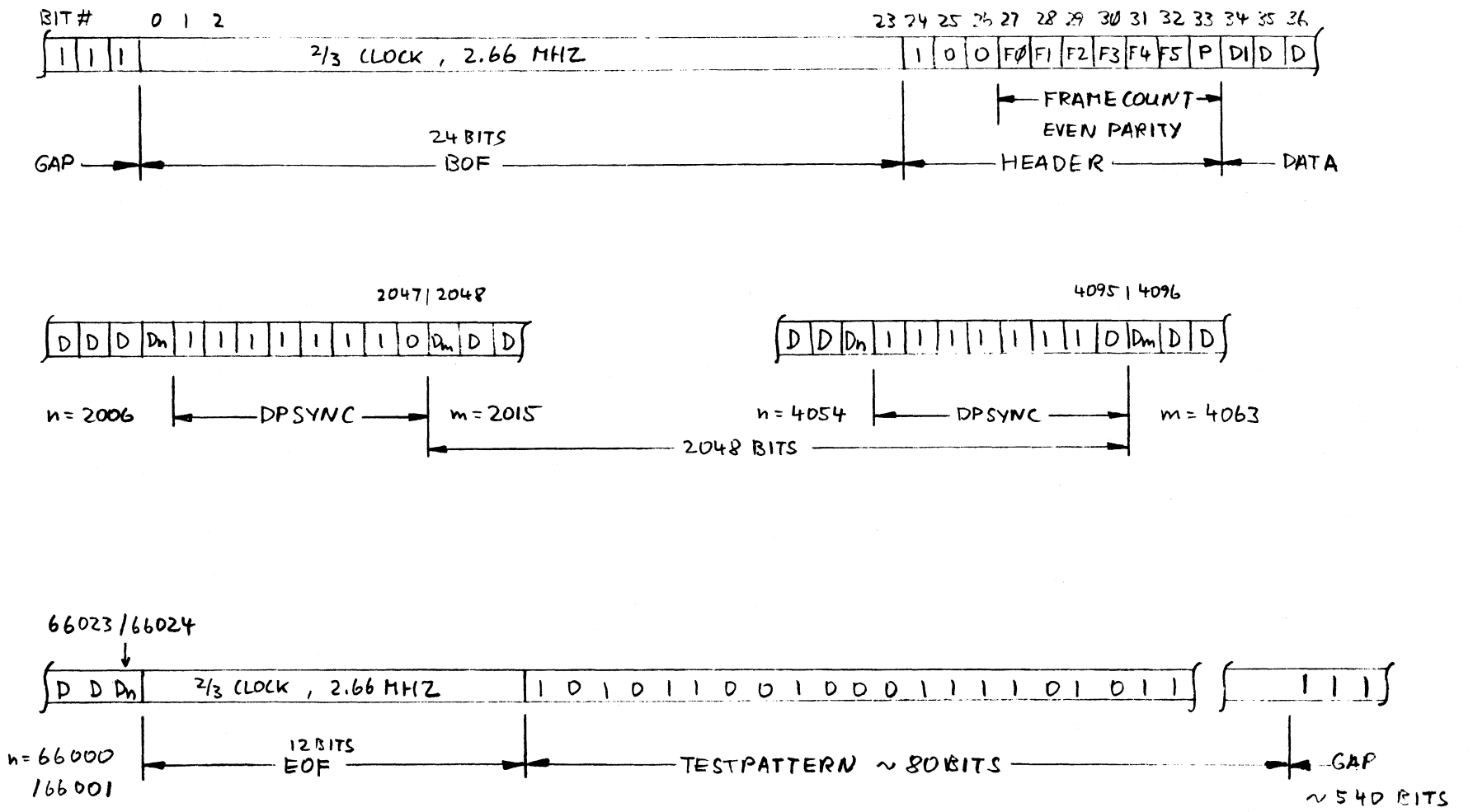


Figure A-1: Mark II Video Format

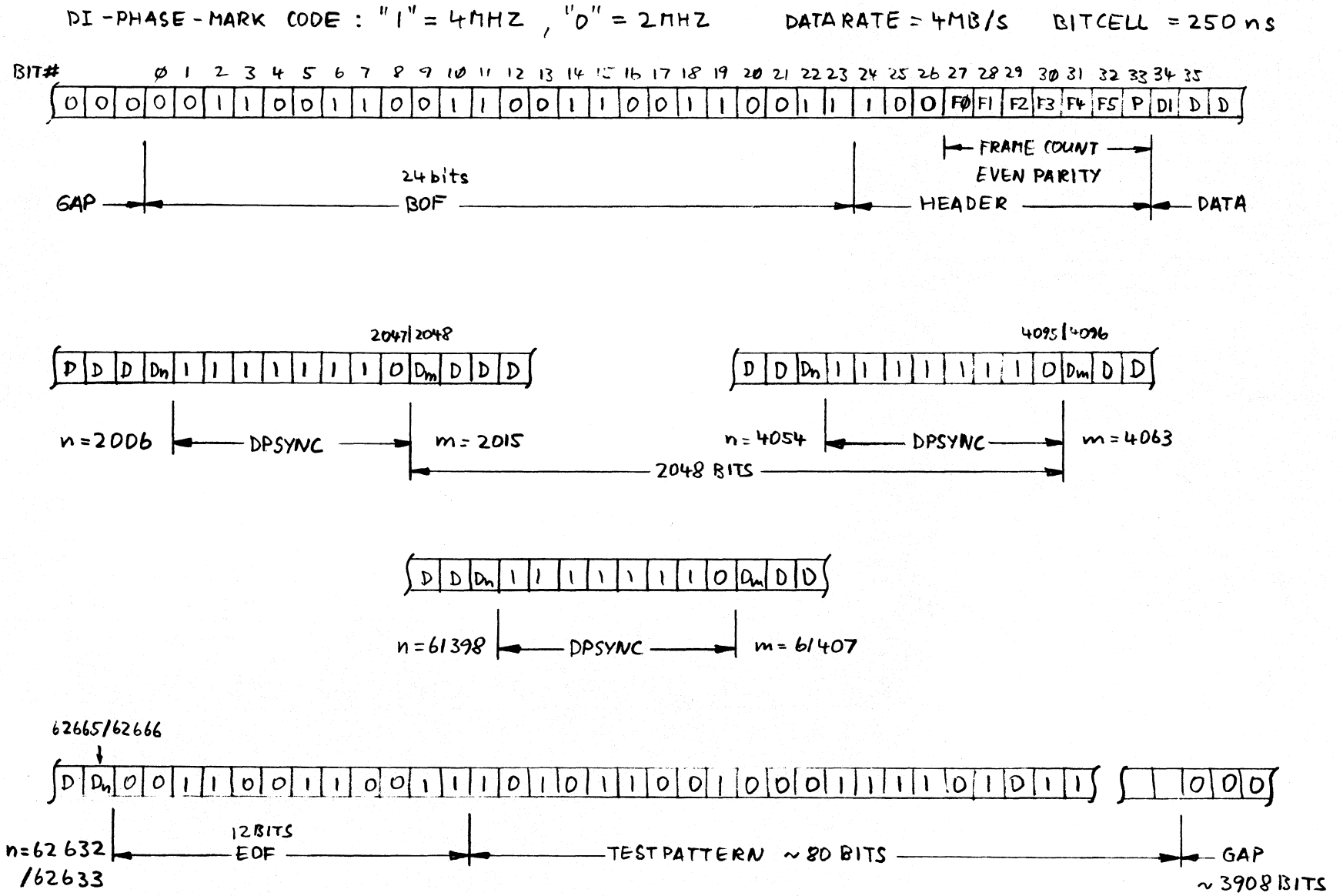


Figure A-2: Mark IIC Video Format

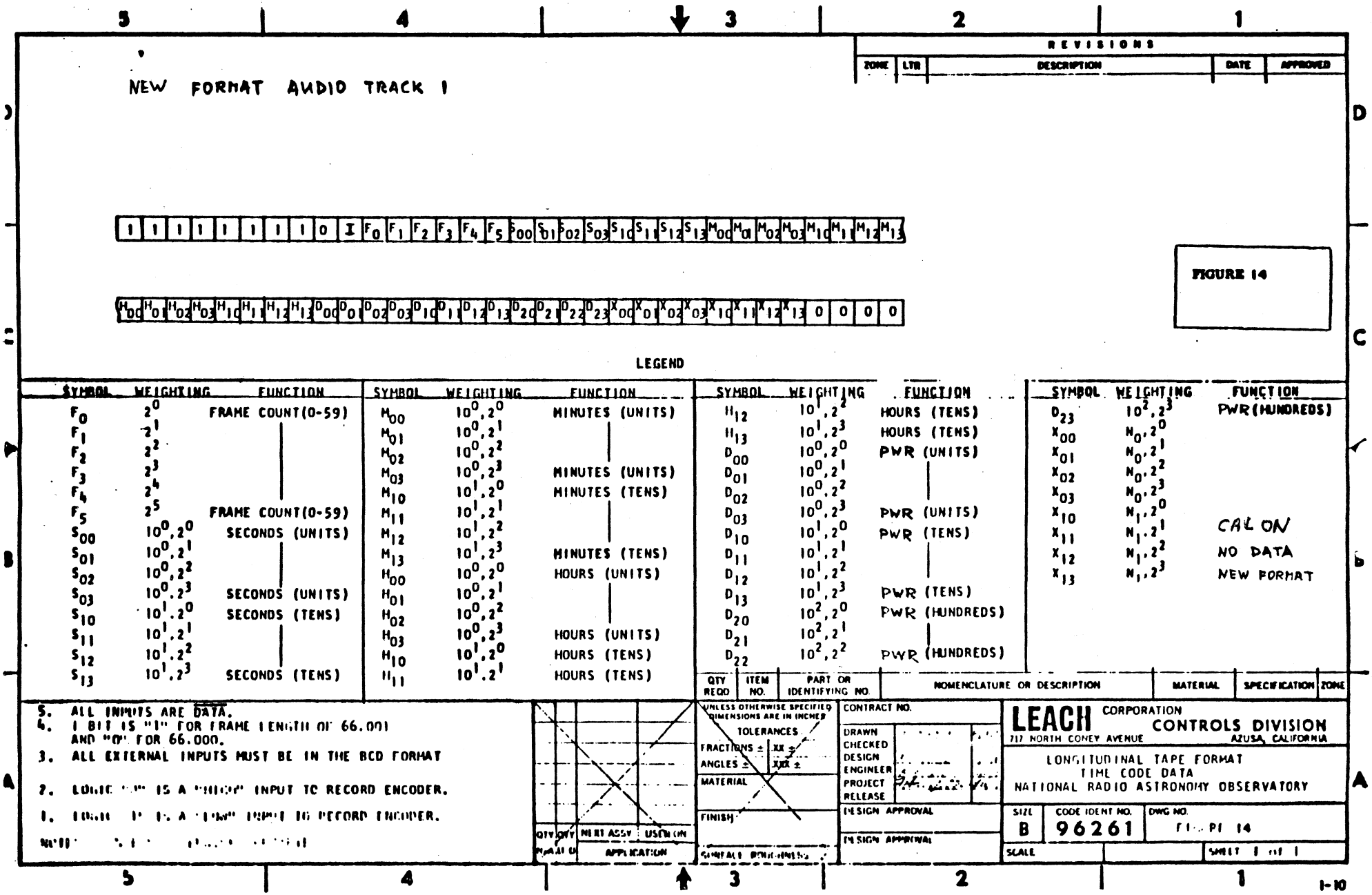


Figure A-3: Audio Track 1

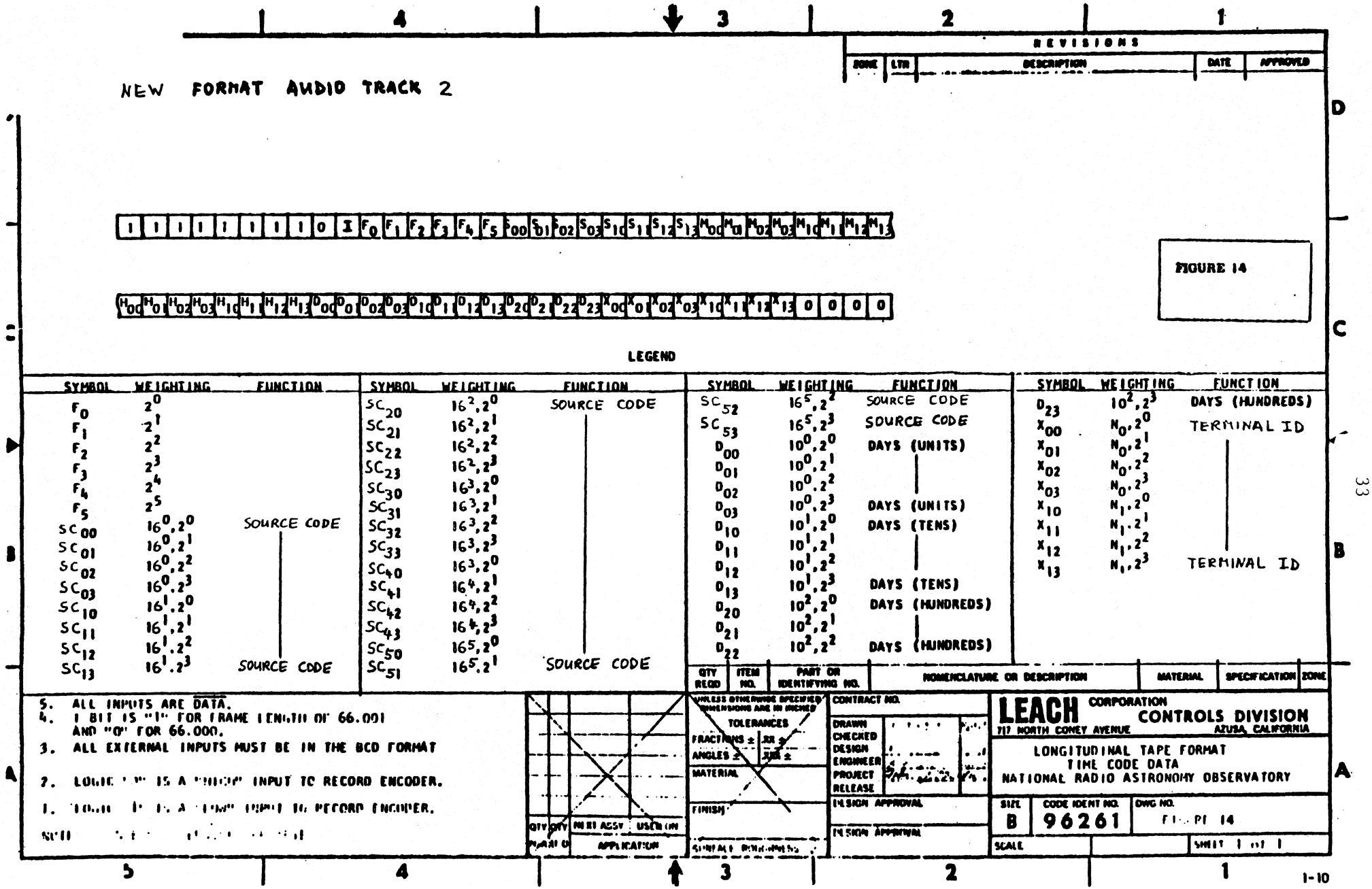


Figure A-4: Audio Track 2

APPENDIX B

INTERFACE AND SET-UP DETAILS

This appendix includes details on how to introduce the DQA/D into a Mark II or Mark IIC recording terminal. A few common problems in getting the unit to work, along with remedies for the problem, are presented as well.

SET-UP INSTRUCTIONS (IVC)

1. Plug the unit in to a 110 V RMS, 60 Hz receptable and turn on the "POWER" switch. The LED directly above the switch should light.

2. Connect the following signals to the rear panel.

   a) "DATA" or "VIDEO COLOR" from recorder to 4 MHz SØM.

   b) Audio 1 output from recorder to Audio 1.

   c) Audio 2 output from recorder to Audio 2.

   d) Recorder reference frequency ("teed-off" at a convenient point). to 60 Hz.

   e) Leave the Headswitch input open.

3. The IVC/AMPEX switch on the rear panel should be in the IVC position.

4. The following signals are available on the front panel:

   a) FRAME: High during the frame, and low for part of the record gap.

   b) DATA: Decoded video data.

   c) B.O.F.: High when a "beginning-of-frame" is detected.

   d) E.O.F.: In IVC format this pulse occurs in the record gap.

5. Front panel displays: The display on the right displays Audio 1 or Audio 2 track data. The display on the left displays error rates in the recorded data. The LED's above the display are pulsed ON to indicate that an error has been added to the appropriate error counter.

6. Front panel switch positions:

   a) POWER: Connects AC power when in the UP position.

   b) INTEGRATION PERIOD: Indicates the length of the time during which errors are accumulated.

   c) RESET: When pushed and released, this switch zeroes the error counters and begins a new error accumulation period. (See note 1.)

   d) PLAYBACK/READ-AFTER-WRITE: Should be in

      PLAYBACK DURING PLAYBACK and

      READ AFTER WRITE DURING RECORD.

      (See note 2.)

6. Continued:

   e) Audio 1/Audio 2: Displays the appropriate audio track data on the audio track display. (See note 3.)

7. If, after setting-up as described above and allowing a 15 minute warm-up period, a stable beginning of frame pulse and data stream (with test-pattern on) are not obtained during playback, then the free-running frequency of the decoder phase locked loop must be adjusted. Follow this procedure:*

   a) Remove the right half of cover on decoder unit to expose two wire-wrap cards.

   b) Remove the 4 MHz SØM input.

   c) Monitor the frequency at output pin 21 of the decoder card (the one towards the rear). Adjust the variable capacitor in row 1 of the decoder card to obtain a frequency of 4.00 MHz ± .01 MHz.

8. If the decoder works well in playback but not in read-after-write, procedure A or B below should remedy the situation.

   A- Optimize the drive on the recorder.

   B- (1) Trigger an oscilloscope from the 60 Hz reference signal.

      (2) Monitor the recorder's "TP3" on one channel and the BOF window (pin 5 of 74S74 in 5D) on the other.

      (3) Place the DQA/D in Read-After-Write mode and record a test pattern.

      (4) Replace the 26.7 K resistor in location 4(b) with a resistor that will center the BOF window pulse on the location of the beginning of frame code. (The location of this code can be observed in playback mode.)

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* First, double check the set-up!

NOTE 1: It is particularly useful to set the integration period to 60 sec, and release the reset switch at xx min 00 sec. This makes it easy to know when the display has been updated.

NOTE 2: There is no E-E signal while recorder is in standby. The recorder must be in either record or playback mode for data to be decoded. Some recorders require the data input ("VLB IN") to be removed during playback.

NOTE 3: While Audio 1 is available in standby mode, Audio 2 is not.

SET-UP INSTRUCTIONS (AMPEX)

1. Plug the unit into a 110 V RMS, 60 Hz receptacle and turn on the power switch.

2. Connect the following signals to the rear panel:

   a) "DATA OUT" from the recorder to 4 MHz SØM.

   b) Audio 1 output from the recorder to Audio 1.

   c) Audio 2 output from the recorder to Audio 2.

   d) Recorder reference frequency ("teed-off" at a convenient point) to 60 Hz.

   e) Headswitch output from the recorder to Headswitch.

3. The IVC/AMPEX switch on the rear panel should be in the AMPEX position. The Playback/Read-After-Write switch has no effect in the Ampex mode.

4. Follow steps 4 through 7 in the IVC Set-Up Procedure with the following exception: Ignord step 6d.

Additional Comments

1. It is possible to eliminate all the components used to generate ± 12 V in the decoder by using a ± 12 V supply.

2. The phase-locked loop trim capacitor should have a multiturn adjustment for convenience's sake.

3. The phase locked loop may be temperature compensated by using a temperature compensating capacitor for the 27 pF frequency determining capacitor. First the temperature coefficient of the PLL must be measured, using a temperature stable 27 pF capacitor.