NATIONAL RADIO ASTRONOMY OBSERVATORY

GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT No. 178

AN IMPULSE NOISE SUPPRESSOR
FOR CONTINUUM RADIOMETRY

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I. Introduction

This report describes a noise blanker which has been developed to alleviate

some of the problems caused by impulse-type interference, such as that generated

by automotive ignition systems and power lines. The blanking system removes all

signal elements containing components in excess of a certain threshold voltage.

The signal is then adjusted to compensate for removed elements by inserting an

average of "nearby" signal elements in place of each blanked element. The input

to the blanker is taken from a fast response detector, converted to digital form

for processing, then returned to analog form. (See Figure 1.)

II. Principle of Operation (Interference Not Present)

The input is fed through a two stage operational amplifier and into a

voltage-controlled-oscillator (VCO). The first op-amp stage has unity gain

and serves only to control the time constant of the circuit. The second stage

provides the required gain to drive the VCO so that the overall system will

have a gain of two. The VCO provides a TTL pulse train output, whose frequency

is proportional to the input voltage. The analog-to-digital conversion is per-

formed in this manner.

The TTL pulse train is then fed to a counter, which is cleared every 100

μsec. Before each clear pulse, the count is clocked into an accumulator, where

it is summed with previous counts. This 100 μsec period over which the counter

counts is known as the sample period and can be changed at the front panel.

If interference is detected further processing is necessary which will be

described separately. At the end of the sixteenth 100 μsec period (i.e., every

1.6 msec), the total in the accumulator is fed to a digital-to-analog (D/A)

converter which produces a voltage output proportional to that value. The accumulator and counter are then cleared and the 1.6 msec cycle repeats. The resulting output from the D/A converter is a stairstep replica of the input waveform having twice the amplitude of the original signal and a step width of 1.6 msec.*

III. Principle of Operation (Interference Present)

The input signal is AC coupled to a separate two-stage operational amplifier followed by a Schmitt trigger and a D-type flipflop. This portion of the circuit detects the presence of interference and signals the blanking portion of the circuit to begin processing. Any signal of sufficient amplitude to exceed the threshold of the Schmitt trigger is considered to be interference.

As before, the first stage governs the circuit response time, while the second stage provides gain.

In this case, the gain stage serves as a level control for the Schmitt trigger threshold. Advancing the threshold level control (front panel) reduces the gain, and, hence, a stronger signal is required to fire the Schmitt trigger. Lowering the gain in this manner effectively increases the level which a pulse must exceed in order to be recognized as interference. Similarly, lowering the threshold control increases the gain, decreasing the level of voltage required to trigger the blanking circuit.

When the Schmitt trigger fires the following flipflop is set indicating the presence of interference of the 100 μsec span of the signal. The flipflop holds its state for the duration of the sample period, and its state determines whether or not the blanking process will be activated. In the set state the flipflop holds the counter cleared so that at the end of the sample

*Note: Sample period is selectable at the front panel -- 300 μsec and 1.0 msec may be selected in addition to 100 μsec. These produce output quantization intervals of 4.8 msec and 16.0 msec, respectively, instead of 1.6 msec. Coarser sampling lowers the upper limit on the frequency allowed for recovery through the analog-to-digital and digital-to-analog conversion process.

period a zero-valued count is added into the accumulator. At the end of 16 sample periods the accumulator contains the sum of contributions from only sample periods which are free of interference. A separate counter (dubbed the "good" counter) keeps track of how many interference-free samples there are in each sixteen-sample interval.

To correct for the error caused by blanking some of the signal data, the signal is passed through a compensation network (16 bit x 4 bit divider) before being converted back to analog form. The digital number in the "good" counter is some fraction of sixteen; the number in the accumulator is the same fraction of the number that should be in the accumulator under noise-free conditions. This number is normalized by multiplying by 16/N, where N is the number of interference-free samples in the 16-sample interval (read from the "good" counter). This is the same as averaging the good data samples in the 16-sample group and substituting the average for all the sample periods thrown out. The adjusted value is then fed to the D/A converter and produces a stairstep replica of the input just as described earlier, except that the effects of interference are almost undetectable.

The only exception allowed in this process is for the case where fewer than four sample periods are interference-free in any 1.6 msec interval. In this event the system will throw the whole interval out and simply hold the previous count.

IV. Compensation Network (Divider) Operation

The integrated signal sample from the VCO counter and accumulator is corrected for missing samples by multiplying the accumulator output by 16 and dividing by the number of interference free samples. This is done by loading 16-bit x 4-bit integer divider with the 12-bit number from the accumulator shifted 4 bits toward the MSB.

The divider is a subtract-test-shift operation. The 4-bit divisor is two's complemented and added to the most significant bits of the dividend for the subtract phase. If the result of the subtraction is positive (carry bit generated by the add) a "1" is loaded into a serial-in parallel-out (answer) shift register; the result is latched around to the adder 16-bit input and the divisor is shifted one bit in the less significant bits direction. If the result is negative a "0" is loaded into the answer shift register and the 16-bit input is not changed. This sequence is repeated 12 times and at the end the answer is latched into the D/A converter.

Figure 12 shows the circuitry for generating the necessary 4-phase clock (ϕ_2 not used) and the 12 pulse burst for the divider. A start pulse is required from external circuitry when the data is available and the divider free runs to the end of the operation and awaits another start pulse. Figure 13 is a block diagram of the divider.

If the divisor is 16 the 12-bit dividend is latched directly into the answer at the time of the start pulse and division is inhibited.

V. Test Results

In addition to DC and simulated interference tests in the lab the Impulse Noise Suppressor was run at the 300-ft telescope in close to actual observing conditions. The 250-500 MHz receiver was used to provide a signal around 300 MHz with a bandwidth of 10 MHz. The detected signal was fed both into the Noise Suppressor and directly to a chart recorder. A rather strong lot of ignition interference was generated by parking a car just far enough away from the 300-ft to see the feed over the lip of the dish. The results are shown in Figures 17 and 18.

The lighter trace in both figures is the unsuppressed detector output and the darker trace is the output of the Noise Suppressor. Calibration signals show that the scale is about the same on both traces. The Noise Suppressor virtually eliminates the effects of the ignition noise without increasing the rms output noise significantly.

A trial was also run with the IF gain modulator switched on and strongly unbalanced to test the recovery time of the blanking circuit. With proper selection of the coupling capacitor to the Schmitt trigger circuit the recovery was sufficiently fast to blank out less than 10% of the 50 Hz switched waveform and still do a good job of suppressing ignition noise.

VI. Some Design and Operating Considerations

The Impulse Noise Suppressor was primarily designed for use with radiometers below 1 GHz, hence with RF bandwidths less than 10 MHz. In a 100 μs sample period the rms noise of a 10 MHz bandwidth signal is 0.03 of the DC level. With a nominal VCO operating frequency of 1 MHz (1 V input, 2 V output) the 100 μs quantization fraction will be 0.01 which will not significantly increase the output noise of the receiver system. The quantization interval would become important, however, for RF bandwidths approaching 100 MHz. Also, if the sample interval is switched to 300 or 1000 μs the rms signal noise will decrease and become equal to the quantization fraction with an RF bandwidth of 10 MHz and a sample interval of 1000 μs. The input level is multiplied by (100 μs)/(sample interval) in a voltage divider to keep the counters from overloading and to keep the overall device gain the same for all sample intervals. The longer sample intervals are best suited for narrower bandwidths.

The purpose of limiting the lower and upper video passbands of the input to the Schmitt triggers is to prevent normal DC changes from blanking the output

and to make the recovery time a bit longer than that of the signal path so that the interference is cleared before blanking is taken away. The low frequency cutoff must be higher than any components present in the desired signal but low enough to respond to broad pulse interference. The high frequency cutoff should be about a factor of two lower than the cutoff in the signal path which in turn is just low enough to keep the normal peak to peak noise in the signal from saturating the op amps and VCO. Ideally the trigger passband and sample interval should match the interference video spectrum, but a compromise must be struck to avoid changing components for each application. Most pulsed interference has a duration of less than a few hundred microseconds. The NRAO standard receiver square law detector circuits have a response time of about 1 ms which is too slow for this application. However, the detectors in the multibandwidth backend have been designed for a 10 μs time constant and would normally be used with the low frequency receivers.

Figures 4 and 6 show that the three video passband controlling capacitors (C101, 102, and 103) have been brought out to sockets for easy change if the need warrants.

APPENDIX I

FUNCTION OF CONTROLS

A. The ± 15 V POWER switch and pilot light pertain only to the internal

    ± 15 volt power supply. The +5 volt power is supplied and switched

    externally.

B. The BLANK control selects the means of controlling which parts of the

    signal are blanked. "EXTernal INPUT" position allows a TTL signal

    applied at the "EXTERNAL BLANK" input on the front panel to blank the

    signal in parallel with the internal interference-detecting circuitry.

    A high level TTL signal causes the blanker to operate; the internal

    detection circuitry governs blanking while the external input is at

    low level. "AUTOmatic" position is the normal operating position.

    The internal circuitry then governs blanking action.

C. The BLANK INHIBIT control provides for interruption of the internal

    blanking circuitry. In the "OFF" position the internal blanking is

    allowed to operate normally unless otherwise restricted by the setting

    of the BLANK control. In "EXTernal INPUT" position an external TTL

    high level will disable the blanking circuitry while a low level will

    allow normal operation. The "ON" position, when selected, disables

    the blanking circuitry allowing the input signal to pass through the

    system unmodified, regardless of interference.

    Note: If the BLANK control setting conflicts with the BLANK INHIBIT

           control setting, the BLANK control will override.

D. The SAMPLE PERIOD control adjusts the rate at which the analog-to-digital

    conversion takes place and, hence, controls the width of the stairstep in-

    tervals of the output signal. See the note at the bottom of page 2 in

the main report. This control also varies the gain of the op-amp stage driving the VCO so that a constant system gain is maintained in spite of varying time base frequencies.

E. The TRIGGER LEVEL control controls the voltage level at which interference is detected. Raising the threshold level requires interference to be of a greater amplitude for detection. Additional description can be found on pages 3 and 4 of the main report.

F. Test points TP1 and TP2 are provided for the purpose of monitoring the signal on each side of the Schmitt trigger: TP1 is connected to the input and TP2 is connected to the output. The blanking threshold is best adjusted while monitoring TP2 on a scope. Set the threshold so only an occasional normal random noise spike fires the blank trigger under the highest input signal level.

G. The EXTERNAL BLANK BNC jack accepts a TTL signal for the purpose of externally activating the blanking circuitry as described in part B of this appendix. This provision is primarily intended for use when the time of occurrence of interference is known and can be blanked with an external signal.

H. The EXTERNAL INHIBIT BNC jack accepts a TTL signal for the purpose of externally disabling the blanking circuitry as described in part C of this appendix.

I. The INPUT and OUTPUT BNC jacks are found on both rear and front panels, and are for the purpose of making connection between the blanker and the equipment with which it is to be used. Either pair of jacks may be used. The input voltage should not exceed +5 volts, and the output will not exceed +10 volts.

APPENDIX II

CHASSIS LAYOUT AND INTERCONNECTING WIRING

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FIG. I   BLOCK DIAGRAM OF NOISE BLANKING SYSTEM
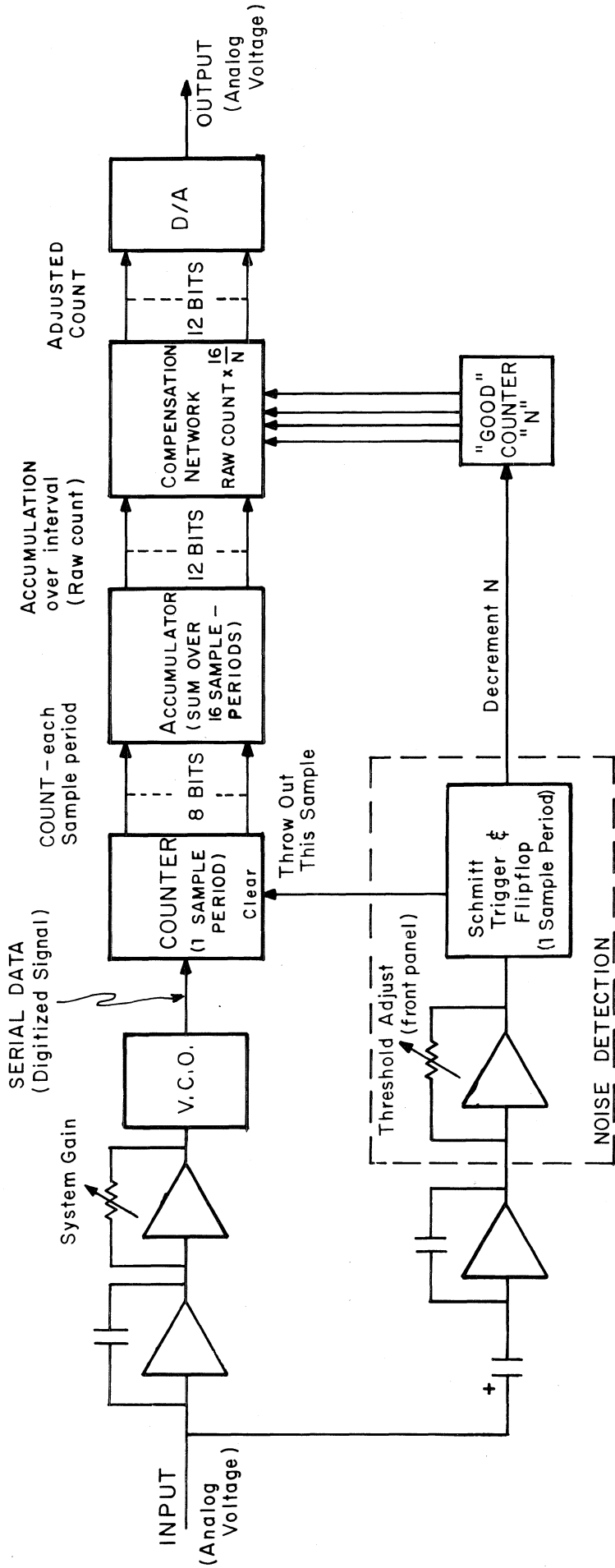
NOTE:
"N" Represents the number of sample periods in each
interval which contain good, interference free data.

One sample period refers to the time elapsed while the
counter is running. Usually 100 μsec. but adjustable
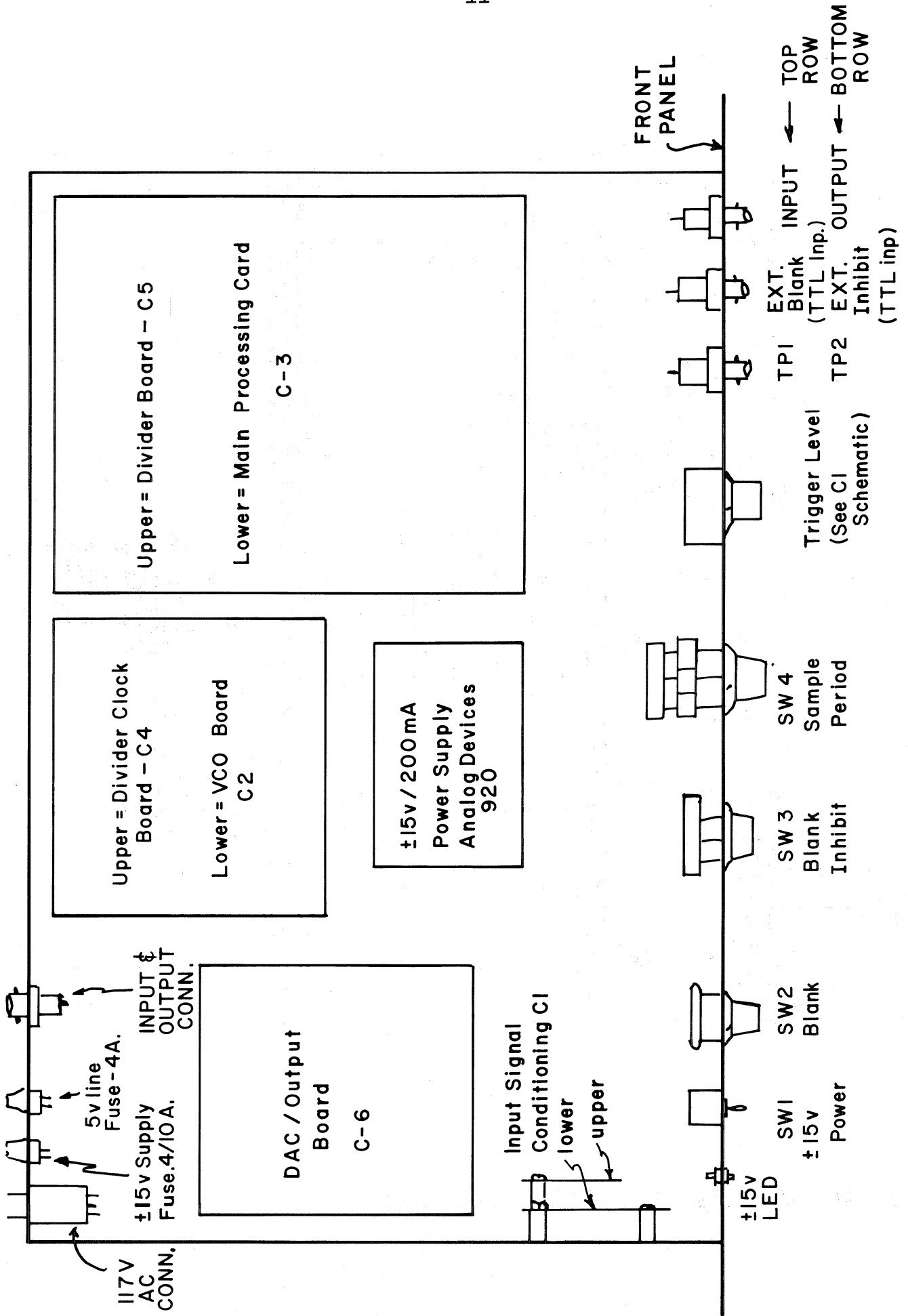at front panel. see note on page 2.

FIG. 2 TOP VIEW OF NOISE SUPPRESSOR SHOWING LOCATION OF MAJOR COMPONENTS
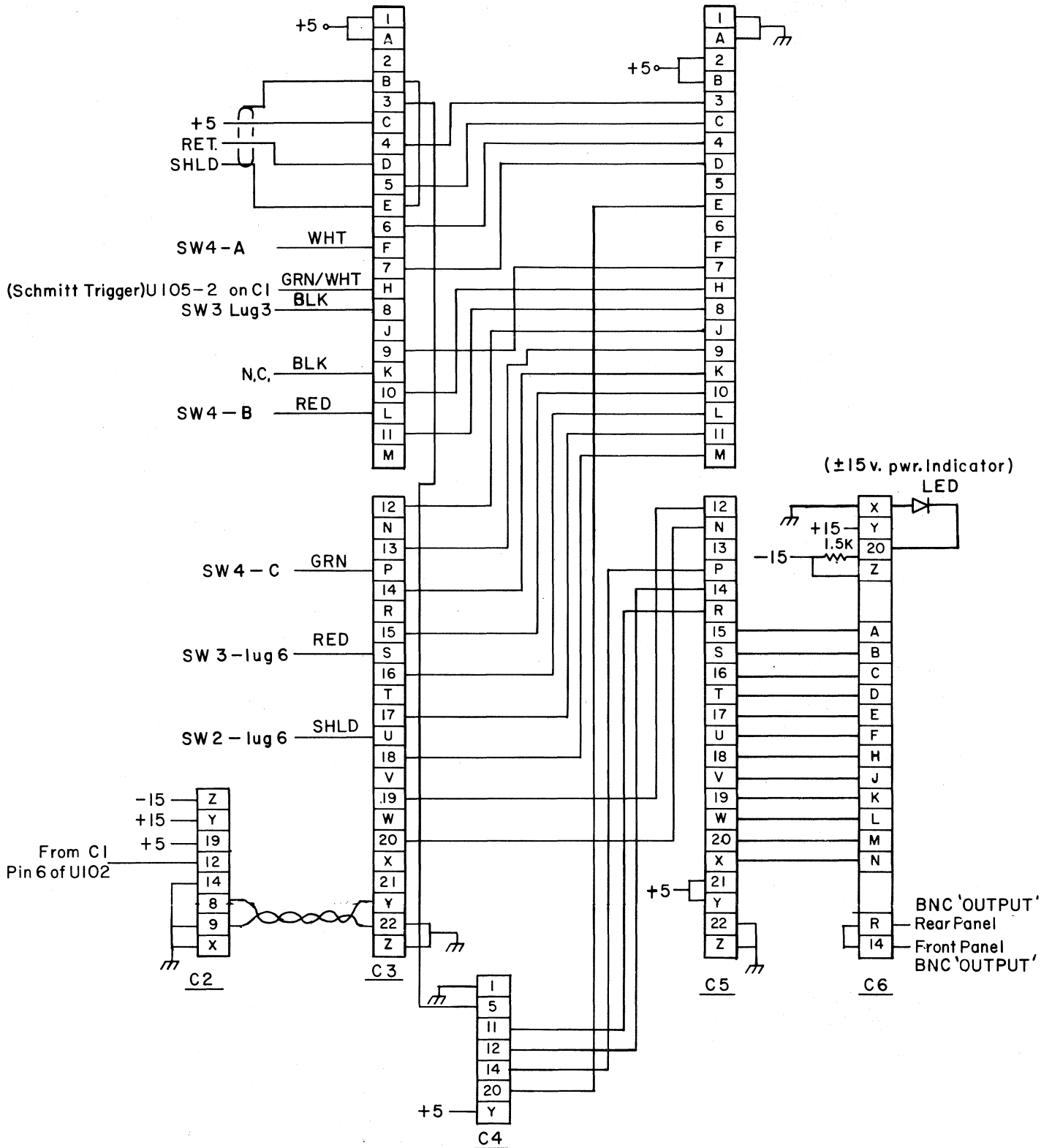
FIG. 3   INTERCONNECTION OF BOARDS INSIDE CHASSIS

APPENDIX III

COMPONENT IDENTIFICATION AND PLACEMENT
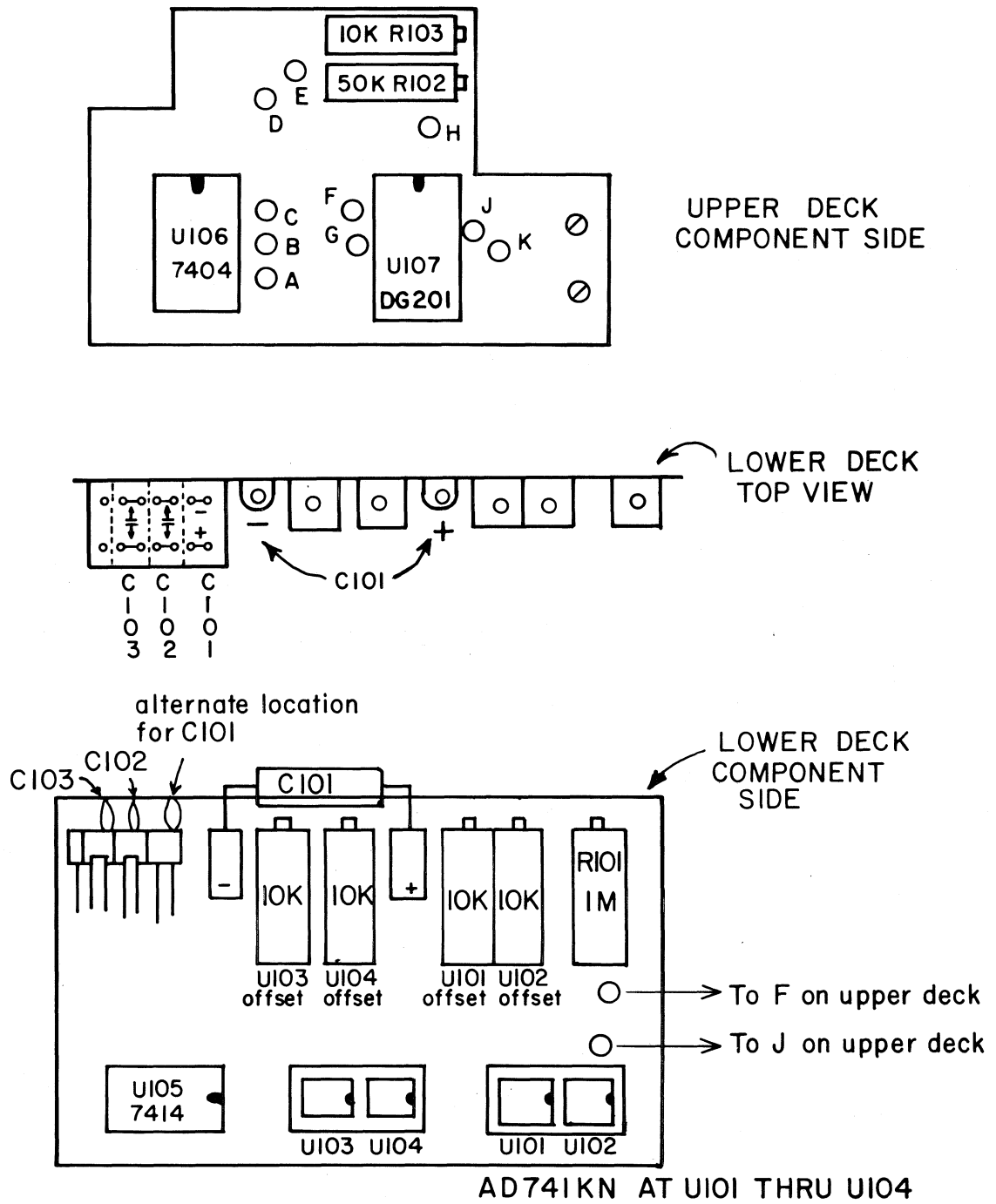
FIG. 4 CARD C1 INPUT SIGNAL CONDITIONING
BOARD LAYOUT SHOWING LOCATION OF COMPONENTS

C5 – DIVIDER

	U526 74174	U523 7432	U518 7483	U512 74194	U506 7483
	U525 74174	U522 7432	U517 7483	U511 74194	U505 74123
	U524 74174	U521 7432	U516 7483	U510 74194	U504 74174
		U520 7402	U515 7483	U509 74194	U503 74174
		U519 7408	U514 74194	U508 74194	U502 74174
			U513 74194	U507 74123	U501 74174

C3 – MAIN PROCESSING BOARD

U336 74192	U333 74193	U316 7414	U323 74123	U322 7474
U325 74193	U334 7492	U332 74192	U317 7400	U320 7432
U326 7442	U330 7432	U335 7473	U318 7474	U302 74193
U327 7404	U319 7474	U303 7408	U329 7402	U305 7474
U313 74193	U315 74123	U314 7425	U308 7483	U307 7483
U328 74193	U321 7410	U312 74174	U311 74174	U310 74174
				U324 74164
				U331 7474
				U301 74193
				U304 74174
				U306 7483
				U309 74174

C4 – DIVIDER CLOCK

	U411 7473	U404 7404
U409 7404	U410 7408	U405 74123
U408 74193	U407 7408	U406 7473
		U403 7442
		U402 74193
		U401 7413

TOP VIEW OF CARDS C3, C4 & C5
Showing Locations Of Integrated Circuits.

FIG. 5

APPENDIX IV

SCHEMATICS AND BLOCK DIAGRAMS
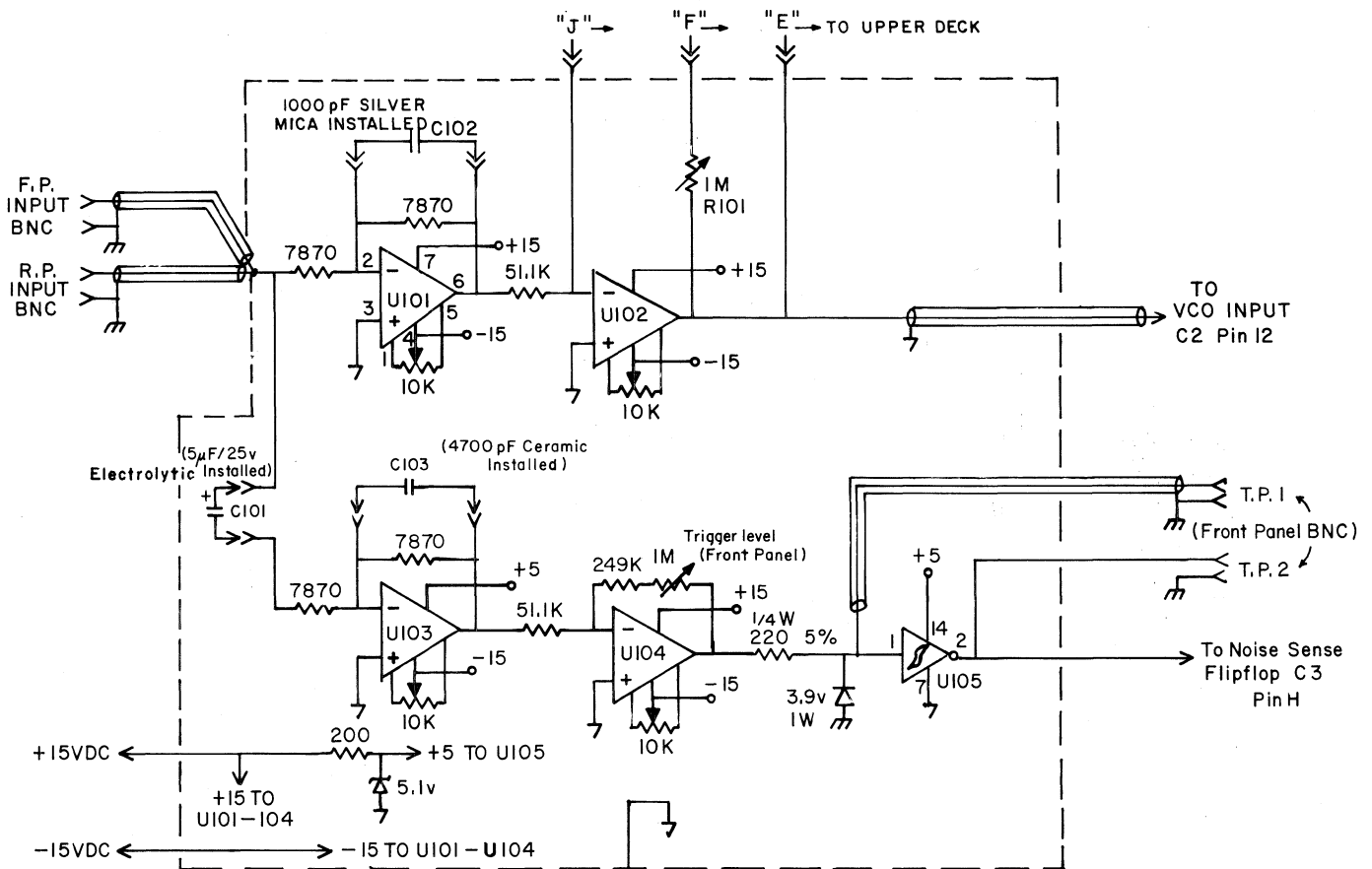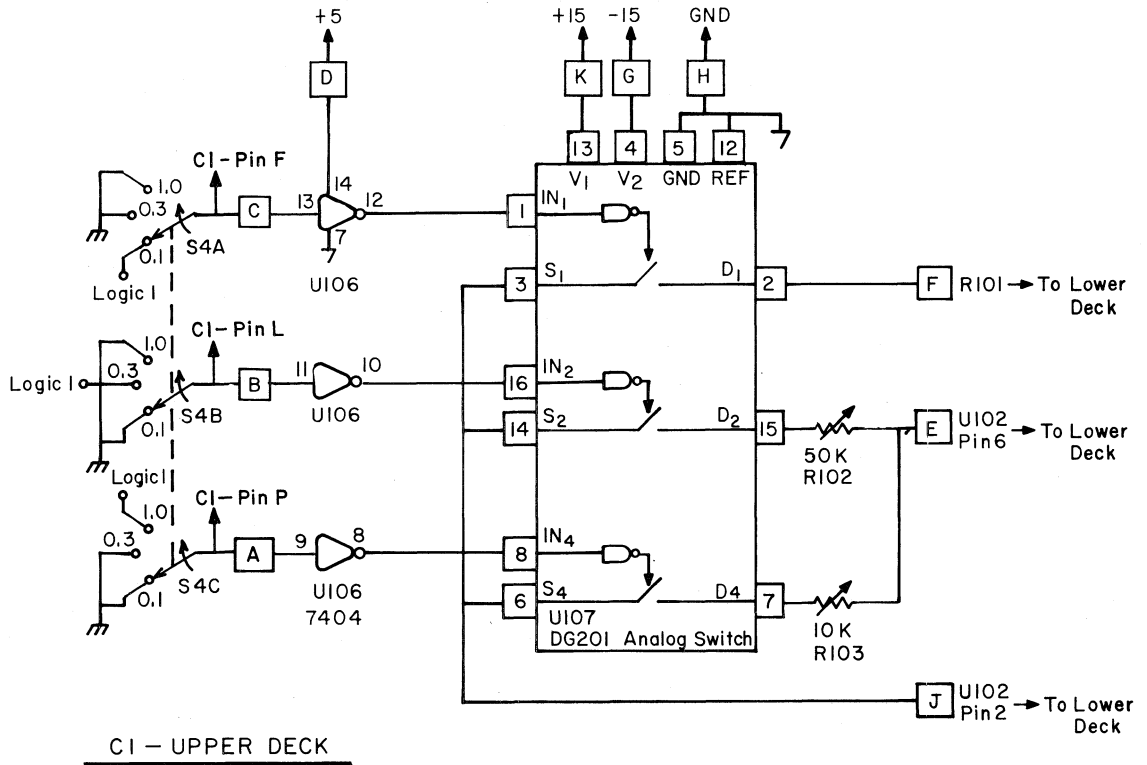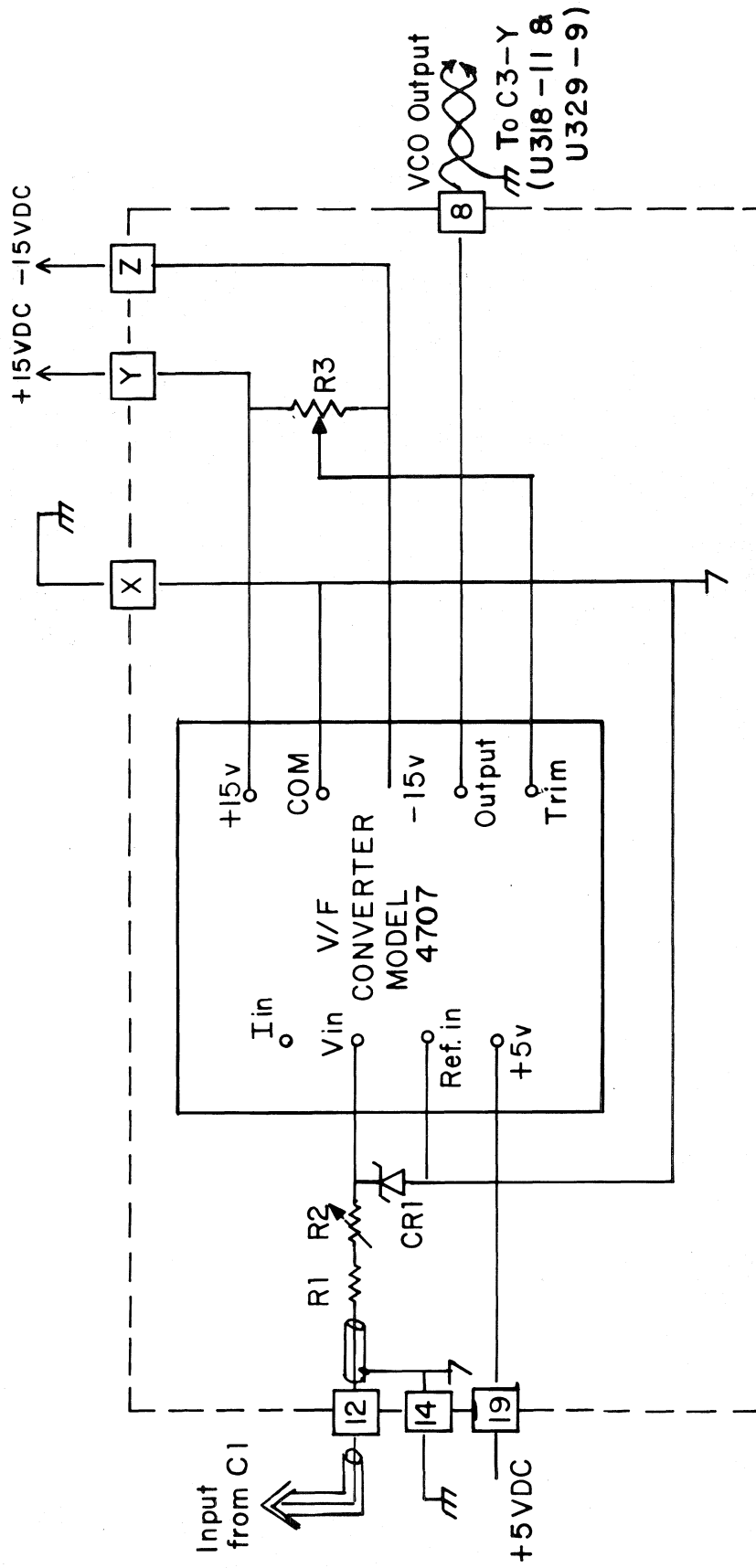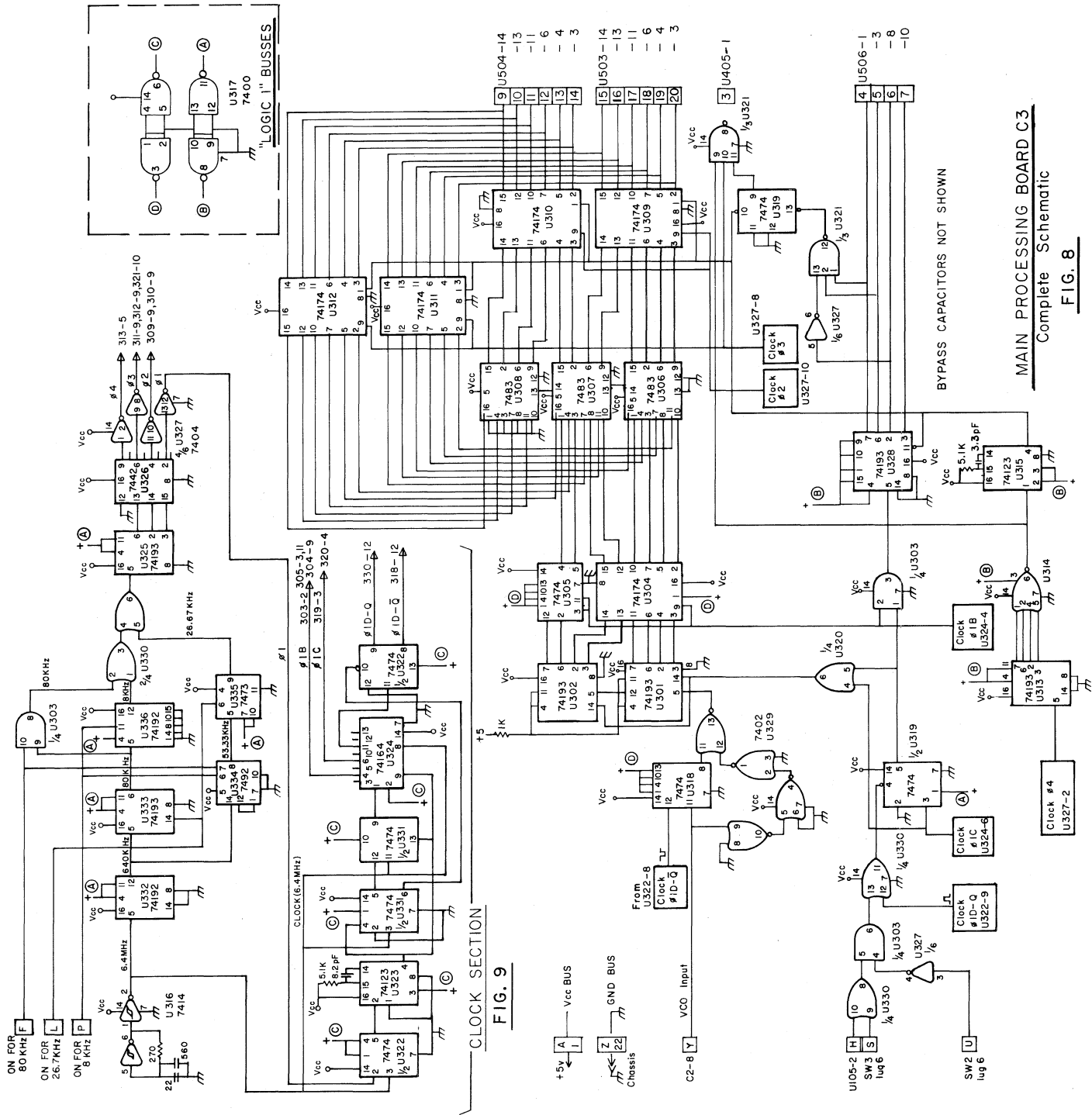
FIG. 6   INPUT   SIGNAL   CONDITIONING   BOARD C1

FIG. 7   VOLTAGE TO FREQUENCY CONVERTER (VCO) BOARD C2

R1 - 100Ω 1% 1/2 W   R3 - 50KΩ CERMET TRIM POT
R2 - 100Ω CERMET TRIM POT   CR1 - 1N4741, 11v. Zener 1W
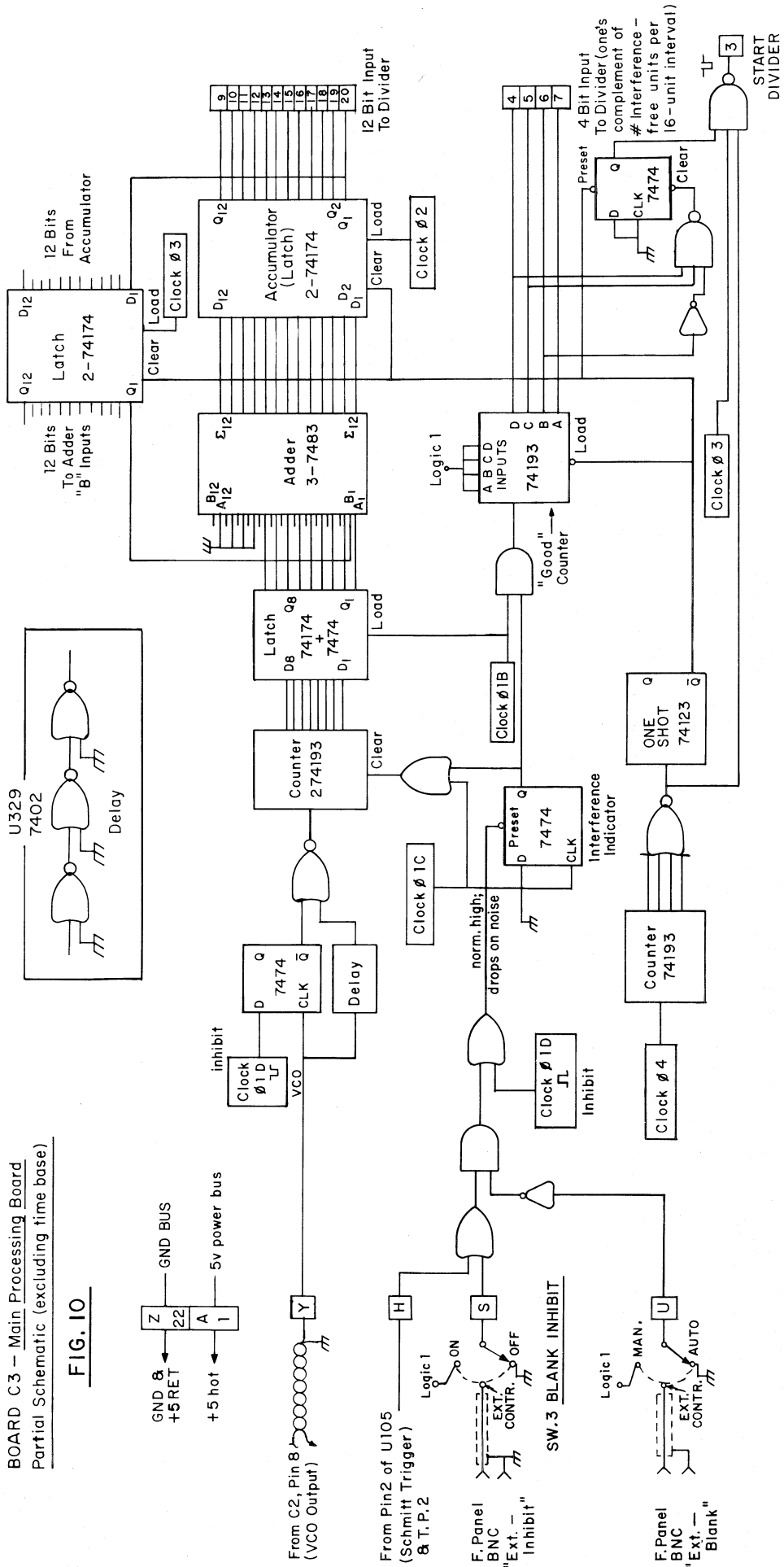
"LOGIC 1" BUSSES

CLOCK SECTION
FIG. 9

MAIN PROCESSING BOARD C3
Complete Schematic
FIG. 8

BYPASS CAPACITORS NOT SHOWN

FIG. 10

BOARD C3 – Main Processing Board
Partial Schematic (excluding time base)

FIG.11   Block Diagram Of Main Clock (part of board C3)
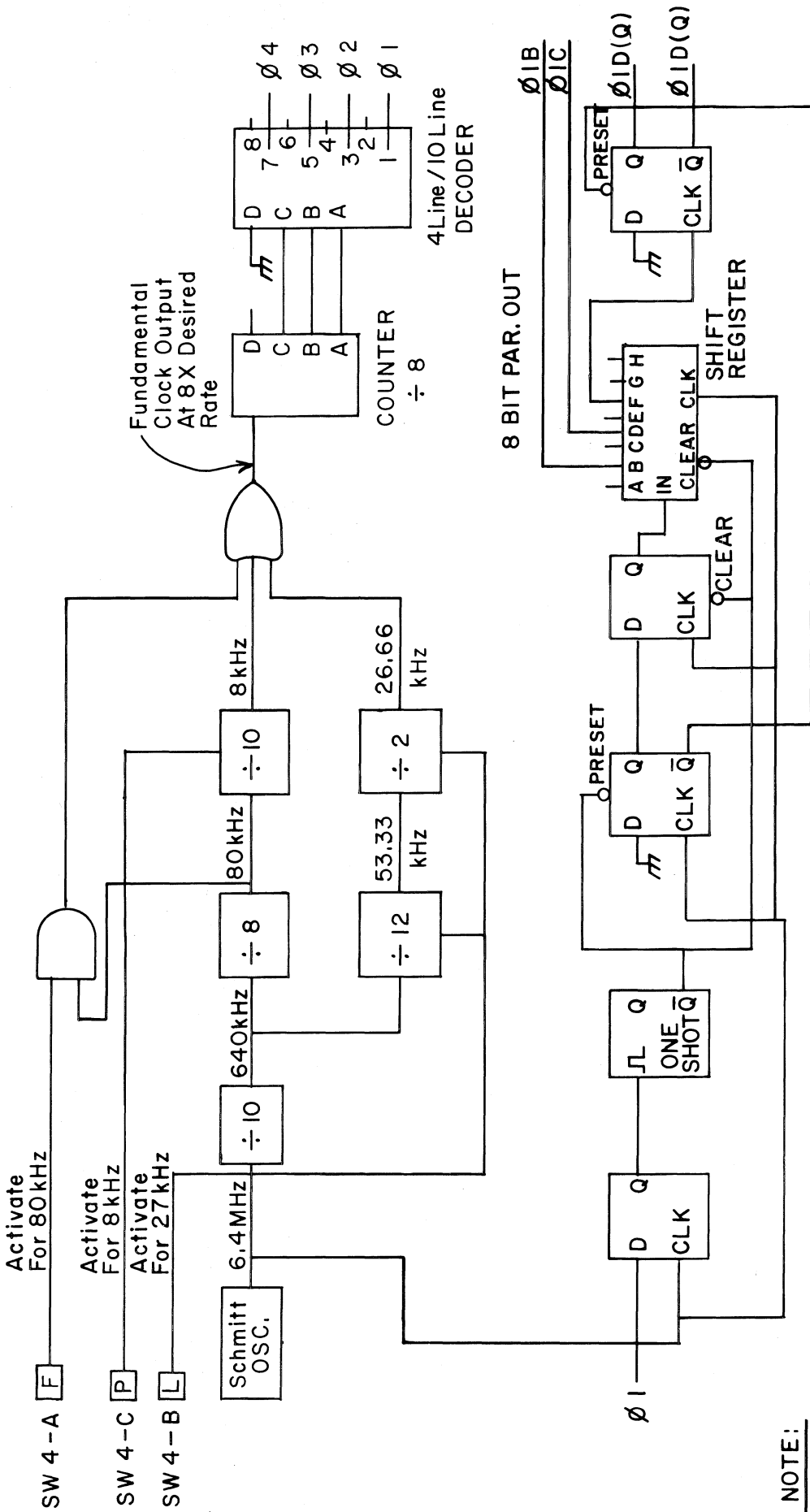
NOTE:
SW 4 Is Sample Period Switch Located On Front Panel.
Schematic Pictured With Board C1 – Upper Deck.
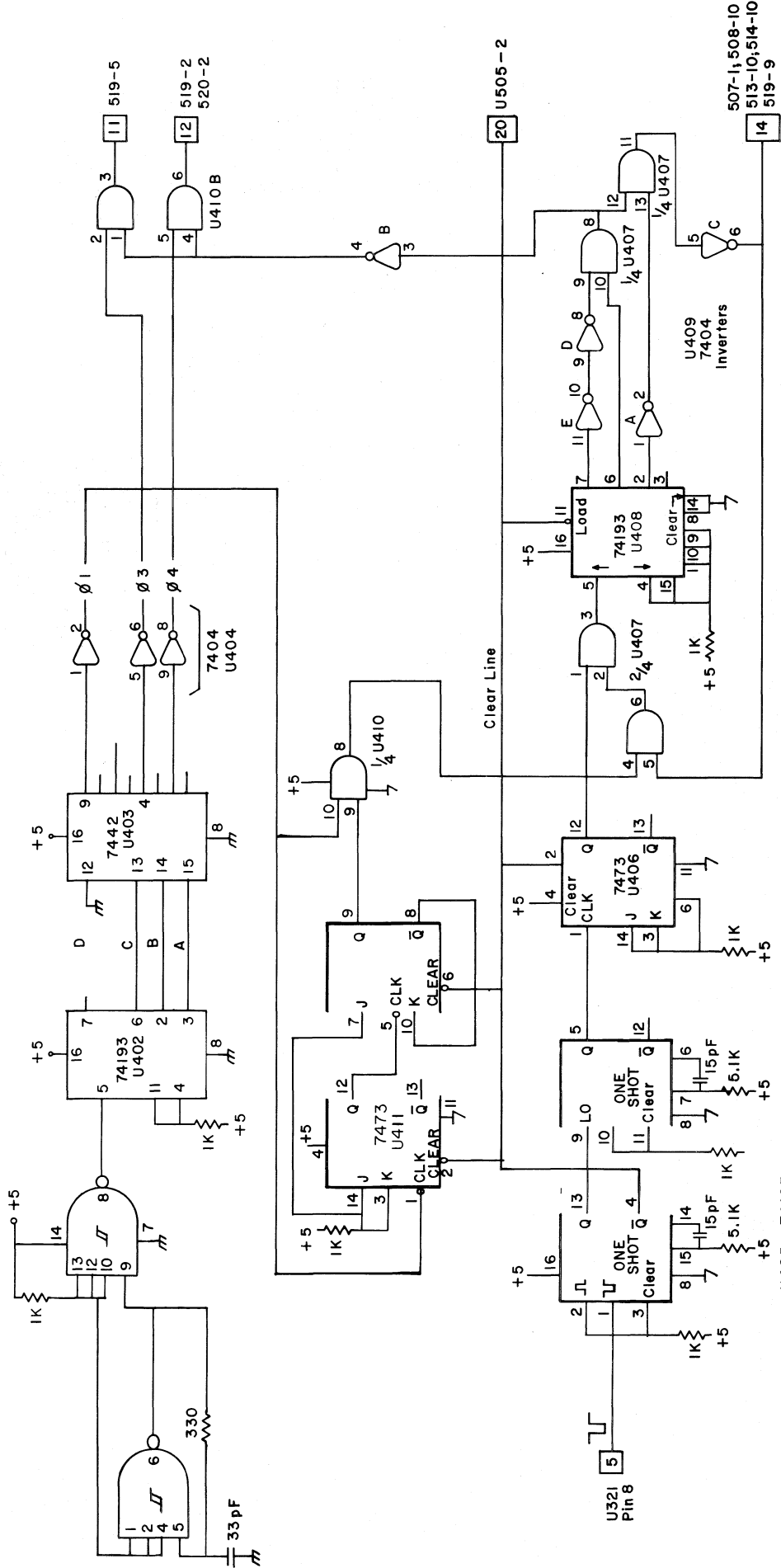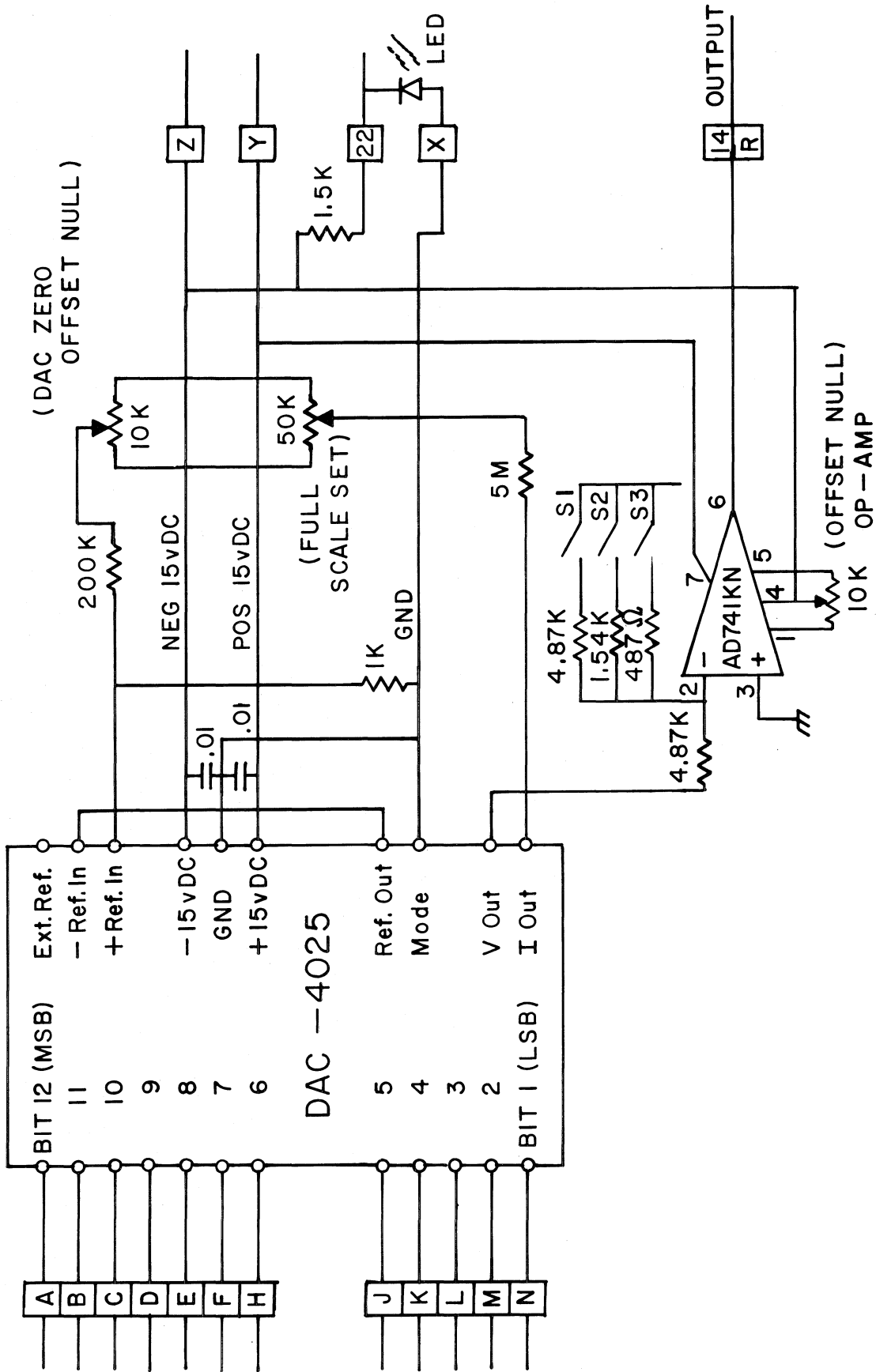
FIG. 12   CARD C4 - DIVIDER CLOCK
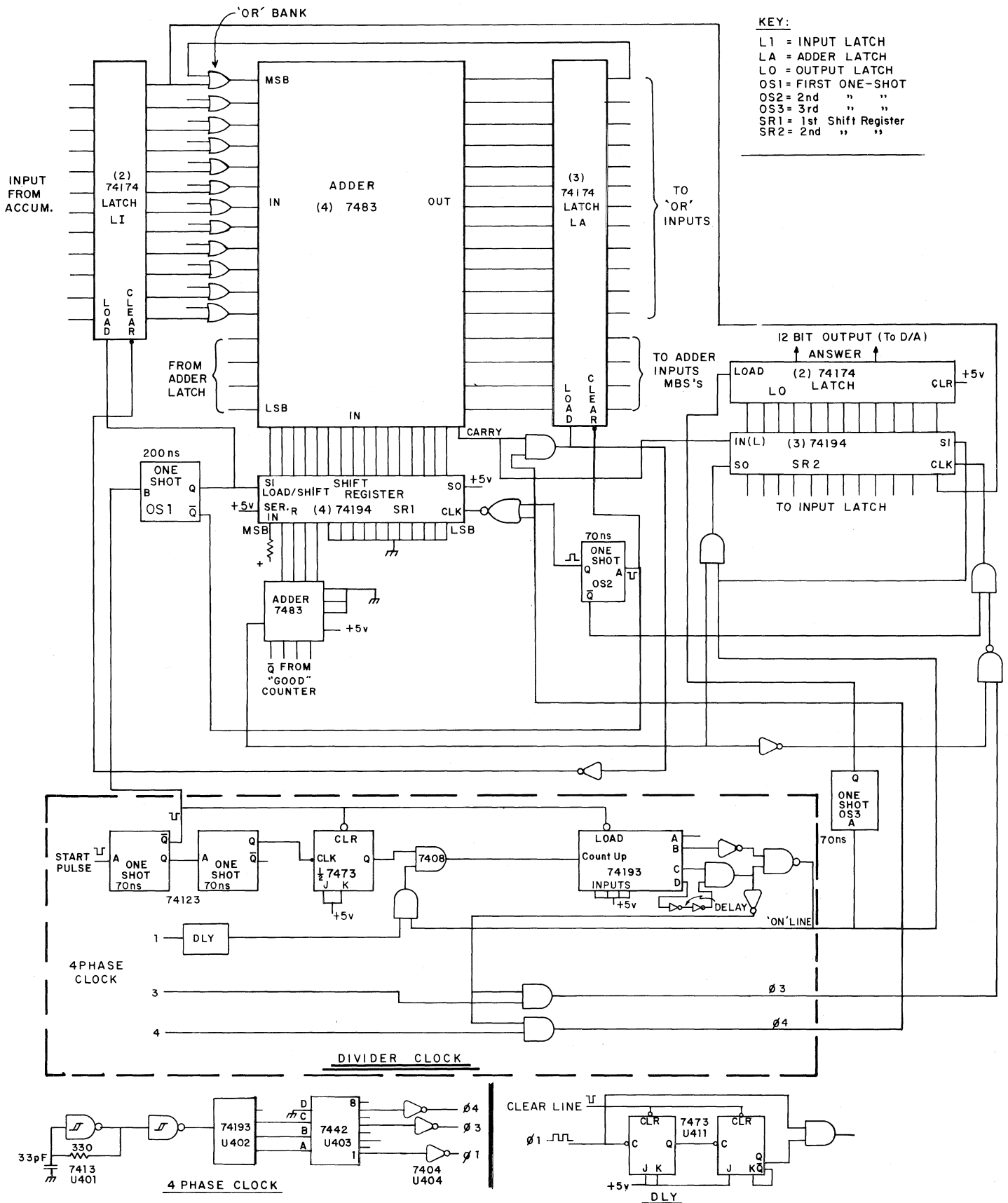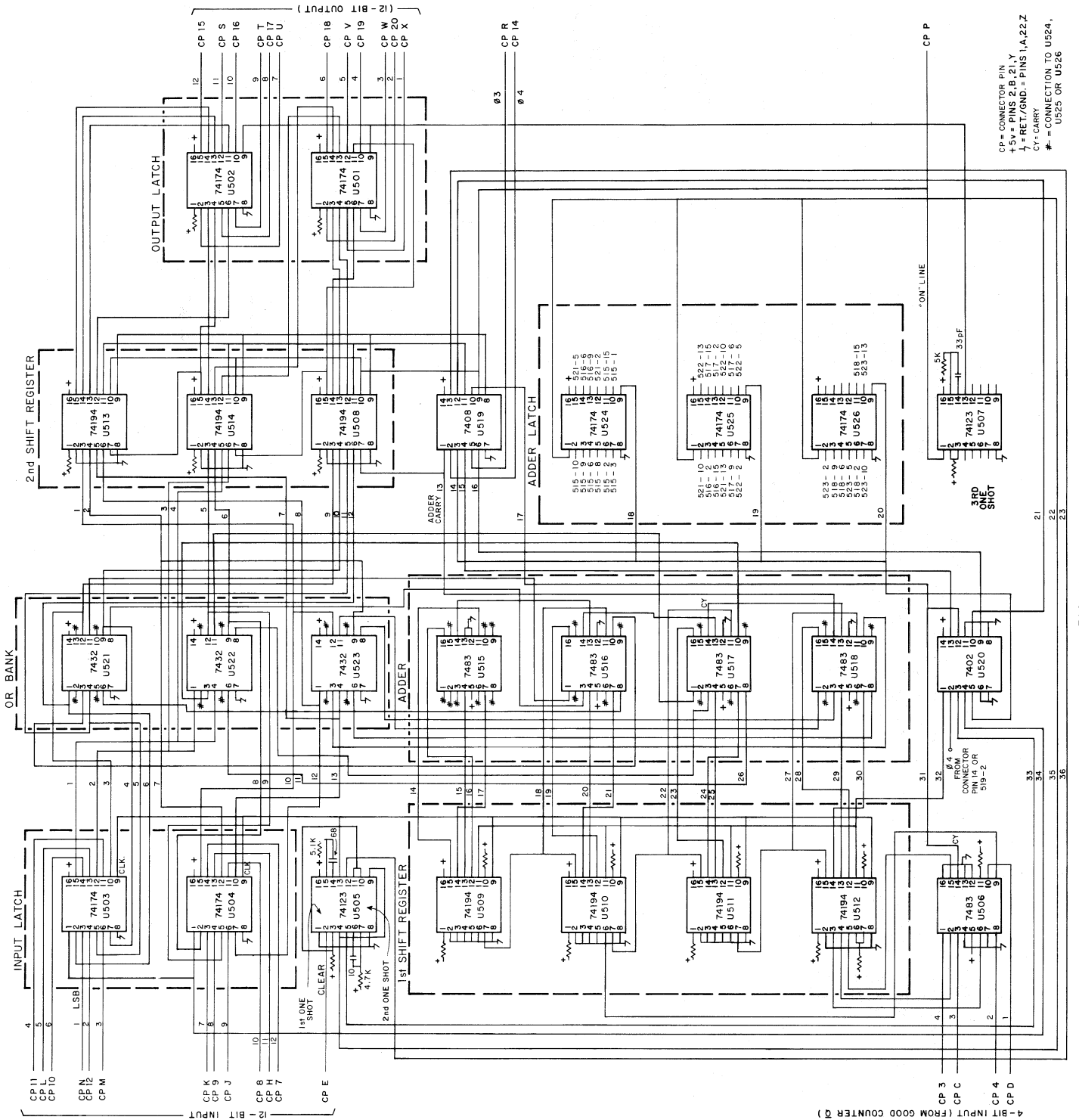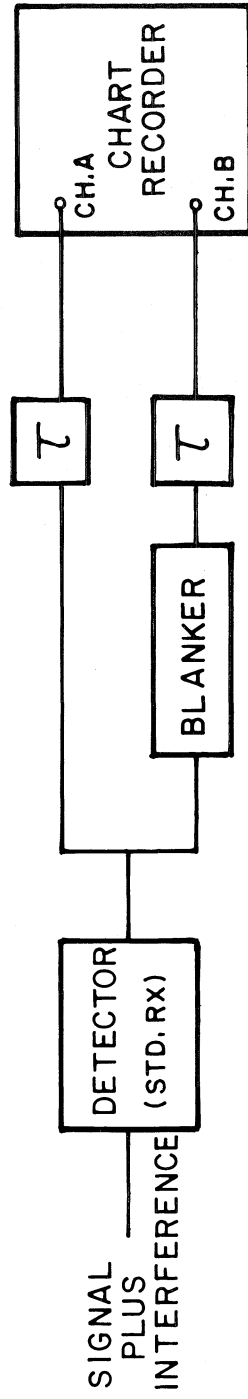
FIG. 13

FIG. 14

FIG. 15   DAC OUTPUT CARD 6

FIG. 16   TEST SETUP UNDER WHICH THE FOLLOWING
GRAPHS WERE MADE.

APPENDIX V

PRELIMINARY TEST DATA

CAL

CAL
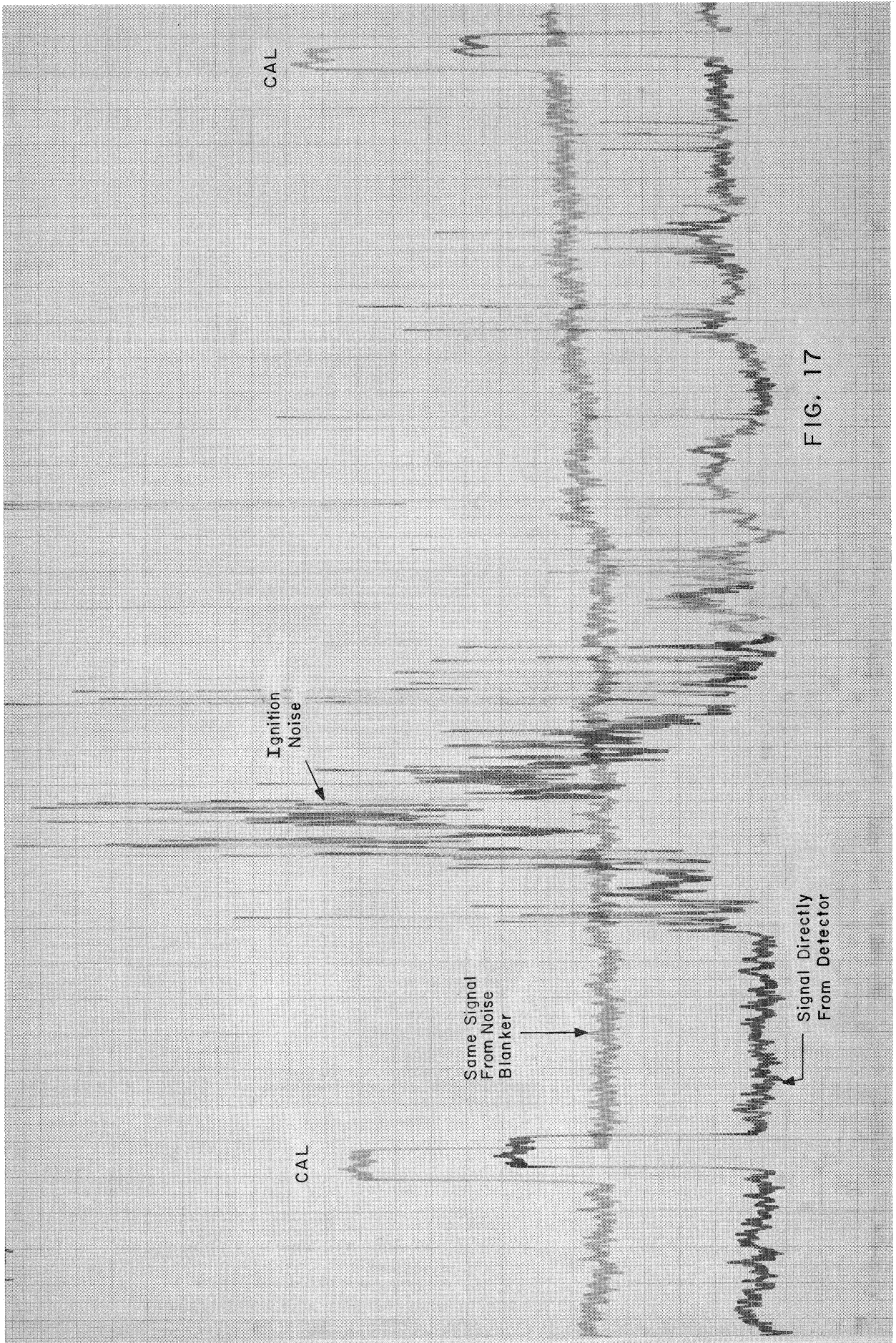
Ignition
Noise

Same Signal
From Noise
Blanker

Signal Directly
From Detector

FIG. 17

CAL

Signal From
Noise Blanker

Signal Directly
From Detector

Blanking
Off

FIG. 18