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SATELLITE VLBI DELAYLINE

BENNO RAYHRER AND BILL WIREMAN

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ILLUSTRATIONS

SATELLITE VLBI DELAYLINE

1. INTRODUCTION

This report is an introduction to the satellite Delayline explaining how to operate it and how the internal circuitry works. Also the various input and output lines are described.

2. POWER DISTRIBUTION

A master circuit breaker is supplied on the bottom front panel of the cabinet. The circuit breaker is rated at 30 amperes with the system dissipating approximately 3600 watts. An external 12 gauge, three conductor cable supplies the necessary 110 volts single phase alternating current. When the circuit breaker is engaged it supplies the various power supplies, cooling fans, and output receptacles with power.

Altogether there are three different direct current voltages necessary to operate the system. They are +5 volts, -5 volts and -12 volts which are all supplied by Lambda power supply modules. The supplies are equipped with overvoltage protection and circuit breakers or fusing for overcurrent protection. On page two, Figure 1 is a power distribution scheme of the system.

A monitor circuit illuminates a red lamp on the CORRELATOR-BUFFER-DELAY panel if any of the voltages is not present.

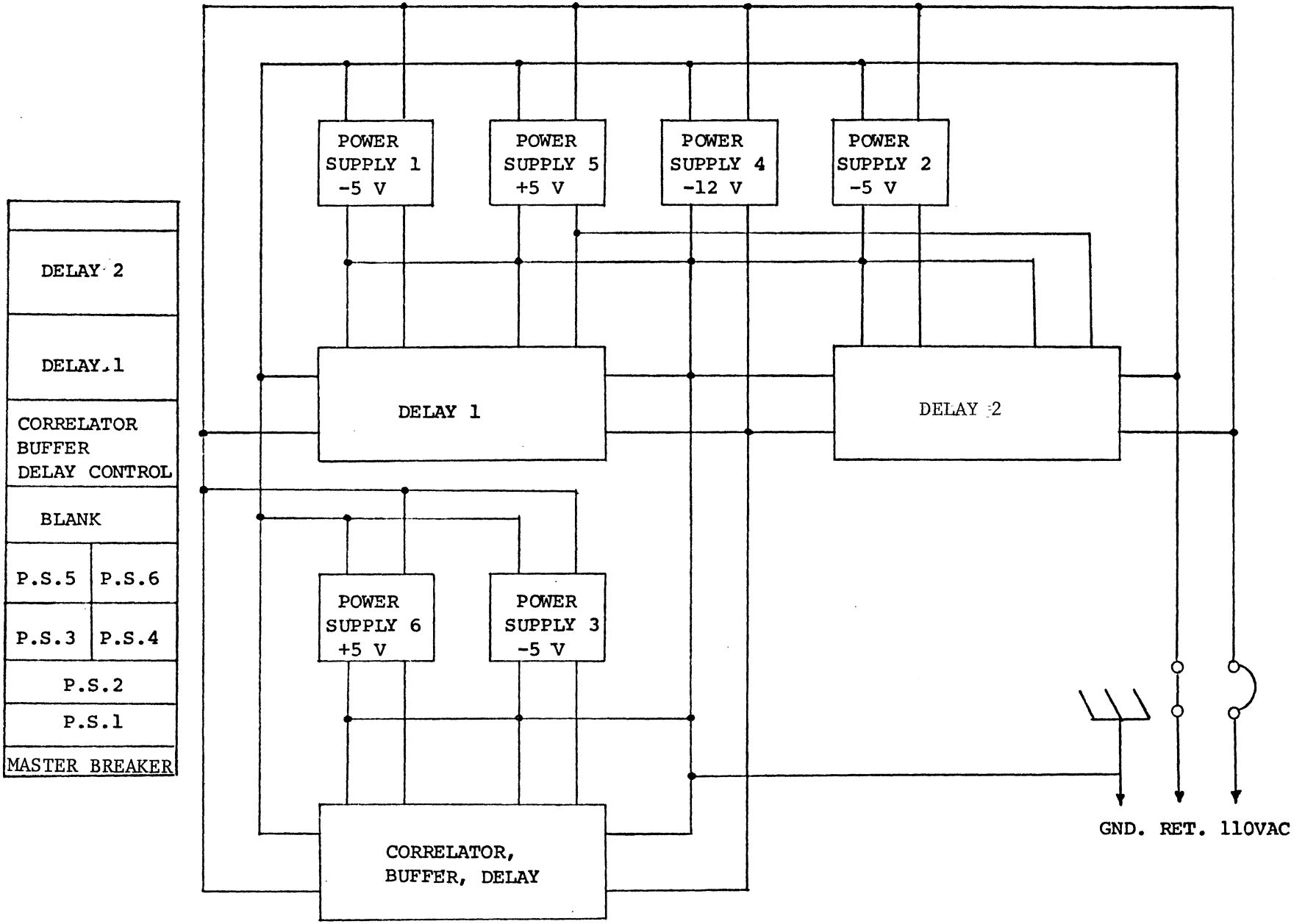


FIGURE 1. SATELLITE DELAYLINE POWER DISTRIBUTION

3. CONTROL AND DISPLAY PANEL

The control panel is labeled so that signals are shown as they would actually appear in the system wiring. The red indicators in the signal lines when illuminated are indications that the data is not being detected on the lines. Under the block DELAYLINE are numbered green indicators that when illuminated correspond to a specified delay which can be entered from the corresponding switches or the computer. A two position switch designated manual in the up position and auto in the down position selects the method of entering the delay. The manual mode requires the operator to enter the delay through the panel switches and the auto mode requires the computer to output the delay. There is a 6 digit plus sign bit decimal display to show the fringe rate in hertz, the system delay in microseconds or the checkerboard errors per second. The two position switch to the right of the decimal display selects the information to be read out except when in the checkerboard test mode the display is forced to show the CHKBD ERRORS/s. Test points are provided along the signal lines to scope selected data.

The Test Pattern Generator block is used to perform a self check of the delay system. There are three switch selectable modes of operation to choose from. First, the Local Pseudo, which generates two known repeatable 255 bit data patterns with variable delay that are applied to the system checking delay and correlator. The correlator is read by the computer and a 100% correlation is observed every 255 channels. Second, the Remote Pseudo, which switches the data through the local input while the remote site generates the same data sequence through the sattelite link. The computer inputs command of data handling to the system and checks delays with the correlated data. Third, is the Checkerboard, which generates a repetitious pattern of 32 ones and

32 zeroes. This data pattern represents the worst case condition for the 1024 bit shift registers and will detect any defective chips in the delay-line. The decimal display indicates the errors that occur in each one second interval while a red indicator to the right of the Test Generator mode switch illuminates with each individual error detected.

At the bottom right hand corner of the panel are two lamps that indicate the condition of the power supplies. A green lamp illuminates when power is applied to the system. A red lamp illuminates when any one of the voltages is missing or drops to less than the monitor circuit can detect or if the master clock signal to any of the delay chassis is missing. On page five, Figure 2 is a layout of the display panel.

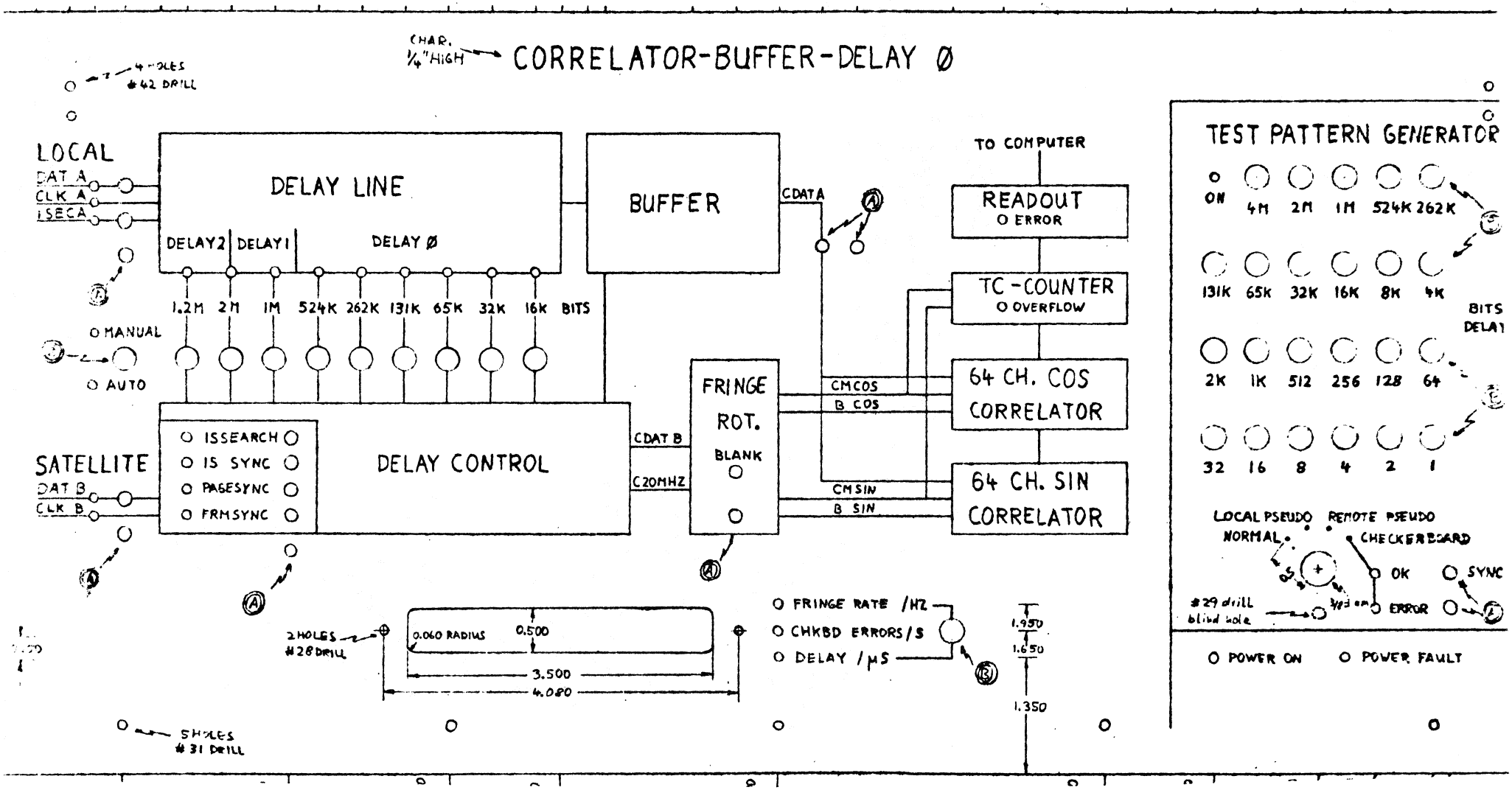


FIGURE 2. CORRELATOR-BUFFER-DELAY CONTROL AND DISPLAY PANEL

4. COMPUTER INPUT/OUTPUT LINES

Interrupts:

1 SIRPT	Interrupt at beginning of every second, from satellite link.
13 MSIRPT	Interrupt every 13.1072 ms after 1 second interrupt, from satellite link.

Outputs to Computer:	20 bits total
COROUT 0-15	16 bits correlator output
CORBSY	Status bit is set while correlator is clearing
BUFOVF	Buffer overflow
BUFSTV	Buffer starve
SYNERR	Sync error
Inputs from Computer:	46 bits total
COR BLK	Blank correlator
COR CLR	Clears and recovers correlator
NXTWRD	Requests next word from correlator
FP 0-3	Fringe phase
FR 0-15	Magnitude of fringerate
NEGFR	Sign of fringerate
DLY 0-19	Geometric delay plus offsets
RESERR	Resets all error flip-flops

The following listing contains jack and pin assignments of the computer input and output lines. The interrupt signals are connected by co-ax cables to the computer with remainder of the signals using three cannon 37-pin connectors and one fifty pin connector.

JACK 04 (37-pin)	COMPUTER I/O LINES	MNEMONIC
32	IO4-0	DLY 4
33	Ret	
30	IO4-1	DLY 5
31	Ret	
28	IO4-2	DLY 6
29	Ret	
26	IO4-3	DLY 7
27	Ret	
24	IO4-4	DLY 8
25	Ret	
22	IO4-5	DLY 9
23	Ret	
20	IO4-6	DLY 10
21	Ret	
18	IO4-7	DLY 11
19	Ret	
16	IO4-8	DLY 12
17	Ret	
14	IO4-9	DLY 13
15	Ret	
12	IO4-10	DLY 14
13	Ret	
10	IO4-11	DLY 15
11	Ret	
8	IO4-12	DLY 16
9	Ret	
6	IO4-13	DLY 17
7	Ret	
4	IO4-14	DLY 18
5	Ret	
2	IO4-15	DLY 19 (sign)
3	Ret	

JACK 05 (37-pin)		
32	IO5-0	NC
33	Ret	
30	IO5-1	NC
31	Ret	
28	IO5-2	NC
29	Ret	
26	IO5-3	FP0
27	Ret	
24	IO5-4	FP1
25	Ret	
22	IO5-5	FP2
23	Ret	
20	IO5-6	FP3
21	Ret	
18	IO5-7	NEGFR
19	Ret	

JACK 05 (37-pin)	COMPUTER I/O LINE	MNEMONICS
16	IO5-8	RESERR
17	Ret	
14	IO5-9	NXTWRD
15	Ret	
12	IO5-10	CORCLR
13	Ret	
10	IO5-11	CORBLK
11	Ret	
8	IO5-12	DLY0
9	Ret	
6	IO5-13	DLY1
7	Ret	
4	IO5-14	DLY2
5	Ret	
2	IO5-15	DLY3
3	Ret	

JACK 06 (37-pin)		
32	IO6-0	FR0
33	Ret	
30	IO6-1	FR1
31	Ret	
28	IO6-2	FR2
29	Ret	
26	IO6-3	FR3
27	Ret	
24	IO6-4	FR4
25	Ret	
22	IO6-5	FR5
23	Ret	
20	IO6-6	FR6
21	Ret	
18	IO6-7	FR7
19	Ret	
16	IO6-8	FR8
17	Ret	
14	IO6-9	FR9
15	Ret	
12	IO6-10	FR10
13	Ret	
10	IO6-11	FR11
11	Ret	
8	IO6-12	FR12
9	Ret	
6	IO6-13	FR13
7	Ret	
4	IO6-14	FR14
5	Ret	
2	IO6-15	FR15
3	Ret	

JACK 67 (50-pin)	COMPUTER I/O LINE	MNEMONIC
48	IO67-0	CORBSY
47	Ret	
46	IO67-1	BUFOVF
47	Ret	
44	IO67-2	BUFSTV
45	Ret	
42	IO67-3	SYNERR
43	Ret	
40	IO67-4	NC
41	Ret	
38	IO67-5	NC
39	Ret	
36	IO67-6	NC
37	Ret	
34	IO67-7	NC
35	Ret	
32	IO67-8	COROUT0
33	Ret	
30	IO67-9	COROUT1
31	Ret	
28	IO67-10	COROUT2
29	Ret	
26	IO67-11	COROUT3
27	Ret	
24	IO67-12	COROUT4
25	Ret	
22	IO67-13	COROUT5
23	Ret	
20	IO67-14	COROUT6
21	Ret	
18	IO67-15	COROUT7
19	Ret	
16	IO67-16	COROUT8
17	Ret	
14	IO67-17	COROUT9
15	Ret	
12	IO67-18	COROUT10
13	Ret	
10	IO67-19	COROUT11
11	Ret	
8	IO67-20	COROUT12
9	Ret	
6	IO67-21	COROUT13
7	Ret	
4	IO67-22	COROUT14
5	Ret	
2	IO67-23	COROUT15
3	Ret	

5. INPUT DATA AND TIMING LINES FROM THE RECEIVERS

There are five input lines which all use coax cables and are terminated into 50 ohm load. They are listed as follows:

DAT A	Data line from local reciever.
CLK A	Local clock timing at 20 MHZ rate.
1 SEC A	1 second pulse from local clock.
DAT B	Data line from remote site via satellite.
CLK B	Clock line from remote site via satellite.

6. DELAYLINE

The delayline contains 5,423,104 bits in 5296 dynamic shift registers (Signetics N2504V), 1024 bits each, and is divided into 83 cards with 4 blocks per card. Each block contains 16,384 bits. Delay is set by the hardware of the buffer from 0 to 271.1552 ms in increments of 819.2 us by the following lines:

1 BK =	16,384 b =	0.8192 ms
2 BK =	32,768 b =	1.6384 ms
4 BK =	65,536 b =	3.2768 ms
8 BK =	131,072 b =	6.5536 ms
16 BK =	262,144 b =	13.1072 ms
32 BK =	524,288 b =	26.2144 ms
64 BK =	1,048,576 b =	52.4288 ms
128 BK =	2,097,152 b =	104.8576 ms
76 BK =	1,245,184 b =	62.2592 ms

There will be spare slots for 5 additional cards: CD 83 to CD 87. This will enable the delay to be increased by 16.384 ms if necessary. On page 11 figure 3 is a block diagram of the delayline.

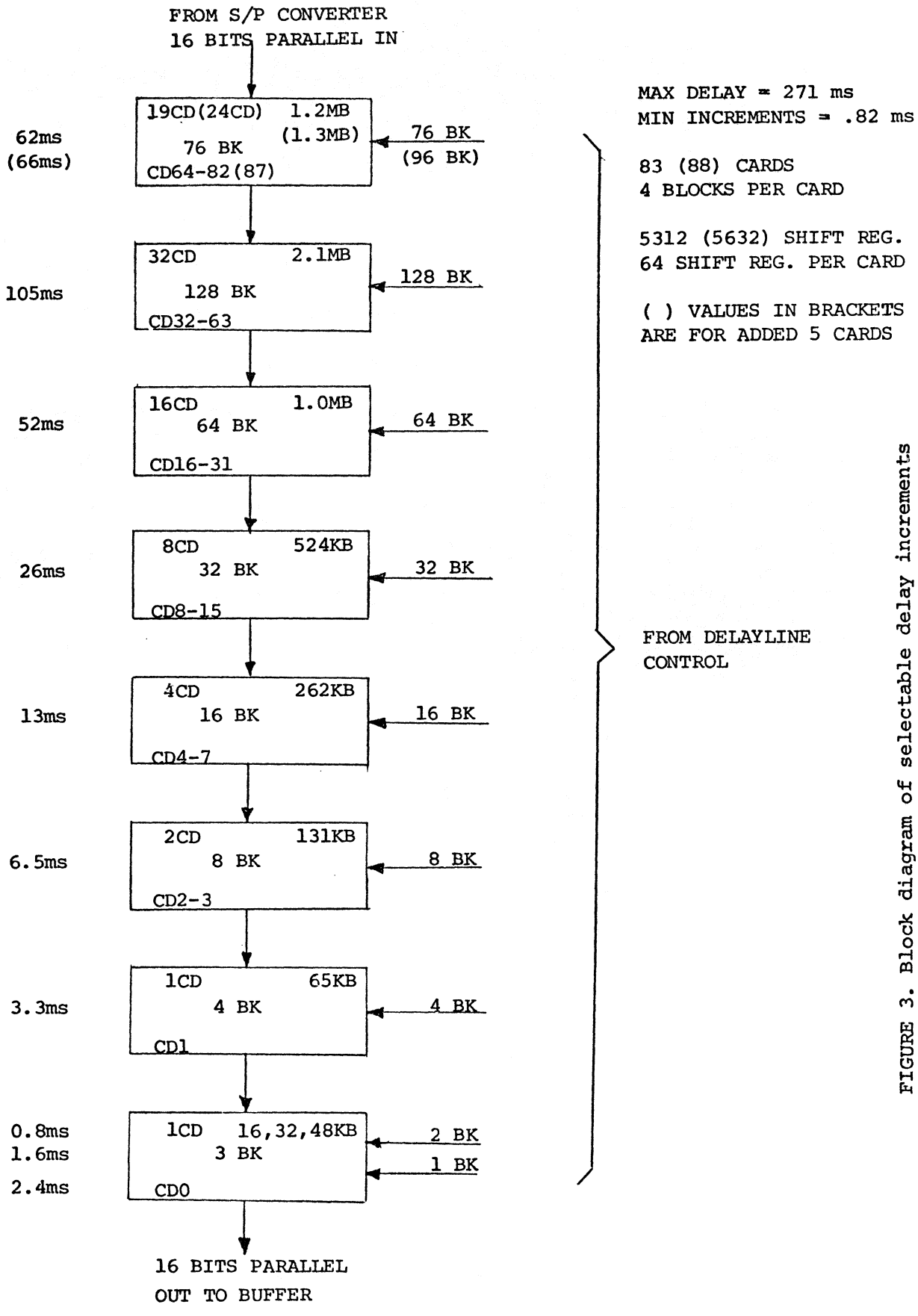


FIGURE 3. Block diagram of selectable delay increments

7. CORRELATOR

The correlator uses the NRAO Model III cards to provide 64 sin and 64 cosine channels. A total of eight printed circuit boards are used of which four are counter circuits and four are logic control modules. Each pair of boards contains thirty two channels. A delay of 0-3.2 milli-seconds is possible using a twenty mega bit data rate. The counters have a twenty-one bit capacity per channel allowing an overflow to occur after 104.8576 milli-seconds if the correlator is not read out by the computer and cleared.

Under computer control the correlator should accumulate data for approximately 104 milli-seconds or eight 13 milli-second interrupts. Then the computer should blank the correlator with CORBLK signal while the channels are readout and cleared. Only the sixteen most significant bits COROUT 0-15 of each channel are read out in parallel. The first channel is always available at the computer interface. Subsequent channels become available after each NXTWRD command by parallel shifting the data to the first channel until all of them have been readout. During the time the correlator is being readout all channels are being cleared, however, if not all the channels are read the correlator needs to be cleared by the CORCLR signal. During the execution of CORCLR the status bit CORBSY is set.

The correlator is readout in the following sequence:

Total count cosine
Total count sine
Channel 0-31 cosine
Channel 32-63 cosine
Channel 0-31 sine
Channel 32-63 sine

Control Signals

COROUT	Parallel 16 bit output of the most significant count in each channel of the correlator.
$\overline{\text{CTROVFL}}$	Signal that illuminates a red indicator on the panel if total count is integrated longer than 104 milliseconds. This condition occurs when correlation is not blanked during readout or NXTWRD is not requested.
NXTWRD	Signal generated in the computer to signal that the logic is ready to accept the COROUT 0-15 data.

8. TEST PATTERN GENERATOR OPERATION

Due to the large amount of circuitry involved with the delayline a selfcheck method was incorporated to assure the reliability of the equipment. A test pattern generator was designed to operate in three modes of testing. The three modes are LOCAL PSEUDO, REMOTE PSEUDO and CHECKERBOARD. On the display panel is a switch for selecting the test modes.
CHECKBOARD- in this mode a pattern of 32 one's followed by 32 zero's are repetively generated. This signal is internally tied to T DAT A and T DAT B with sync words superimposed on the T DAT B line. The test pattern is switched through the circuitry checking all the logic up to the Fringe Rotator. The two data lines are returned to the test generator where the signals are compared for errors. To isolate errors in the delayline each block of delay can be systematically switched in to determine if any specific block is causing errors. When using this mode the BITS DELAY switches should all be in the normal down position.

There are three indicator lamps and one digital readout associated with this circuit. The red "ON" lamp will illuminate when anyone of the test modes is selected. A green "OK" lamp and a red "ERROR" lamp monitor the data for accuracy. If no errors occur the "OK" lamp is fully illuminated and the "ERROR" lamp remains dark. As errors start to occur at a slow rate the "OK" lamp starts to dim and the "ERROR" lamp lights faintly. As the error rate increases the "OK" lamp completely darkens while the "ERROR" lamp fully illuminates. A six digit display is forced to readout the "CHKBD ERRORS/S" giving the operator the actual errors detected.

LOCAL PSEUDO- The pseudo generator provides two identical 255 bit data patterns. The patterns are generated by two eight bit shift registers with feedbacks selected for a given output signal. The output of the first generator is connected to T DAT A. At 1 SEC A pulse is also provided along with a 20 mega-hertz clock signal. The second generator has the capability of being delayed in time by the BITS DELAY switches a set amount of time from T 1SEC A. The second signal is connected to T DAT B line.

The T DAT B signal has three signals encoded in the data at timed intervals. First is the one second sync word which is 24 bits long, that occurs at the beginning of every one second interval. Second is the page sync word that is also 24 bits long and occurs 38 times per second at every 26.2144 milli-second after the initial one second sync. Third is the frame sync word which is also 24 bits and occurs every .8192 milli-seconds after the initial one second sync if it is not page sync time. There are a total of 1220 frames of data each of which contains 16,384 bits of data. After

the data there is a final frame (1221) followed by 11520 bits that are all set high. This period is a gap time provided to give the logic a window before the one second sync to enable initial latch up of timing circuitry.

The BITS DELAY switches in the test generator can be manually selected to simulate a delay as would be experienced with the satellite link. The Unload Control circuit will automatically compensate for this delay by enabling the equivalent delay to be set in the local data line. The data after being correlated is transferred to the computer where each channel can be checked to see if the correlator is working. By using the LOCAL PSEUDO test generator and the computer with the Deltest program all the electronics in the system can be checked.

REMOTE PSEUDO- The Remote Pseudo differs from the Local Pseudo with only one major change. That is the pseudo pattern that is connected to DAT B is actually being transmitted from the remote site via the satellite link. The data pattern from the remote site is identical to that produced in the test generator. By the use of the Deltest program in the computer and running a correlation the channels can be checked for accuracy of counts. A 100% correlation should be observed every 255 channels.

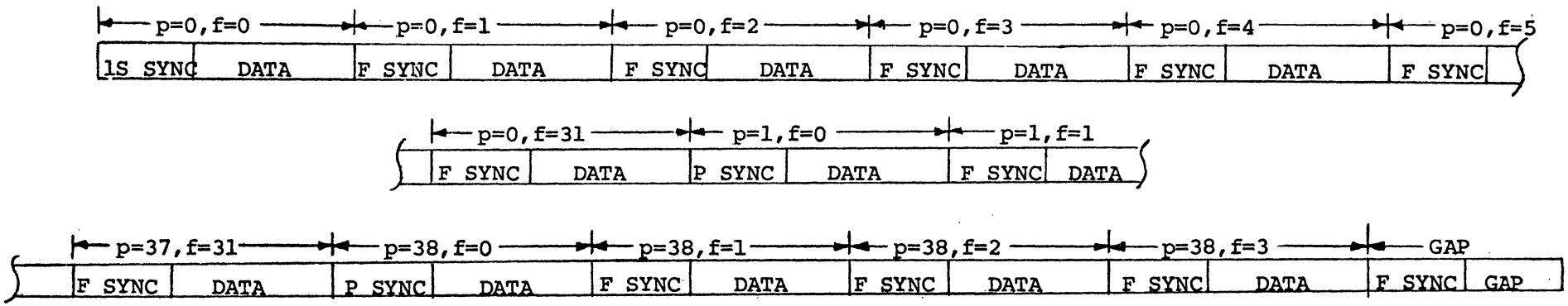
The delay between the two data streams can be checked by setting the "DELAY/us" switch on the panel to enable display of that function. The fringe rate can also be displayed by setting the same switch in the up position to indicate the "FRINGE RATE/HZ".

On page 16 is a diagram of the satellite link format and a break-down of the timing and bit counts.

FORMAT SATELLITE LINK

PAGE COUNT = p = 0-38

FRAME COUNT = f = 0-31



				1 FRAME = 1 BLOCK	
				1 FRAME = 2^{14} BITS	= 0.8192 ms
			1 BUFFCYCLE =	2 FRAMES = 2^{15} BITS	= 1.6384 ms
		1 INTRUPT =	8 BUFFCYCLE =	16 FRAMES = 2^{18} BITS	= 13.1072 ms
	1 PAGE =	2 INTRUPT =	16 BUFFCYCLE =	32 FRAMES = 2^{19} BITS	= 26.2144 ms
1 SEC INTVAL =	38p + 4f =	76 INTRUPT =	610 BUFFCYCLE =	1220 FRAMES	= 19.9 MBITS = 999.4240 ms
				GAP	= 11520 BITS = 0.5760 ms
				DATA	= 16360 BITS = 0.8180 ms
				SYNC	= 24 BITS = 0.0012 ms

FIGURE 4. FORMAT SATELLITE LINK

9. TOTAL COUNT, READOUT AND SERIAL/PARALLEL CONVERTER

The Serial to Parallel Converter circuit samples the local receiver by checking 1 SEC A, CLK A and DAT A. Each of the three lines is monitored for presence of signals. If no signal is present a corresponding alarm indicator is illuminated on the control panel. The test generator is connected through multiplexers to supply the same three signals mentioned above to enable an internal system check.

The local 20 mega bit datastream is clocked through shift registers to produce a 16 bit parallel output which is clocked out to the delayline every 800 nanoseconds. There are 1,250,000 of these 800 nanosecond cycles in a second. At the beginning of each second this 800 nanosecond cycle is synchronized by the local 1 SEC A timing signal.

The Total Count circuit counts the number of bits correlated and provides an output circuit from the correlator to the line drivers. If the count in the sine or cosine counters overflows an alarm indicator is illuminated on the control panel which is marked "OVERFLOW". This condition would occur if the correlator wasn't blanked during readout or computer failed to request the "NXTWRD". The output of the correlator is fed through the counter circuit under computer control by the "NXTWRD" command. The output of the correlator is marked "COROUT" 0-15 which are the 16 most significant bits of the counters. Each successive channel of the correlator is shifted to the readout station until all the data has been read. The "CORCLR" signal is used to clear the correlator during initialization or if only a partial readout was attempted. This command takes approximately 70 microseconds during which time the "CORBSY" signal is set.

10. UNLOAD CONTROL

The Unload Control contains a bit counter B and a sync window timing circuit to keep track of data from the satellite link. The bit counter uses the $\overline{1\ SEC\ B}$ to synchronize the counting logic. After the counter is initially locked up it can use either the next $\overline{1\ SEC\ B}$ or an internally decoded 1 second to resync the counter.

The sync circuit provides three timed windows to enable detection of a 1 second, page or a frame word. The windows are timed to occur 31 bits early and will continue for 32 bits after the expected decode time. This produces a window that is total of 63 bits long which will be reset as soon as the sync word is detected. While the window is being reset the bit counter is updated by setting the next higher bit in the counter. If the data from the link is lost, the counter will continue to open the 1 sec. window at the expected times for up to 8 seconds. At that time the Sync Detector will have to initialize itself again by seeking the gap time then the 1 second sync word. When the $\overline{1\ SEC\ B}$ is detected the counter will again be synchronized.

The $\overline{1\ SEC\ B}$ or decoded 1 second used to reset the bit counter is also connected to a line driver which ties into the computer as a 1 SIRPT signal. One other point is tapped off the counter that is BCB-17 which is also feed to the computer as the 13 MSIRPT signal.

The Unload Control will blank the correlator during the time the three sync words would be correlated or if the 1 second sync is missing during the complete 1 second period. If the page or frame is missing that time would also be blanked. Also the gap time is blanked when the bit count equals 19988480 until the one second is detected.

11. LOAD CONTROL

The Load Control sets the delayline and controls the Buffer storage. When the manual switch is set or CHKBD mode is selected the delay can be entered manually from the control panel switches. If the auto switch is set, the delay is calculated by determining the time difference between REF 1 SEC A from the Serial to Parallel Converter and 1 S UP from the Unload Pointer. In the AUTO mode the delay can be set to the least significant bit by using the Buffer delay. The delayline indicator drivers illuminate the corresponding lamps to the selected blocks of delayline circuitry.

The Buffer loading is controlled by a $\overline{\text{WRREQ}}$ that is generated every 800 nano seconds. When the write cycle is completed the Buffer generated a $\overline{\text{WRRES}}$ to the Loader to reset the $\overline{\text{WRREQ}}$. If the write request is not reset before the next $\overline{\text{WRREQ}}$ signal then both the BUFSTV and BUFOVF output lines to the computer are set indicating a memory write error. BUFOV is set when a delay is attempted that exceeds the capacity of the delayline. BUFSTV is set when the total delay is negative or less than 4096 bits (200 μs). If either bit is set a fatal error has occurred and bad data has been correlated. The correlator is blanked when these errors occur so the program is required to discard the bad data. These signals are set at the beginning of every one second cycle and can only be reset by the computer via the RESERR line. The correlator is blanked whenever a new delay is requested which may take from 0 to a maximum of 1.28 seconds.

12. BUFFER

The Buffer contains 32 static RAM's, with each having a capacity of 1024 bits. There are 16 input lines with each having two RAM's in series to store 2048 bits or a total of 16,384 bits for all 16 lines. It acts as a first in first out silo with delay of 800 nanoseconds to 1.6384 ms.

The load pointer sets the write location and steps sequentially thru all Buffer locations in sychronism with the delayline. The unload pointer sets the read location and sequentially follows the load pointer with a delay of 200 micro seconds to 1.63 milli seconds. The unload pointer is clocked by the 20 megabit clock from the satellite link. If the unload pointer advances to within 4000 bits of the load pointer an error bit BUFSTV is set. If the unload pointer runs behind until the load pointer advances to within 4000 bits of the unload pointer then BUFOVF is set. The computer needs to acknowledge the errors and reset the error flip-flop with RESERR. If a write error occurs then both the error bits BUFOVF and BUFSTV are set.

The unload pointer is controlled by the delay control circuit. The 1 second sync word 1 SEC B is decoded and compared with local 1 second word 1 SEC A. The difference is time represents the propagation delay thru the sattelite link. Added to this number is the geometric delay given to the delay control from the computer in a 20 bit (19 bits+sign) word, DLY 0-19 in two's complement format. A positive delay from the computer adds delay to the link which makes the delay through the system smaller. The computer may add up to $\pm$ 26.2144 milli-seconds of geometric delay including clock offset.

The systems delay needs to be updated periodically. Under the worst case condition (half way around the world on the equator) the update rate is 1 bit every 16.1 milli-seconds. Therefore an update at the 13 milli-second interupt period is sufficient.

13. FRINGE ROTATOR

The Fringe Rotator is a three level rotator having a maximum frequency of 62.5 kilo hertz with a resolution of 0.95 hertz. The three levels are high, low and transition periods are disregarded. The 62.5 kilo hertz frequency is present when bits FR 0-15 are all set to cause an overflow condition in the adder. This outputs a 1 mega hertz signal which is feed to a 16 bit divider to give a 62.5 kilo hertz rate. The resolution of 0.95 hertz is a result of setting FR 0.

The computer needs to supply 4 bits fringephase FP 0-3 and 16 bits magnitude of fringerate FR 0-15 plus the sign bit NEGFR. Fringe phase is interpreted as the output of a 4 bit counter counting from 0 degrees to 360 degrees in 16 increments, each increment representing 22.5 degrees. The fringe rate is loaded at the 13 MSIRPT time along with the fringe phase. If the new fringe data is not present on the data line whatever is present will be loaded. The NEGFR is loaded when a transition is made from positive to a negative rate.

14. DISPLAY

There are three miscellaneous circuits wired on the Display board because of the small amount of logic required for each. The three circuits are the control logic for the green decimal display, the power monitor and a comparator that test for $\overline{\text{NEWDLY}}$.

The digital display can monitor the Fringe Rate or the Delay with an accuracy of $\pm$1 the least significant digit. Whenever the CHKBD mode is selected the display will always readout the checkerboard error rate. The displya has 6 digits plus a sign to indicate negative Fringe Rate when the computer outputs a negative rate.

The delay comparator test the $\overline{\text{DLYR}}$ 0-19 that is currently in the system against that on the computer input lines DLY 0-19. If the two delays are equal no update is required but if they are not equal a $\overline{\text{NEWDLY}}$ signal is generated to enable the delay to be updated.

A voltage monitor is used to indicate if the voltage supplies are functioning properly. Each of the three chassis contain a similar circuit with a signal looping through them and returning to the CORRELATOR-BUFFER-DELAY 0. If anyone of the monitors detects a power fault or a missing clock it will cause the POWER FAULT lamp to be illuminated. As long +5V is supplied to the chassis the green POWER ON lamp will remain illuminated.

SUMMARY

The following Figure 5 shows a complete block diagram of the VLBI Satellite Delayline. The computer I/O lines are all TTL logic levels. Signetics 8T13 line drivers are used to drive the output signals to the computer requiring a 100 ohm load termination. The input data and timing pulses from the local clipper and satellite link are terminated into 50 ohm loads. Input lines from the computer terminated with 100 ohms. The 1 SEC A should be a positive going pulse of >50 nsec.

At each observing site a 20 MHz signal is generated from the local frequency standard to clock the data. Because of doppler shifts in the Satellite link the system was designed to work within 17.5 MHz to 22.8 MHz. To align the two data streams, remote CLK B is used to read DAT A out of the buffer whereas local CLK A writes DAT A into the buffer.

In the delay system there are inherent delays which are necessary for data processing. Due to these delays C DAT A is delayed 45 bits with respect to C DAT B at channel one of the correlator. In the correlator there are a total of 64 sine and 64 cosine channels. To center the correlation function at channel 32 requires a delay of 77 bits be subtracted from the calculated geometric delay.

An overall system delay of approximately 200 μsec to 273 msec was determined to be sufficent to compensate for the satellite link. The computer can set a delay that varies with the least significant bit or one clock pulse which is 50 nsec. If a delay is set which exceeds the buffer capacity an error bit BUFOVF is set. If the delay decreases to less than 200 μsec an error bit BUFSTU is set.

The fringe rotator is a three level digital mixer having a maximum frequency of .95 Hz. The computer needs to update the fringe phase and magnitude of fringe rate at every 13 msec interrupt. The fringe phase is a 4 bit binary number with the last significant bit representing 22.5°.

The correlator when used at a 20 megabit data rate will give a delay of from 0 to 3.2 μsec. The total count sine and cosine channels count the number of bits correlated. Under computer control the correlator is read out every 104 msec (8-13 msec interrupts) during which time the correlator is blanked. The read-out time is a function of the computer program cycle. The correlator can be cleared without reading out the data, by setting the CORCLR bit from the computer. The execution of this cycle will take approximately 70 μsec.

The DAT B is made up of blocks of data of which are preceded by sync words. Every 1 second the DAT B is synchronized with a 24 bit sync word which is encoded on the data stream. The 1 second sync word is preceded by a gap of all one's which is used initially to set up the sync detector to search for the word. After the 1 second search mode has been aborted an internal clock provides windows that open at the appropriate times to allow the sync words to be detected. Beside the 1 second there are page and frame sync words which are shown in Figure 6. If during any of the sync windows no sync words are decoded the correlator is blanked. If the 1 second sync word is not detected the window continues to open for 7 consecutive one second periods before the sync detector returns to the initial search cycle.

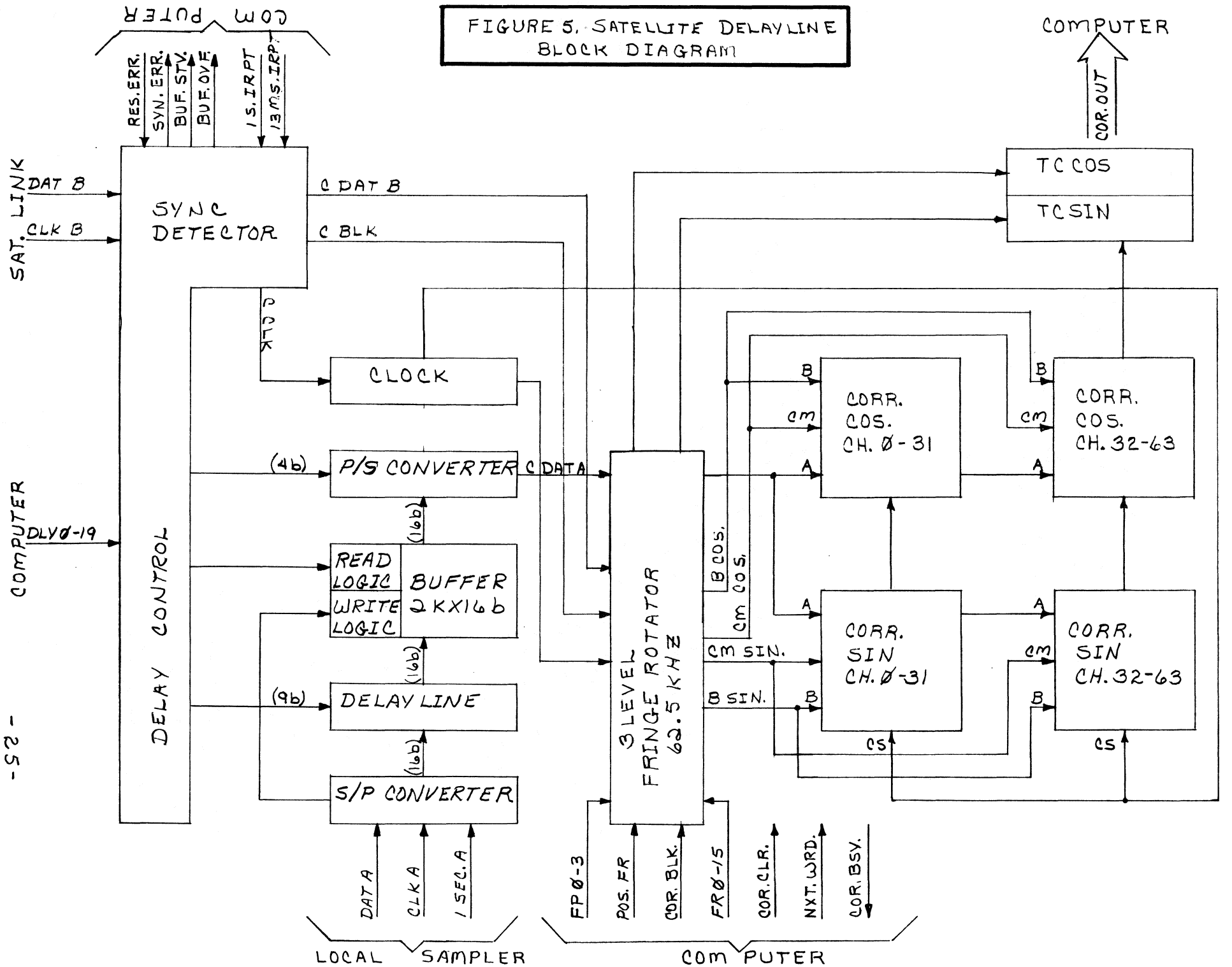


FIGURE 5. SATELLITE DELAYLINE BLOCK DIAGRAM
COMPUTER
COR. OUT
RES. ERR.
SYN. ERR.
BUF. STV.
BUF. OVF.
1 S. IRPT
13 M.S. IRPT
COMPUTER
SAT. LINK
DAT B
CLK B
SYNC DETECTOR
C DAT B
C BLK
C CLK
TC COS
TC SIN
CLOCK
DELAY CONTROL
COMPUTER
DLY Ø-19
(4b)
P/S CONVERTER
C DATA
(16b)
READ LOGIC
WRITE LOGIC
BUFFER 2 KX16b
(16b)
(9b)
DELAY LINE
(16b)
S/P CONVERTER
3 LEVEL FRINGE ROTATOR 62.5 KHZ
B COS.
CM COS.
CM SIN.
B SIN.
B
CM
A
CORR. COS. CH. Ø - 31
CORR. COS. CH. 32-63
CORR. SIN CH. Ø-31
CORR. SIN CH. 32-63
CS
DAT A
CLK A
1 SEC. A
LOCAL SAMPLER
FP Ø-3
POS. FR
COR. BLK.
FR Ø-15
COR. CLR.
NXT. WRD.
COR. BSY.
COMPUTER

BOF	XX XX11 1100	Beginning of frame
BOP	XX XX11 0011	Beginning of page
BOS	XX XX00 1111	Beginning of second
EOSY	XX 0000 0001	End of sync
BOSY	01 0101 1111	Beginning of sync

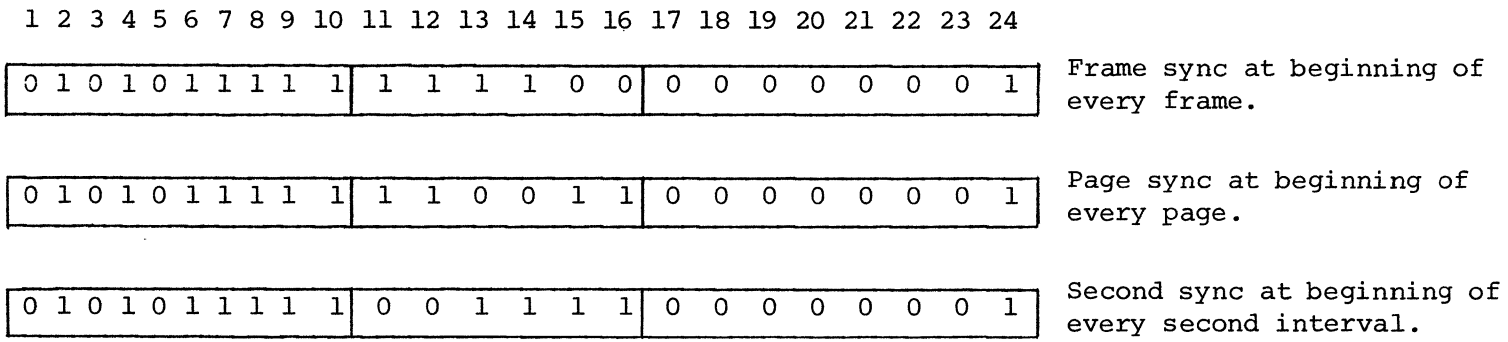


FIGURE 6. SYNC WORD FORMAT