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300-FT TELESCOPE H-316 COMPUTER INTERFACE

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## 300-FT TELESCOPE H-316 COMPUTER INTERFACE

Dwayne Schiebel

### 1. Introduction

This report describes the interface necessary to install the H-316 computer at the 300-ft telescope. This interface was installed in a modified "Shalloway" chassis which is mounted above the 316 computer.

### 2. Programming

#### Card Reader

A documentation M300 card reader was installed on the 316 computer. This card reader reads a maximum of 300 cards per minute.

#### OCP 105 - read one binary card:

This command will cause the card reader to feed one card.

#### SKS 005 - skip if card reader is ready:

This command will skip, if the card reader is ready to send a column of data to the computer. The card reader will be left in a ready state if all 80 columns are not read.

#### SKS 105 - skip if card reader not busy:

This command will skip if the card reader is not busy. The card reader will be busy for about 170 msec during one card read.

#### SKS 305 - skip if card reader operational:

This command will skip if the card reader is operational. The following four conditions will make the card reader not operational:

1. Error

An error is an indication of a failure of the light or dark check.

- a. Dark check: Usually the card has a tear at the leading or trailing edge.
- b. Light check: This is caused by an emitter sensor failure.

2. Hopper check

This indicates that either the input hopper is empty or the output stacker is full.

3. Motion check

This indicates that there was a pick check or a stack check.

4. Not ready

Ready indicates the following has occurred:

- a. Power on + 3 sec delay is over.
- b. Input hopper has been loaded.
- c. Reset button has been pressed.

INA 005 - input from card reader if ready:

Data is ORed into the A register if the card reader is ready.

Data is input into the A register as shown below:

Row	12	11	0	1	2	3	4	5	6	7	8	9
A Reg. Bit	5	6	7	8	9	10	11	12	13	14	15	16

INA 1C05 - input from the card reader if ready.

This command is the same as INA 005 except the A register is cleared before the data is transferred.

INTERRUPTS - The card reader is connected to interrupt line 8, memory location 73<sub>8</sub>. An interrupt should occur every time data is available. The first should be 26.6 msec after an OCP 105. The other interrupts should occur every 870 μsec. The computer must take the data in this time or it will be lost.

DMV Input

OCP 50 - This OCP must be executed before doing 4 INA's.

INA 1050 - Do four INA's to read all four digital voltmeters. The input number will be binary 15 bits (bit 16 not used). Bit 1 will be sign (a one = minus); bits 2-15 will be the binary number. This binary number will be the same for plus and minus except for sign.

The four words read in will represent the following:

1. Sterling mount or traveling feed.
2. Rotation.
3. Focus.
4. Spare.

Encoder

OCP 150 - Do this OCP before doing two INA 1150's.

INA 1150 - Doing two INA's will read in the encoder reading. The contents of the two words is listed below.

Bit	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16
First Word	80 40 20 10	8 4 2 1	80 40 20 10	8 4 2 1
	Degree	Degree	Minute	Minute
Second Word	80 40 20 10 Second			S 1 = + I G N

### Telescope Control

OTA 250 - This OTA has the same bit structure as OTA 1070 did in the 116 computer. (See Electronics Division Internal Report No. 110.)

### Drive System Status

INA 1350 - This INA will input the telescope drive system status; its format is listed below.

- Bit 1 - North Back Up Limit
- 2 - North Limit
- 3 - South Back Up Limit
- 4 - South Limit
- 5 - Computer/Manual Declination
- 6 - Feed/Mount Hour Angle
- 7 - Computer/Manual Hour Angle
- 8 - Computer/Manual Rotation
- 9 - Computer/Manual Focus

- Notes:
1. For limits exceeded input bit is a "0".
  2. Computer/manual bit is a "0" when in computer.
  3. Feed/mount bit is a "0" when in tracking feed mode.

### 316-116 Link

Commands for both computers.

OCP 001 - Set transmit channel in output mode.

OCP 101 - Reset transmit channel from output mode.

OCP 201 - Set receive channel in input mode.

OCP 301 - Reset receive channel from input mode.

OCP 401 - Resets transmit from output mode, resets the other computer from its receive mode, and interrupts the other computer.

316-116 Link (continued):

116 DMC channels: 2 = Transmit = Locations 12 and 13  
3 = Receive = Locations 14 and 15  
316 DMC channels: 2 = Transmit = Locations 22 and 23  
3 = Receive = Locations 24 and 25  
116 Interrupt lines: 10 - 316 OCP 401 = Location 41  
11 = Transmit End of Range = Location 42  
12 = Receive End of Range = Location 43  
316 interrupt lines: 2 = 116 OCP 401 = Location 65  
3 = Transmit End of Range = Location 66  
4 = Receive End of Range = Location 67

3. Diagnostic Aid

A display of the I/O bus is provided on the front panel of the interface chassis above the 316 computer. Any input or output transfer of the 316 can be displayed by a number selected on a digi switch. This display can be updated in three conditions as listed below:

1. With toggle switch in normal position the display will be updated every time a transfer is made.
2. With toggle switch in normal position, the hold pushbutton can be pressed and the last transfer before the button was pressed will be displayed.
3. With the toggle switch in single, the display will update once after the arm pushbutton is pressed. An arm indicator will light and then go out when the display is updated. This arm indicator can also be used when the toggle switch is in the normal position to indicate when the display has been updated.

#### 4. Card Reader Interface

All of the card reader interface is contained on one card located in slot 1. The card reader address is decoded on this card. When an OCP 105 is issued, the pick flip-flop (chip 13, pin 9) is set. When an index mark from the card reader is received, the pick flip-flop is reset and the ready indication is set (13-6). This index mark also sets data into a buffer (chips 9, 10 and 11) and interrupts the computer on line 8. When the computer does an INA, the ready indication is reset. The interface will again be ready when the next index mark is received. One index mark is received for each column on the card.

#### 5. Digital Voltmeter Interface

Interface for the digital voltmeters are contained on two cards. One card, "DVM Multiplexer Control", is located in slot 2 of the interface chassis; the other card, "DVM Multiplexer BCD-Binary Converter", is located in the operator's console.

DVM Multiplexer Control. All of the addresses (except for card reader and DMC link) are decoded on this card. The address for the digital voltmeters is 50. An OCP 50 will reset a two bit counter (chip 12). This counter is used to control a four position switch on the "DVM Multiplexer BCD-Binary Converter" card. The data from the multiplexer gated with "AD050+A/B" is applied to the input bus. When the computer takes the data the counter is incremented once and the switch is moved to its next position.

DVM Multiplexer BCD-Binary Converter. A sixteen pole, four position switch is controlled by the counter previously discussed. This switch will connect one DVM after another to a BCD-binary converter. This converter (74184) converts BCD data to binary data. Another



two pole, four position switch switches conversion period and the sign bit from the DVM's. The conversion period signal is used to prevent the computer from taking data while the DVM is converting. This is done by triggering a 5  $\mu$ sec one shot with conversion period. This one shot will then inhibit the DRL line for 5  $\mu$ sec. A test plug has been built to plug into the spare DVM connector. This test plug has two positions which can be selected by a switch. The BCD word and the corresponding computer word is listed below:

<u>BCD</u>	<u>Computer</u>
9 9 9 9	0 2 3 4 1 7
-6 3 8 4	1 1 4 3 6 0

#### 6. Limit Switch/Control Mode/Markers

The card located in slot 3 is used to input the limit switches and control mode by an INA 1350. This address AD 350 gated with the limit switch or control mode switch is applied to the input bus.

There are two marker circuits. One circuit gives a mark every time the 1's of minutes is equal to zero. The other marker is a combination of two markers. One mark is when 10's of minutes is equal to zero. The other mark is when 10's of degrees is equal to zero and 20 and 30 minutes are on. The two markers are selected by a switch on the operator's console.

#### 7. Encoder Board 1

This card, located in slot 4, is used to level convert the encoder signals to TTL levels (8820), then store the data in a buffer (77174) and convert from gray to binary (7486). The gray to binary conversion is the standard exclusive or configuration.

7. Continued:

This card also contains a driver to light a "LED" to indicate if the east or west encoder is connected. This east or west indication also decides if the sign bit will be inverted or not.

8. Encoder Board 2

This card, located in slot 5, converts the binary number from encoder board 1 to data usable by the computer. It also generates an encoder strobe, a latch signal for the buffers, and interrupts the computer when encoder data is available.

The data from board 1 is BCD excess 3 or excess 1 as shows below:

10's degrees	Excess 3
1's degrees	Excess 3
10's minutes	Excess 1
1's minutes	Excess 3
10's seconds	Excess 1

Therefore, this data must have either three or one subtracted from it. This is accomplished by doing a 2's complement and add (7483). The data from the adders is gated with either the first or second AD 150 to apply data to the input bus. Data from the adders also drive the local readouts on the console.

The timing for the encoder strobe, buffer latch, and interrupt is controlled by a 10 Hz clock from the timing generator.

9. I/O Display

As a diagnostic aid it is possible to display data that the computer has input or data that was output by the computer. The logic for this display is located in slot 6.

A digi-switch is used to select which device is displayed. This digi-switch controls four data selector/multiplexers (74151). Two of the multiplexers

9. Continued:

select which decoded address will be gated with RRLIN to strobe data into a 16 bit shift register (74157). The other two multiplexers control what will be loaded into the shift register. After this data is loaded into the shift register, the data is serially shifted to the front panel display. This data will be inverted or not inverted, depending on whether the INB or OTB is selected.

10. 316 Receiver

The 316 receiver is located in slot 7. This card decodes all addresses used in the 116-316 computer link.

To receive data the 316 must issue an OCP 201. This sets the receiver in the input mode. When the 116 sends "116 Ready" after a delay of 75  $\mu$ sec, the 316 will do a DMC input transfer. When this transfer is complete, a "Set 116 DIL" is sent back to the 116. When the 116 completes another DMC output transfer, it again sends a "116 Ready" to the 316 and the cycle is repeated. This process repeats until the 316 DMC receive channel has reached its "End of Range". When this happens, the receiver is reset from its input mode and the computer is interrupted on line 4. This input mode can also be reset by the 116, doing an OCP 401, or by pressing "Master Clear" on the 316. This OCP 401 will also interrupt the 316 on line 2.

11. 316 DMC Out

The 316 DMC out card is located in slot 8. This card transfers data from the 316 to the 116. To initiate a transfer the 316 must do an OCP 001. This OCP will set the transmitter in the output mode and cause the DMC transmit channel to output a word and set "316 Ready". When the 116 receives this ready condition, it will take the data and reply with "RESET 316 READY". This "RESET 316 READY" will cause the 316 DMC transmit channel to output another word and

11. Continued:

the cycle is repeated. This will continue until the transmit channel has reached its "End of Range". This will reset the transmitter from the output mode and interrupt the 316 on line 3. This output mode can also be reset by the 316 doing an OCP 401 or pressing "Master Clear" on the 316. The OCP 401 will also interrupt the 116 computer on line 10 and reset the 116 receiver from its input mode.

12. Telescope Control

The logic necessary to control the telescope is located in slot 9. By doing an OTA 250, data is stored in a buffer which is connected to the "Digital Control Interface Box" (reference EDIR #110). This "Digital Control Interface Box" was previously driven by the DDP-116. To change to different logic levels, the following changes had to be made:

1. The level conversion was accomplished in this interface box by using 8820's, slicing at about -3 volts. The 8820's will now slice at about +2 volts.
2. A 500 pF capacitor was removed from pin 5 of chip MM on "Computer Interface Card #1" (reference schematic 6, EDIR #110).
3. The Dec Comp/Man signal went directly to the DDP-116. This signal had to be rerouted via J7/J9 of the "Interface Box" to the H-316.

13. 100 Hz Interrupt, Strobe Amplifier, -3 V DC Regulator

The printed circuit card located in slot 10 is used for three functions. These three functions are listed below:

13. Continued:

1. 100 Hz Interrupt. The timing generator 100 Hz is level converted and connected to interrupt line 1 of the 316.
2. Strobe Amplifier. The strobe signal generated on encoder board 2 (slot 5) is amplified to drive the encoder.
3. -3 V DC Regulator. All level conversion in the 316 interface requires -3 V DC. This is provided by the three volt regulator.

14. 116 Receiver

The 116 receiver located in slot 3 of the level conversion system of the 116 is identical to the 316 receiver except for signal names.

15. 116 Transmitter

The 116 transmitter is located in slot 4 of the level conversion system in the 116.

To set the transmitter in the output mode, the computer must execute an OCP 001. This OCP 001 will also generate a DIL 02 to the 116. When the 116 transfers a word of data, this data is stored, DIL 02 is reset, and "116 READY" is sent to the 316. When the 316 takes the data, it replies with "RESET 116 READY" (DAL 03) and "SET 116 DIL" (DAL 03 · RRLIN). When the 116 receives "RESET 116 READY", the "116 READY" condition is reset. Upon receipt of "SET 116 DIL", another DIL 02 is set and the process continues until end of range is reached. When this happens, the transmitter is reset from its output mode. The output mode can also be reset by master clear or the 116 doing an OCP 401. This OCP 401 will also reset the 316 receiver from its input mode.

The 116 transmitter also contains all three interrupts used by the DMC link. The three interrupts and their use is listed below:

1. P1L 10 — interrupts when the 316 does an OCP 401.
2. P1L 11 — interrupts when the 116 transmitter has reached its end of range.
3. P1L 12 — interrupts when the 116 receiver has reached its end of range.

#### 16. DMC Link Interconnecting Signals

Reset 116 Ready. This signal is used to reset the 116 ready flip-flop.

It is generated in the 316 by DAL 03.

Set 116 DIL. This signal is used to set DIL 02 in the 116. It is generated by DAL 03 · RRLIN in the 316.

Reset 316 Ready. This signal is used to reset the 316 ready condition and set DIL 02. It is generated in the 116 by DAL 03 · RRL.

116 OCP 401. This signal interrupts the 316 on interrupt line 2 and resets the 316 receiver from its input mode. The 116 transmitter will also be reset from its output mode. This signal is generated by the 116 doing an OCP 401.

316 OCP 401. This signal interrupts the 116 on interrupt line 10 and resets the 116 receiver from its input mode. The 316 transmitter will also be reset from its output mode. This signal is generated by the 316 doing an OCP 401.

116 Ready. This signal is used to inform the 316 that the 116 has data ready. It is generated by DAL 02 · OTP.

316 Ready. This signal informs the 116 that the 316 has data ready. It is generated by DAL 02 · RRLIN.

D Data Out 1-16. Output data from a computer to the other computer.

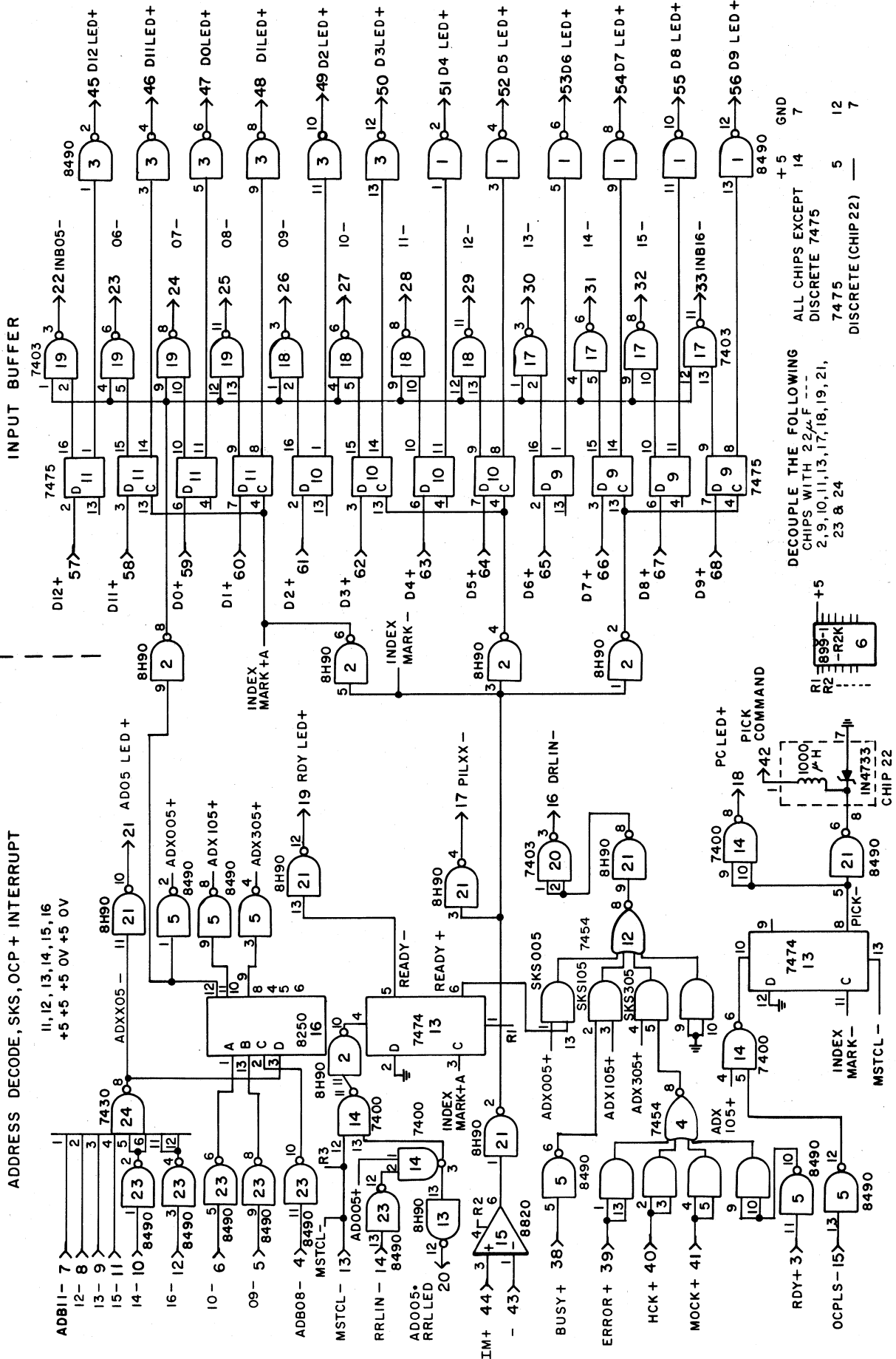
D Data In 1-16. Data that is received by a computer from the other computer.

17. Connector List

- J1 H-316
- J2 Card Reader
- J3 DVM Multiplexer BCD-Binary Converter
- J4 Digital Control Interface Box
- J5 Encoder
- J6 Encoder Display
- J7 116 Computer
- J8 116 Computer
- J9 10 Hz, 100 Hz from Timing Generator
- J10 Special, for Encoder Test Box

18. Credits

Credit should be given to George Patton for design of the encoder boards, limit switch/control mode/markers, and 100 Hz interrupt card. Credit should also be given to Doreen Morris, R. Skaggs, J. Turner, W. Vrable, and the Green Bank Machine Shop for their help in constructing this system.



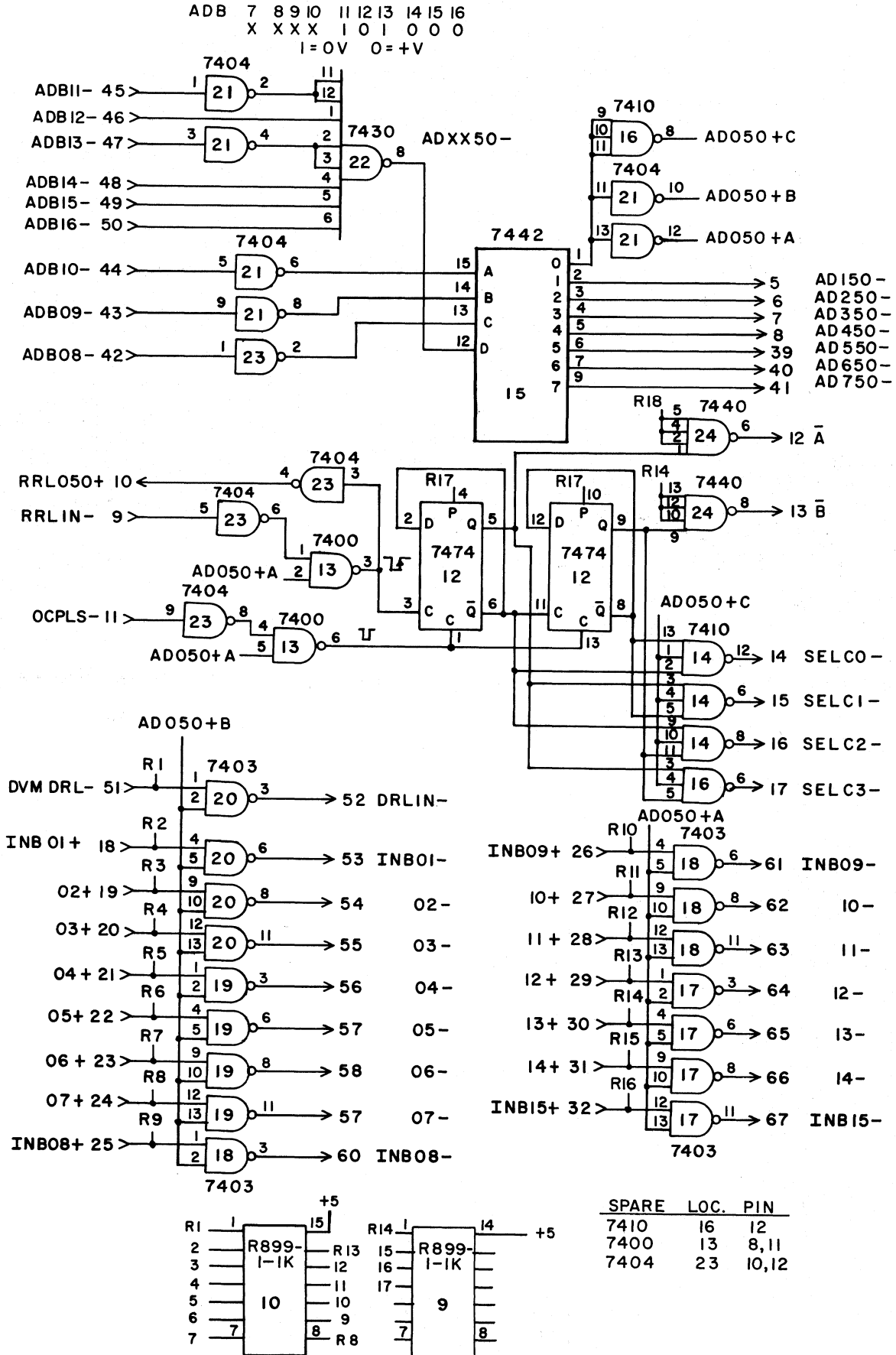
ADDRESS DECODE, SKS, OCP + INTERRUPT

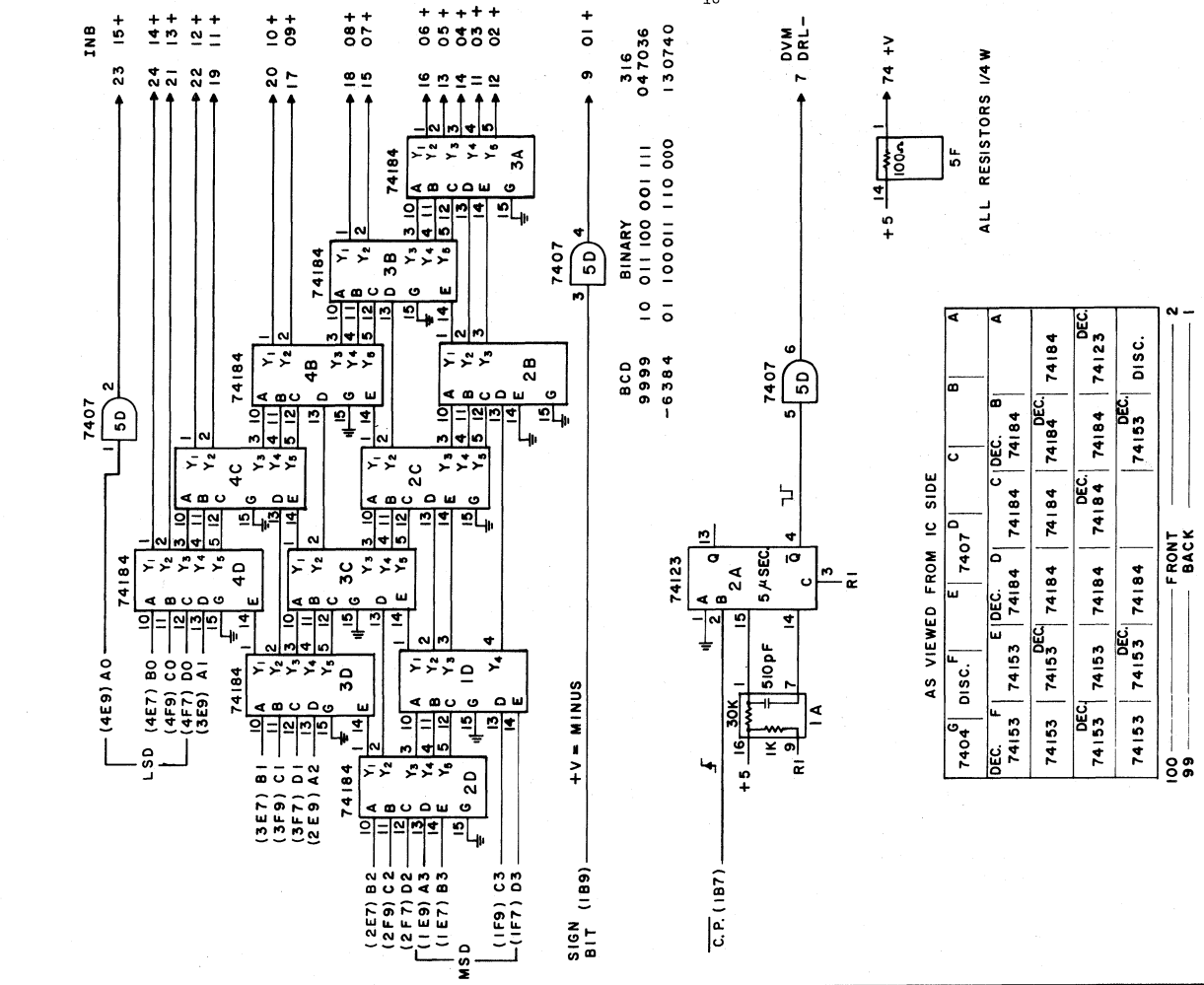
INPUT BUFFER

DECOUPE THE FOLLOWING  
CHIPS WITH 22µF ---  
2, 9, 10, 11, 13, 17, 18, 19, 21,  
23 & 24

CARD READER INTERFACE FOR H316 316 SLOT-1







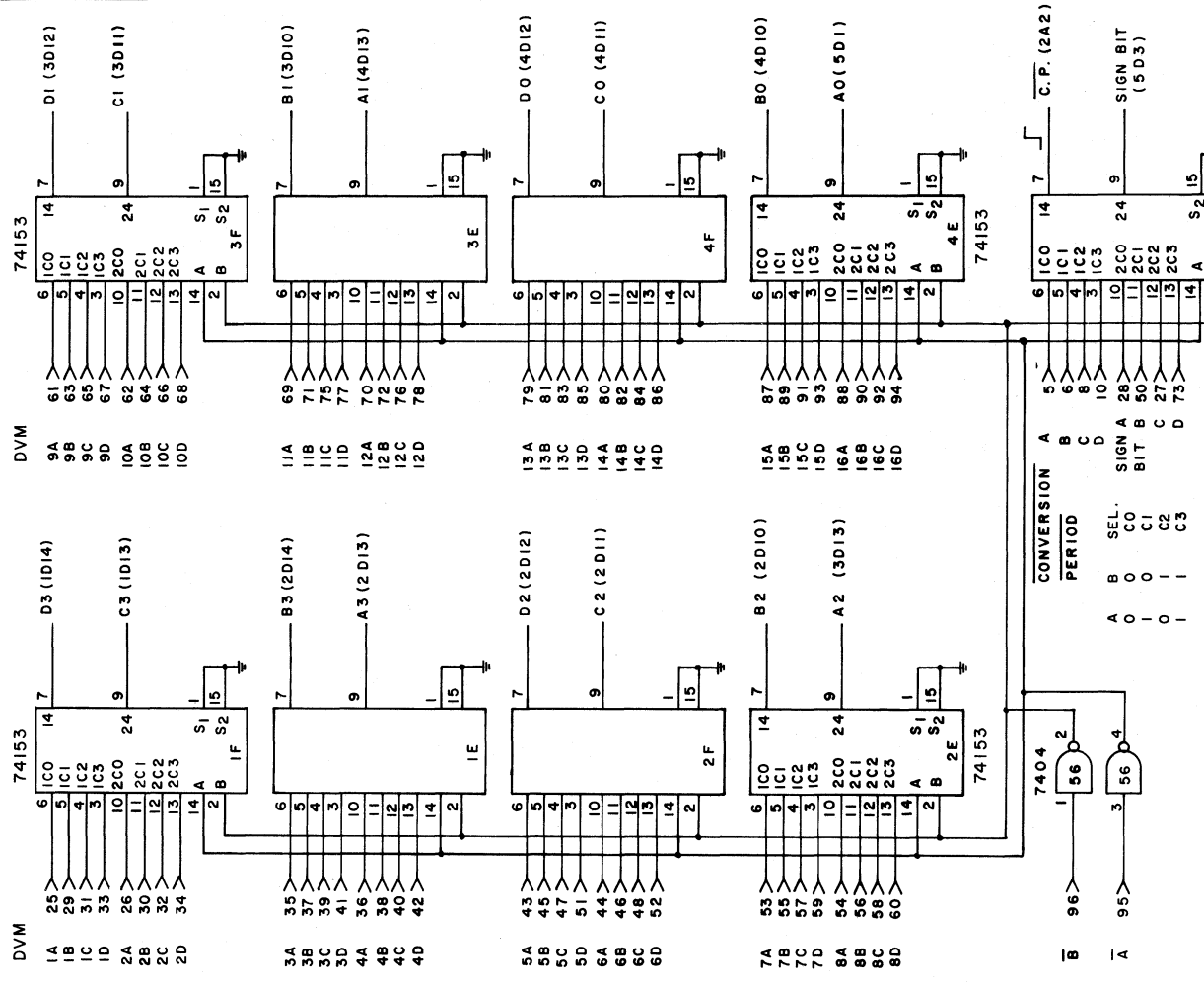
(4E9) A0  
 LSD (4E7) B0  
 (4F9) C0  
 (4F7) D0  
 (3E9) A1  
 (3E7) B1  
 (3F9) C1  
 (3F7) D1  
 (2E9) A2  
 (2E7) B2  
 (2F9) C2  
 (2F7) D2  
 (1E9) A3  
 (1E7) B3  
 (1F9) C3  
 (1F7) D3  
 MSD

7407 5D 2  
 7407 5D 4  
 7407 5D 6  
 7407 5D 8

+V = MINUS  
 SIGN (1B9)  
 BIT (1B7)  
 BINARY  
 BCD  
 9999 10 011 100 001 111  
 -6384 01 100011 110 000  
 316  
 047036  
 130740

+5  
 100Ω  
 5F  
 74  
 +V

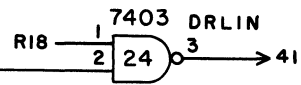
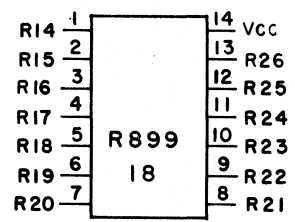
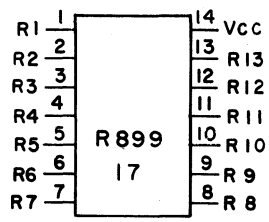
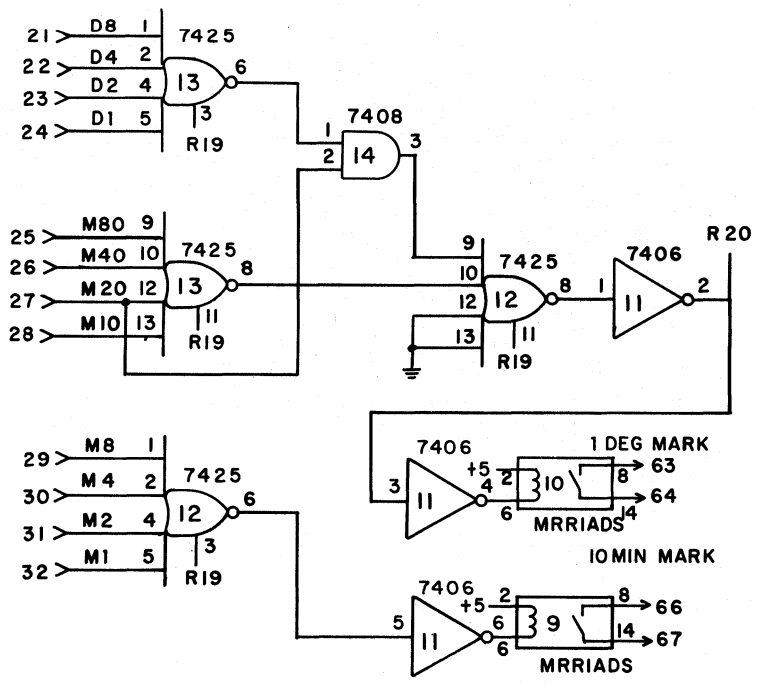
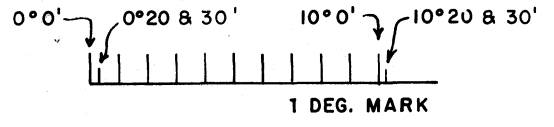
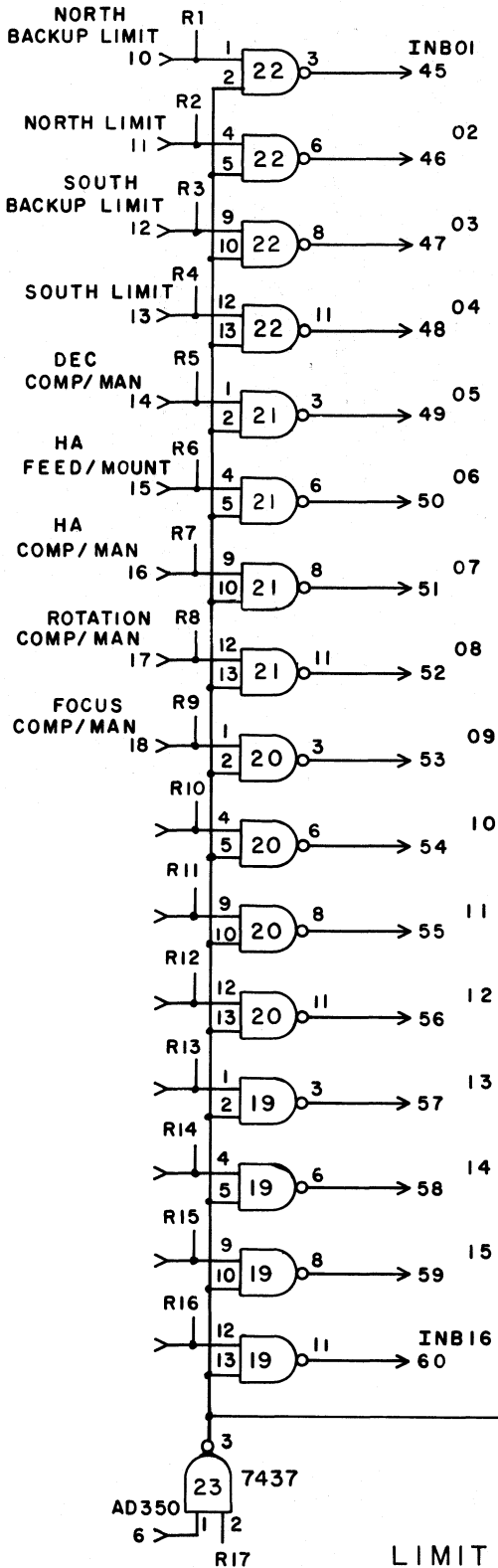
ALL RESISTORS 1/4W

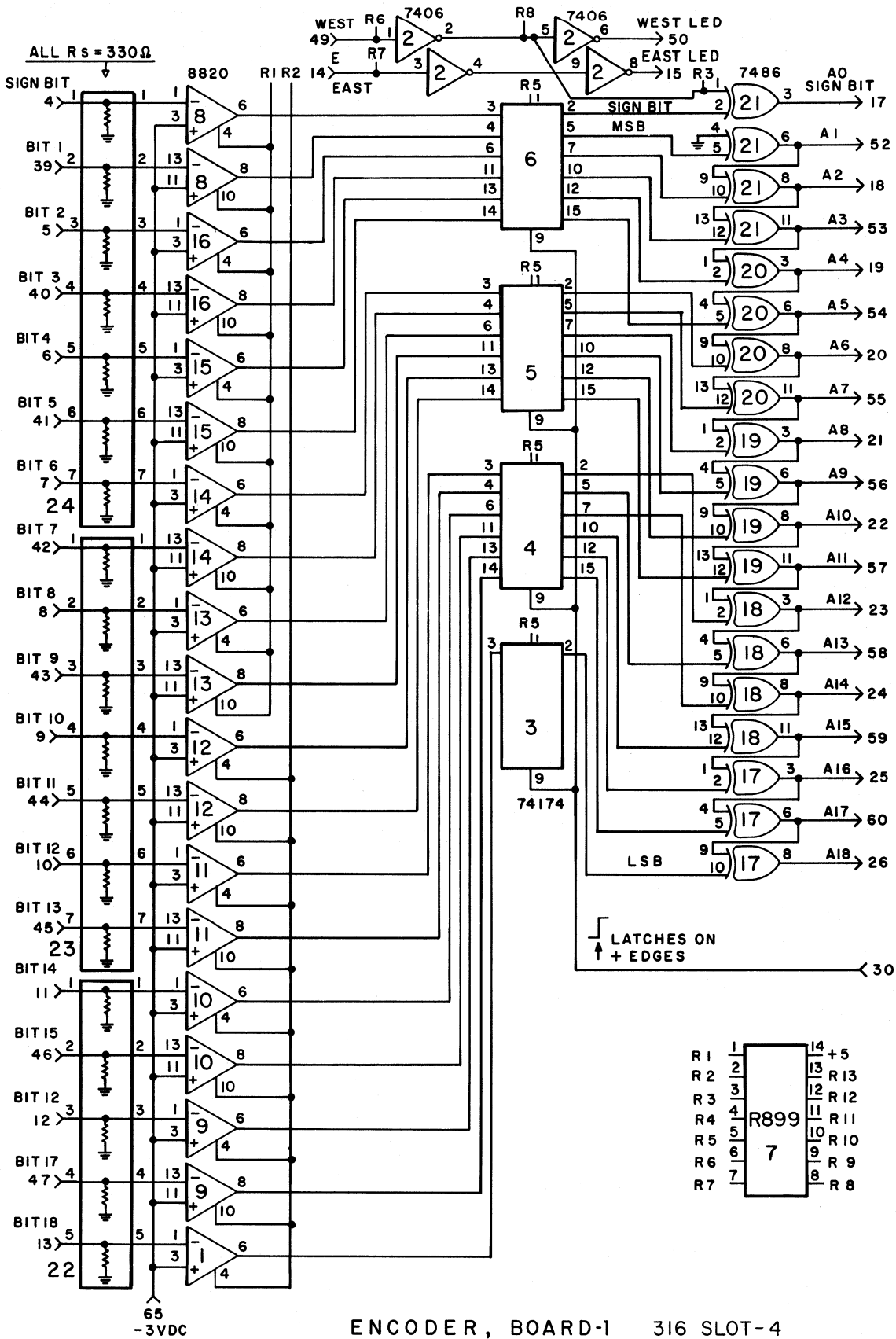


DEC. = DECOUPLE WITH .019μF  
 +5 = PINS 2, 4, 98, 100  
 GND = PINS 1, 3, 27, 49, 50, 73, 97, 99

DVM MULTIPLEXER BCD - BINARY CONVERTER PAGE 2 OF 2

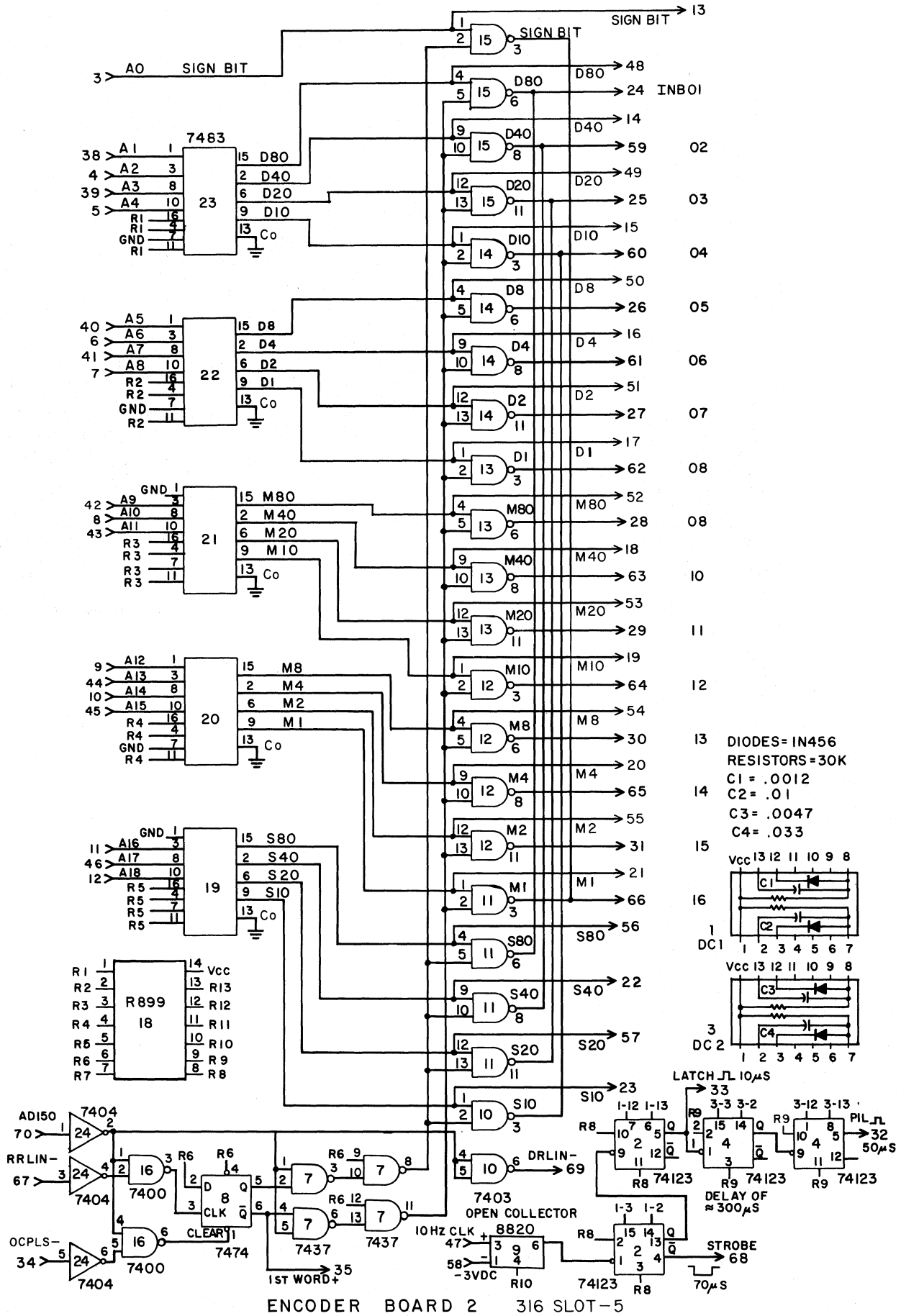
LOCATED IN CONSOLE

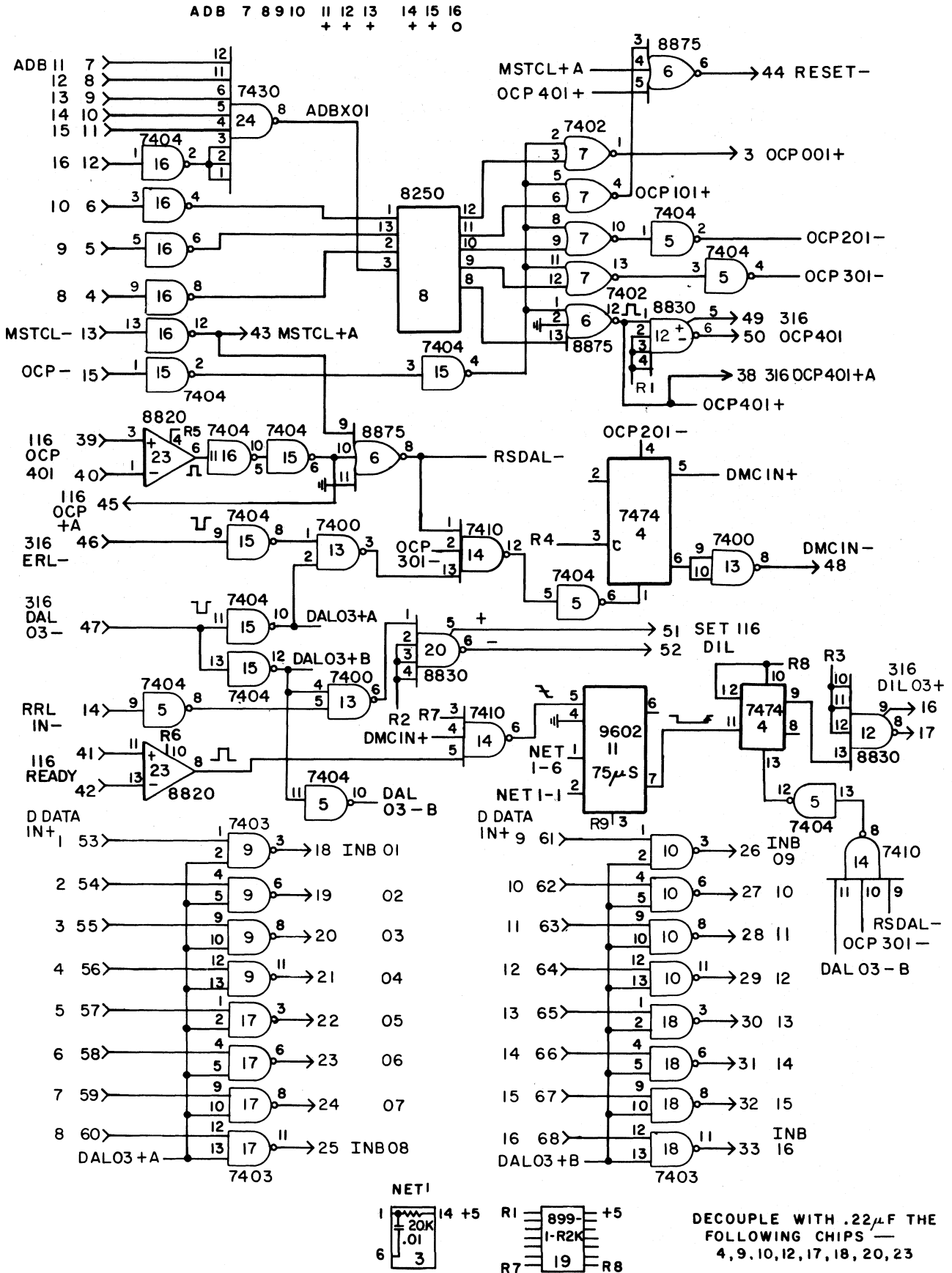




ENCODER, BOARD-1

316 SLOT-4

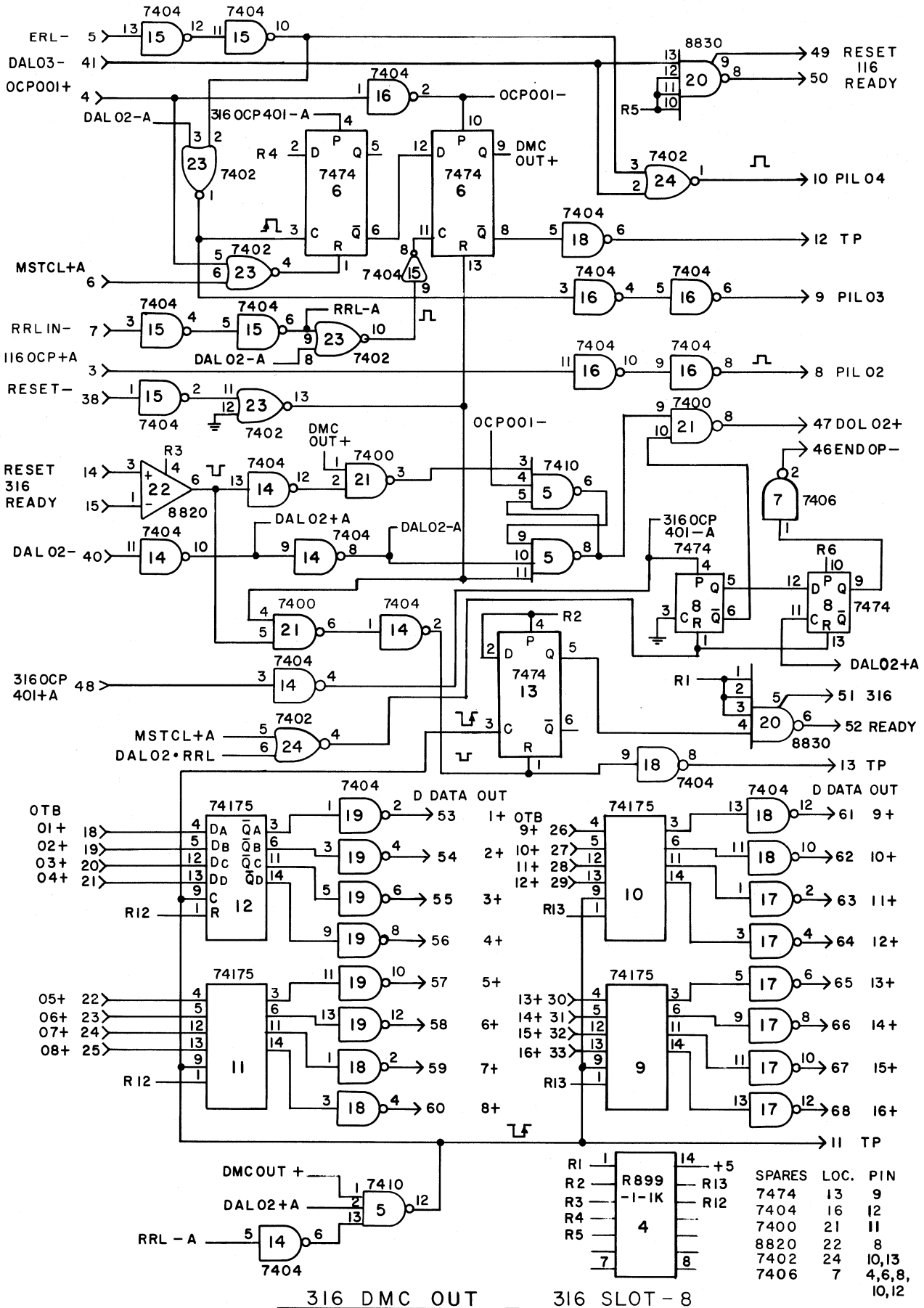


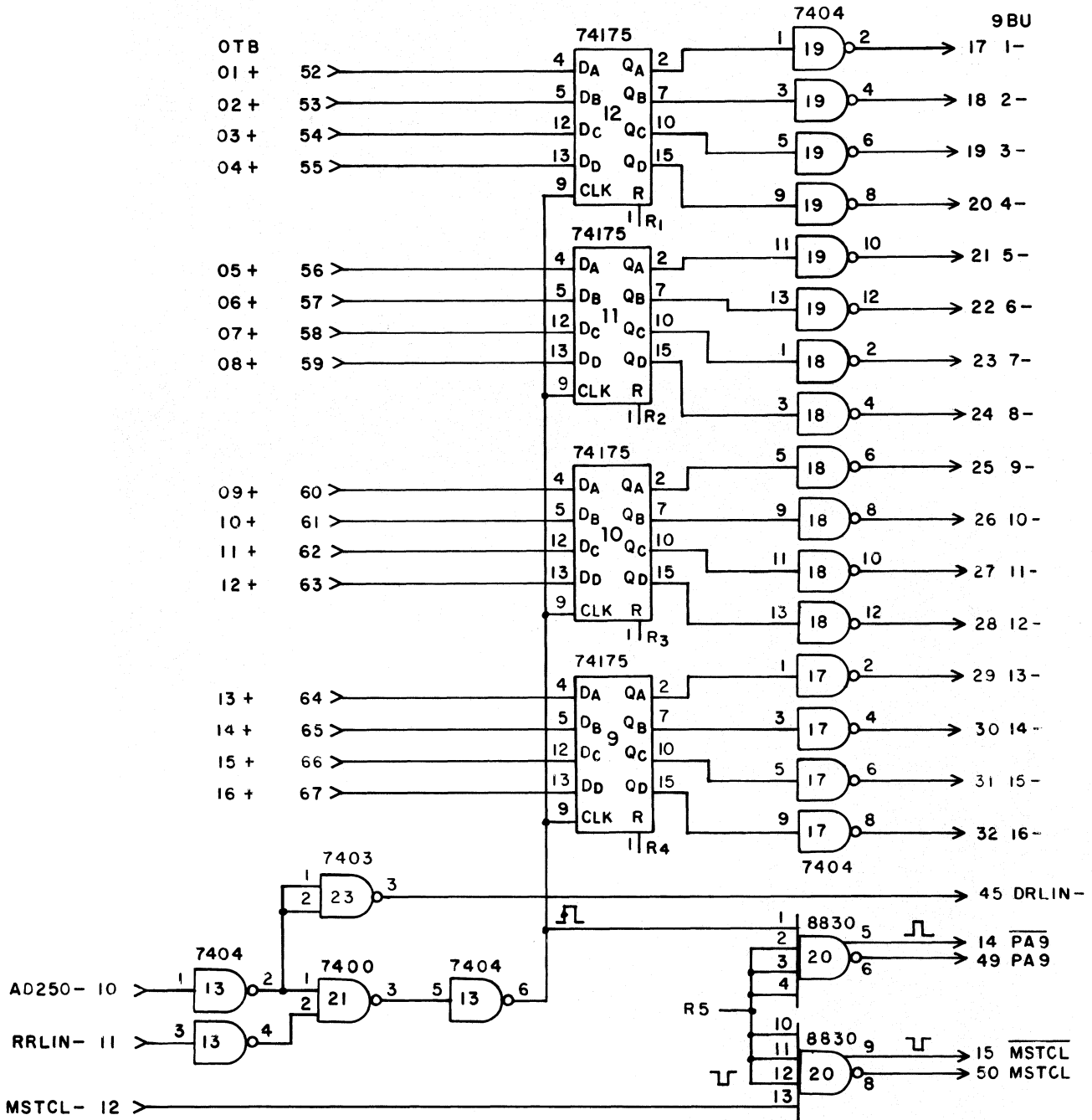


316 - 116 LINK

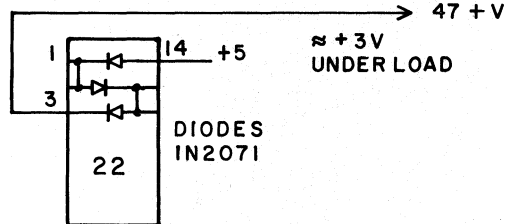
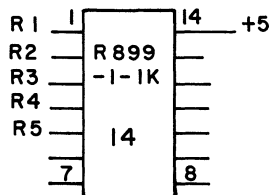
316 REC'R.

316 SLOT-7

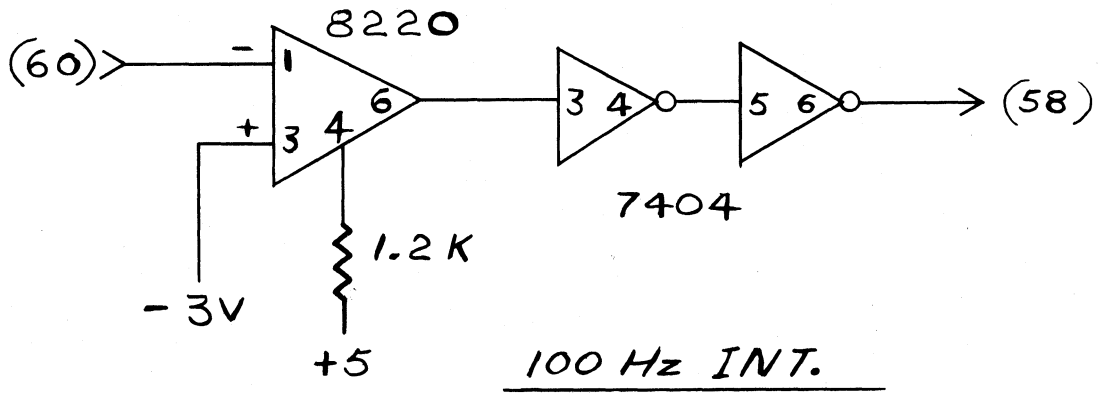




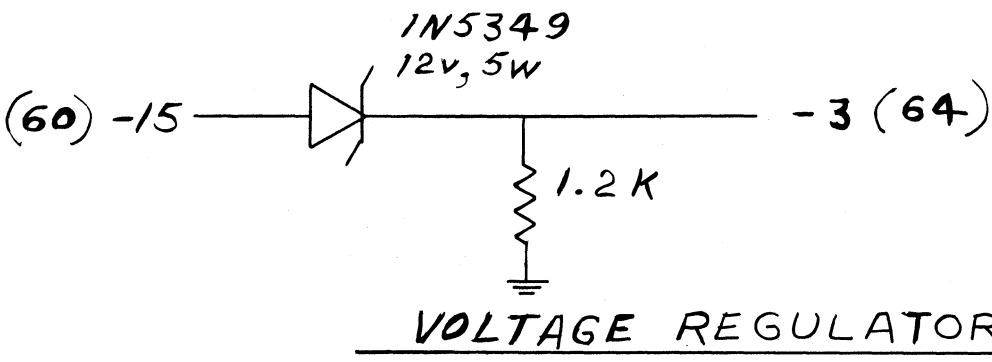
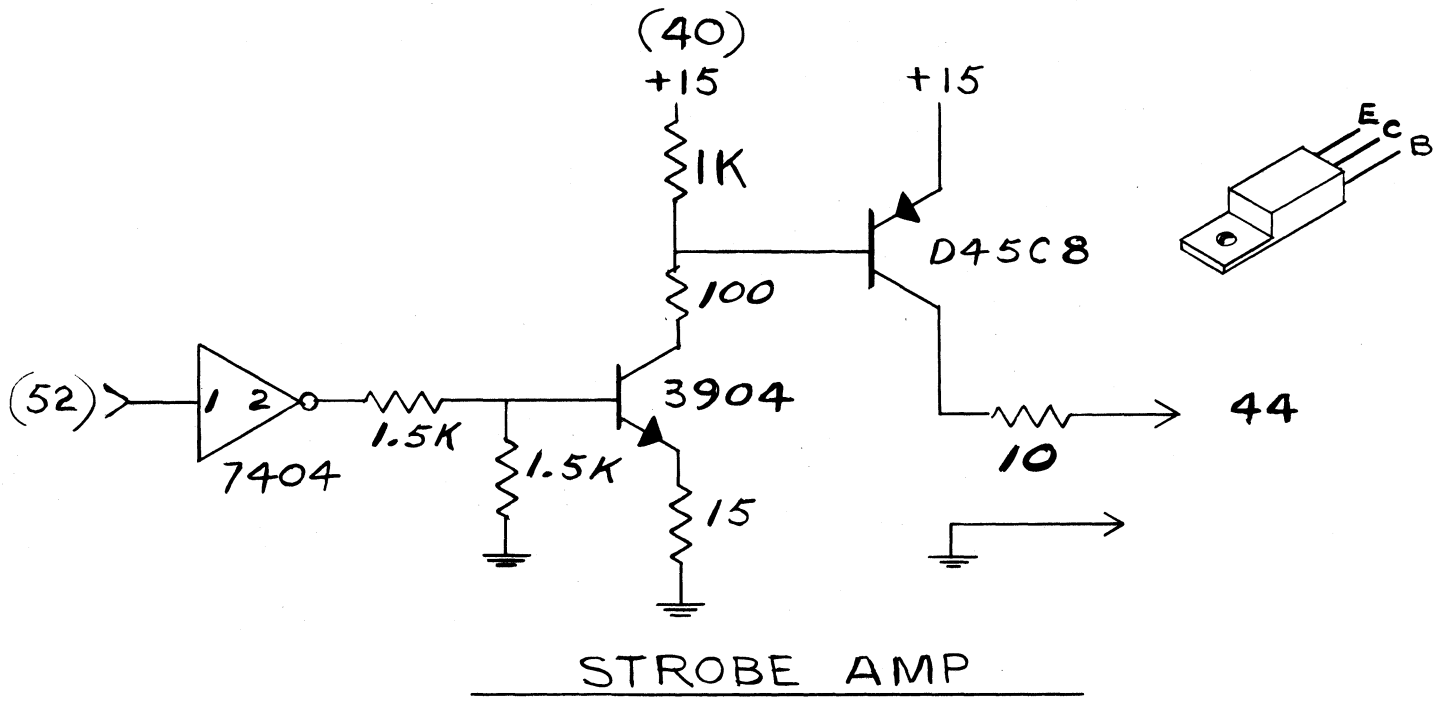
SPARE	LOC.	PINS
7404	17	10, 12
7404	13	8, 10, 12
7400	21	6, 8, 11
7403	23	6, 8, 11

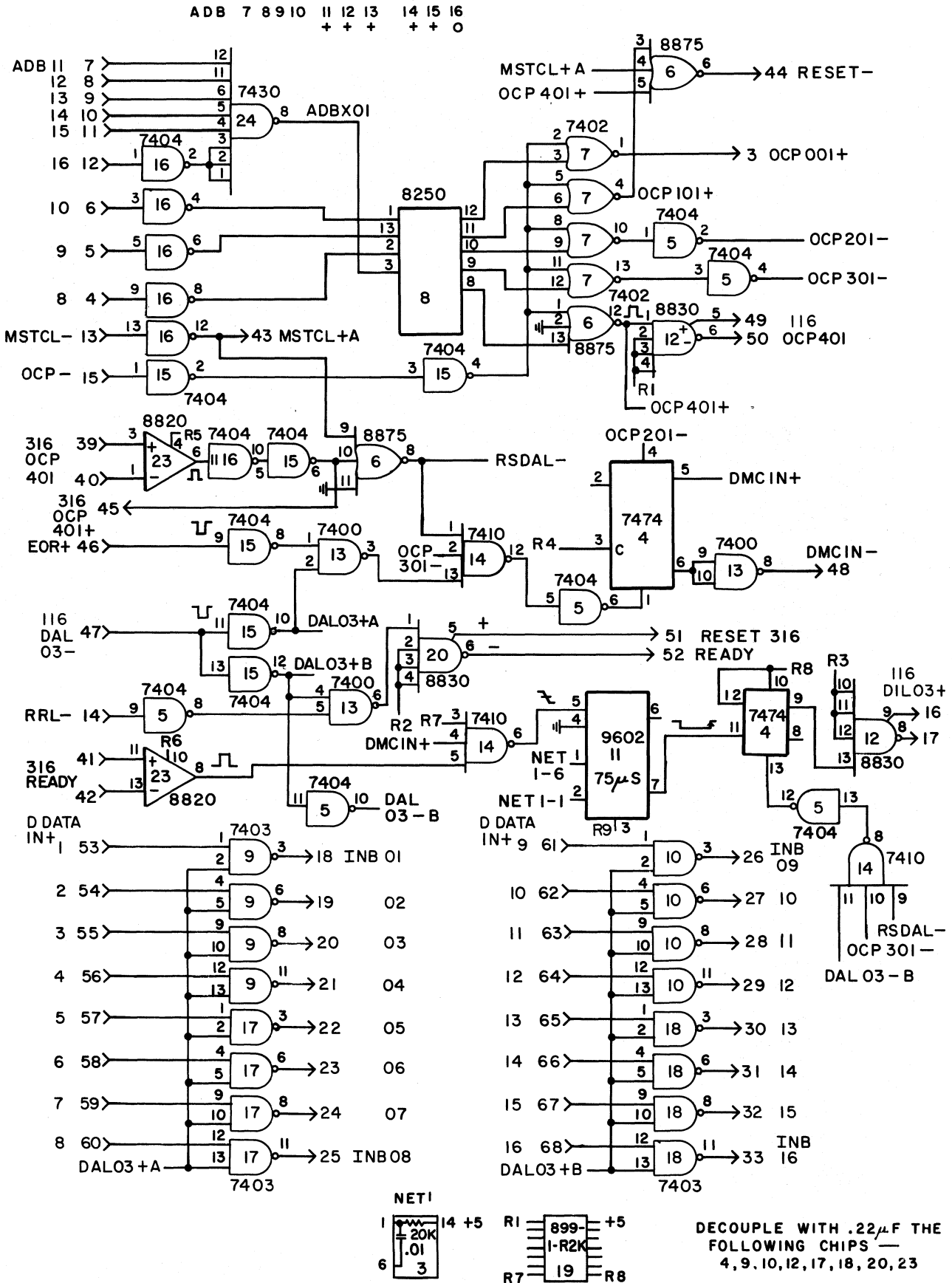


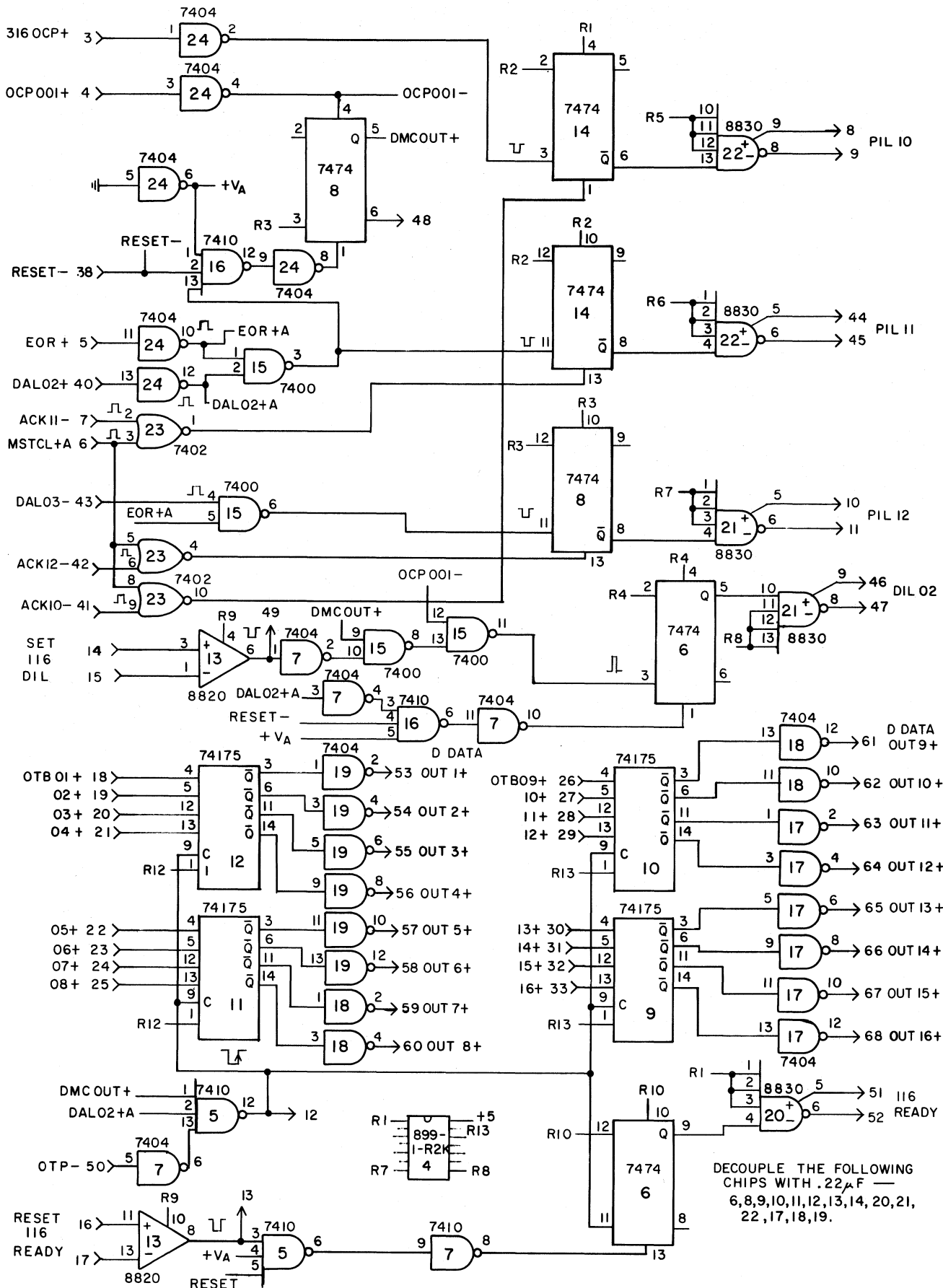




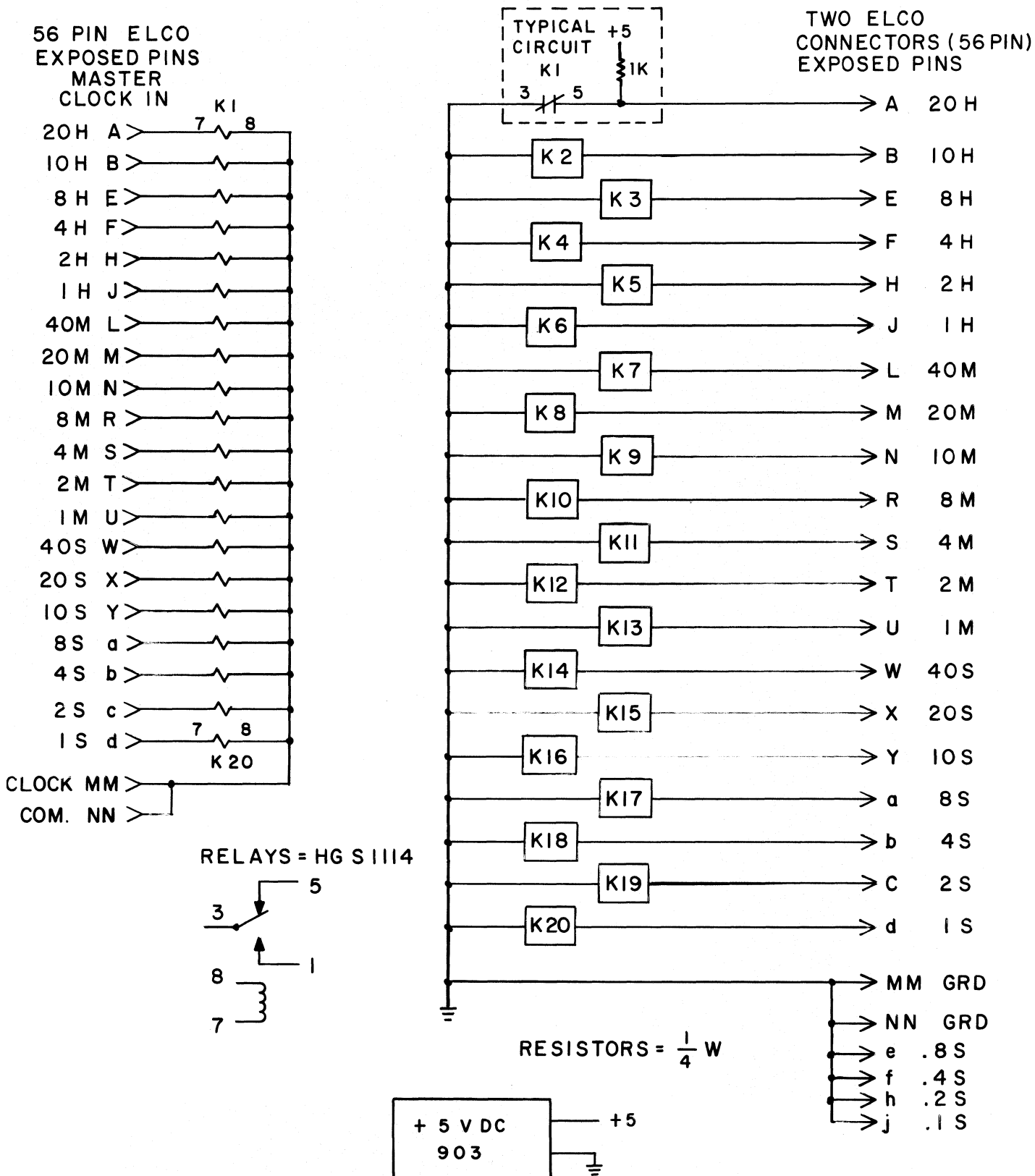
TM







316 - 116 LINK 116 XMITTER 116 SLOT-4



CLOCK SLAVE FOR TTL LEVELS