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DDP-116/MODCOMP DATA LINK AT THE 140-FT TELESCOPE

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I. Introduction

A Modcomp II/25 digital computer has been installed in the 140-ft telescope to permit the observer to perform some real time data reduction. The data, collected by the DDP-116 computer, can be transferred via a data link to the Modcomp and stored for processing by the observer. This report gives a description of the data link between the two computers.

II. Description

A. Modcomp Computer and Peripheral Equipment.

The Modcomp II/25 purchased for the 140-ft telescope is a general purpose 16-bit computer with 32 K words of core memory. Two general purpose controller modules were also purchased to facilitate interfacing the Modcomp computer to special NRAO devices. One of these controllers is used in the data link.

The peripheral equipment consists of a punched card reader (Documation M200), a moving head disc with 2,598,400 words of storage (Diablo), a computer display terminal (Tektronix 4012), and a hard copy unit (Tektronix 4610). This equipment is located adjacent to the CPU unit in the control room.

B. Data Link

The data link is designed to transfer data between the two computers in block form (DMC mode for the DDP-116 and DMP mode for the Modcomp) and can operate in either direction. At the present time, the link is active only in the direction for data transfer from the DDP-116 to the Modcomp, but can be activated in the other direction when required and the software becomes available.

Once initialized, the transfer occurs at a rate of approximately one word every 75 μsec times the number of words being transferred.

III. Programming

A. Link Address

The link address is different for the DDP-116 and the Modcomp since it was chosen not to coincide with any planned additions to either computer. The link address and associated information for each computer is as follows:

DDP-116 Link Arrangements:

Link Address: 50

DMC Channel: 05*

PIL Line: 15

* The start and stop addresses for DMC channel 05 are 20 and 21 respectively.

Modcomp Link Arrangements:

Link Address: 1C

DMP Channel: 05*

* The TA (transfer address) and TC (transfer count) locations are 75 and 65 respectively.

B. Link Status

The link status may be checked by the DDP-116 with the following commands:

SKS 250: The DRL (device ready line) will be low if the DDP-116 has reached an end of range.

SKS 350: The DRL will be low if the Modcomp is ready to receiver or transmit data.

SKS 450: The DRL will be low if the link is set to transfer data from the Modcomp to the DDP-116. The computers need not be ready to transfer data as this SKS just indicates the present condition of the direction flip-flop.

The Modcomp can check the link status by performing an input status command for device 1C. The status word has the following configuration:

Bit 0	1 = Link controller power on.
Bit 1	0
Bit 2	0
Bit 3	0
Bit 4	1 = Memory Parity Error.
Bit 5	0
Bit 6	0
Bit 7	1 = Modcomp Ready to Transfer Data.
Bit 8	0
Bit 9	0
Bit A	0
Bit B	0
Bit C	1 = DDP-116 Ready to Transfer Data.
Bit D	1 = EOBLK (End of Block) Flip Flop Set.
Bit E	1 = ERL (End of Range) Flip Flop Set.
Bit F	1 = Direction Flip Flop Set for Transfer from Modcomp.

C. Link Commands

The link commands for the DDP-116 are listed below:

OCP 050: This command is used by the DDP-116 to initiate data transfer from it to the Modcomp. When the command is issued, the following flip-flops are set:

1. 116 Ready.
2. Direction (indicates transfer from Modcomp).
3. DIL

Providing DMC channel 05 has previously been set up in the DDP-116, this command will load the first word to be transferred into the link buffer register and wait for the Modcomp to acknowledge the transfer request. The Modcomp would recognize the transfer request by monitoring the link status word bits C (DDP-116 Ready) and F (Direction).

OCP 150: This command is used by the DDP-116 to acknowledge a data transfer request initiated by the Modcomp for transfer from the Modcomp. This request would be via an interrupt on PIL 15 in the DDP-116. When interrupted, the DDP-116 needs to perform a series of SKS's to determine the reason for the interrupt. When this command is executed, the following flip-flops are set:

1. 116 Ready.
2. DMP Request.

When the Modcomp receives the DMP request, it will load the first word to be transferred into the link register and generate a PIL to the DDP-116. If DMC channel 05 has been set up, the transfer will take place.

OCP 250: This command is used by the DDP-116 to initiate data transfer from the Modcomp to it. When the command is executed, the following flip-flops are set:

1. 116 Ready.
2. DMP Request.

Also, the Direction flip-flop is reset so as to indicate a data transfer from the Modcomp. With the DMP Request flip-flop set, the link waits for the Modcomp to acknowledge the request which it detects by monitoring the link status and observing the DDP-116 going ready. When the Modcomp acknowledges the

OCP 250 (continued):

request, and the Mod Ready flip-flop is set, the DMP Request will be sent on to the CPU and the first word will be loaded into the link register. The transfer will then occur providing DMC channel 05 is set up in the DDP-116.

OCP 350: This command is used by the DDP-116 to acknowledge a data transfer request initiated by the Modcomp for transfer to the Modcomp. The transfer request would be via an interrupt on PIL 15 and the DDP-116 would need to perform the necessary SKS's to detect the reason for the interrupt. This command sets the following flip-flops:

1. 116 Ready.
2. DIL.

Setting the DIL flip-flop will cause the DDP-116 to load the first data word to be transferred into the link register, thus starting the block transfer.

Any of the OCP's listed above will also reset the ERL (End of Range) and EOBLK (End of Block) flip-flops.

The Modcomp controls the link via the command OCB to device 1C. This instruction outputs a command word which permits control of the link by changing the word's bit pattern. The configuration of the command word is as follows:

Bit 0	1 = Transfer Initiate (0 = Control)
Bit 1	1
Bit 2	1 = Data Interrupt Connect
Bit 3	1 = Service Interrupt Connect
Bit 4	1 = End of Block
Bit 5	1 = Terminate
Bit 6	1 = Direction into Modcomp
Bit 7	1 = DDP-116 Interrupt
Bit 8	1 = Modcomp Ready
Bit 9	0
Bit A	0
Bit B	0
Bit C	0
Bit D	0
Bit E	0
Bit F	0

The following gives a brief explanation of the bits in the control word.

BIT 2 and BIT 3: These two bits connect (or enable) the data and service interrupts respectively in the general purpose control of the Modcomp.

BIT 4: This bit can be used to signify an end of block of data. It is not needed for the link as an end of block is already generated in the DMP mode.

BIT 5: This bit can be used to terminate a transfer any time. A terminate command will also cause a Service Interrupt if this interrupt is enabled.

BIT 6: This bit controls the direction flip-flop in the link along with commands from the DDP-116.

BIT 7: This bit when set will interrupt the DDP-116 on PIL 15 (normally used when the Modcomp wants to initiate a transfer).

BIT 8: This bit controls the Modcomp Ready flip-flop and is used to enable the link on the Modcomp end.

The appropriate selection of bits can then handle all combinations of transfer requests either when the Modcomp initiates the request or acknowledges one from the DDP-116.

D. Interrupts

The DDP-116 can be interrupted on PIL 15 by two methods (PIL 15 entrance location = 46_8):

1. An interrupt will be generated on PIL 15 when an end of range (ERL) is generated by the DDP-116 along with an input or output data command (INDCM or OUDCM) from the Modcomp, depending on the direction of transfer.
2. An interrupt can also be generated on PIL 15 by the Modcomp when it does an OCB to the link with bit 7 set.

The Modcomp has two interrupts connected to the link. These are the data interrupt (DI) and the service interrupt (SI) for device address 1C (DI entrance location = $9C_{16}$, SI entrance location = DC_{16}). If these interrupts are enabled, the following will generate an interrupt to the Modcomp.

DATA INTERRUPT: A DI will be generated when the Modcomp reaches an end of block (EOBLK) in a DMP transfer.

SERVICE INTERRUPT: A SI will be generated when one of three conditions are met.

1. When a terminate command is executed by the Modcomp.
2. When the Modcomp either reaches an end of block or outputs an end of block command.
3. When a complete (CMPT) is generated in the link. This is generated when either computer has transferred its entire block of data.

Additional information on the programming for the computers can be found in their respective Programmers' Reference Manuals.

IV. Circuit Description

The electronics for the link is located in two locations, with the main portion located with the General Purpose Controller in the Modcomp. The remainder, which consists of two buffer cards, is located in the expansion rack in the DDP-116.

Figures 1, 2 and 3 show the circuit built on the board with the General Purpose Controller. This controller is designed with room for customer additions to interface with special systems. The circuits shown are just the addition to the controller.

Along with the customer interface, there were four wiring connections to be completed in the controller. They were as follows:

1. Link address 1C.
2. Interrupt priority code.
3. Source ID for interrupt.
4. DMP channel address.

The location for these connections and diagrams for the General Purpose Controller can be found in the Technical Manual, Peripheral Controllers, Volume II for the Modcomp computer.

Figure 1 shows the logic for decoding commands from the DDP-116, logic for SKS instructions, logic for generating CLEAR signals, and inverters for the bits from the output bus in the DDP-116. Output commands 050, 150, 250, 360, and 450 are decoded and gated with the OCP pulse. OCP 450 is not used at the present time but is available for future expansion. An output command pulse OCP 50 is also generated anytime an OCP is executed in the link. This pulse is used to reset the ERL and EOBLK flip-flops. The pulse OCP 50A is OCP 50 delayed by a few μsec and is used to set the 116 READY flip-flop.

Three types of clear signals are generated: CLEAR A, CLEAR B, and CLEAR. CLEAR A is generated from MSTCL (Master Clear from the DDP-116) or ICBFB (Master Clear from the Modcomp), CLEAR B is generated from a CLEAR A signal or a TERM (Terminate) from the Modcomp, and CLEAR is generated from a CLEAR B signal or a HALT from the link. The three clear signals reset flip-flops as follows:

CLEAR A: Resets - SI REQUEST F/F

CLEAR B: Resets - PIL F/F
116 READY F/F
DIL F/F
ERL F/F
EOBLK F/F
OUT/IN F/F
DMP REQUEST F/F

Also clears - BUFFER 1
BUFFER 2

CLEAR: Resets - MOD READY F/F

Figure 2 shows the buffer register in the link used in data transfer between the two computers. BUFFER 1 is used in transfer from the DDP-116 to the Modcomp. The output word from the DDP-116 is latched into this buffer by an OTP pulse gated with a DAL pulse. These two pulses gated together also generate a DATA READY pulse which sets the DMP REQUEST flip-flop notifying the Modcomp that a word is in the buffer. BUFFER 2 is used for transfer in the other direction (Modcomp to DDP-116). The output word from the Modcomp is latched into the register by an OUDCM pulse which also sets the DIL flip-flop notifying the DDP-116 that the buffer contains data. The data contained in BUFFER 2 is then gated on to the DDP-116 input bus by a DAL pulse for transfer in this direction.

Figure 3 contains the remaining of the custom logic for the link which is located with the General Purpose Controller. This figure contains most of the receivers for command pulses from the DDP-116 along with the link control logic. The flip-flops used for control are explained in the following:

MOD READY F/F: This flip-flop is set when the Modcomp performs an OCB with bit 8 set. It signifies that the Modcomp is ready to transfer data. It also gates the output of the DMP REQUEST F/F to the Modcomp and gates the RRL signal to the input of the DMP REQUEST F/F.

SI REQUEST F/F: This flip-flop, when set, generates a service interrupt to the Modcomp. It can be set by an end block (EOBLK) or terminate command from the Modcomp, and by a complete of transfer (CMPT) from the link. It is reset by reset service interrupt (SIRSTN), CLEAR A, or load command register (LDCMR) pulse.

DMP REQUEST F/F: This flip-flop is set when the link wants to transfer a word either to or from the Modcomp via a DMP channel. It can be set by an RRL pulse gated with the MOD READY signal, DATA READY signal, OCP 250, or OCP 150, depending on direction of transfer and whether initiating transfer or transfer in progress. The flip-flop is reset by a data command (DCM), end of block (EOBLK), data command delayed (DMCA) gated with end of range (ERLA) or CLEAR B. The DCM signal resets the flip-flop after every word transfer, while the rest of the reset signals are either associated with an end of block of data, a terminate command, of a master clear from either computer.

PIL F/F: This flip-flop, when set, will interrupt the DDP-116 on priority interrupt line 15. It can be set by an OCB from the Modcomp with bit 7 = 1 or with a CMPT B. (CMPT B is an end of

PIL F/F (continued):

range gated with data command pulse from the Modcomp.) It is reset by an acknowledge (ACK) signal from the DDP-116 or a CLEAR B signal.

116 READY F/F: This flip-flop, when set, signifies that the DDP-116 is ready to transfer data. It is set by an OCP 50. (OCP 50 is generated anytime the DDP-116 executes an OCP on the link.) It is used to gate signals to the DIL F/F for data transfers. They are (1) an end of range (ERL) from the DDP-116, (2) an end of block (EOBLK) from the Modcomp gated with the OUT/IN direction signal, (3) an end of block gated with a DAL, and (4) a CLEAR B. The second and third methods of reseting the flip-flop deal with an end of block from the Modcomp and are gated with the appropriate signal to make sure the last word to or from the Modcomp is removed from the link's buffer register before the flip-flop is reset.

DIL F/F: The DIL flip-flop is set every time the link wants to transfer a word in or out of the DDP-116 via DMC channel 05. This is done by an OCP 50, output data command gated with the OUT/IN FF for transfer from the Modcomp, or input data command gated with the $\overline{\text{OUT/IN}}$ F/F for transfer in the other direction. There is a delay of approximately 75 μsec in the clock pulse to the DIL F/F to slow down the rate of transfer in order to avoid any conflict with the DDP-116's normal functions. The DIL flip-flop is reset by all the signals which reset the 116 READY F/F plus it is reset by a DAL pulse each time a word is transferred in or out of the DDP-116.

ERL F/F: This flip flop is set when the DDP-116 reaches an end of range in a DMC data transfer. It is reset by a load command register (LDCMR) pulse from the Modcomp, by an OCP 50 from the DDP-116, or by a CLEAR B.

EOBLK F/F: This flip-flop is set when the Modcomp reaches an end of block in a DMP data transfer. It is reset by the same signals as the ERL F/F.

A one shot multivibrator, location U4H, is used to generate a delayed data command pulse from the Modcomp. This delayed pulse, gated with end of range (ERL) from the DDP-116 generates a pulse called complete B (CMPT B). CMPT B indicates that an end of range has been reached and the last word removed from the link buffer for data transfer to the Modcomp. Likewise, an end of block from the Modcomp (EOBLK) gated with a DAL from the DDP signifies that the entire data block has been transferred from the Modcomp and the DDP-116 has removed the last word from the link buffer register.

The rest of Figure 3 contains gating for the various control signals.

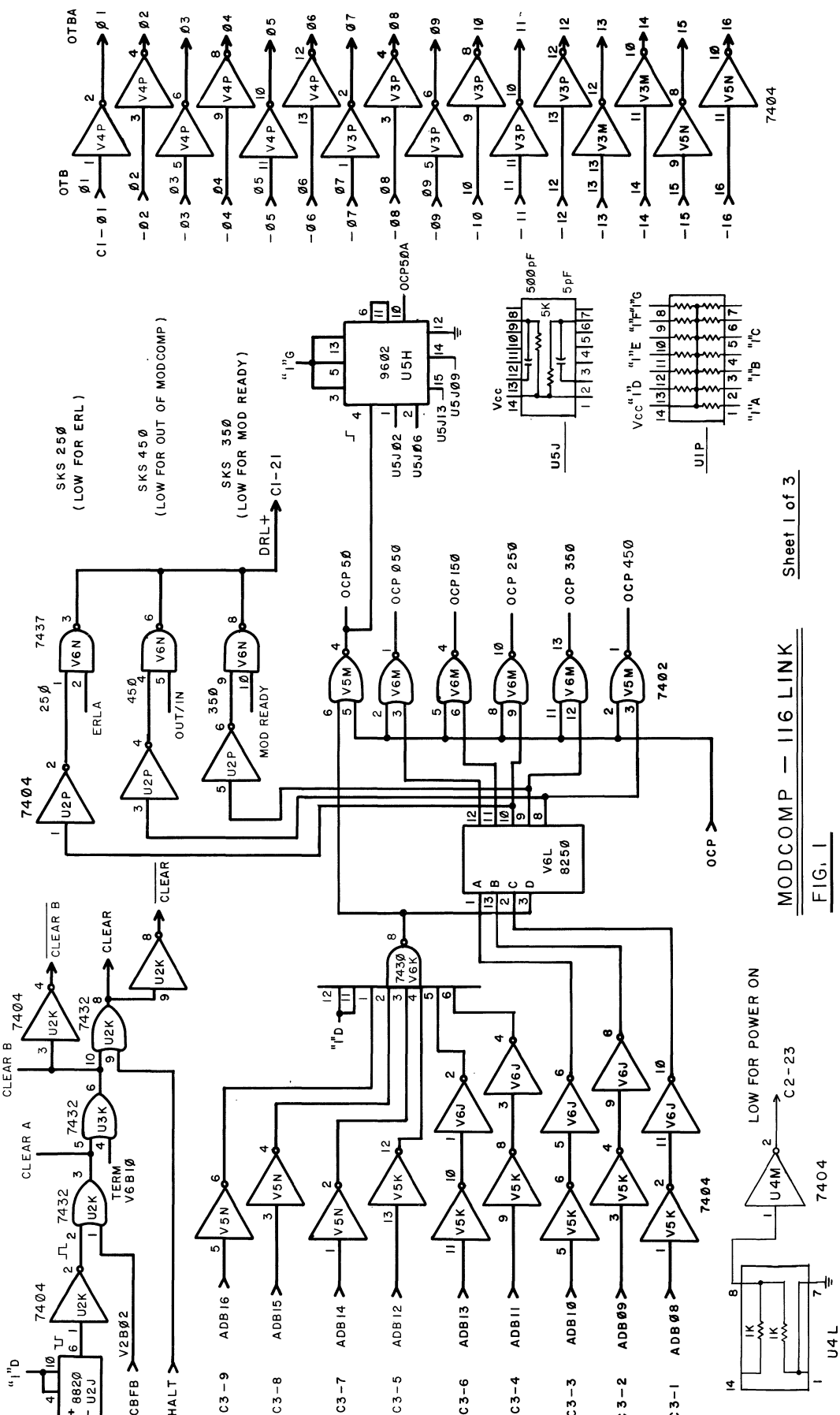
Figures 4 and 5 are the buffer cards for the DDP-116. These cards contain the necessary line drives and gates to drive the 60 feet of cable between the DDP-116 and the Modcomp and are located in the DDP-116 expansion rack.

V. Acknowledgements

Credit should be given to R. Weimer, D. Schiebel and W. Vrable for their help in the design and construction of the data link.

VI: Mnemonic List

Mnemonic	Description
ACK	Acknowledge signal from DDP-116 used to reset PIL F/F.
ADBxx	Address bits from DDP-116.
CLEAR	Generated by Master Clear, ICBFB, TERM, or HALT.
CLEAR A	Generated by Master Clear, or ICBFB.
CLEAR B	Generated by Master Clear, ICBFB, or TERM.
CMPT	Generated by CMPT A or CMPT B.
CMPT A	Complete A, generated by EOBLKA gated with DAL.
CMPT B	Complete B, generated by ERLA gated with DCMA.
DAL	Signal from DDP-116 when a DMC work transfer occurs.
DATA READY	Signal which signifies data is in the link buffer for the Modcomp.
DATARS	Signal used for DMP word transfer request in Modcomp.
DCMA	Pulse to gate data to or from the Modcomp.
DFB	Output data from buffer - Modcomp.
DIL	Request for data transfer in DMC - DDP-116.
DTLM	Input data to computer - Modcomp.
EOBLK	Signal generated at end of DMP block transfer - Modcomp.
EOBLKA	Signal from F/F in link set by EOBLK.
ERL	Signal generated at end of DMC block transfer - DDP-116.
ERLA	Signal from F/F in link set by ERL.
HALT	Signal generated by EOBLKA or ERLA.
ICBFB	Master clear - Modcomp.
INB	Input bits to DDP-116.
INDCM	Input data command - Modcomp.
ISLM xx	Input status bit - Modcomp.
LDCMR	Load command register pulse - Modcomp.
LDCMRA	$\overline{\text{DFB06}}$ gated with LDCMR.
LDCMRB	DFB06 gated with LDCMR.
MOD READY	Signal which signifies the Modcomp is ready to transfer data.
OCP	Output control pulse from DDP-116.
OCP xxx	Output command gated with OCP.
OCP 50	Pulse generated any time an OCP to the link is executed.
OCP 50A	Delayed OCP 50.
OTB xx	Output bit from DDP-116.
OTB A xx	Inverted OTB xx.
OTP	Output pulse for gating output bits from DDP-116.
OUDCM	Output data command - Modcomp.
OUT/IN	Signal from F/F in link which determines direction of transfer.
PIL 15	Priority interrupt line 15 - DDP-116.
RRL	Pulse used to reset ready condition in the link.
SIRSTN	Signal to reset Service Interrupt F/F - Modcomp.
SKS xxx	Sensing commands from DDP-116.
STSIRQ	Set Service Interrupt request to Modcomp.
TERM	Terminate command from Modcomp.


MODCOMP – 116 LINK
Sheet 1 of 3
FIG. 1
OTBA
OTB
7404
7437
7432
7430
7402
8250
8820
9602
SKS 250 (LOW FOR ERL)
SKS 450 (LOW FOR OUT OF MODCOMP)
SKS 350 (LOW FOR MOD READY)
DRL+
CI-21
ERLA
OUT/IN
MOD READY
OCP 50
OCP 050
OCP 150
OCP 250
OCP 350
OCP 450
OCP
CLEAR
CLEAR B
CLEAR A
TERM V6B10
HALT
ICBFB
V2B02
MSTCL
CI-25
CI-26
ADB16
ADB15
ADB14
ADB12
ADB13
ADB11
ADB10
ADB09
ADB08
C3-9
C3-8
C3-7
C3-5
C3-6
C3-4
C3-3
C3-2
C3-1
LOW FOR POWER ON
C2-23
U4L
U5J
U1P
500pF
5pF
5K
Vcc

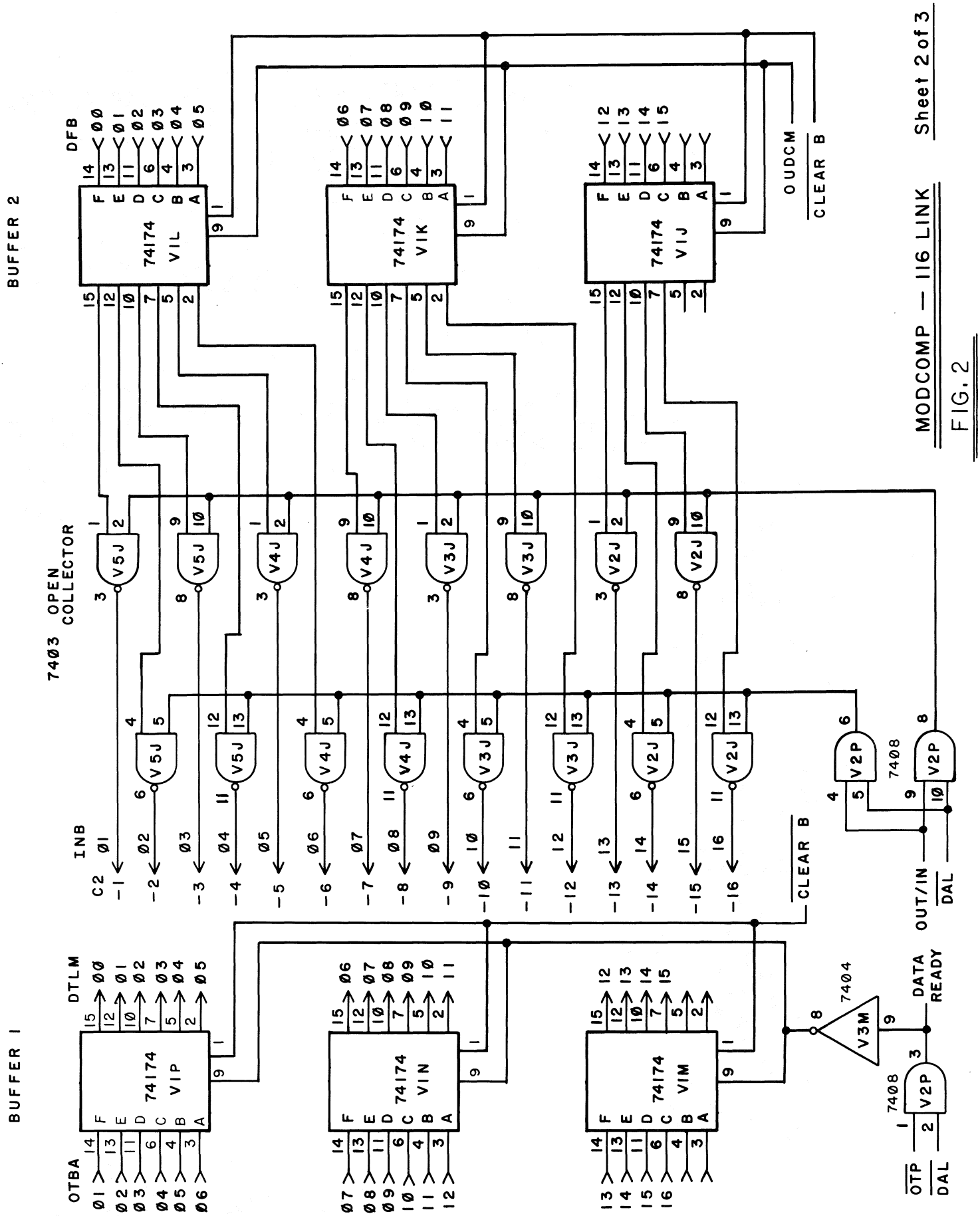

BUFFER 2
BUFFER 1
DFB
DTLM
74174 VIL
74174 VIK
74174 VIJ
74174 VIP
74174 VIN
74174 VIM
7403 OPEN COLLECTOR
INB
OTBA
OUDCM
CLEAR B
7404
7408
DATA READY
OUT/IN
DAL
OTP
MODCOMP — 116 LINK
Sheet 2 of 3

FIG. 2

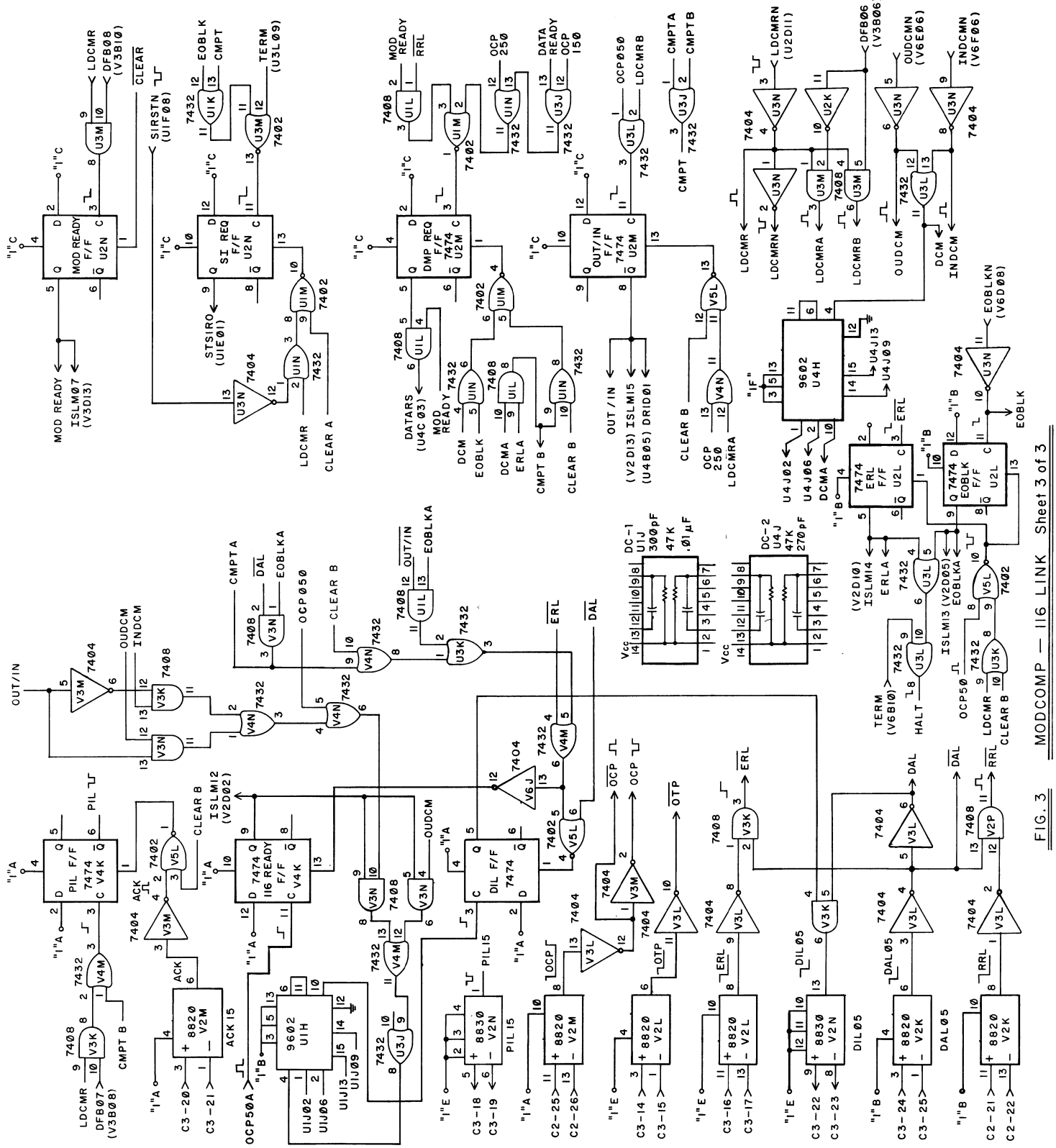
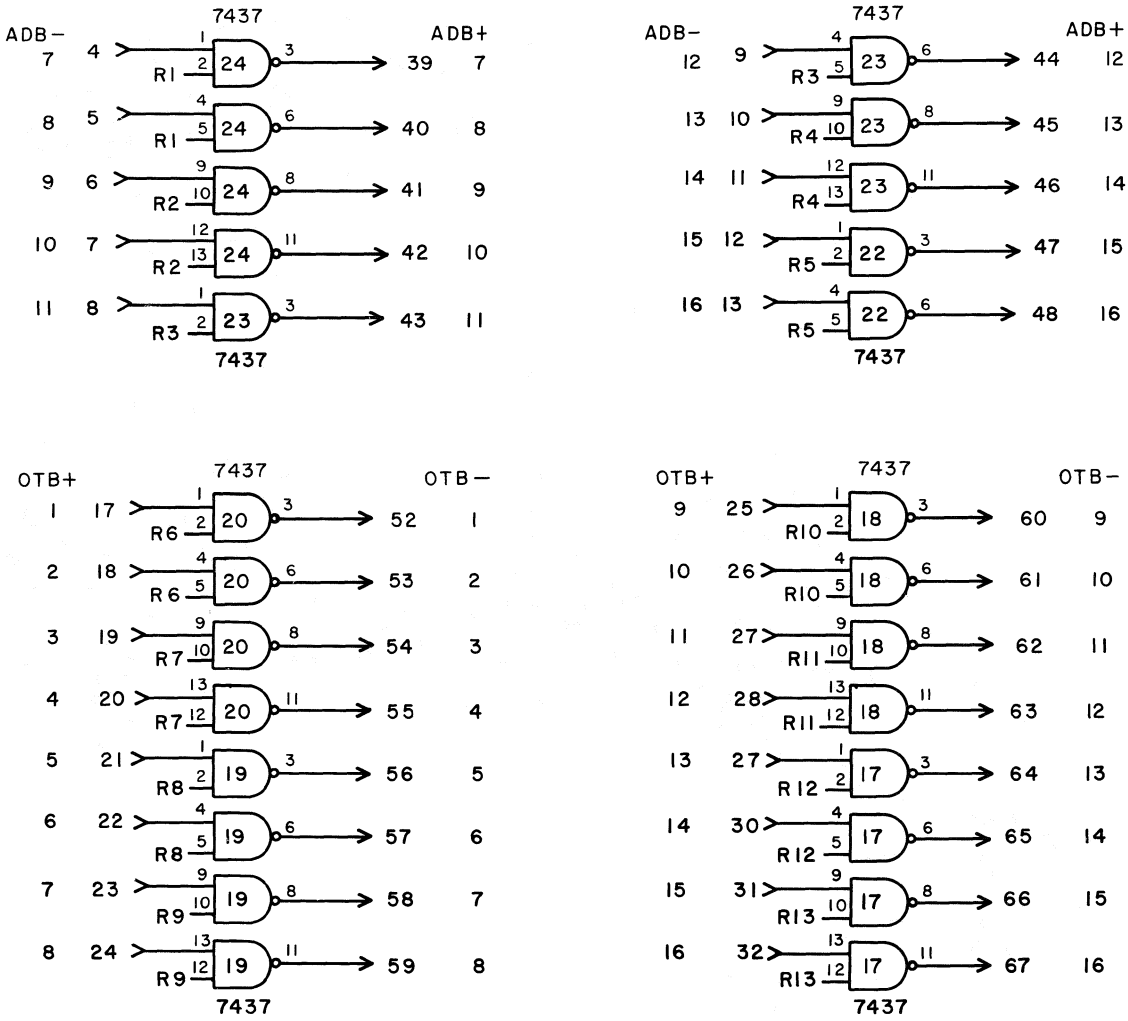
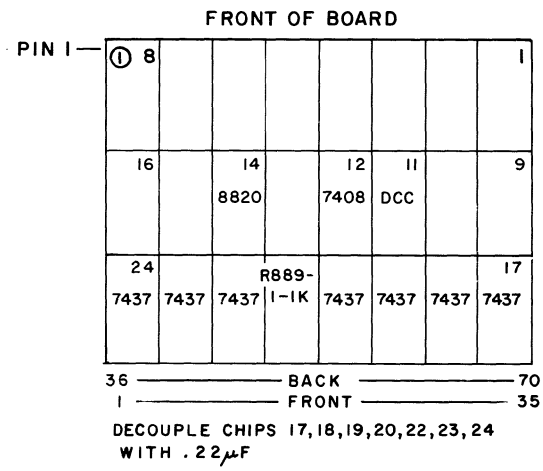
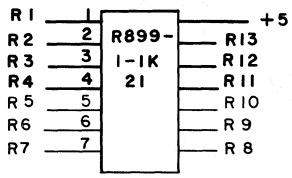
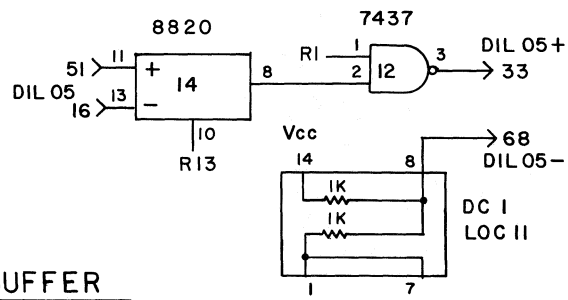


FIG. 3 MODCOMP — 116 LINK Sheet 3 of 3





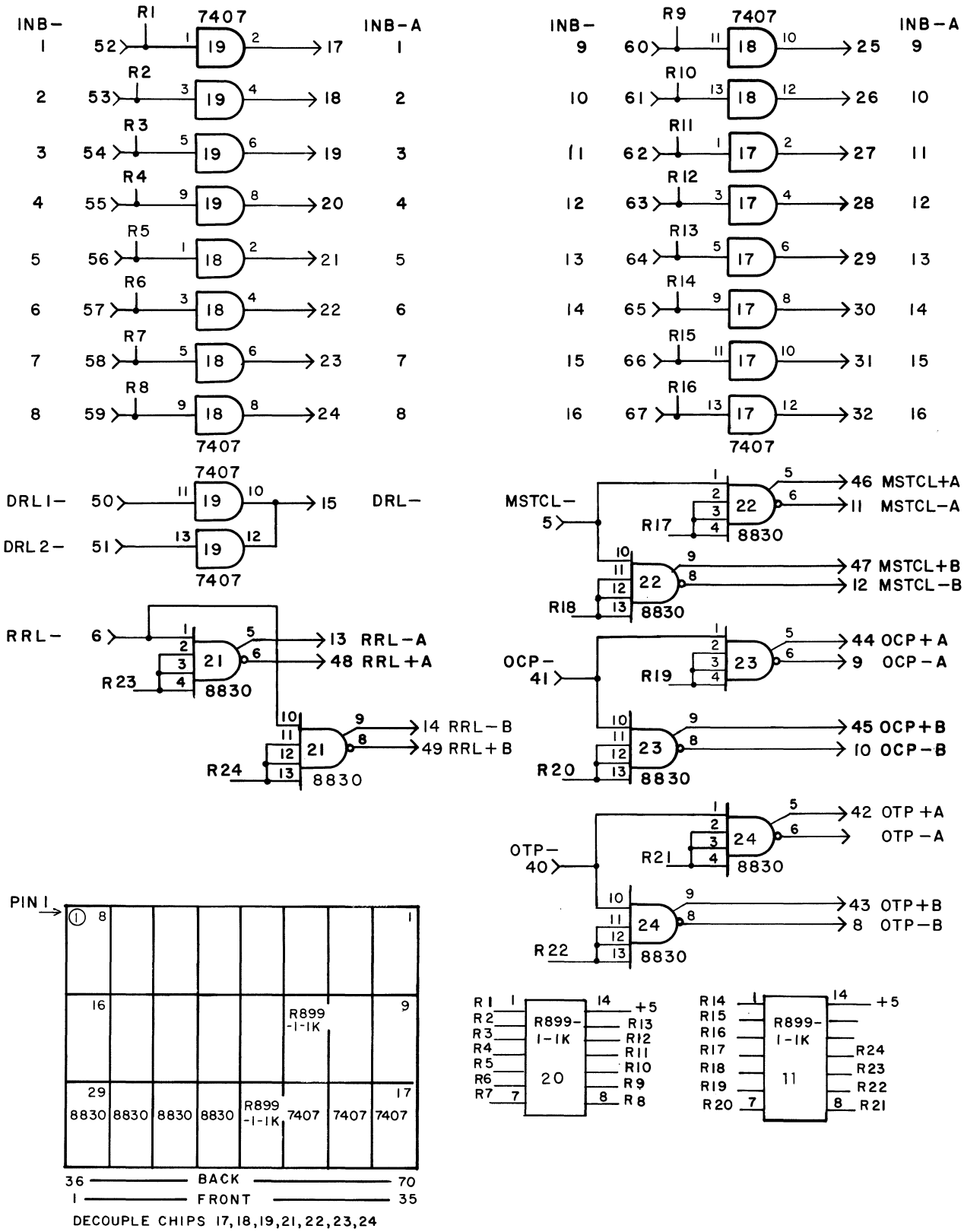




116 − MODCOMP LINK BUFFER

CARD 1

FIG. 4



116 MODCOMP LINK BUFFER CARD 2

FIG. 5