NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

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NRAO CROSS-CORRELATOR RECEIVER DIGITAL DELAY GENERATOR

J. RAY HALLMAN

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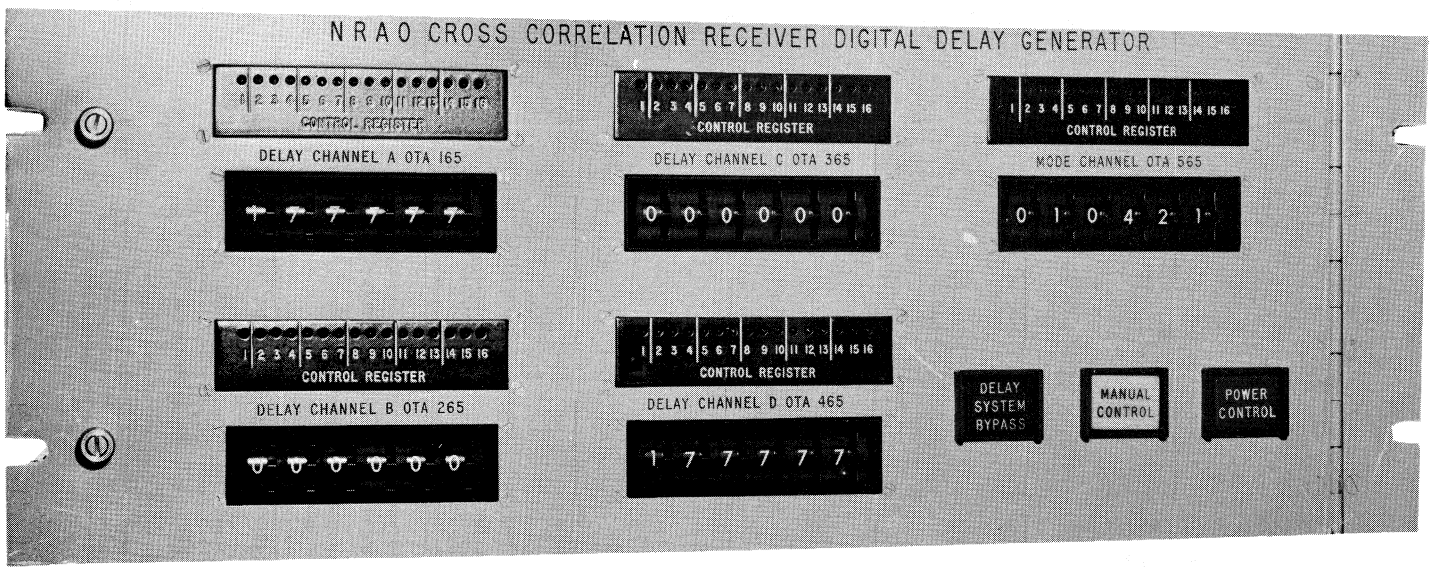
NRAO CROSS-CORRELATOR RECEIVER
DIGITAL DELAY GENERATOR

J. Ray Hallman

General Description

The digital delay system incorporated into the NRAO cross-correlator receiver shown below is normally controlled by the interferometer DDP-116 computer. The programmable control functions are described followed by a description of the manual controls shown in the pix.



Computer Control Functions

OTA 165	Delay Magnitude Channel "A"
OTA 265	Delay Magnitude Channel "B"
OTA 365	Delay Magnitude Channel "C"
OTA 465	Delay Magnitude Channel "D"
OTA 565	Mode Control Channels A, B, C, D

Delay Magnitude Control

Format: For logical "0" in "A" register — 2° = 0.0 nanosecond
For logical "1" in "A" register — 2° = 3.125 nanoseconds

Mode	Bits															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	0	0	0	0	2^{3}	2^{2}	2^{1}	2^{0}
B	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	0	0	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
D	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞

Delay System Mode Control

Format: x = Don't care.

Bit 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

x x C_1 C_2 x x C_1 C_2 x x C_1 C_2 x x C_1 C_2

Ch. A Ch. B Ch. C Ch. D

Mode	BW	Maximum Delay	Control Bits	C_1	C_2
A	10.0 MHz	12.796875 μs	12	0	0
B	2.5 MHz	51.196875 μs	14	0	1
C	.625 MHz	204.796875 μs	16	1	0
D	Illegal	∞	x	1	1

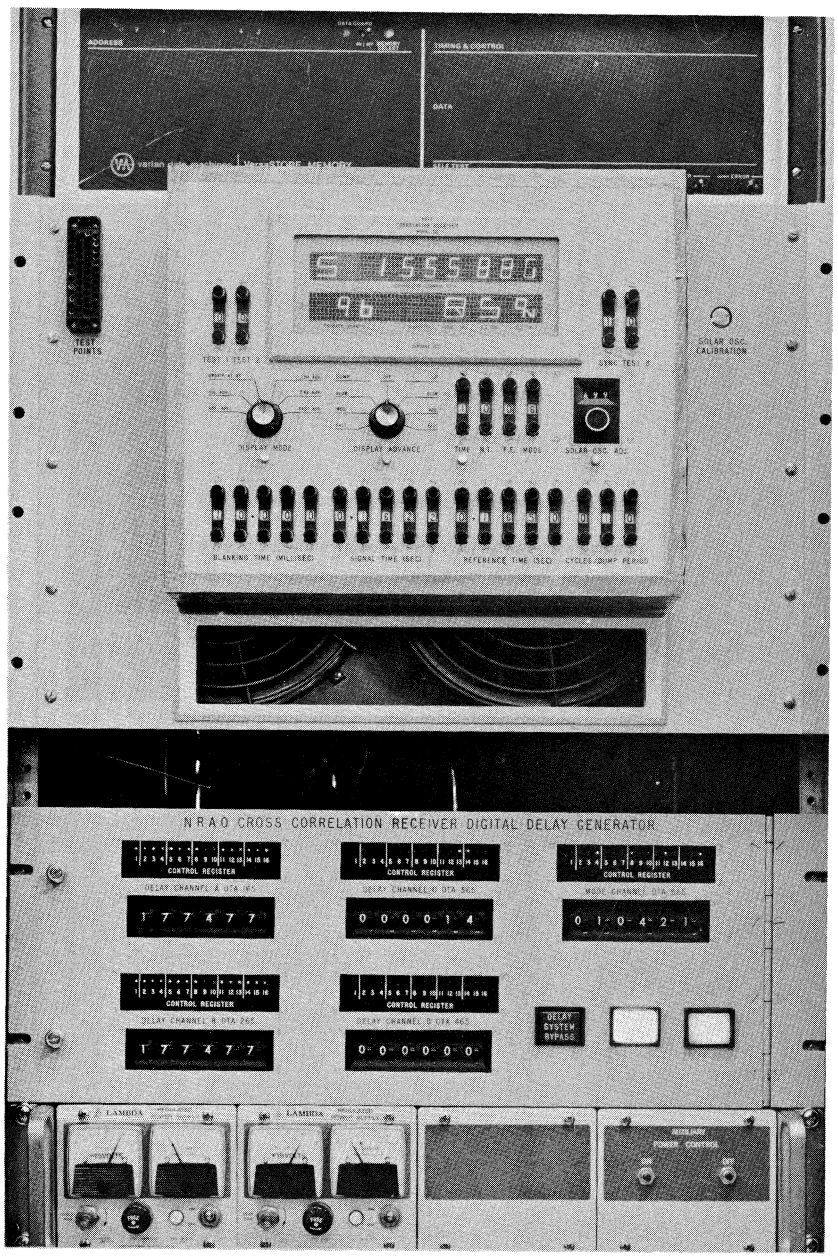
Notes

The computer/delay system interface comprises a serial unidirectional optical isolated data link which operates assynchronously at 1.25 mega bits/second. A 20-bit serial word issues from the computer with each OTA X65 in 18 μs which is the minimum time between successive OTA's to the delay generator controller.

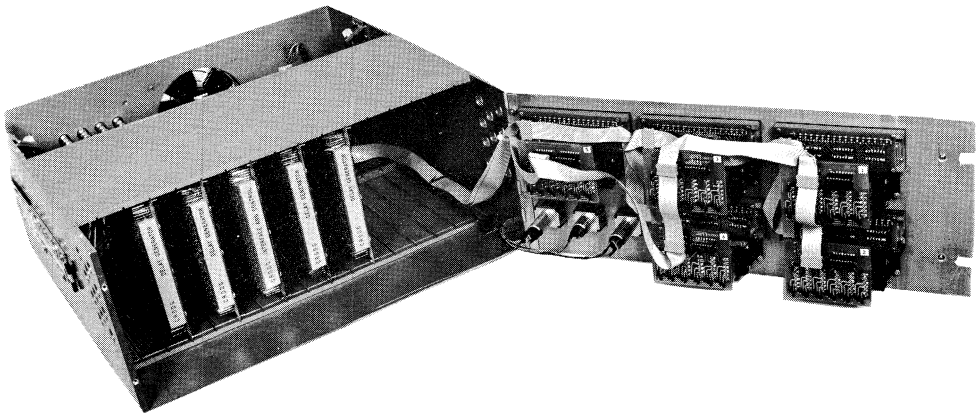
Manual Control and Display Aids

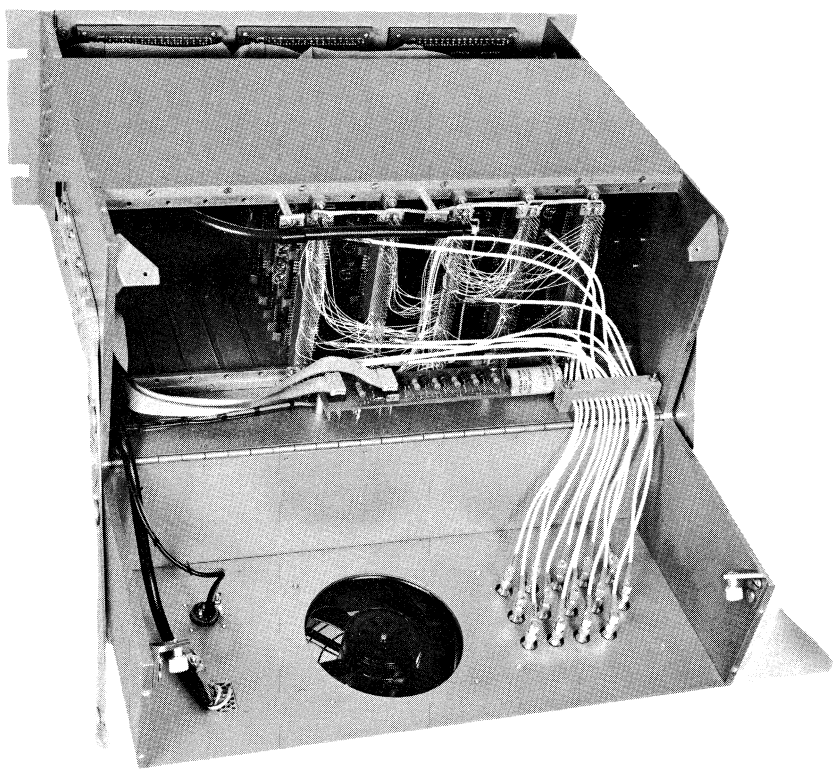
It is possible to monitor and verify the delay magnitude and mode commands as issued from the computer by inspecting the five "control register" displays each comprising 16 LED lamps, one for each of 16 bits issued from the computer. (See picture.) You may seize the device under manual control by depressing the yellow manual control button which lights to indicate manual control. If and when the computer executes an OTA X65, the device controller returns automatically to computer control; thus, the yellow indicator is extinguished, indicating computer control. When in manual control, the thumbwheels may be set to provide any desired delay and mode setting. For normal operation, the green "power control" should be lit and the red "delay system bypass" should be extinguished.

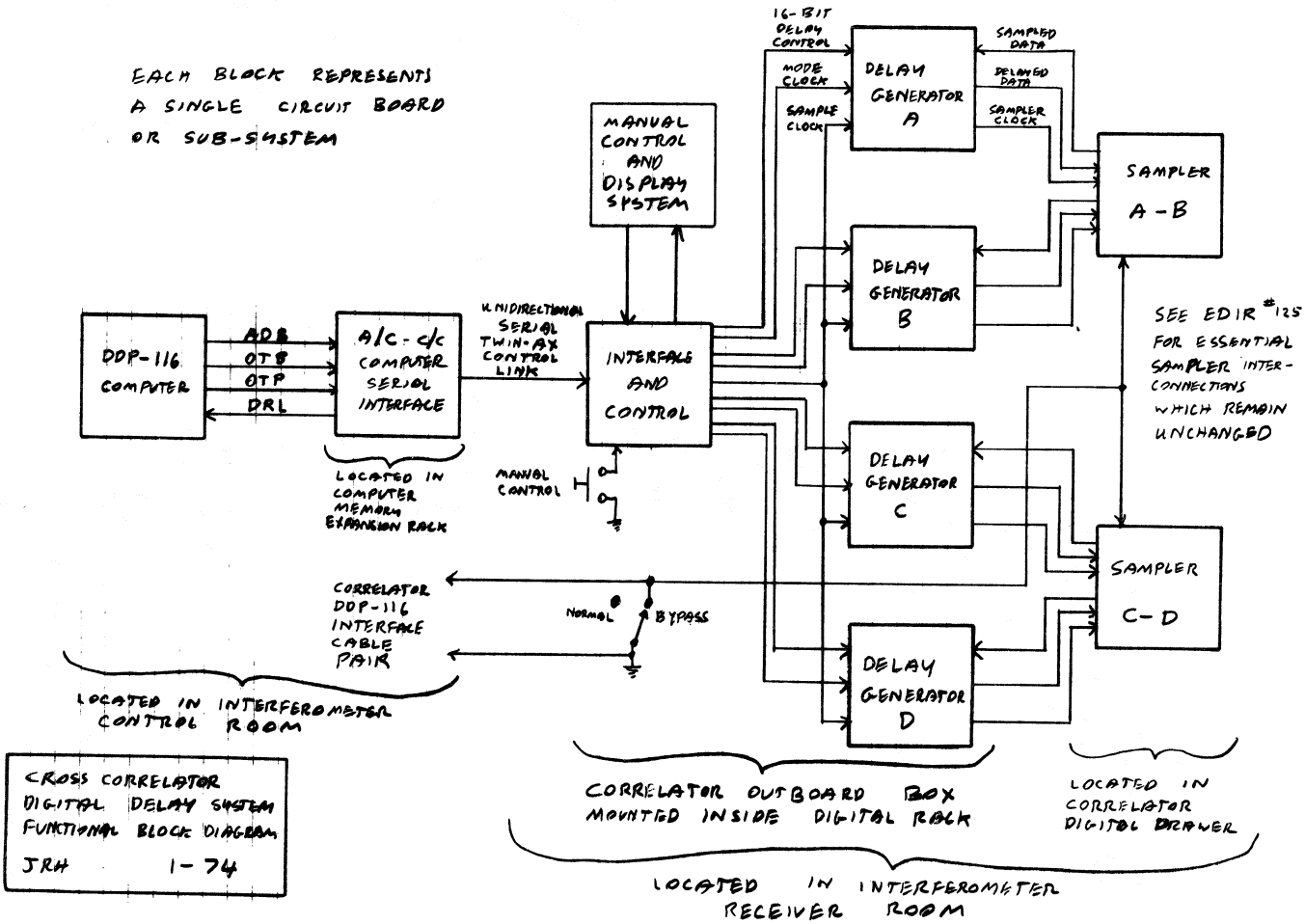
View showing arrangement in correlator digital rack:



Pictures showing delay system outboard packaging:

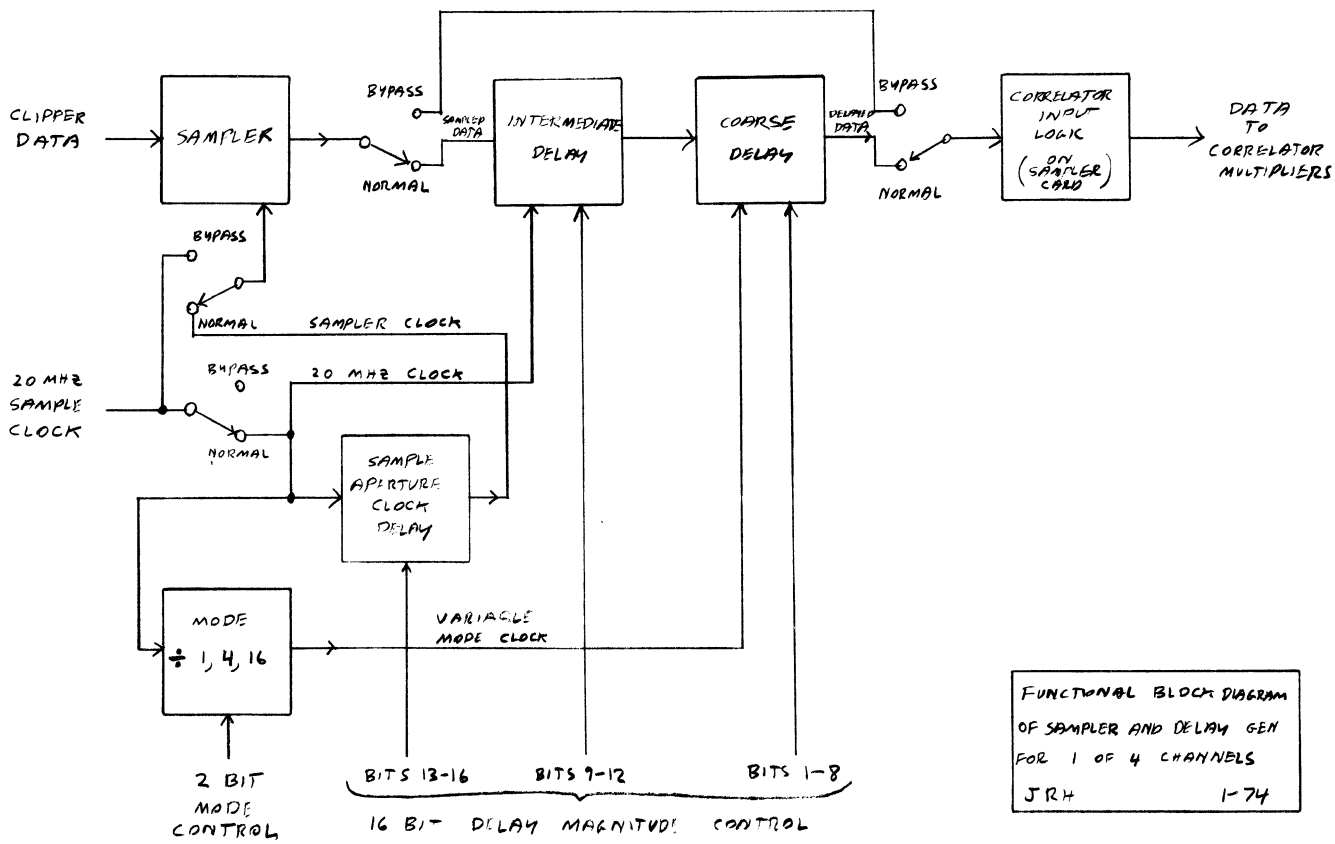




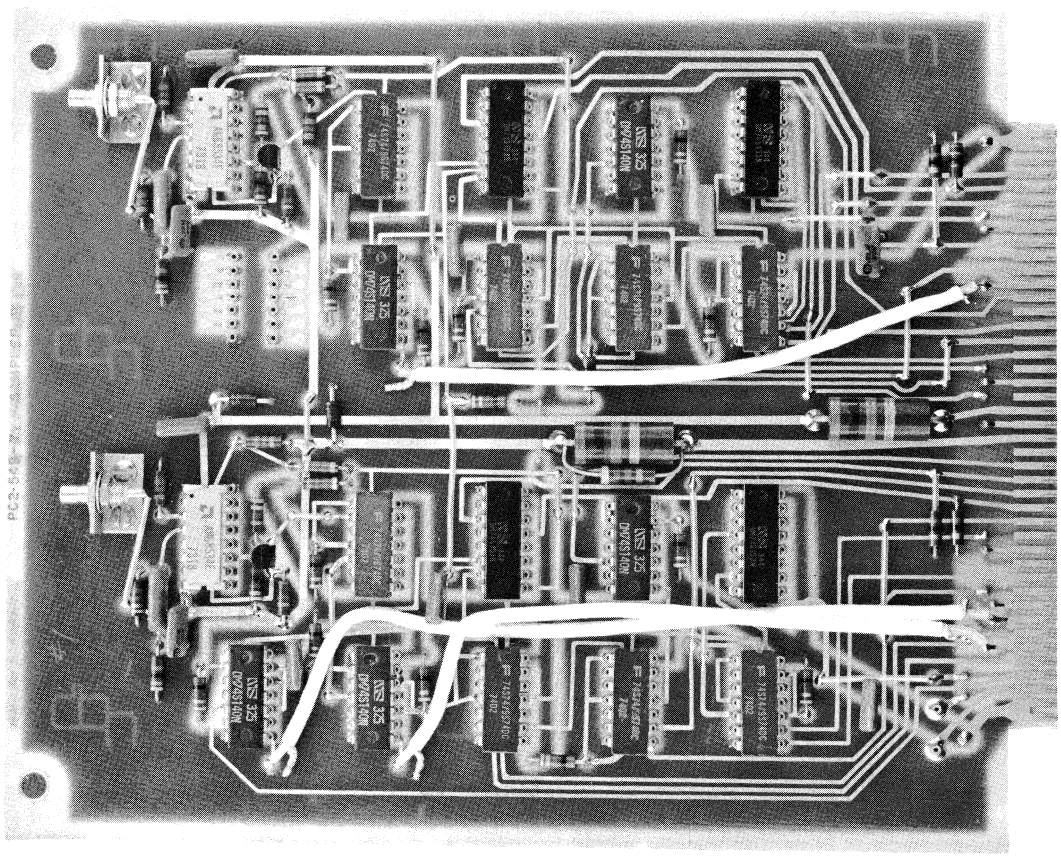


In the above block diagram, the general functional organization of the digital delay system and interface to the DDP-116 control computer and cross-correlator is given. Note that the interconnections between the sampler and correlator are not given since this information is available in EDIR #125. A good block diagram is worth a thousand words, so the following block diagram is presented to give a functional view of the delay generator electronic circuit card and its interface with the sampler. There are four of these cards required in the outboard box comprising the delay system. New sampler circuit cards were fabricated with newer IC technology including the sample and hold

and 50 ohm interface circuitry that couples to the delay generator circuit cards. The bypass circuits shown are required to enable the correlator to remain compatible with the 300-ft observing system. Changeover is accomplished by means of a jumper installed in the 300-ft DDP-116 computer/correlator interface cable. The jumper grounds the bypass circuits, thus disabling the delay generator clocks, and completely bypassing the delay system I/O circuits on the sampler cards, thus minimizing any possible internal RFI crosstalk problems, if any. At the interferometer no bypass jumper is provided in the DDP-116/correlator I/O cable so that bypass is not effected. Bypass may be accomplished, however, by depressing the red bypass switch, if desired. The red button illuminates to verify "bypass" when effected.

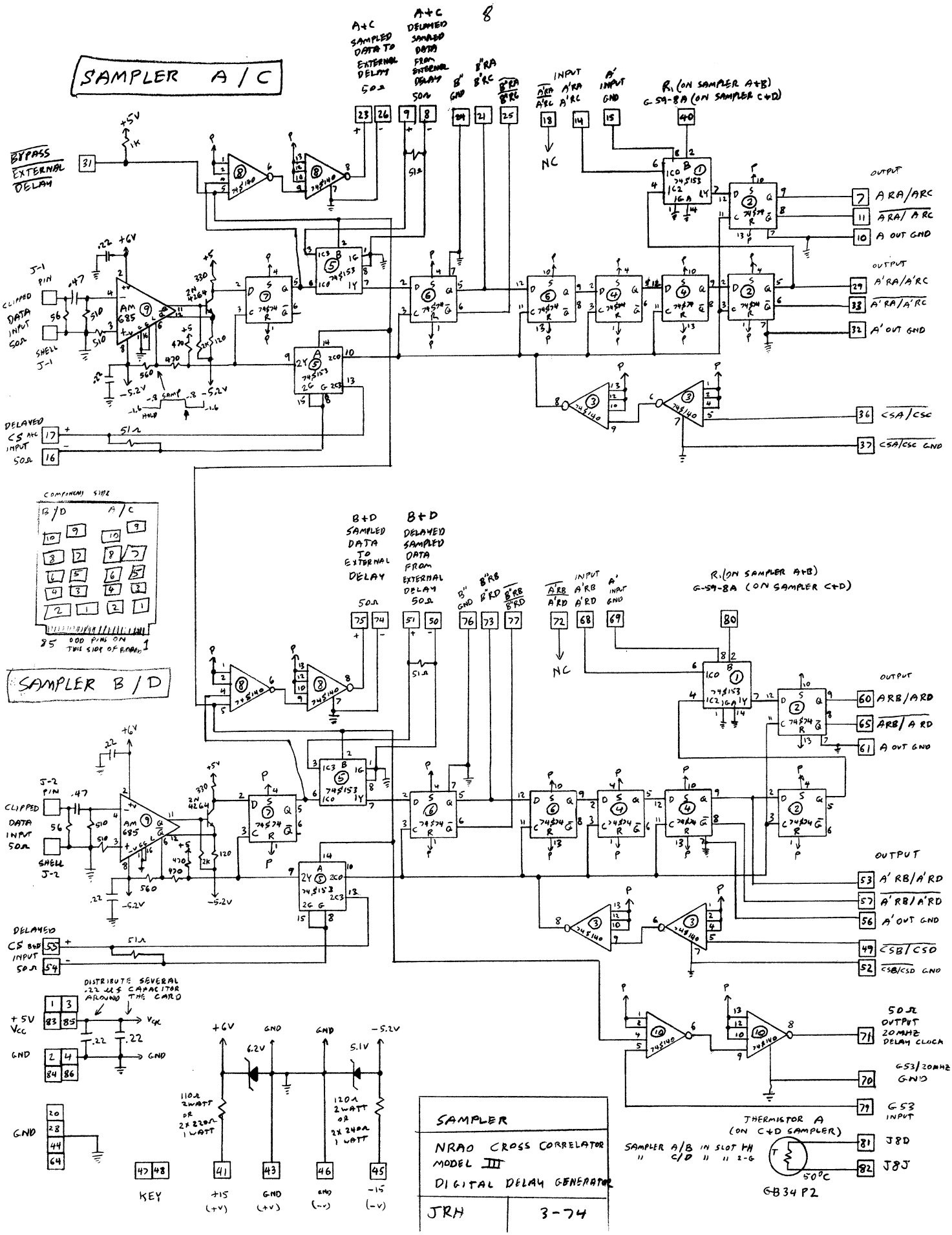


General Circuit Description

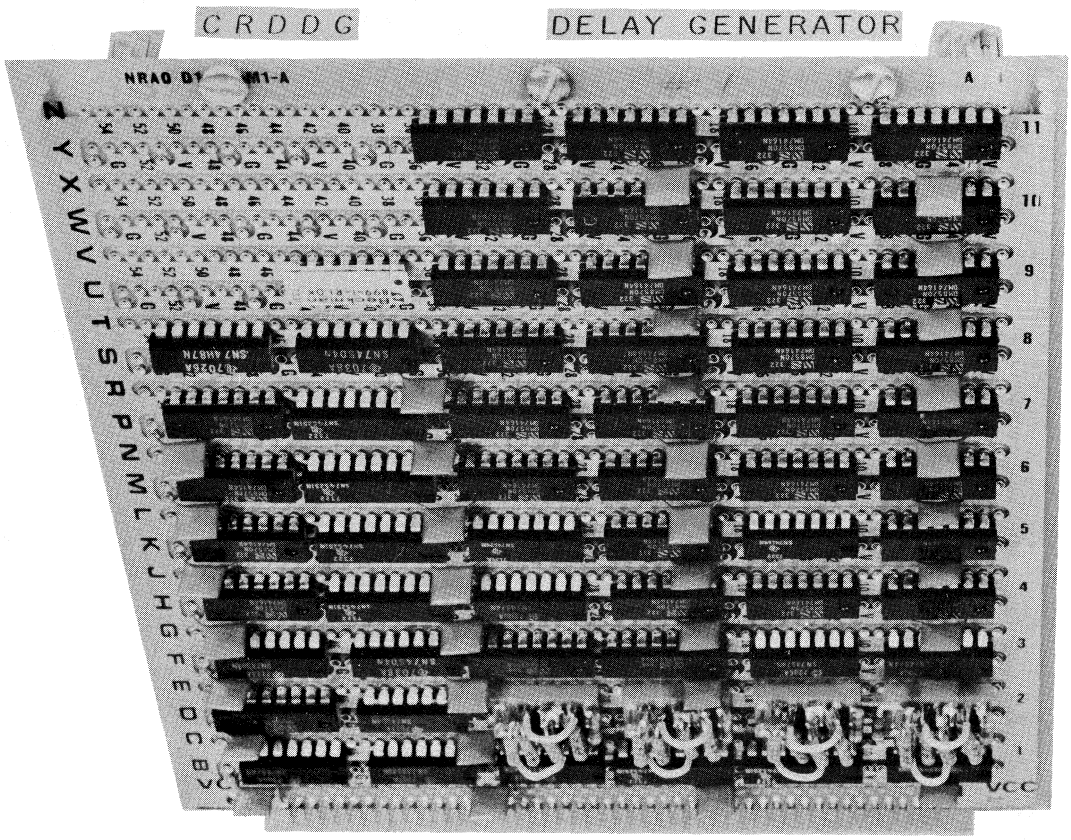


Two new sampler PC cards as above replace the original samplers in the correlator digital drawer. They are completely compatible with, and provide equal performance to, the original samplers and in addition provide 50 ohm I/O and bypass circuits for the digital delay generators. The two bright chips on the left next to the 50 ohm clipper signal connector 1 are the sample and hold circuit type AM68534E which are ECL compatible. Level shifting to TTL is accomplished by the discrete transistor circuit which drives Schottky TTL circuits comprising the correlator input retiming and switching circuits which are functional copies of the circuits of the original sampler cards. The white coax wiring are the 50 ohm I/O circuits to the digital delay system.

The sampler circuit schematic is presented on the following page. The upper half is the channel "A" or "C" circuit while the bottom half is channel "B" or "D". Note the thermistor in the lower right corner which is not interchangeable and must therefore be removed from the defective card and plugged into the spare when troubleshooting. The thermistor which provides thermal monitoring with shutdown protection is required only on the "C-D" sampler in slot 2-G.


SAMPLER A/C
A+C SAMPLED DATA TO EXTERNAL DELAY 50Ω
A+C DELAYED SAMPLED DATA FROM EXTERNAL DELAY 50Ω
B" GND
B"RA B'RC
B"RA B'RC
INPUT A'RA A'RC
A' INPUT GND
R1 (ON SAMPLER A+B) G-59-8A (ON SAMPLER C+D)
BYPASS EXTERNAL DELAY
+5V
1K
NC
OUTPUT
7 A RA/ARC
11 ARA/ARC
10 A OUT GND
OUTPUT
29 A'RA/A'RC
33 A'RA/A'RC
32 A' OUT GND
J-1 PIN
CLIPPED DATA INPUT 50Ω
SHELL J-1
.47
56
510
510
Am 685
+6V
.22
330
2N 4264
470
470
2K
120
560
.22
-5.2V
-.8 SAMP
-1.6 HOLD
-1.6
DELAYED CS A+C INPUT 50Ω
51Ω
36 CSA/CSC
37 CSA/CSC GND
COMPONENT SIDE
B/D
A/C
35 ODD PIN ON THIS SIDE OF BOARD 1
SAMPLER B/D
B+D SAMPLED DATA TO EXTERNAL DELAY 50Ω
B+D DELAYED SAMPLED DATA FROM EXTERNAL DELAY 50Ω
B" GND
B"RB B'RD
B"RB B'RD
INPUT A'RB A'RD
A' INPUT GND
R1 ON SAMPLER A+B) G-59-8A (ON SAMPLER C+D)
NC
OUTPUT
60 ARB/ARD
65 ARB/ARD
61 A OUT GND
OUTPUT
53 A'RB/A'RD
57 A'RB/A'RD
56 A' OUT GND
J-2 PIN
CLIPPED DATA INPUT 50Ω
SHELL J-2
DELAYED CS B+D INPUT 50Ω
51Ω
49 CSB/CSD
52 CSB/CSD GND
DISTRIBUTE SEVERAL .22 μF CAPACITOR AROUND THE CARD
+5V Vcc
GND
.22
.22
Vcc
GND
+6V
GND
GND
-5.2V
6.2V
5.1V
110Ω 2WATT OR 2x220Ω 1 WATT
120Ω 2WATT OR 2x240Ω 1 WATT
50Ω OUTPUT 20MHz DELAY CLOCA
G53/20MHz GND
G53 INPUT
THERMISTOR A (ON C+D SAMPLER)
SAMPLER A/B IN SLOT HH
C/D 2-G
J8D
J8J
50°C
GB34 P2
KEY
+15 (+V)
GND (+V)
GND (-V)
-15 (-V)
SAMPLER
NRAO CROSS CORRELATOR MODEL III
DIGITAL DELAY GENERATOR
JRH
3-74

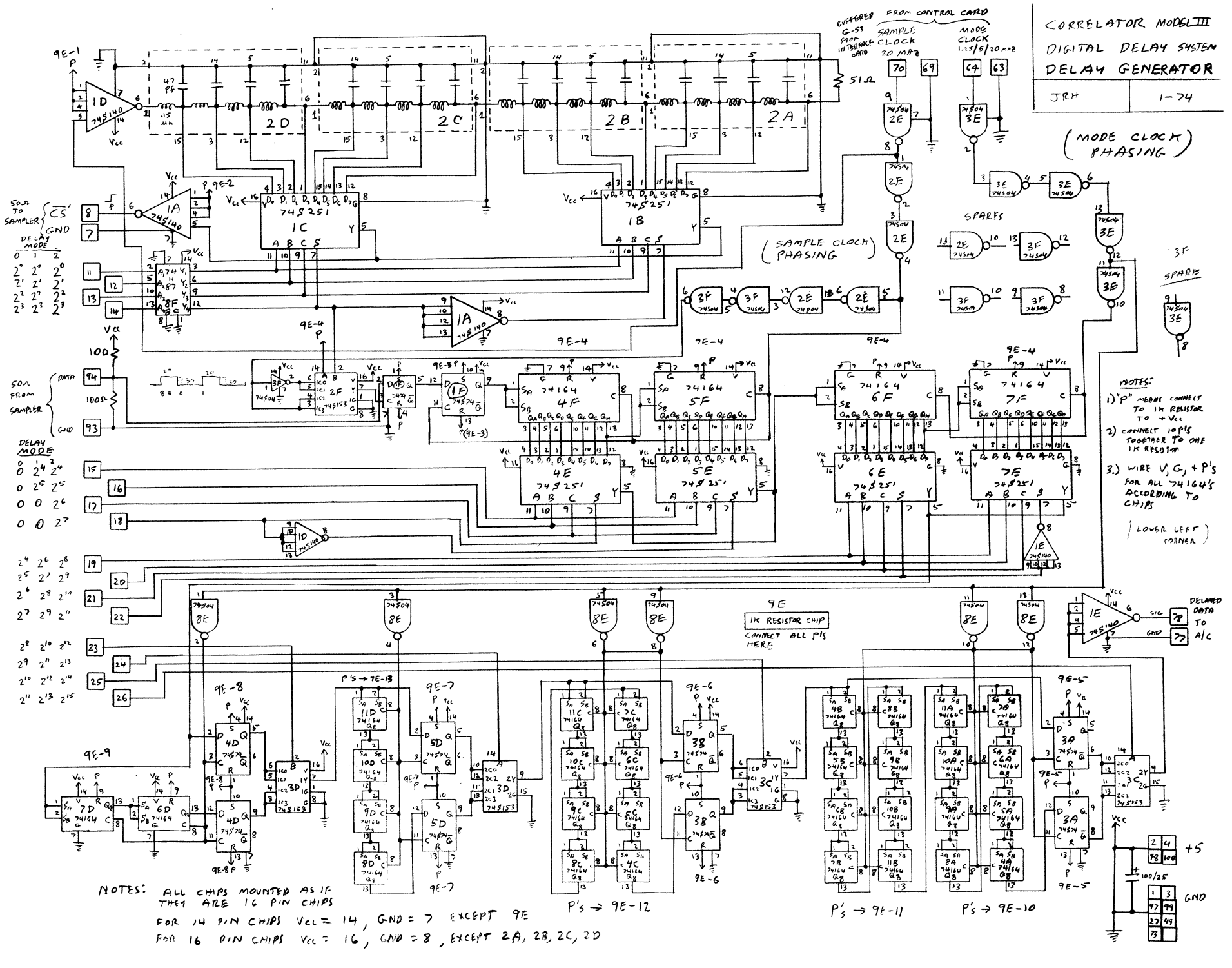
Delay Generator



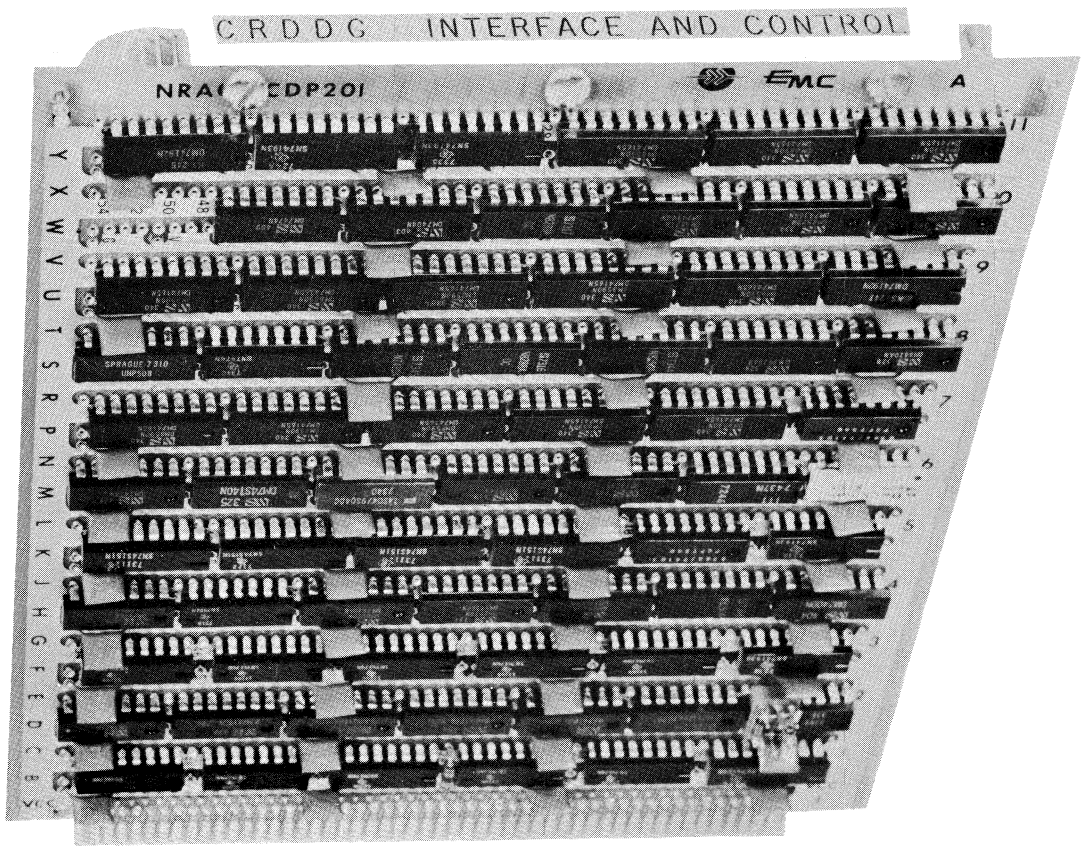
The pix of the delay generator shows the "fine delay system LC delay lines at the bottom right corner. The card is a "standard" large Shalloway wire wrap card which holds 66 IC's when laid out as 16 pin chips using the "card shark" wire wrap program. Four of these cards are required in the system as shown in the previous functional block diagram.

The circuit is presented in the delay generator drawing on the following page.

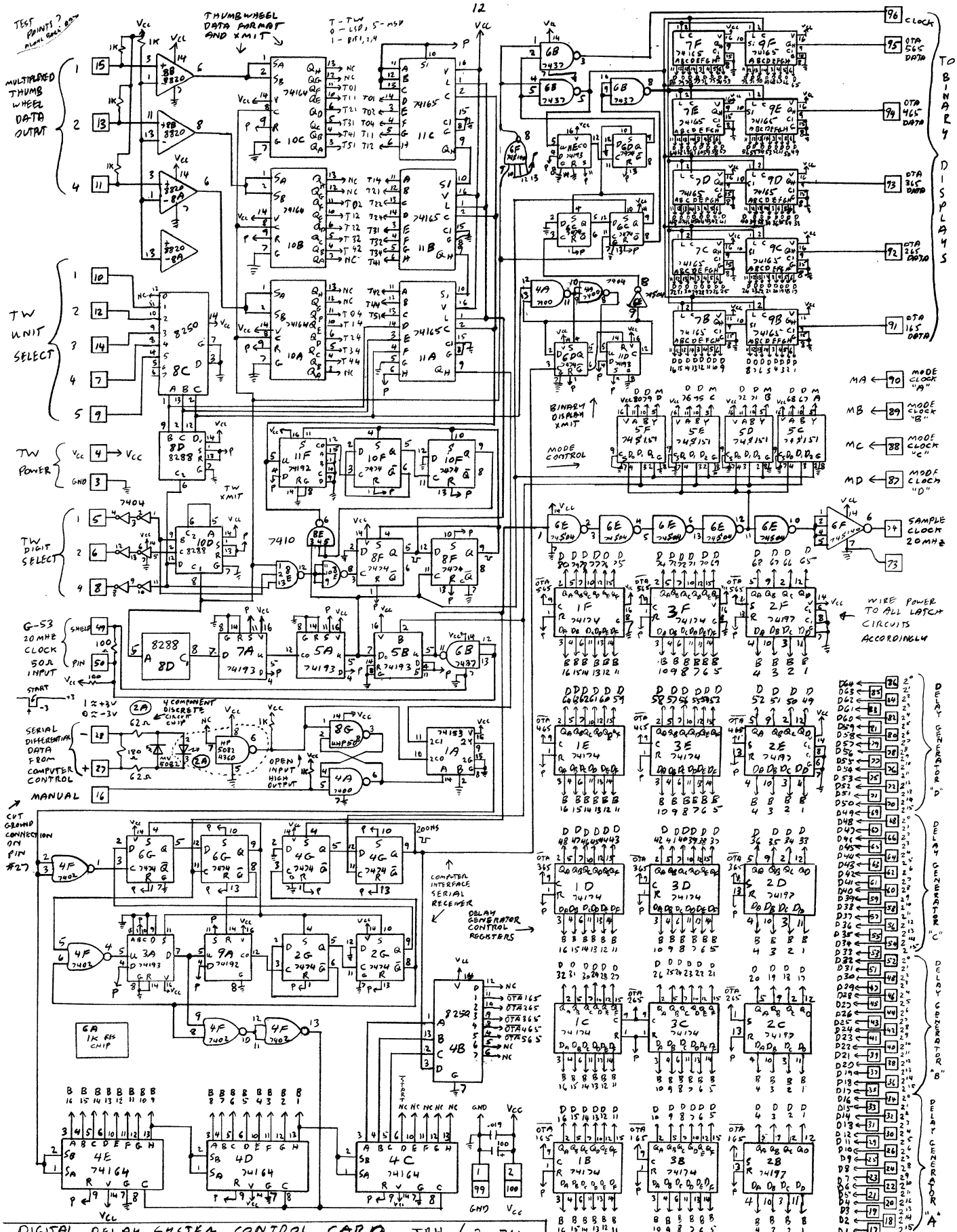
The "fine" delay system LC tapped delay lines are shown along the top of the drawing. Selected taps under control of the four LSB's of magnitude control provide the clock signal to the sampler. The intermediate delay system is shown in the middle left of the drawing while the coarse delay is shown in the right middle and along the bottom of the drawing. The "fine" delay system is analog in nature while the other delay systems are digital, using shift registers. The programming control instructions at the front of this report provide restrictions required to insure monoticity of the delay magnitude function.


CORRELATOR MODEL III
DIGITAL DELAY SYSTEM
DELAY GENERATOR
JRH
1-74
(MODE CLOCK PHASING)
(SAMPLE CLOCK PHASING)
SAMPLE CLOCK 20 MHz
MODE CLOCK 1.25/5/20 mHz
BUFFERED FROM CONTROL CARD G-53 FROM INTERFACE CARD
SPARES
NOTES:
1) "P" MEANS CONNECT TO 1K RESISTOR TO +Vcc
2) CONNECT 10 P'S TOGETHER TO ONE 1K RESISTOR
3.) WIRE V, G, + P'S FOR ALL 74164'S ACCORDING TO CHIPS
(LOWER LEFT CORNER)
9E
1K RESISTOR CHIP
CONNECT ALL P'S HERE
DELAYED DATA TO A/C
50Ω TO SAMPLER
50Ω FROM SAMPLER
DELAY MODE
NOTES: ALL CHIPS MOUNTED AS IF THEY ARE 16 PIN CHIPS
FOR 14 PIN CHIPS Vcc = 14, GND = 7 EXCEPT 9E
FOR 16 PIN CHIPS Vcc = 16, GND = 8, EXCEPT 2A, 2B, 2C, 2D
P's → 9E-12
P's → 9E-11
P's → 9E-10
+5
GND
10

The Control Logic Card

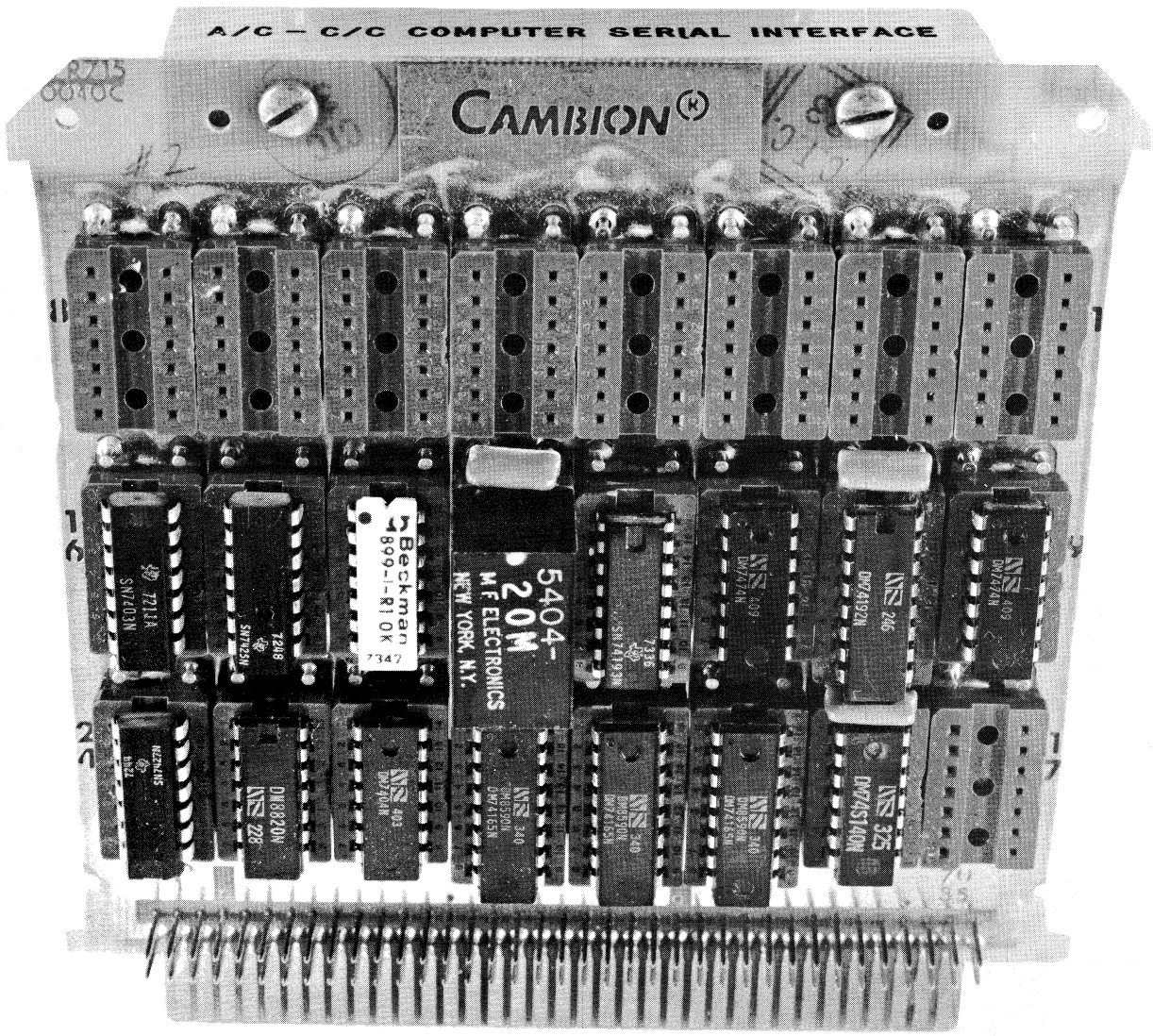


The interface and control logic card interfaces the delay generators to either the serial interface of the DDP-116 computer or the front panel manual thumb-wheel controls and binary displays providing direct control of the 80-bit mode and magnitude of all four channels simultaneously. The card contains four basic subsystems laid out roughly in quadrants as shown in the schematic (next page). The manual control system in the upper left interfaces in place of the computer input to the serial receiver lower left quarter. Data from the serial line receiver is latched into the respective control registers (lower right) under control of the three high order bits of the (19 bit plus start bit) asynchronous data control word. The registers are connected directly (via 64 output pins) to the four delay generator cards. The circuits in the upper left quarter drive the five binary register displays in the front panel. The mode clocks to the delay system are provided by the circuits at the right middle of the page while the system reference clock is derived by the circuits of the middle left page from the 20 MHz correlator clock.



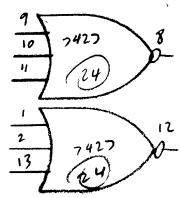
DIGITAL DELAY SYSTEM CONTROL CARD JRH / 3-74

Computer Serial Interface



A small Cambion circuit card installed in the DDP-116 computer provides the serial interface to the digital delay system. A 20 MHz ÷ 16 clock provides an asynchronous data rate of 1.25 M bits/sec. The circuit schematic (next page) shows the signals that connect to the computer and delay system.

SPARES:



PIN 1

8	7	6	5	4	3	2	1
16 7403	7425	R 899 1-1K RES	5404 -20M OSC	7493	7474	7492	9 7474
24 7427	8820	7404	74165	7465	74165	74S140	17

36 ← BACK → 70
1 ← FRONT → 35

SOCKET # 9, 11, 13, 14, 15, 16, 18, 22, 23 ARE 14 PIN
SOCKET # 10, 12, 19, 20, 21 ARE 16 PIN
INSTALL .22 μf CAPACITORS ON POWER PINS OF CHIPS 10, 13, 18, 21

ADB16- 56
ADB15- 55
ADB14- 54
ADB13- 53
ADB12- 52
ADB11- 51
ADB10- 50
ADB9- 49
ADB8- 48

OTB 1+ 11
OTB 2+ 12
OTB 3+ 13
OTB 4+ 14
OTB 5+ 15
OTB 6+ 16
OTB 7+ 17
OTB 8+ 18
OTB 9+ 19
OTB 10+ 20
OTB 11+ 21
OTB 12+ 22
OTB 13+ 23
OTB 14+ 24
OTB 15+ 25
OTB 16+ 26

OTP+ 4
OTP- 5

39 DRL-
58 TP1 SR1
28 SDC-
27 SDC+
29 SHIELD
62 TP2 XMIT
63 TP-3 CLOCK 21 CLOCKS
59 TP4 SR2
65 TP5 SYNC START 800NS
60 TP6 SR3

+5 (36, 37, 69, 70)
GND (1, 2, 34, 35)

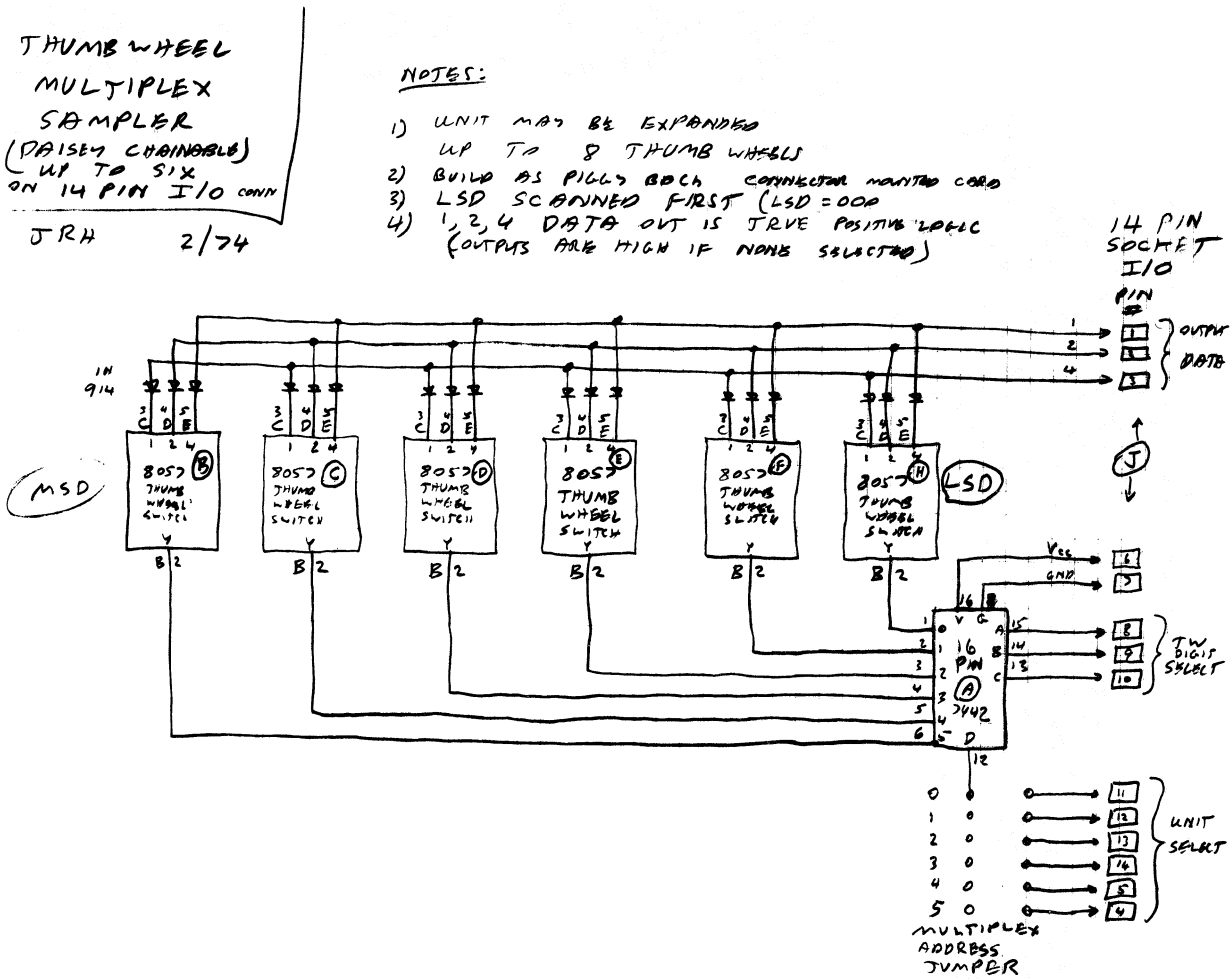
14 R899-1-1K RESISTOR CHIP
R_{13} R_{12} R_{11} R_{10} R_9 R_8
R_1 R_2 R_3 R_4 R_5 R_6 R_7

CROSS CORRELATION RECEIVER
DIGITAL DELAY GENERATOR
COMPUTER INTERFACE
SERIAL XMIT LINK

JRM 4-72

Thumbwheel Multiplex

The schematic of the thumbwheel interface circuits is presented. The circuit interfaces directly with the "interface and control" card with all five gangs of thumbwheels on the same ribbon cable.

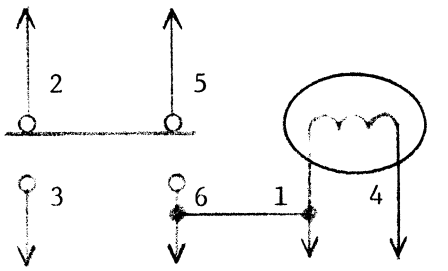


Wire Lists

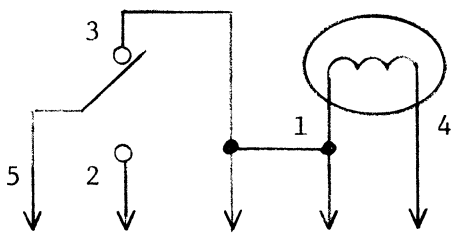
The following are the wire lists for the outboard box and changes to the correlator digital rack.

WIRE LIST FOR
CROSS-CORRELATION RECEIVER DIGITAL DELAY GENERATOR

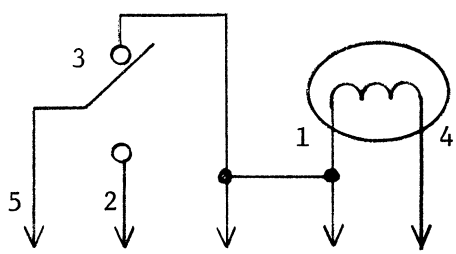
Manual Control



Delay System Bypass

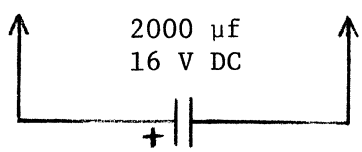


Power Control

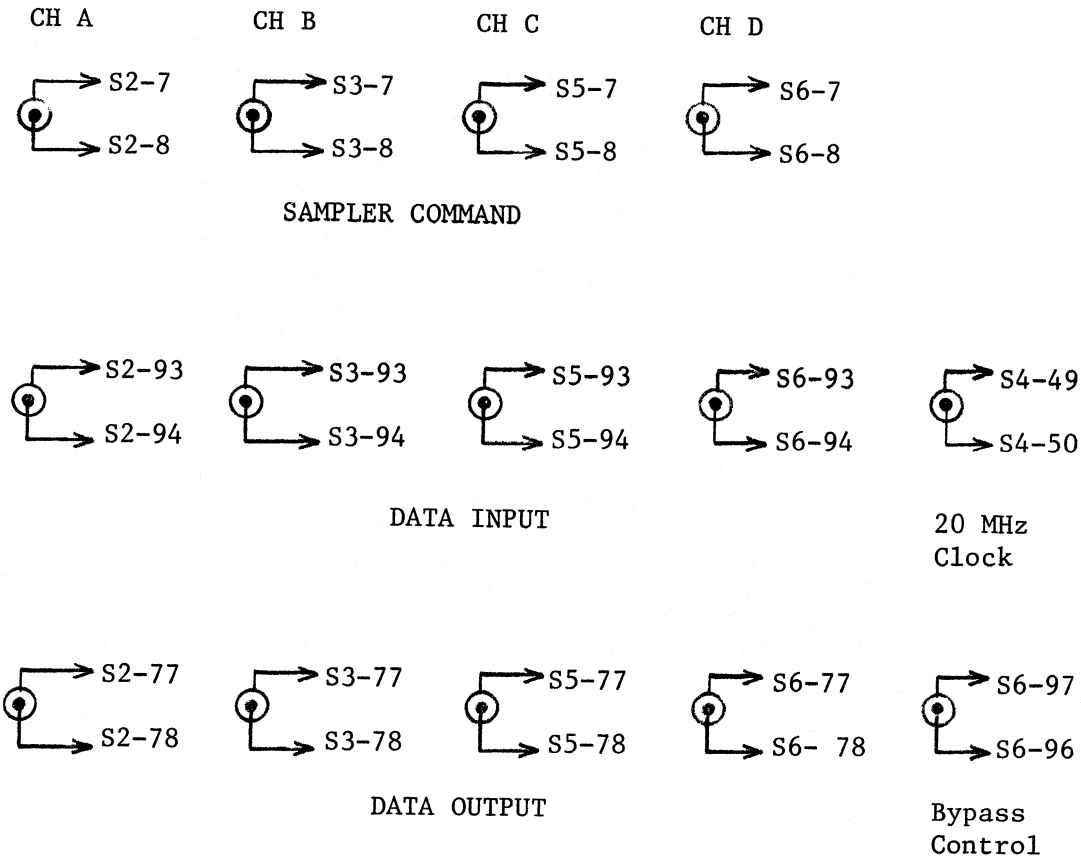


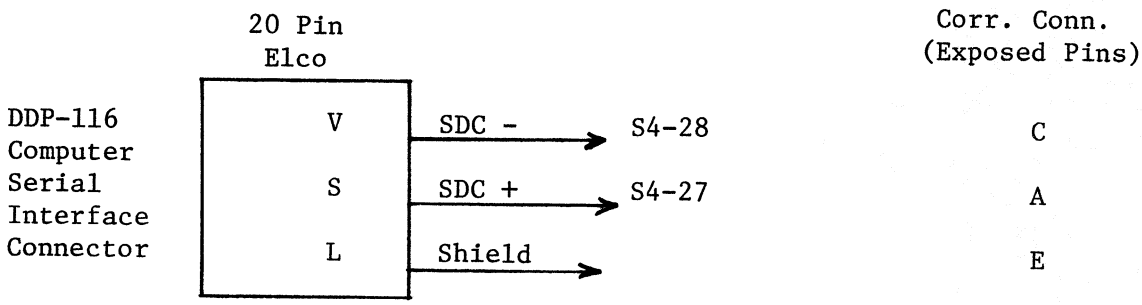
Make the following connections for power to the logic cards:

+5	Gnd
S2-2	S2-1
S2-4	S2-3
S2-98	S2-97
S2-100	S2-99
S3-2	S3-1
S3-4	S3-3
S3-98	S3-97
S3-100	S3-99
S4-2	S4-1
S4-4	S4-3
S4-98	S4-97
S4-100	S4-99
S5-2	S5-1
S5-4	S5-3
S5-98	S5-97
S5-100	S5-99
S6-2	S6-1
S6-4	S6-3
S6-98	S6-97
S6-100	S6-99

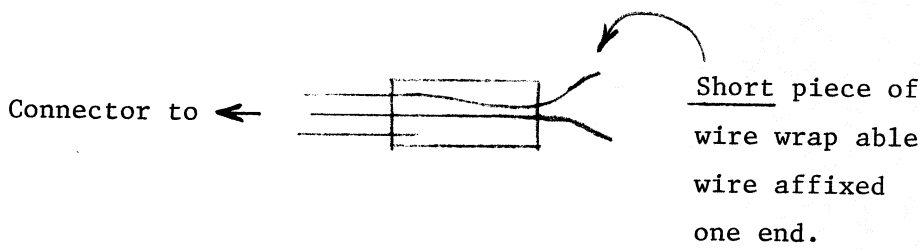


Use large buss wire for all power connections and solder, being careful not to get solder on portion of wire wrap pins needed for wire wrap connections. (Leave room for two standard wire wrap wires on each power pin.)





Use 50 ohm coax to make connections.



- 18a -

CARD: DG (A)

SLOT: 2

1	Gnd Buss	2	+5 Buss
3	Gnd Buss	4	+5 Buss
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55		56	
57		58	
59		60	
61		62	
63		64	
65		66	
67		68	
69	S3-69	70	S3-70
71		72	
73		74	
75		76	
77		78	
79		80	
81		82	
83		84	
85		86	
87		88	
89		90	
91		92	
93		94	
95		96	
97	Gnd Buss	98	+5 Buss
99	Gnd Buss	100	+5 Buss

- 18b -

CARD: (Control)

PI = Panel Interface Card

SLOT: 4

1	Gnd	2	+5
3	Gnd, T-7	4	+5, T-6
5	T-8	6	T-9
7	T-5	8	T-10
9	T-4	10	T-12
11	T-3	12	T-13
13	T-2	14	T-14
15	T-1	16	---
17	S2-26	18	S2-25
19	S2-24	20	S2-23
21	S2-22	22	S2-21
23	S2-20	24	S2-19
25	S2-18	26	S2-17
27	DDP Control Input Pin S	28	DDP Control Input Pin J
29	S2-16	30	S2-15
31	S2-14	32	S2-13
33	S2-12	34	S2-11
35	S3-26	36	S3-25
37	S3-24	38	S3-23
39	S3-33	40	S3-21
41	S3-20	42	S3-19
43	S3-18	44	S3-17
45	S3-16	46	S3-15
47	S3-14	48	S3-13
49	---	50	---
51	S3-12	52	S3-11
53	S5-26	54	S5-25
55	S5-24	56	S5-23
57	S5-22	58	S5-21
59	S5-20	60	S5-19
61	S5-18	62	S5-17
63	S5-16	64	S5-15
65	S5-14	66	S5-13
67	S5-12	68	S5-11
69	S6-26	70	S6-25
71	S6-24	72	S6-23
73	S3-69, S5-69	74	S3-70, S5-70
75	S6-22	76	S6-21
77	S6-20	78	S6-19
79	S6-18	80	S6-17
81	S6-16	82	S6-15
83	S6-14	84	S6-13
85	S6-12	86	S6-11
87	S6-64	88	S5-64
89	S3-64	90	S2-64
91	B-7	92	B-6
93	B-5	94	B-4
95	B-3	96	B-14
97	Gnd, B-1, B-2	98	+5, B-9, B-8
99	Gnd	100	+5

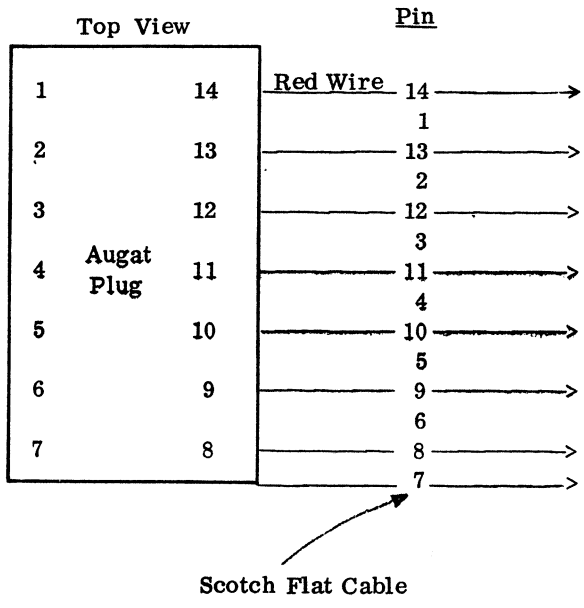
- 18c -

CARD: DG (D)

SLOT: 6

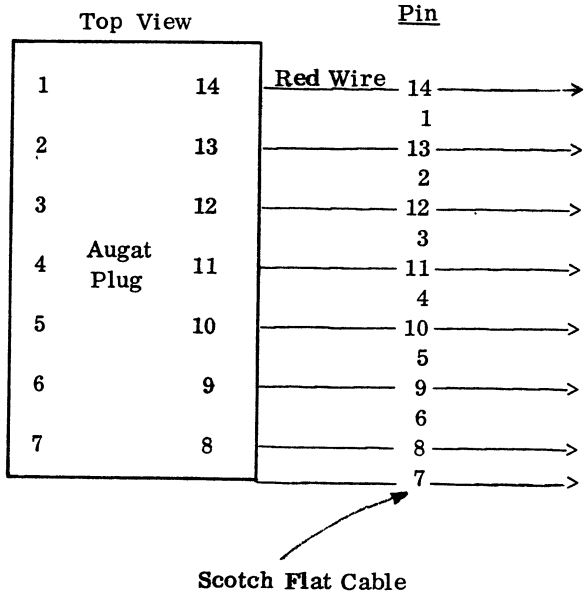
1		2	
3		4	
5		6	
7		8	
9		10	
11		12	
13		14	
15		16	
17		18	
19		20	
21		22	
23		24	
25		26	
27		28	
29		30	
31		32	
33		34	
35		36	
37		38	
39		40	
41		42	
43		44	
45		46	
47		48	
49		50	
51		52	
53		54	
55		56	
57		58	
59		60	
61		62	
63		64	
65		66	
67		68	
69	S5-69	70	S5-70
71		72	
73		74	
75		76	
77		78	
79		80	
81		82	
83		84	
85		86	
87		88	
89		90	
91		92	
93		94	
95		96	
97		98	
99		100	

14 PIN AUGAT/SCOTCH CABLE FAN OUT



FOR: THUMBWHEEL MULTIPLEX

14 PIN AUGAT/SCOTCH CABLE FAN OUT



FOR: BINARY DISPLAY (CONTROL REGISTER) (BINARY WORD)

UC = Unit Clock

UD = Unit Data

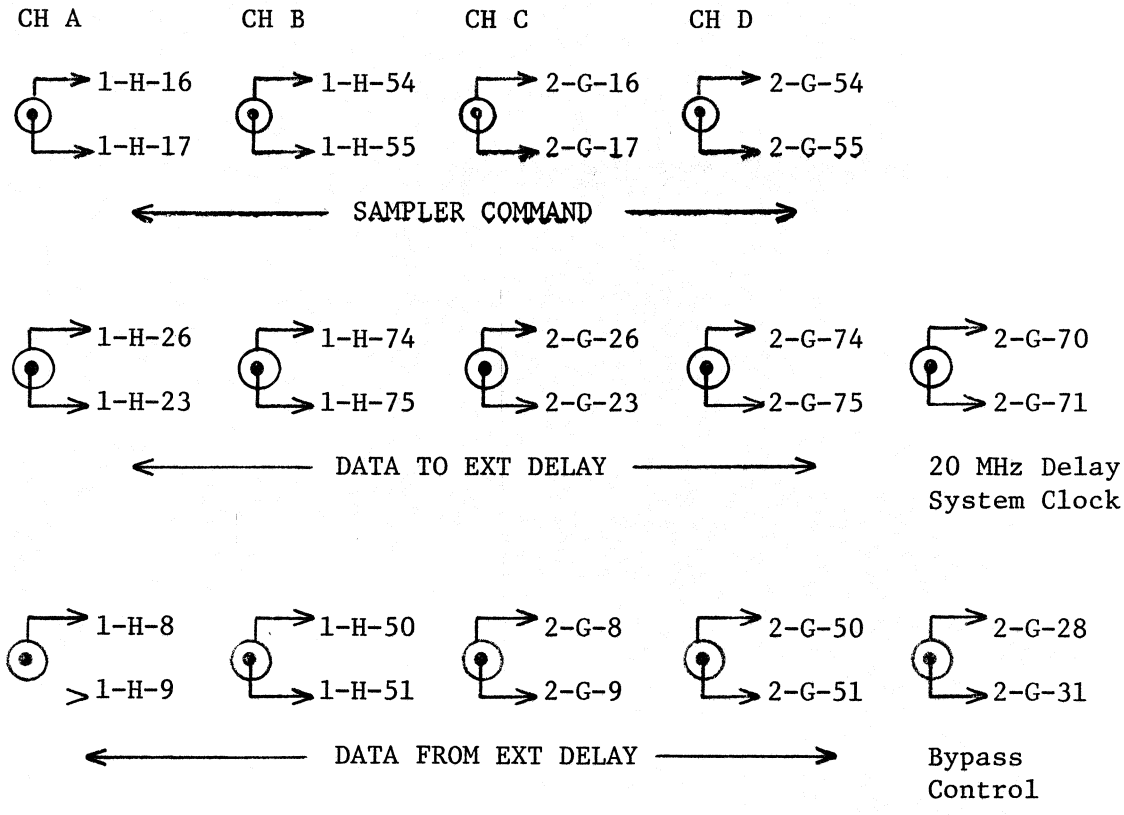
WIRE LIST

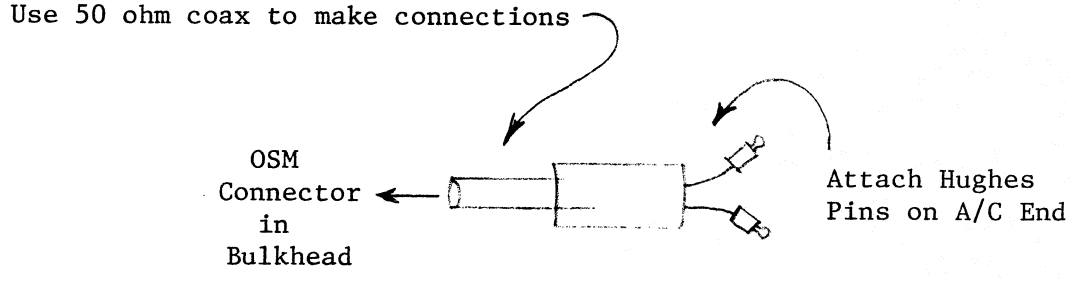
4-CHANNEL DIGITAL DELAY SYSTEM
ADDITIONS TO AUTO/CROSS-CORRELATION RECEIVER DIGITAL RACK

CARD: Sampler II

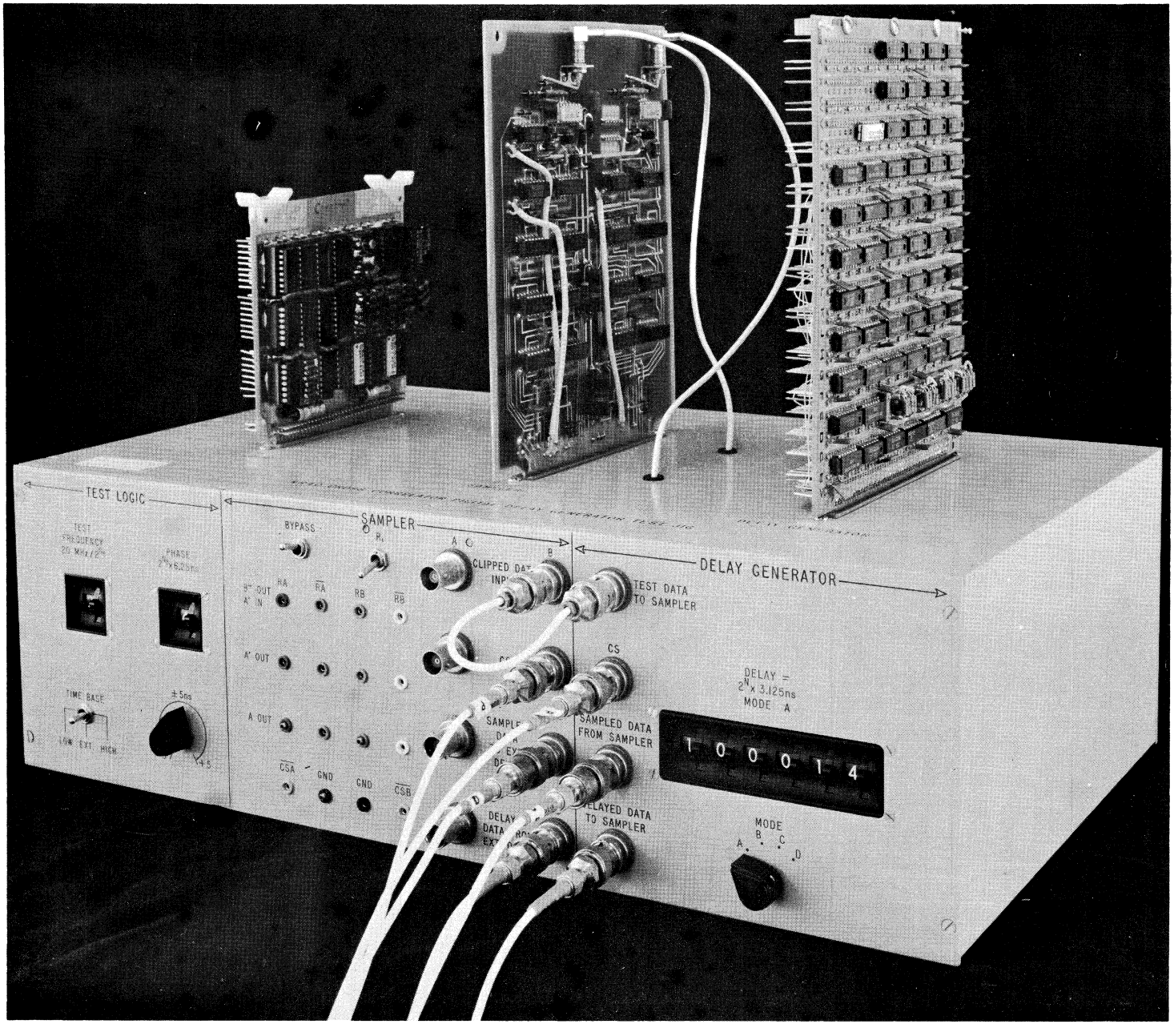
SLOT: 2-G (There were no modifications made to Slot 1-H (Sampler A & B)).

1			2	
3			4	
5			6	
7			8	
9			10	
11			12	
13			14	
15			16	
17			18	
19			20	
21			22	
23			24	
25			26	
27			28	1-H-28
29			30	
31	1-H-31		32	
33			34	
35			36	
37			38	
39			40	
41			42	
43			44	
45			46	
47			48	
49			50	
51			52	
53			54	
55			56	
57			58	
59			60	
61			62	
63			64	
65			66	
67			68	
69			70	1-H-70
71			72	
73			74	
75			76	
77			78	
79	1-G-27	(G-53)	80	
81			82	
83			84	1-G-28
85			86	
87			88	
89			90	
91			92	
93			94	
95			96	
97			98	
99			100	


CH A
CH B
CH C
CH D
1-H-16
1-H-17
1-H-54
1-H-55
2-G-16
2-G-17
2-G-54
2-G-55
SAMPLER COMMAND
1-H-26
1-H-23
1-H-74
1-H-75
2-G-26
2-G-23
2-G-74
2-G-75
2-G-70
2-G-71
DATA TO EXT DELAY
20 MHz Delay
System Clock
1-H-8
1-H-9
1-H-50
1-H-51
2-G-8
2-G-9
2-G-50
2-G-51
2-G-28
2-G-31
DATA FROM EXT DELAY
Bypass
Control

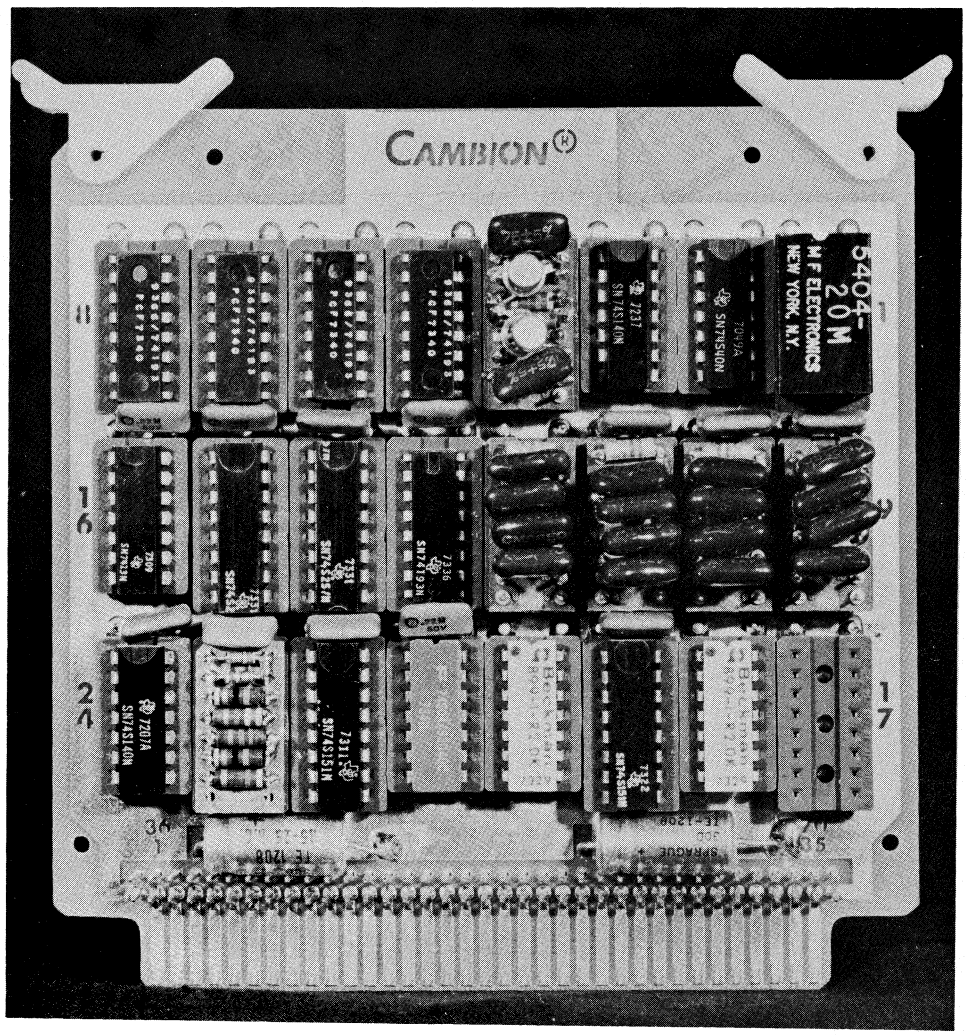

Use 50 ohm coax to make connections
OSM
Connector
in
Bulkhead
Attach Hughes
Pins on A/C End

The Delay System Test Jig



The test set will completely test the sampler card and the delay generator card by manipulation of the controls which are self explanatory. The phase control on the left adjusts the phase between the test waveform and the sampler clock.

A picture and schematic of the test jig control card follow after which the wire lists finish it.



Acknowledgment

Thanks to Ron Weimer for many helpful thoughts and suggestions and to Dick Skaggs, Jerry Turner, Bill Vrable and Doreen Morris for their aid in assembly and Martin Barkley and the Machine Shop for an excellent fabrication job.

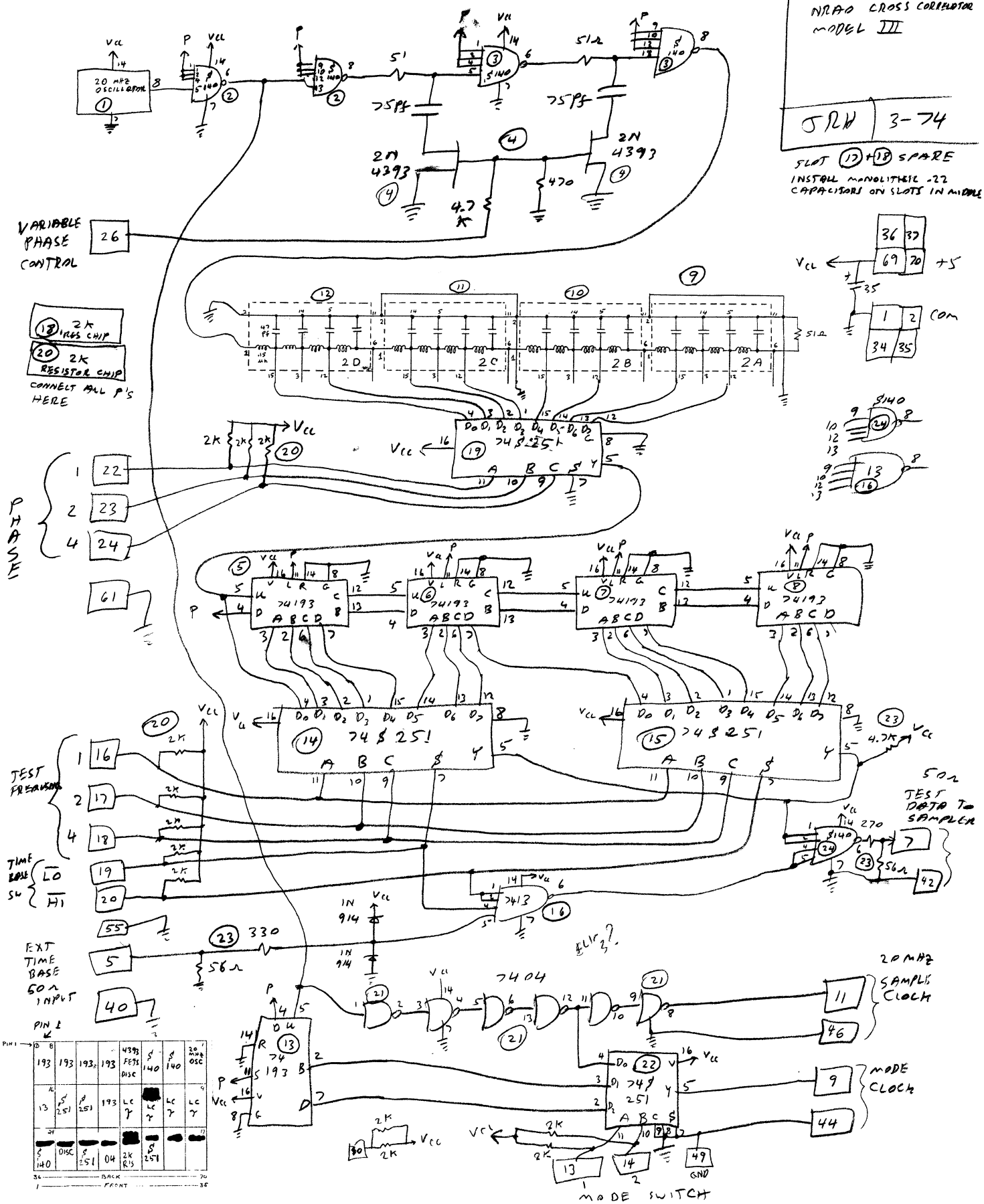
TEST LOGIC (TEST JIG)

NRAO CROSS CORRELATOR MODEL III

SRW 3-74

SLOT (12) + (18) SPARE

INSTALL MONOLITHIC .22 CAPACITORS ON SLOTS IN MIDDLE



PIN 1

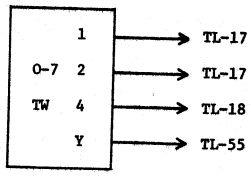
193	193	193	193	4393 FETS DISC	S 140	S 140	20 MHz OSC
13 S 251	S 251	193	LC 7	LC 7	LC 7	LC 7	
S 140	DISC	S 251	04	2K RES	S 251		

BACK 36 — 70

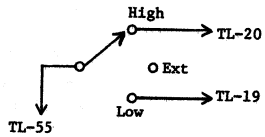
FRONT 1 — 35

TESTER MAINFRAME CIRCUITS

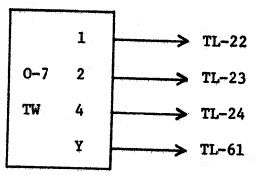
Test Frequency



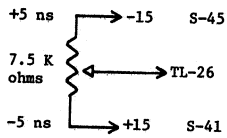
Time Base



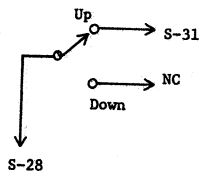
Phase



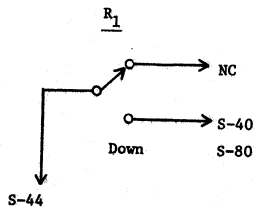
± 5 ns



Bypass



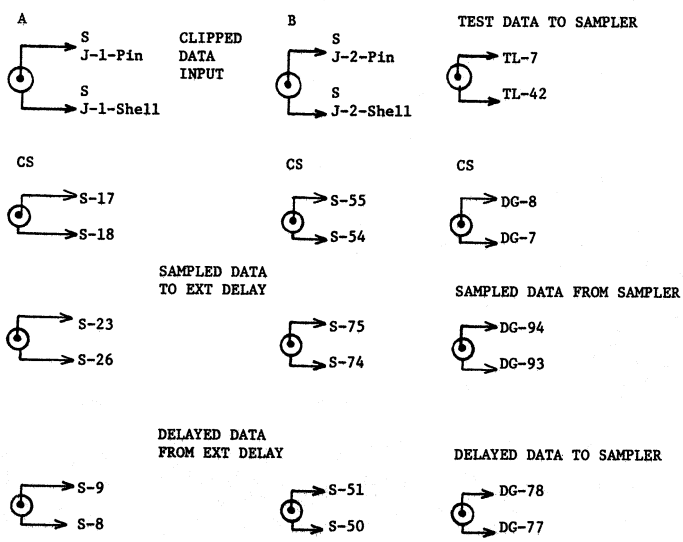
R_1



TESTER MAINFRAME CIRCUITS

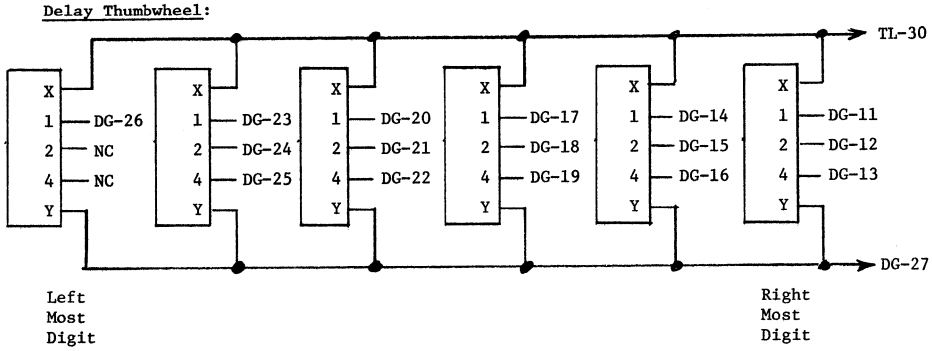
		RA	$\overline{RA}$	RB	$\overline{RB}$
B″	Out	S-21	S-25	S-73	S-77
A′	In	S-14	S-18	S-68	S-72
A′	Out	S-29	S-33	S-53	S-57
A	Out	S-7	S-11	S-60	S-65
		$\overline{CSA}$	GND	GND	$\overline{CSB}$
		S-36	S-37	S-52	S-49

Use 50 ohm coax for the following connections:

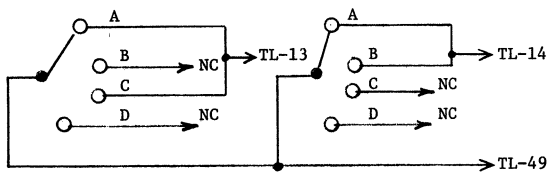


TESTER MAINFRAME CIRCUITS

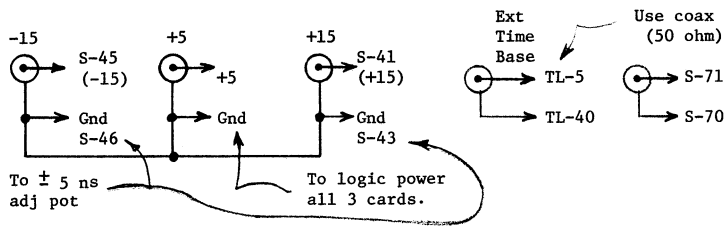
Delay Thumbwheel:



Mode Switch:



BNC's on Each Panel:



LOGIC CARD INTERCONNECTIONS

+5 BNC	to	TL-36	Gnd BNC	to	TL-1
		TL-37			TL-2
		TL-69			TL-34
		TL-70			TL-35
		S-1			S-2
		S-3			S-4
		S-83			S-84
		S-85			S-86
		DG-2			DG-1
		DG-4			DG-3
		DG-98			DG-97
		DG-100			DG-99
TL-11	to	S-36	TL-46	to	S-37
		S-49			S-52
		S-79			S-70
DG-70	to	S-36	DG-69	to	S-37
TL-9	to	DG-64			
TL-44	to	DG-63			
S-24	to	S-15	S-76	to	S-69
S-21	to	S-14	S-73	to	S-68
S-25	to	S-18	S-77	to	S-72