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256-CHANNEL FILTER RECEIVERS

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Introduction

This report discusses the design of a series of four 256-channel filter receivers having individual channel bandwidths of 0.1, 0.25, 0.5 and 1.0 MHz. These systems have an input IF center frequency of 150 MHz and can be operated as two parallel, independent, overlapping 128-channel systems or as a single series 256-channel system. They, along with a 512-channel integrator-multiplexer system ^{1/} and computer, are being used for spectrum analysis at millimeter wavelengths. Each filter system is contained in a 19 inch rack mounted drawer 8 3/4 inches high by 21 inches deep. A front view is shown on the facing page. Power supplies are in a separate 5 1/4 inch drawer, one drawer providing power for two receivers.

Channel Filters

The individual channel filters are two pole networks designed for about 0.1 dB ripple so that with coil Q variations and other tolerances the band shape remains flat. The band edges or adjacent channel crossover points are defined as 3 dB down. To obtain a constant bandwidth per channel for a series of side-by-side channels the Q's and L's must change while parallel C's and R's remain constant. Figures 1A, B, C and D show component values for sets of 16 channels for each system.

The inductors chosen are Cambion 7107 series coils. They were preferred because of metal can shielding, small size, low cost and specified ferrite

^{1/} A 512-Channel Integrator and Multiplexer by C. Pace and J. Payne, EDIR No. 134.

material. The core materials used for the values required are either Carbonyl SF or TH having permeability stabilities of .0025 and .0015%/°C. Q stability is -.04%/°C for both types. Silvered mica capacitor stability is typically +40 ppm/°C. These coefficients will produce filter shifts of less than 2% of a channel width for 10°C change. Measurements on a 1 MHz bandwidth filter at 23.5 MHz gave less than 1% of channel width shift for a 10°C change. Special coils were obtained for the 0.1 MHz system to meet higher Q requirements.

Examples of filter shapes are shown in Figure 2. The two extremes in center frequency are shown superimposed here to show the maximum shape change due to the required difference in Q's. The filter is driven from a transistor collector and its output feeds a Darlington follower. Channel circuit schematics are shown in Figure 3. The extra resistor and capacitor at the Darlington input are to suppress high frequency oscillations. Adjustments are made with a slow sweeper and with maximum post detector bandwidth (op amp input and feedback C's removed).

Detector

In previous NRAO filter systems the GE BD-7 back diode has been used as a square law detector. It is more stable with temperature than conventional diodes and provides a fairly wide square law range. The curve is adjusted by varying the DC load on the output. This adjustment did not always give satisfactory results, and in our tests it was found that the load changed the shape of the error curve as well as the tilt. It appeared to be an indirect method of curve control.

In the process of experimenting with the circuit it was discovered that source impedance was also a handle on the curve. As this was pursued, more accurate square law curves were obtained with the diode working from a controlled source impedance and into a high resistance DC load. Optimum source impedance for

for the BD-7 appeared to be around 200 ohms. This seemed rather high so some lower impedance and more economical BD-4's were ordered. These worked well with a source impedance around 25 ohms so could be driven directly from an emitter follower. DC current in the driver then became the curve control adjustment if required. A sample of diodes in the new circuit showed that the error spread without adjustment was not excessive. Replacing a few diodes could be less expensive than adding another adjustment.

The first large quantity experience with the circuit was in the 1.0 MHz system. The average error curve for CW had a 1.2% positive slope from the peak output to a level 10 dB below. This slope is less on noise but warranted a change in later systems. The emitter resistor on the detector driver was changed from 2.7 K to 2.2 K ohms. The remaining systems gave the average CW error curve and met the limits shown in Figure 4. The equivalent curve for a 0.5 MHz bandwidth noise signal is also shown. The data was recorded at minimum op amp gain but has been shifted to represent an average gain setting. Using the limits shown about 10% of the diodes were rejected. In most cases a resistor change rather than the diode would have given a flat curve but there would have been more spread in the peak point level. The BD-3 may be equally satisfactory with somewhat lower source impedance and at lower cost but samples were not received in time for test.

Op Amp

The Analog Devices 741KN op amp was selected because of its excellent drift spec vs. cost. Maximum voltage drift is less than 15 $\mu\text{V}/^\circ\text{C}$. One order had very poor reliability which led to our testing of all op amps. The problem was due to a chip change to fix another problem and the result was spurious oscillations that would show up in the first few hours of operation. It resulted in the input current increasing and the output becoming noisy and drifting to saturation.

As reliability was very important a test board was made to burn in 72 op amps at a time. Each chip was operated at least 24 hours, sufficient time to catch nearly all bad actors as the manufacturer stated and our experience supported. As an additional test the IC's were cycled from 25 to 45°C, the drifts measured and all units exceeding 1/2 the voltage drift specifications were not used. This rejected about 10%. All oscillating chips were replaced by Analog Devices without charge. Had the reliability problem been suspected at the time the p.c. board layout was made, space for some type of socket or individual pins would have been provided.

The op amp is operated at a gain of about 400, so 15 $\mu\text{V}/^\circ\text{C}$ would produce 6 $\text{mV}/^\circ\text{C}$ at the output. If the normal output is 4 V this represents 0.15%/°C. This figure could be reduced by use of a more expensive op amp such as the Precision Monolithics OP-05CJ but the improvement was not considered justified. The detector diode has a drift of about 0.15%/°C. Also, new computer programs measure and correct for zero and square law errors. Molded carbon resistors drift about .02%/°C so precision resistors would be desirable if significant improvement were attempted.

Filter Board

The channel circuit, as with all other parts of the system, was designed with compactness, simplicity, and cost in mind. To build 256 channels in the space of some previous 50 channel receivers made packaging a prime consideration. On the filter boards it was necessary to provide convenient access to op amp gain and zero controls. Individual channel monitoring on the boards would permit uninterrupted output wiring from the filter card connector to the back panel connector. As many as 25 filter cards have been stacked side-by-side across the width of a drawer but without shields and with very limited height for components.

The 256 channels makes 16 a convenient number to work with and a 16-channel multiplexer chip suitable for monitoring became available at that time. So as originally suggested in the job outline the cards were designed for 16 channels each.

The logical arrangement for best high frequency performance and location of adjustments was to feed a signal down the middle of the board and have the channel circuits branch out in opposite directions. Refer to Figure 5 for the board layout. There was concern over coupling between adjacent channels with close physical spacing, so three things were done to reduce the probability. First, shields were added between cards. Second, the channel layout was arranged to return all grounds to one side of the circuit so that ground currents from two sections would not flow in common land areas. Third, the channels were staggered so that adjacent frequencies were not physically adjacent. There are at least two channel widths between adjacent circuits. Breadboard checks showed the coupling between adjacent circuits tuned to adjacent channels to be negligible but staggering was included as no cost insurance. Board channel numbers are identified by the color coded test points, channels 1 thru 9 along the long edge and 10 thru 16 along the short edge. White dots mark the zero pots to distinguish them from the gain controls.

The large IC is a multiplexer chip used for monitoring the output of each channel individually. Siliconix introduced the DG 506, 16-channel multiplexer shortly before this design was begun. Procurement was very slow and units failed frequently. Harris Semiconductor came to the rescue by releasing their version (HI 506) with built-in protective circuits. These proved much less susceptible to burnout and are the only recommended replacement. These chips are controlled through the digital control card by the front panel slew switch. Channel outputs are also summed thru resistors adjacent to the multiplexer IC for total power monitoring.

A second circuit near the edge connector is the input amplifier. The IF signal enters the board via small coax, is amplified 17 dB and fed to the filter circuit inputs. See Figure 25. A snap-on coax connector, mating with the Oscillator-Mixer unit, permits easier card removal.

Each filter board contains about 690 components and 160 wires and jumpers mounted in 2000 holes in an area 7.6 x 7.85 inches. The 16 filter cards, a multiplexer driver and a power monitor card are mounted in a hinged card holder. See Figure 6. This arrangement allows convenient access to zero and gain pots and channel output test points.

Channel Monitor Digital Controller

The channel monitor provides a conventional analog readout (meter) of all 256 channels selectively by connecting any one channel to the monitor meter via analog gate integrated circuits. There are 16 integrated circuits, one located on each of 16 filter bank cards; each integrated circuit comprises 16 analog gates for monitoring any one of 16 channels on a particular filter bank card.

In the schematic, Figure 7, the 16 outputs "EN-0" through "EN-15" select one only of the filter bank cards by selection of the particular analog gate integrated circuit located on the card. The 4 outputs labeled A_0 , A_1 , A_2 , and A_3 are binary controls which select, within a filter bank card, which channel is to be monitored.

In Figure 7, chips "C" and "R" are octal decoders which convert the binary counter "D" output to provide the "EN-" signals via inverters "J", "P", and "U" to the analog gate circuits. Binary counter "L" provides the binary count to the analog gates to select one of sixteen channels within a filter bank card.

The count control input, pin 1, is grounded in the 1.0 and 0.5 MHz systems and open in the others to modify the counting sequence. The Rev "B" input, pin E,

is grounded in the parallel mode by the Series-Parallel switch on the back panel to reverse the B section. Figures 11A, B, C, and D show the system channel numbers vs. card and card channel numbers.

The binary count provided by the up/down counters is converted to "Human" decimal terms (BCD) by "ROM" chips "A", "B", and "H". The "LCR" circuits 20 and 21 suppress any possible RFI which may issue from the TTL logic system.

Clock oscillator "E" is the system time base providing the fast (when enabled by the "ENB Fast" control input) channel step up/down sequency as controlled by the up/down select input pin 5. The "ENB Slow" signal causes the channel monitor select sequence to occur at a slower rate (4, 5, 6, 8, 10, 12, or 16 times slower) with the dividing action of chip "M" according to an arrangement of the "Speed Ratio Selector" strap pins "2", "3", and "4" and the select pin "D" and chip "M" type. Chips "N" and "BB" retime the control signals, thus preventing spurious counts when changing the monitor system control selector switch.

System

In an effort to minimize equipment the card input spectrums and oscillator frequencies were arranged to require a minimum number of oscillators. The arrangements are shown in Figures 8A, B, C, and D. The system is split into two identical sections of 128 channels each with the input center frequency at 150 MHz. By going thru the IF Processor the two sections are arranged side-by-side, still centered on 150 MHz. Ignoring the Processor for the moment, the figures show that the inputs to sections A and B are mixed with four oscillators to obtain the frequency bands for the cards. In the 1.0 and 0.5 MHz systems the oscillators are 1/2 of a card width from the closest channel. For the 0.25 and 0.1 MHz systems the spacing is 3/2 of a card bandwidth. The close spacing in the

first two systems limits the maximum frequencies on the filter cards to 24 and 12 MHz. If this arrangement were used on the second two systems the cards would have input frequencies as low as 0.8 MHz, requiring large capacitors. A second and more serious problem exists with the card filters located in the 150 MHz region. These would have to provide unusual sharpness to reject images one card bandwidth anyway. For this reason the 3/2 spacing was used. The filters provide greater than 25 dB rejection at the edge of the image band. In-band filter flatness was specified at < 1 dB, or 0.5 dB when convenient, to limit variations in power between channels.

The maximum spread of signal levels out of the detectors was limited to 1.5 dB. This was obtained by tight in-band flatness limits on the card filters, adjusting the slope on the Amplifier-Splitter units to compensate for increased mixer and filter losses at higher frequencies, and trimming some filter card input amplifier gains and individual channel gains. Close tolerances on the levels and some restricting of detector variations made it possible to operate at higher average detector levels. The 1.5 dB remaining was removed by the op amp gain controls.

Parallel input signals A and B of -30 to -40 dBm are level adjustable by 10 dB variable attenuators on the front panel. The signals are then band limited, amplified, divided and fed to four splitters. System block diagrams are shown in Figures 9A, B, C, and D. The splitters are active dividers to give good reverse isolation. Reference to an IF processing diagram will show that an LO for two card bandpasses is in the center of a third bandpass. The LO's are too close to the desired bands to obtain high rejection in the bandpass filters. It is, therefore, necessary to provide good isolation in the Splitters and Amp-Splitters. Figure 10 shows typical signal power levels and LO leakage.

Channel designations for the A and B receivers as read on the front panel and frequency charts (Figures 11A, B, C, and D) go from 0 thru 127 and 128 thru 255. Increasing channel numbers denotes increasing IF frequency for both sections in either series or parallel mode. A toggle switch on the back panel controls the reversal of the B section counting in the channel monitor circuits and provides a closure for the computer so it can arrange the data properly.

IF Processor and Oscillator-Multipliers

The IF processor input is limited by a filter to reject the image and out-of-band signals. The desired band is amplified, converted, filtered, and divided; one output feeding the B section and the second output feeding a second mixer to position the spectrum for the A section. See Figure 12. This simplified rearrangement of the spectrum is possible because mixer RF-IF isolation is > 30 dB.

The Oscillator-Multiplier units provide LO signals for the Processor. A crystal oscillator signal in the 75 to 107 MHz range is fed thru two balanced doublers and an amplifier to provide an output of about +8 dBm. See Figure 13 for a typical schematic. Unwanted signals are more than 50 dB down. One in-band signal at twice the crystal frequency is suppressed by shielding to obtain at least -65 dB. Photos of the Processor and Oscillator-Multiplier units are shown in Figure 14.

Other Units

The Amplifier-Splitters, Splitter units, Oscillator-Mixers, Power Monitor card and zero check circuit are conventional circuits that are self-explanatory by referring to their schematics in Figures 15 thru 19. Photos are shown in Figures 20 and 21.

Drawer Layout

Figures 22 and 23 show the location of major assemblies in the drawer. Access to assemblies in the bottom of a deep, crowded chassis is a problem. It was reduced on these systems by mounting the tubular card filters, Splitters and Oscillator-Mixers on two bars extending across the width of the drawer. By disconnecting the snap-on card cables, 4 Amp-Splitter output cables, a power connector and 4 screws the entire assembly can be removed. Access to the active circuits with the system operating is available by lowering the rear panel as in Figure 23. The back panel is shown in Figure 24.

Power

The power supply drawer contains two sets of supplies and a voltage monitor circuit. The supplies have isolated ground to prevent ground currents from flowing in the rack.

Power required per system

+15 V	0.95 A
-15 V	2.4 A
+5 V	0.8 A

Cost

An estimate of parts cost is as follows:

Channel circuit	\$ 16.00	
Filter board	\$ 314.00	... \$19.62/channel
System	\$8500.00	... \$33.20/channel

A spare filter card and power supplies are included in the system cost.

Acknowledgements

Recognition is given to Lewis Beale who did a major part of the construction and all of the testing. Ray Hallman contributed the digital card and readout design, and wrote the description given here.

$$Q = 1.5 f_0 / \Delta f \cdot 15 f_0 \quad L = 1/59.5 f_0^2$$

0.1 Mc/ch

$$C' = 71/f_0$$

Ch.	f_0	Q	C	L	L-	R	$R_{L_{c_{max}}}$	R_1	R_2	C'	
1	2.45 MHz	36.7	1000p	4.22μ	-20	2387	4754*	5.1k	6.2k	15	29.9
2	2.55	38.2	↑	3.90	-20	↑	4432	5.6	6.2	15	27.8
3	2.65	39.7	↑	3.61	-20	↑	4110*	6.2	7.5	15	26.8
4	2.75	41.2	↑	3.35	-19	↑	4800*	5.1	5.6	15	25.8
5	2.85	42.7	↑	3.12	-19	↑	4470*	5.6	6.2	15	24.9
6	2.95	44.2	↑	2.91	-18	↑	4540*	5.1	6.2	15	24.1
7	3.05	45.7	↑	2.72	-18	↑	4260	5.6	6.8	15	23.3
8	3.15	47.2	↑	2.55	-18	↑	3980*	6.2	7.5	10	22.5
9	3.25	48.7	↑	2.40	-17	↑	4145*	6.2	7.5	10	21.8
10	3.35	50.2	↑	2.26	-17	↑	3921	6.2	8.2	10	21.2
11	3.45	51.7	↑	2.13	-17	↑	3698	7.5	9.1	10	20.6
12	3.55	52.2	↑	2.01	-17	↑	3475*	8.2	11.	10	20.0
13	3.65	54.7	↑	1.90	-16	↑	3768*	6.8	9.1	10	19.5
14	3.75	56.2	↑	1.80	-16	↑	3581	7.5	10.	10	18.9
15	3.85	57.7	↓	1.71	-16	↓	3393	9.1	12.	10	18.4
16	3.95	59.2	1000	1.62	-16	2387	3206*	10.	15.	10	18.0

FIG. 1A

2-12-73
RSTW

0.25 MHz/ch

$$Q = 6.08 f_0$$

$$R = .194 Q/f_0$$

$$q_1 = 1.52$$

$$L = 1/32.4 f_0^2$$

$$C' = 145.6/f_0$$

$$k_{12} = .71$$

Ch	f_0	Q	C	L	L-	R	$R_{L_{c_{max}}}$	R_1	R_2	C'
1	6.125 MHz	37.2	820p	.823μ	-12	1180	1670	4.02k 3.9	4.82 4.7	23.8p
2	6.375	38.8	↑	.759	-12	↑	1670	4.02 3.9	4.82 4.7	22.8
3	6.625	40.3	↑	.703	-11	↑	1560	4.84 4.7	6.04 6.2	22.0
4	6.875	41.8	↑	.653	-11	↑	1550	4.94 5.1	6.20 6.2	21.2
5	7.125	43.3	↑	.608	-10	↑	1480	5.82 5.6	7.65 7.5	20.4
6	7.375	44.8	↑	.567	-10	↑	1430	6.75 6.8	9.33 9.1	19.7
7	7.625	46.4	↑	.531	-10	↑	1390	7.81 7.5	11.49 12.	19.1
8	7.875	47.9	↑	.498	-9	↑	1390	7.81 7.5	11.49 12.	18.5
9	8.125	49.4	↑	.468	-9	↑	1340	9.89 10.	16.62 16.	18.0
10	8.375	50.9	↑	.440	-9	↑	1290	13.84 15.	31.99 33.	17.4
11	8.625	52.4	↑	.415	-8	↑	1290	13.84 15.	31.99 33.	16.9
12	8.875	54.0	↑	.392	-8	↑	1260	18.58 18.	78.12 82.	16.4
13	9.125	55.5	↑	.371	-8	↑	1230	29.03 30	- -	16.0
14	9.375	57.0	↑	.351	-7	↑	1300	12.78 13.	26.87 27.	15.5
15	9.625	58.5	↓	.333	-7	↓	1250	21.07 22.	155.00 -	15.1
16	9.875	60.0	820	.316	-7	1180	1200	70.80 -	- -	14.7

FIG. 1B

0.5 Mc/ch

$$Q = \frac{1.5}{.5} f_0 = 3.0 f_0$$

$$L = \frac{1}{4\pi^2} \cdot 47 \cdot 10^{-9} f_0^2 = \frac{1}{195} f_0^2$$

$$C' = 166.8/f_0$$

2-5-73
1-11-74

Ch	f_0	Q	C	L	L-	R	R_{Lmax}	R_1	R_2	C'
1	4.25 MHz	12.75	470p	2.99 μ	-19	1016	4.16	1344	1.3	39.25p
2	4.75	14.25		2.39	-17		3.50	1432	1.5	35.1
3	5.25	15.75		1.96	-16		2.96	1547	1.6	31.8
4	5.75	17.25		1.63	-15		3.00	1536	1.5	29.0
5	6.25	18.75		1.38	-15		2.9	1515	1.5	26.7
6	6.75	20.25		1.18	-14		2.64	1652	1.6	24.7
7	7.25	21.75		1.03	-13		2.55	1676	1.6	23.0
8	7.75	23.25		.998	-12		2.49	1716	1.8	21.5
9	8.25	24.75		.792	-12		2.25	1762	1.8	20.2
10	8.75	26.25		.704	-11		2.28	1833	1.8	19.1
11	9.25	27.75		.630	-11		2.2	1873	1.8	18.0
12	9.75	29.25		.567	-10		2.07	1945	2.0	17.1
13	10.25	30.75		.513	-10		1.96	2044	2.0	16.3
14	10.75	32.25		.466	-9		1.93	2145	2.2	15.5
15	11.25	33.75		.426	-9		1.67	1.80	2.4	14.8
16	11.75	35.25	470	.390	-8	1016	1.676	1.81	2.4	14.2

FIG 1C

$$Q = 1.62 f_0$$

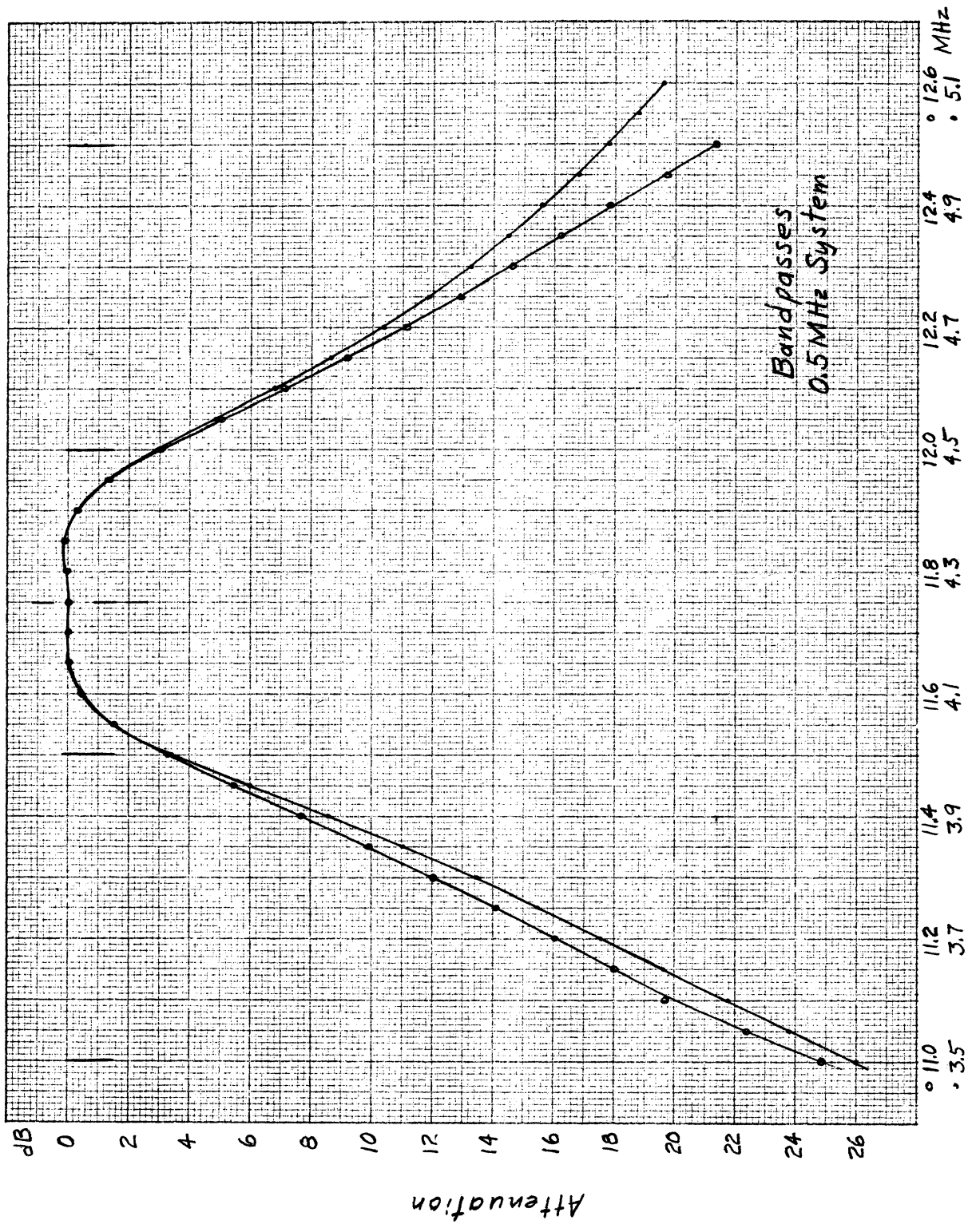
$$C' = 184/f_0$$

1.0 MHz/ch

$$L = \frac{1}{1017} f_0^2$$

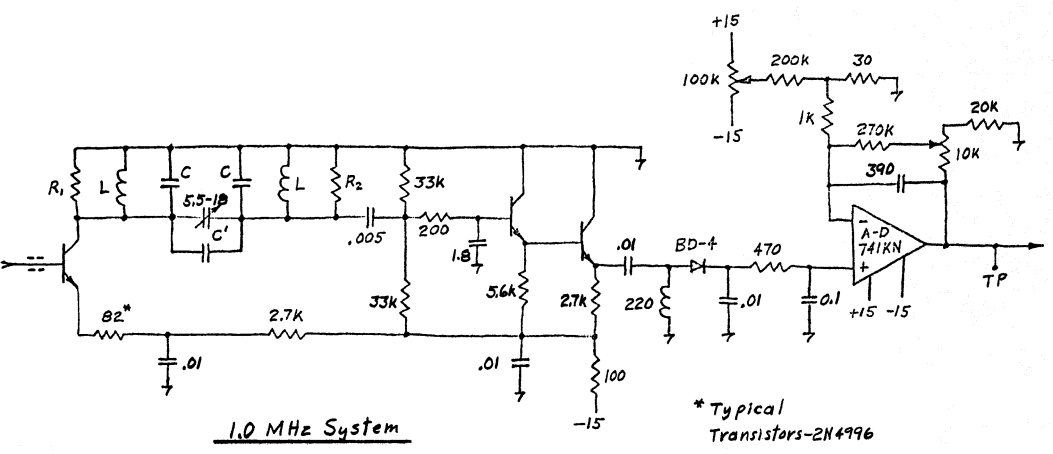
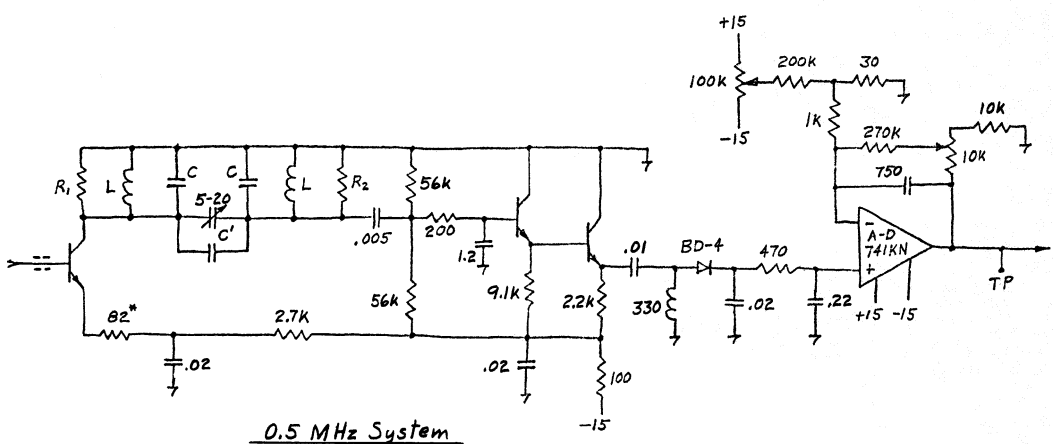
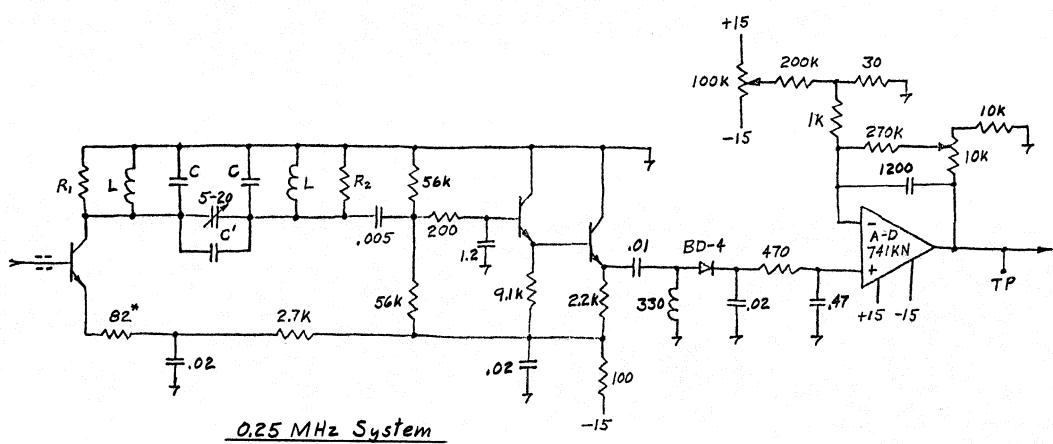
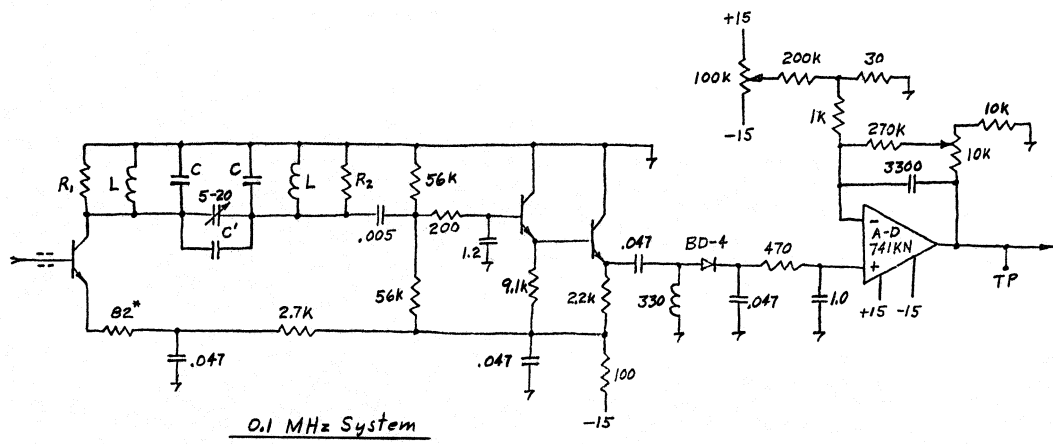
Ch.	f_0	Q	C	L	L-	R	R_{Lmax}	R_1	R_2	C'
1	8.5 MHz	13.8	250p (25p)	1.361 μ	15	1000	4.55k Ω	1.31k Ω	1.43k Ω	21.6p
2	9.5	15.4		1.089	13		4.00	1.36	1.50	19.3
3	10.5	17.0		.992	12		3.58	1.42	1.57	17.5
4	11.5	18.6		.743	11		3.45	1.44	1.60	16.0
5	12.5	20.2		.629	11		3.32	1.47	1.62	14.7
6	13.5	21.9		.539	10		3.20	1.49	1.65	13.6
7	14.5	23.5		.468	9		3.10	1.52	1.68	12.7
8	15.5	25.1		.409	8		2.95	1.56	1.73	11.8
9	16.5	26.7		.361	7		2.85	1.59	1.77	11.1
10	17.5	28.3		.321	7		2.70	1.64	1.83	10.5
11	18.5	30.0		.287	6		2.60	1.68	1.88	9.9
12	19.5	31.6		.258	6		2.48	1.74	1.94	9.4
13	20.5	33.2		.234	5		2.35	1.81	2.03	9.0
14	21.5	34.8		.213	5		2.23	1.90	2.14	8.5
15	22.5	36.5		.194	4		2.11	2.00	2.26	8.2
16	23.5	38.1	250	.178	4	1000	2.00	2.12	2.41	7.8

FIG. 1D



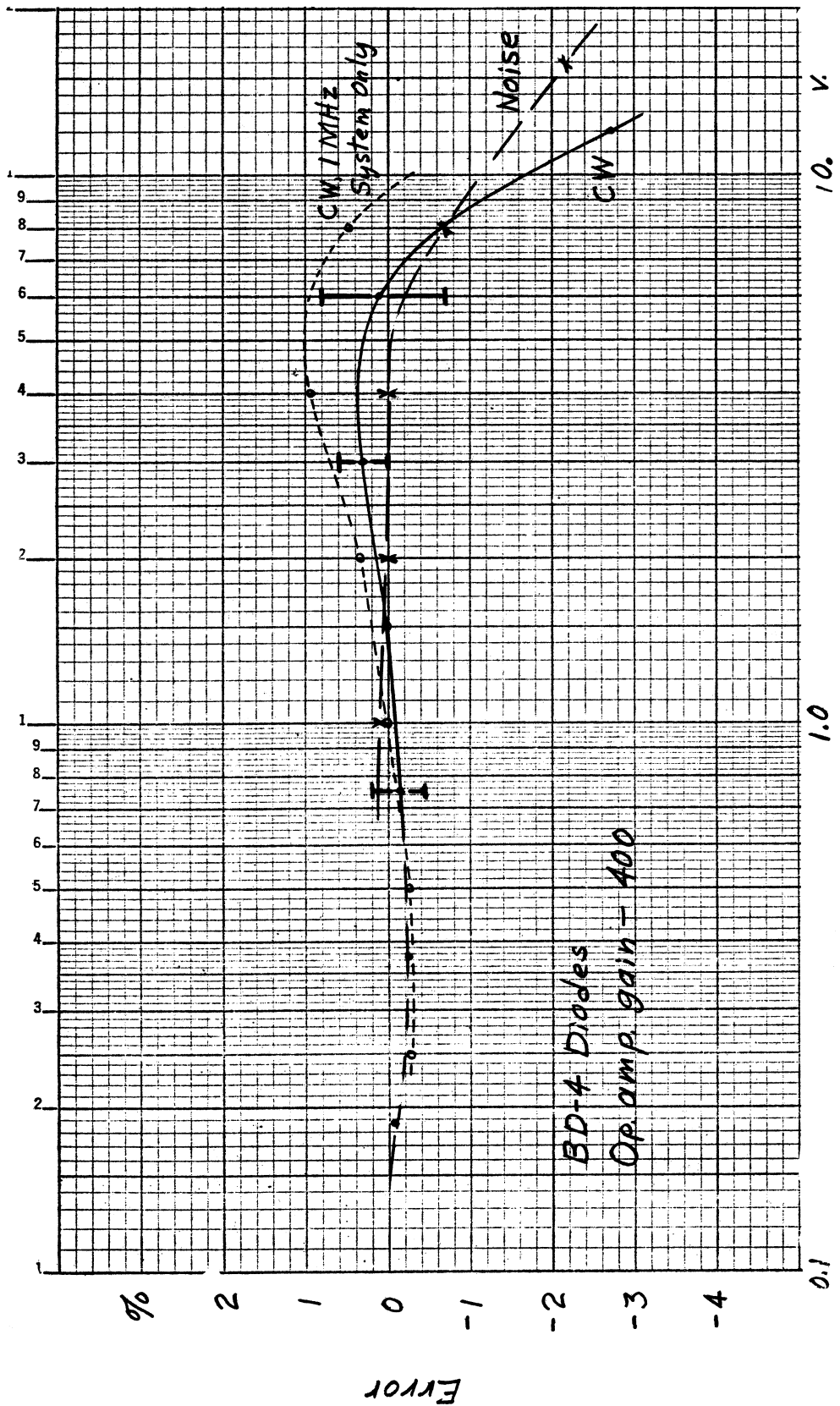
Frequency

FIG. 2



* Typical Transistors-2N4996

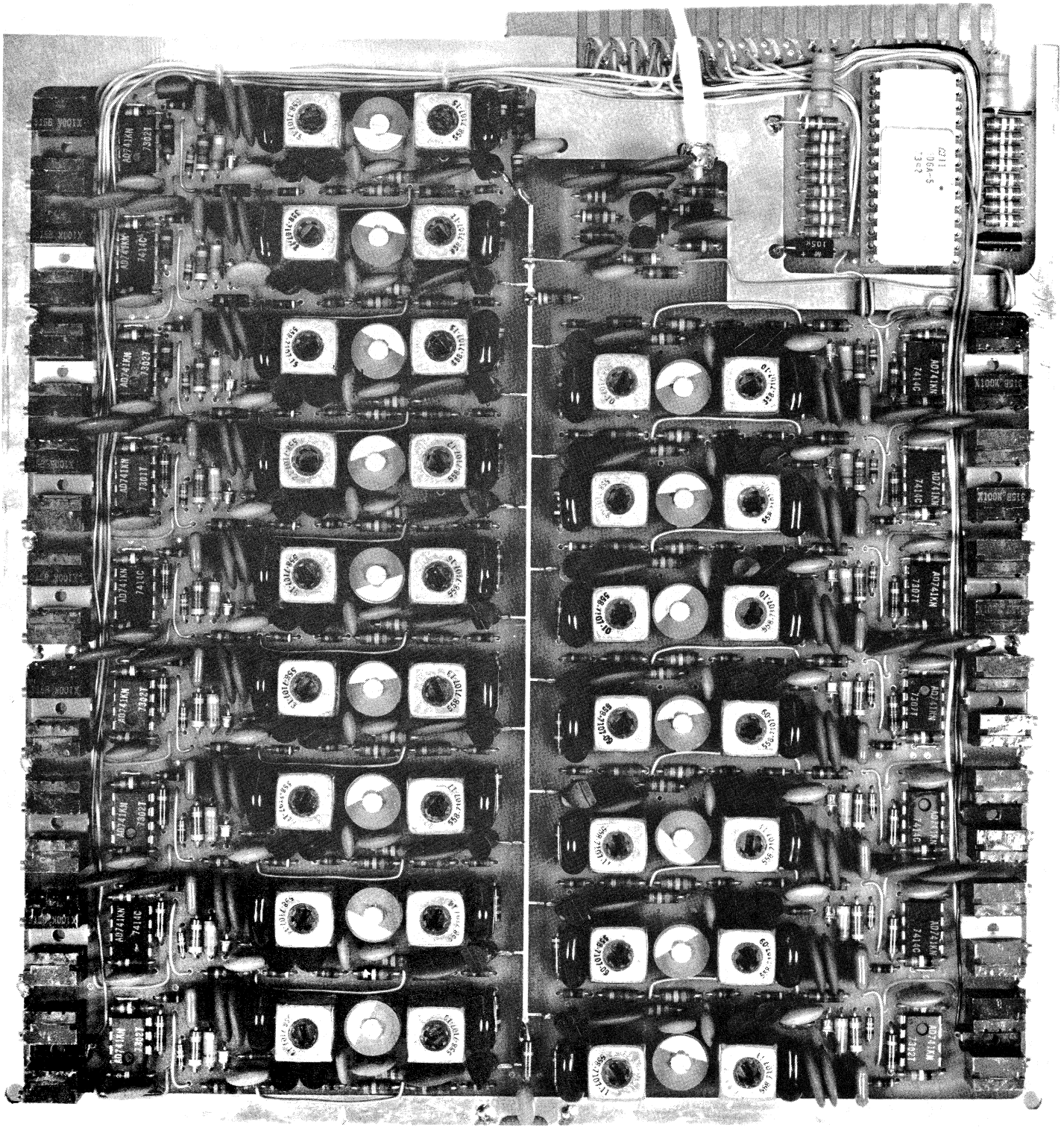
FIGURE 3



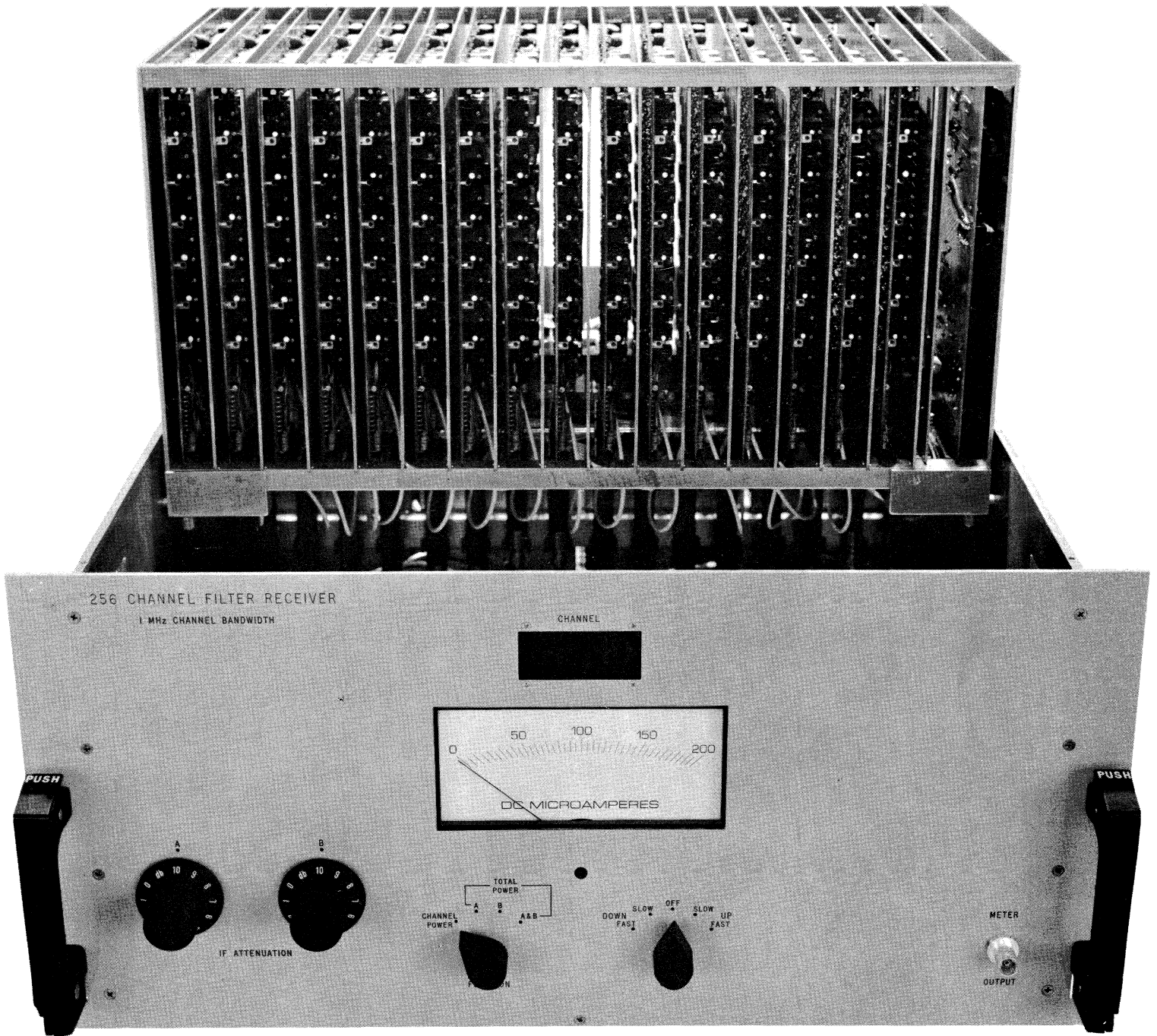
Output Voltage

Square Law Detector Error

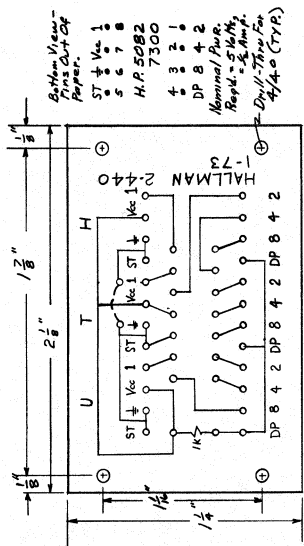
FIG. 4



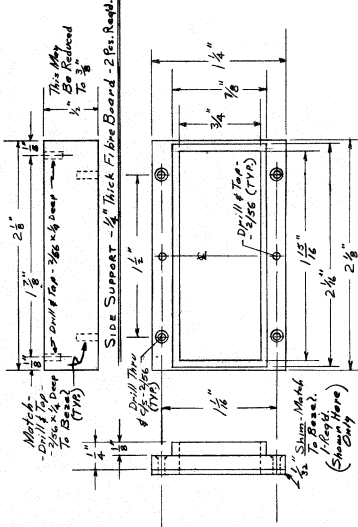
FILTER CARD
FIGURE 5



CARD HOLDER UP
FIGURE 6



3 DIGIT GENERAL PURPOSE DISPLAY - M.S. 2579-1
 Independent Panel BCD Data / Simple Side
 No Drive / Print On / Stroke / P.C. Board
 Copper Side Shows I/O 1/8 Pin Conn. Mounting
 This Side. Displays Mount on Other Side.
 For Use With Standard Bezel & Digit Gen.
 Repose Display With Parallel Data.



BEZEL - 1. Repose - Scale 2:1
 Paint With BLACK Epoxy -
 Berke On External.

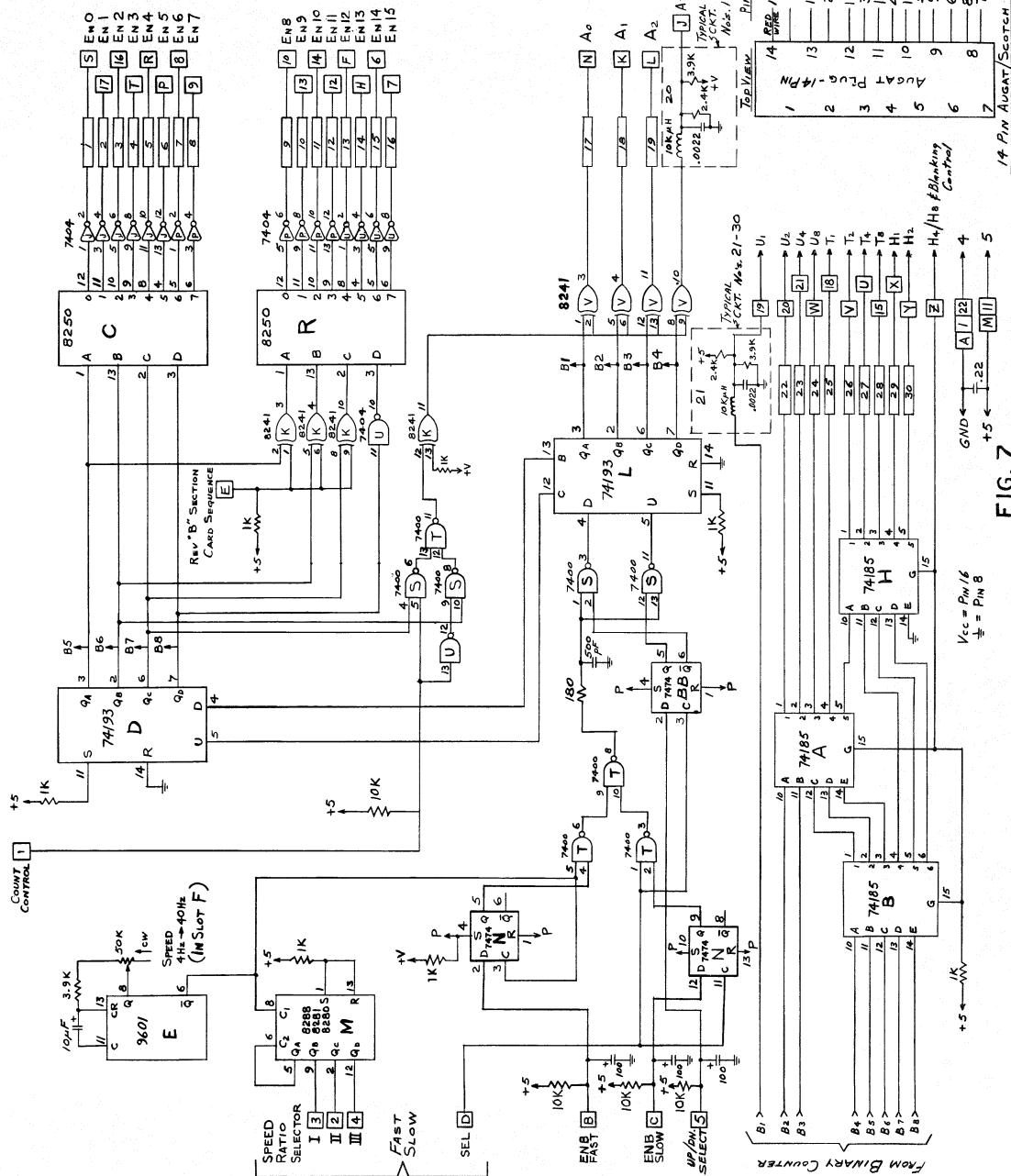
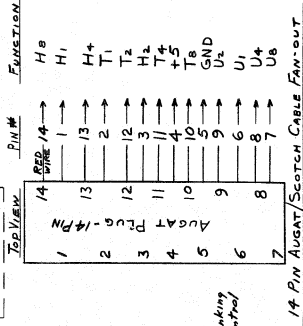


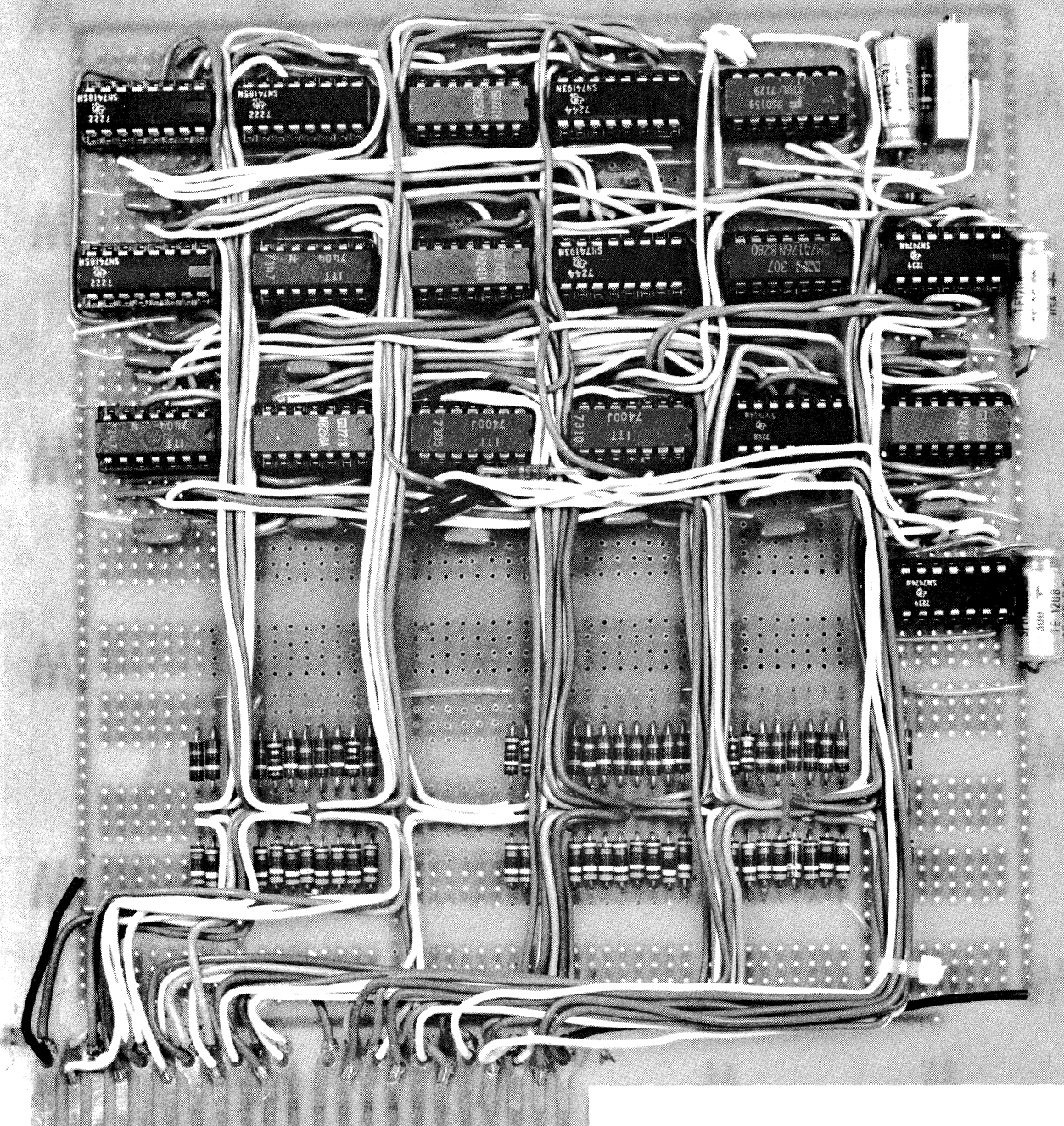
FIG. 7

V_{CC} = Pin 16
 ⚬ = Pin 8

NATIONAL RADIO ASTRONOMY OBSERVATORY		
TITLE 256 Channel Multiplex Receiver Channel Monitor System - Driver Channel Multiplex Control		
DESIGNED BY J.H.	DATE 3-29-73	DRAWN BY
APPROVED BY		
NO. REVISIONS		
1		
REV. NO. S-2579-1		



OK
4



CHANNEL MONITOR DIGITAL CONTROLLER

1.0 MHz IF Processing

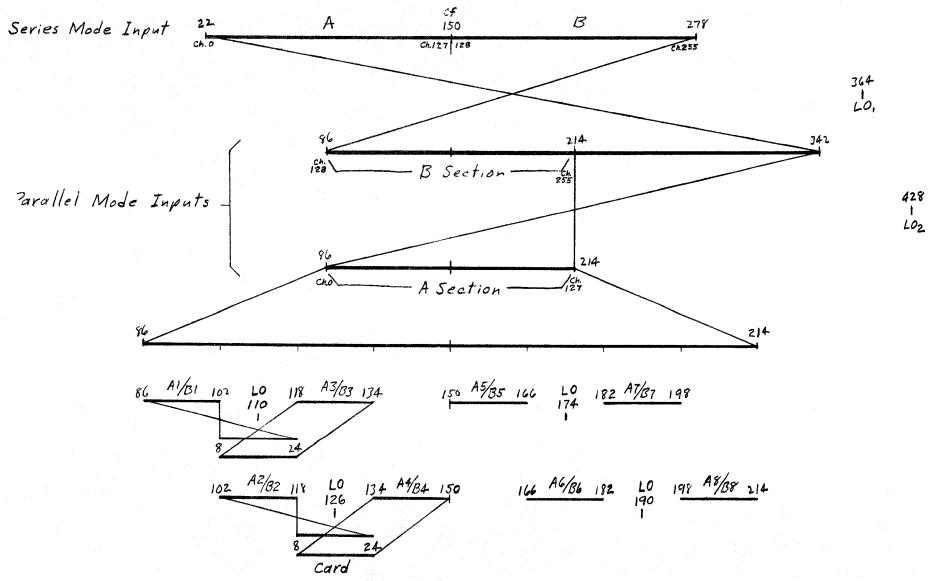


FIGURE 8A

0.5 MHz IF Processing

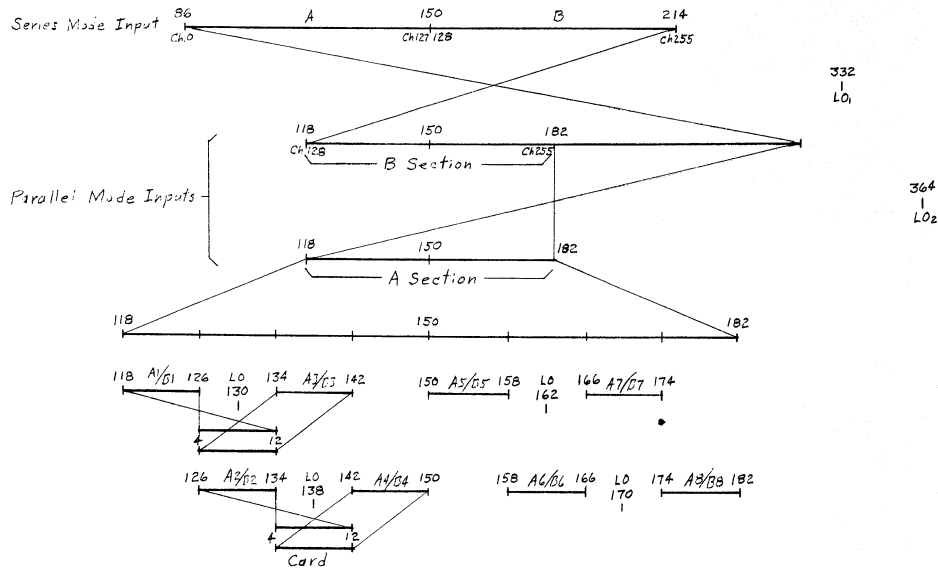


FIGURE 8B

0.25 MHz IF Processing

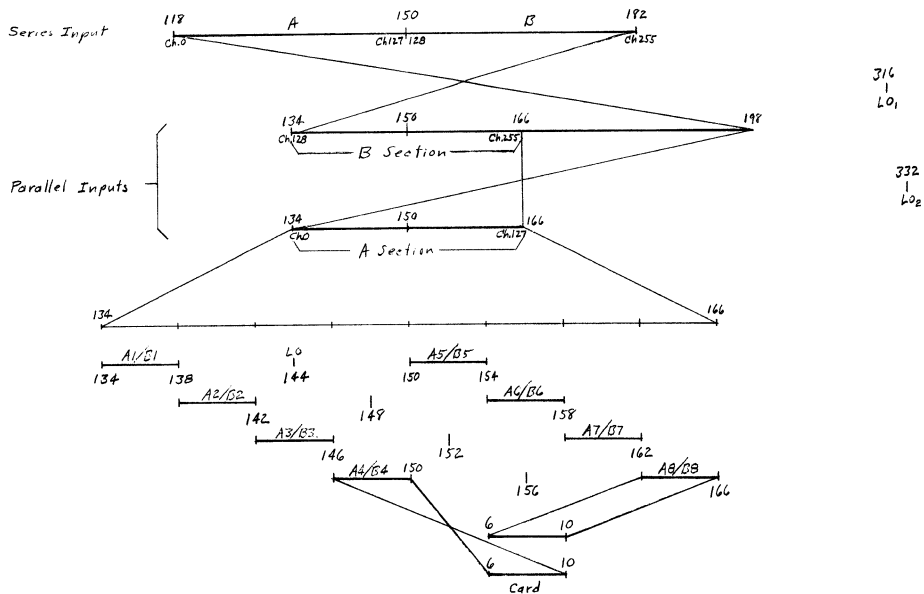


FIGURE 8C

0.1 MHz IF Processing

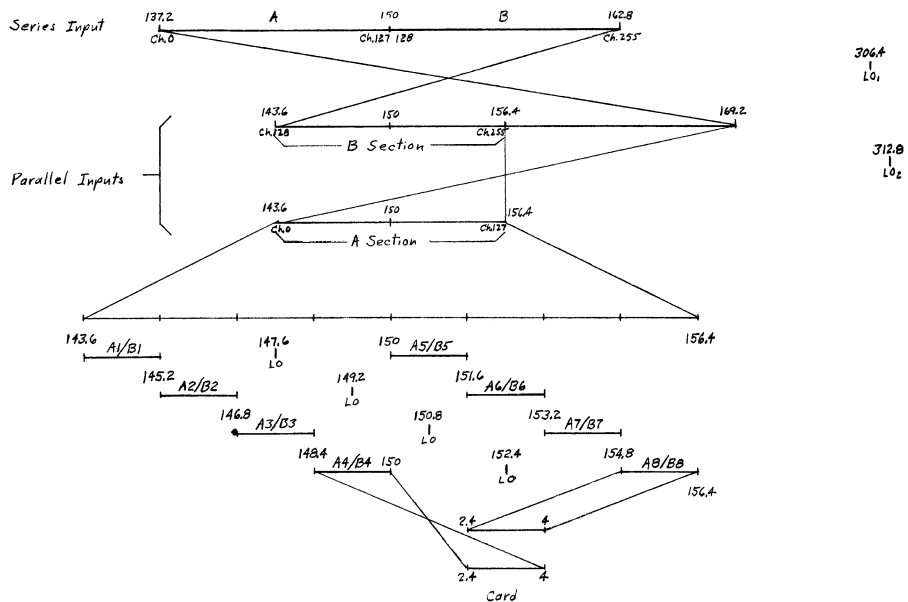
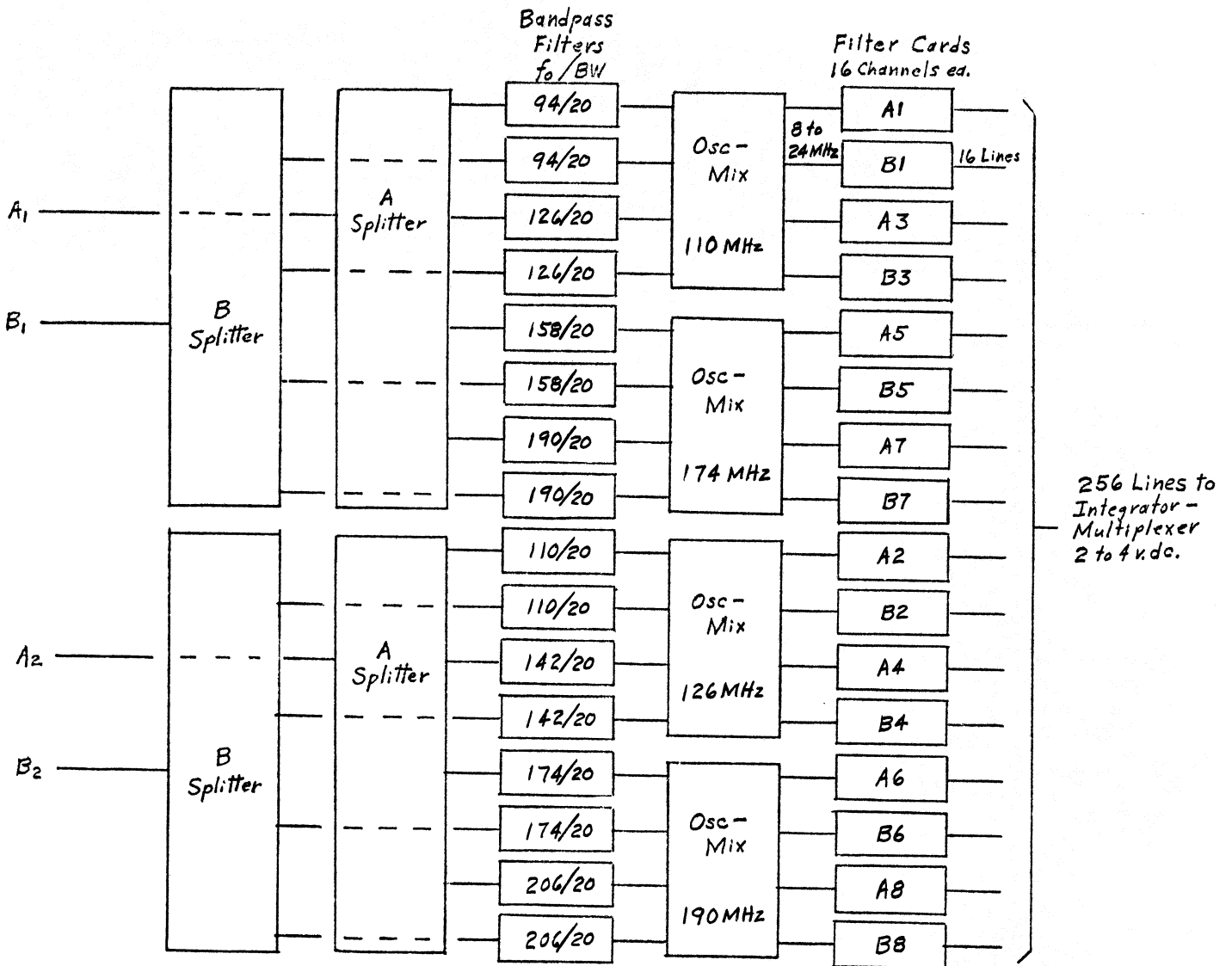
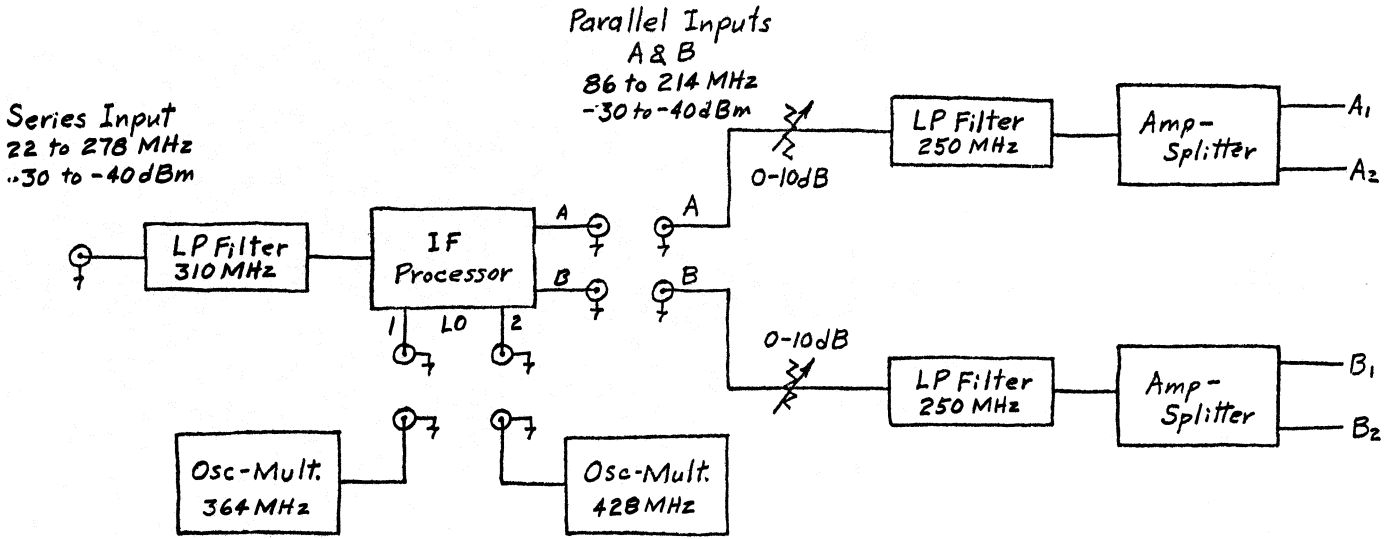
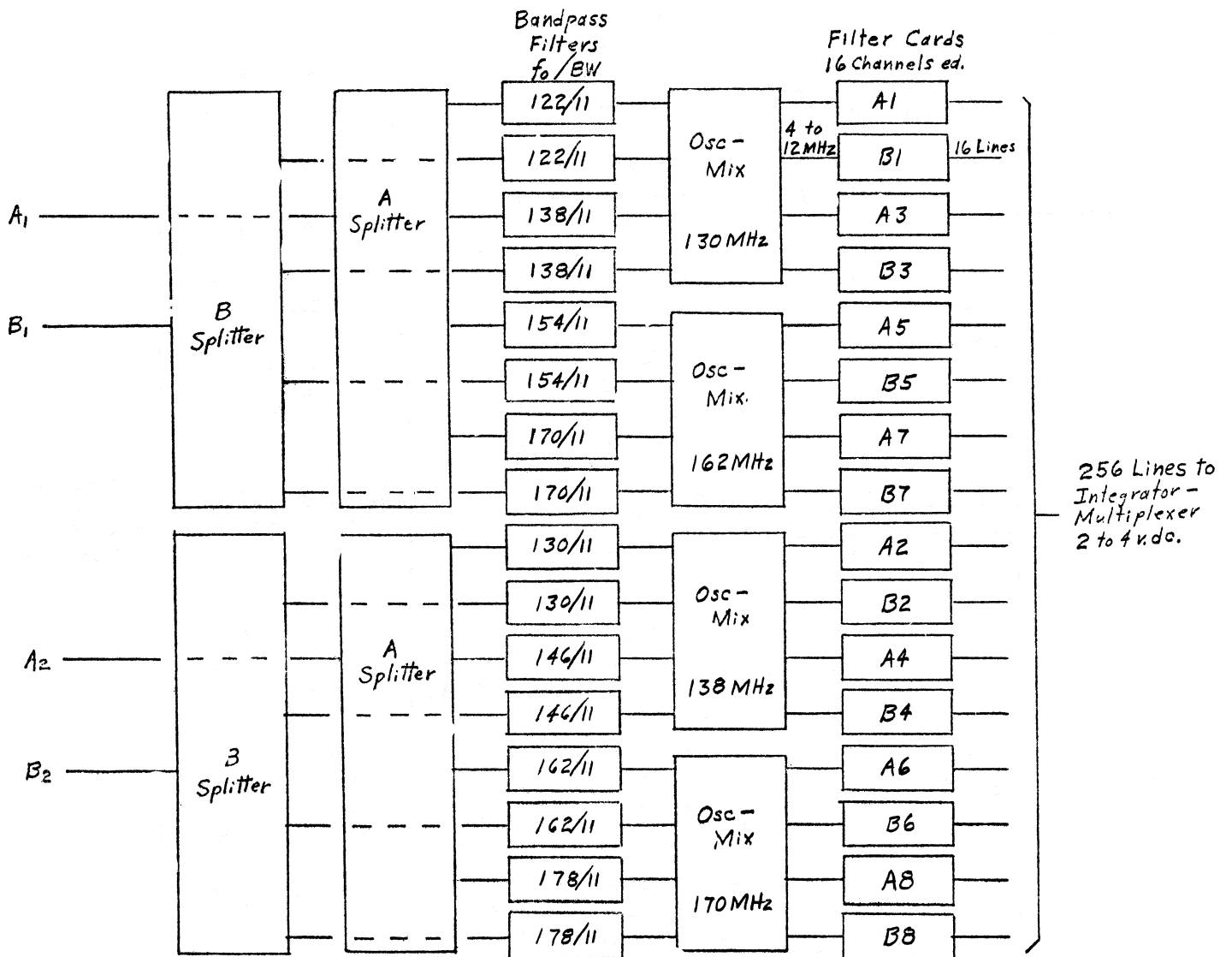
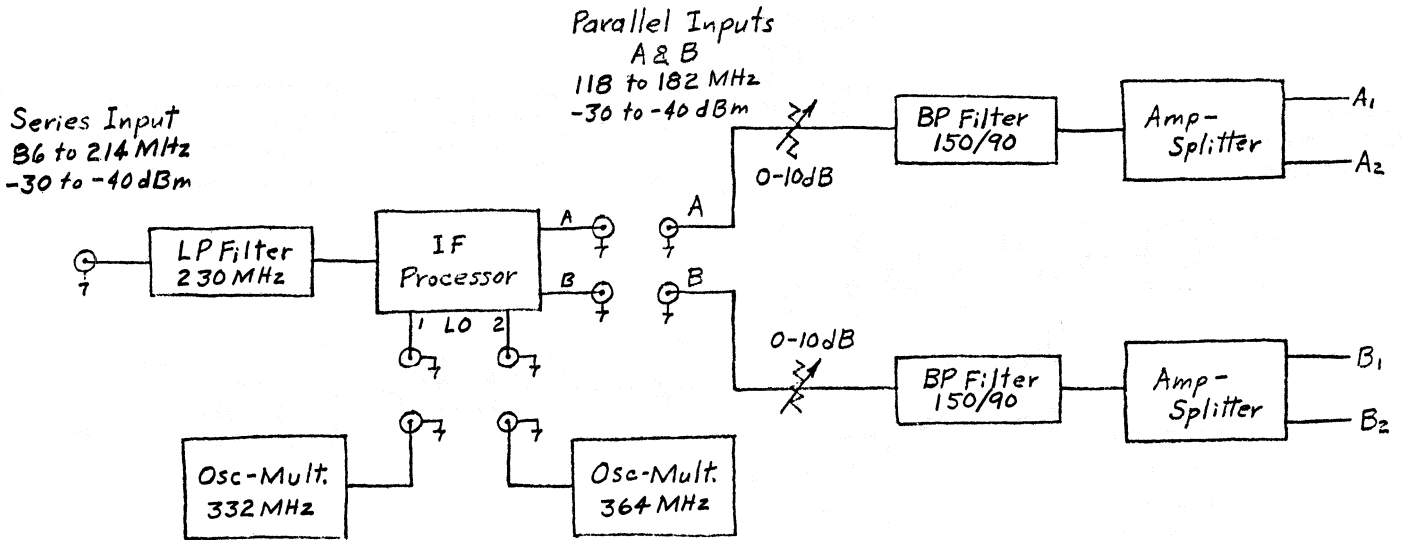


FIGURE 8D



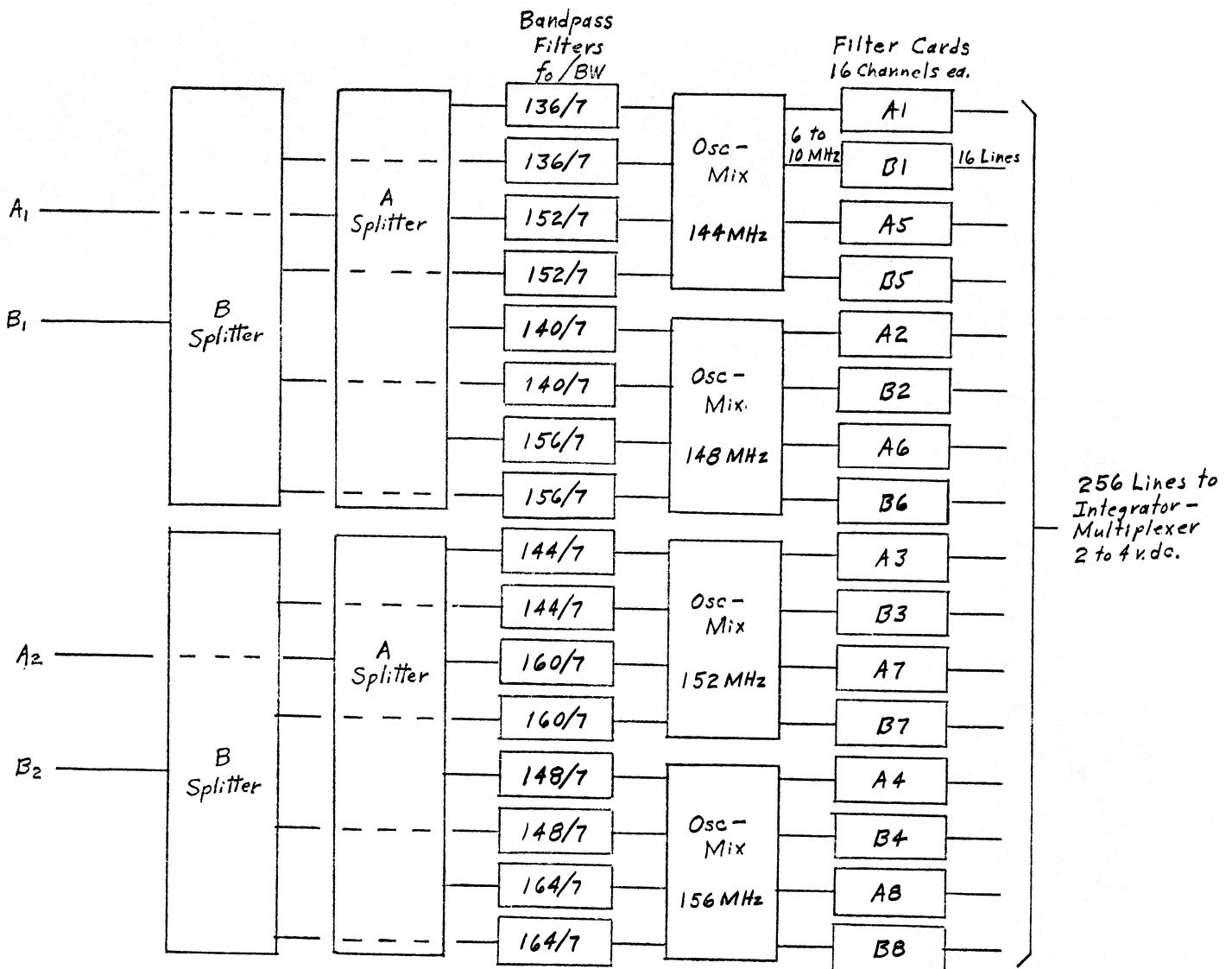
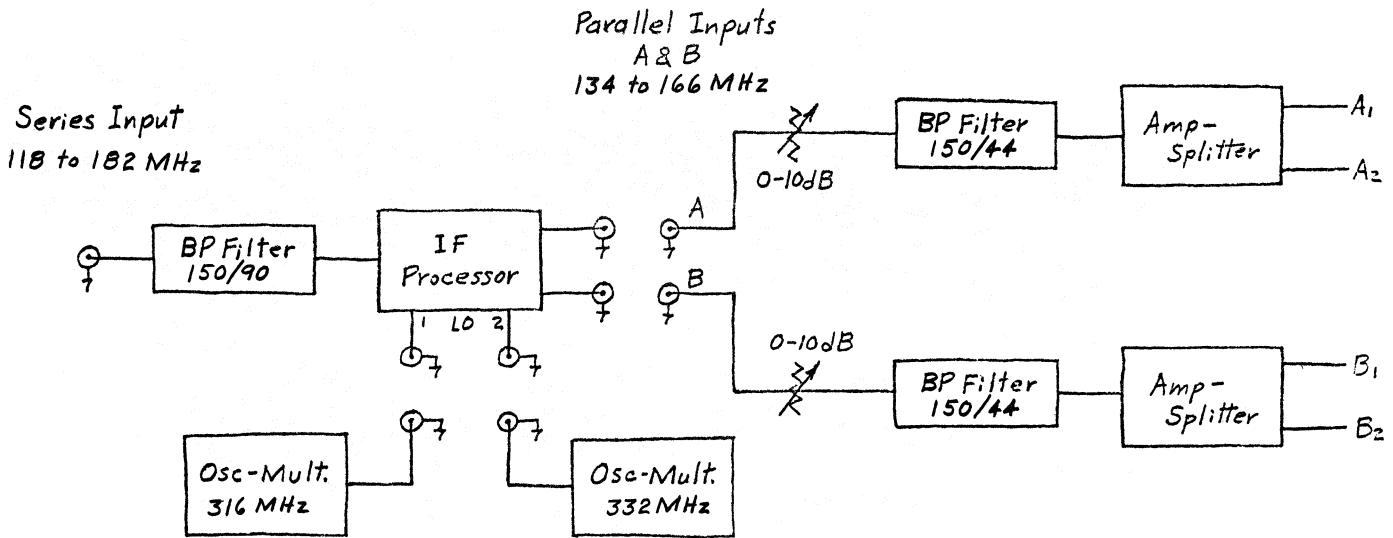
256 Channel Filter Receiver
1.0 MHz Channel Bandwidth

FIG. 9A



256 Channel Filter Receiver
0.5 MHz Channel Bandwidth

FIG. 9B

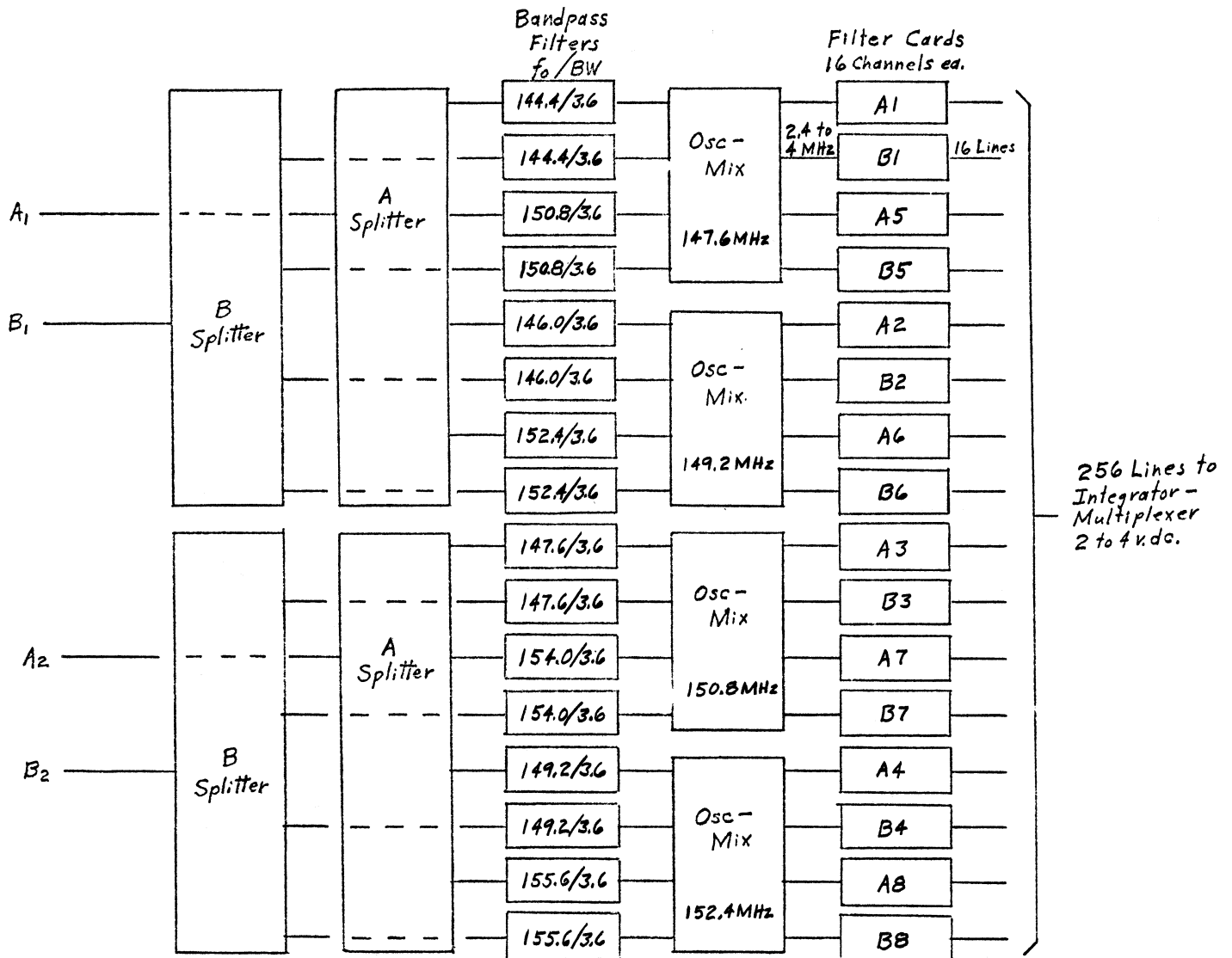
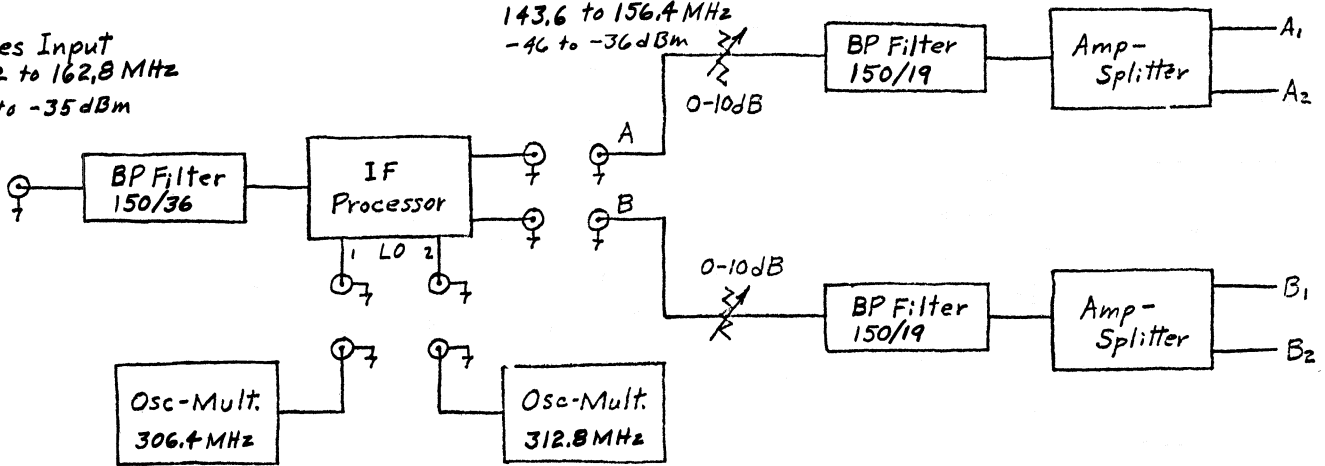


256 Channel Filter Receiver
0.25 MHz Channel Bandwidth

FIG. 9C

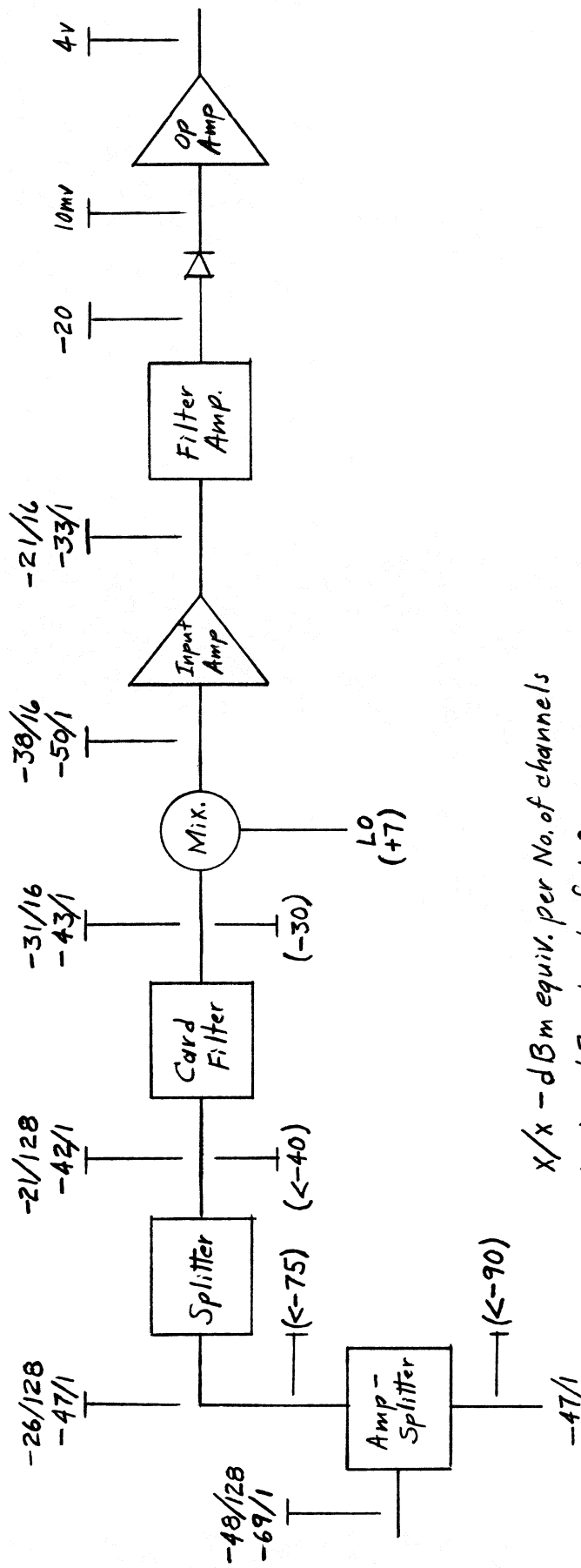
Series Input
137.2 to 162.8 MHz
-45 to -35 dBm

Parallel Inputs
A & B
143.6 to 156.4 MHz
-46 to -36 dBm



256 Channel Filter Receiver
0.1 MHz Channel Bandwidth

FIG. 9D



x/x - dBm equiv. per No. of channels
 (x) - dBm level of LO

System Power Levels

FIG. 10

256 CHANNEL FILTER RECEIVER

1 MHz/CHANNEL

INCREMENT= 1.000

FREQUENCY CHART

CHANNEL NO. REC. A	CHANNEL NO. REC. B	PARALLEL	A	B
0	128	86.500	22.500	150.500
1	129	87.500	23.500	151.500
2	130	88.500	24.500	152.500
3	131	89.500	25.500	153.500
4	132	90.500	26.500	154.500
5	133	91.500	27.500	155.500
6	134	92.500	28.500	156.500
7	135	93.500	29.500	157.500
8	136	94.500	30.500	158.500
9	137	95.500	31.500	159.500
10	138	96.500	32.500	160.500
11	139	97.500	33.500	161.500
12	140	98.500	34.500	162.500
13	141	99.500	35.500	163.500
14	142	100.500	36.500	164.500
15	143	101.500	37.500	165.500
16	144	102.500	38.500	166.500
17	145	103.500	39.500	167.500
18	146	104.500	40.500	168.500
19	147	105.500	41.500	169.500
20	148	106.500	42.500	170.500
21	149	107.500	43.500	171.500
22	150	108.500	44.500	172.500
23	151	109.500	45.500	173.500
24	152	110.500	46.500	174.500
25	153	111.500	47.500	175.500
26	154	112.500	48.500	176.500
27	155	113.500	49.500	177.500
28	156	114.500	50.500	178.500
29	157	115.500	51.500	179.500
30	158	116.500	52.500	180.500
31	159	117.500	53.500	181.500
32	160	118.500	54.500	182.500
33	161	119.500	55.500	183.500
34	162	120.500	56.500	184.500
35	163	121.500	57.500	185.500
36	164	122.500	58.500	186.500
37	165	123.500	59.500	187.500
38	166	124.500	60.500	188.500
39	167	125.500	61.500	189.500
40	168	126.500	62.500	190.500
41	169	127.500	63.500	191.500
42	170	128.500	64.500	192.500
43	171	129.500	65.500	193.500
44	172	130.500	66.500	194.500
45	173	131.500	67.500	195.500
46	174	132.500	68.500	196.500
47	175	133.500	69.500	197.500
48	176	134.500	70.500	198.500
49	177	135.500	71.500	199.500
50	178	136.500	72.500	200.500
51	179	137.500	73.500	201.500
52	180	138.500	74.500	202.500
53	181	139.500	75.500	203.500
54	182	140.500	76.500	204.500
55	183	141.500	77.500	205.500
56	184	142.500	78.500	206.500
57	185	143.500	79.500	207.500
58	186	144.500	80.500	208.500
59	187	145.500	81.500	209.500
60	188	146.500	82.500	210.500
61	189	147.500	83.500	211.500
62	190	148.500	84.500	212.500
63	191	149.500	85.500	213.500
64	192	150.500	86.500	214.500
65	193	151.500	87.500	215.500
66	194	152.500	88.500	216.500
67	195	153.500	89.500	217.500
68	196	154.500	90.500	218.500
69	197	155.500	91.500	219.500
70	198	156.500	92.500	220.500
71	199	157.500	93.500	221.500
72	200	158.500	94.500	222.500
73	201	159.500	95.500	223.500
74	202	160.500	96.500	224.500
75	203	161.500	97.500	225.500
76	204	162.500	98.500	226.500
77	205	163.500	99.500	227.500
78	206	164.500	100.500	228.500
79	207	165.500	101.500	229.500
80	208	166.500	102.500	230.500
81	209	167.500	103.500	231.500
82	210	168.500	104.500	232.500
83	211	169.500	105.500	233.500
84	212	170.500	106.500	234.500
85	213	171.500	107.500	235.500
86	214	172.500	108.500	236.500
87	215	173.500	109.500	237.500
88	216	174.500	110.500	238.500
89	217	175.500	111.500	239.500
90	218	176.500	112.500	240.500
91	219	177.500	113.500	241.500
92	220	178.500	114.500	242.500
93	221	179.500	115.500	243.500
94	222	180.500	116.500	244.500
95	223	181.500	117.500	245.500
96	224	182.500	118.500	246.500
97	225	183.500	119.500	247.500
98	226	184.500	120.500	248.500
99	227	185.500	121.500	249.500
100	228	186.500	122.500	250.500
101	229	187.500	123.500	251.500
102	230	188.500	124.500	252.500
103	231	189.500	125.500	253.500
104	232	190.500	126.500	254.500
105	233	191.500	127.500	255.500
106	234	192.500	128.500	256.500
107	235	193.500	129.500	257.500
108	236	194.500	130.500	258.500
109	237	195.500	131.500	259.500
110	238	196.500	132.500	260.500
111	239	197.500	133.500	261.500
112	240	198.500	134.500	262.500
113	241	199.500	135.500	263.500
114	242	200.500	136.500	264.500
115	243	201.500	137.500	265.500
116	244	202.500	138.500	266.500
117	245	203.500	139.500	267.500
118	246	204.500	140.500	268.500
119	247	205.500	141.500	269.500
120	248	206.500	142.500	270.500
121	249	207.500	143.500	271.500
122	250	208.500	144.500	272.500
123	251	209.500	145.500	273.500
124	252	210.500	146.500	274.500
125	253	211.500	147.500	275.500
126	254	212.500	148.500	276.500
127	255	213.500	149.500	277.500

FIG. 11 A

256 CHANNEL FILTER RECEIVER

500 kHz/Channel

INCREMENT= 0.500

FREQUENCY CHART

CHANNEL NO.		SERIES			CARD NO. & CHANNEL	
REC. A	REC. B	PARALLEL	A	B	PARALLEL	SERIES
0	128	118.250	86.250	150.250	16	16
1	129	118.750	86.750	150.750	15	15
2	130	119.250	87.250	151.250	14	14
3	131	119.750	87.750	151.750	13	13
4	132	120.250	88.250	152.250	12	12
5	133	120.750	88.750	152.750	11	11
6	134	121.250	89.250	153.250	10	10
7	135	121.750	89.750	153.750	9	9
8	136	122.250	90.250	154.250	8	8
9	137	122.750	90.750	154.750	7	7
10	138	123.250	91.250	155.250	6	6
11	139	123.750	91.750	155.750	5	5
12	140	124.250	92.250	156.250	4	4
13	141	124.750	92.750	156.750	3	3
14	142	125.250	93.250	157.250	2	2
15	143	125.750	93.750	157.750	1	1
16	144	126.250	94.250	158.250	16	16
17	145	126.750	94.750	158.750	15	15
18	146	127.250	95.250	159.250	14	14
19	147	127.750	95.750	159.750	13	13
20	148	128.250	96.250	160.250	12	12
21	149	128.750	96.750	160.750	11	11
22	150	129.250	97.250	161.250	10	10
23	151	129.750	97.750	161.750	9	9
24	152	130.250	98.250	162.250	8	8
25	153	130.750	98.750	162.750	7	7
26	154	131.250	99.250	163.250	6	6
27	155	131.750	99.750	163.750	5	5
28	156	132.250	100.250	164.250	4	4
29	157	132.750	100.750	164.750	3	3
30	158	133.250	101.250	165.250	2	2
31	159	133.750	101.750	165.750	1	1
32	160	134.250	102.250	166.250	16	16
33	161	134.750	102.750	166.750	15	15
34	162	135.250	103.250	167.250	14	14
35	163	135.750	103.750	167.750	13	13
36	164	136.250	104.250	168.250	12	12
37	165	136.750	104.750	168.750	11	11
38	166	137.250	105.250	169.250	10	10
39	167	137.750	105.750	169.750	9	9
40	168	138.250	106.250	170.250	8	8
41	169	138.750	106.750	170.750	7	7
42	170	139.250	107.250	171.250	6	6
43	171	139.750	107.750	171.750	5	5
44	172	140.250	108.250	172.250	4	4
45	173	140.750	108.750	172.750	3	3
46	174	141.250	109.250	173.250	2	2
47	175	141.750	109.750	173.750	1	1
48	176	142.250	110.250	174.250	16	16
49	177	142.750	110.750	174.750	15	15
50	178	143.250	111.250	175.250	14	14
51	179	143.750	111.750	175.750	13	13
52	180	144.250	112.250	176.250	12	12
53	181	144.750	112.750	176.750	11	11
54	182	145.250	113.250	177.250	10	10
55	183	145.750	113.750	177.750	9	9
56	184	146.250	114.250	178.250	8	8
57	185	146.750	114.750	178.750	7	7
58	186	147.250	115.250	179.250	6	6
59	187	147.750	115.750	179.750	5	5
60	188	148.250	116.250	180.250	4	4
61	189	148.750	116.750	180.750	3	3
62	190	149.250	117.250	181.250	2	2
63	191	149.750	117.750	181.750	1	1
64	192	150.250	118.250	182.250	16	16
65	193	150.750	118.750	182.750	15	15
66	194	151.250	119.250	183.250	14	14
67	195	151.750	119.750	183.750	13	13
68	19					

256 CHANNEL FILTER RECEIVER
 INCREMENT = 0.250
 250kHz/CHANNEL

FREQUENCY CHART

CHANNEL NO.		SERIES	
REC-A	REC-B	A	B
0	128	134.125	150.125
1	129	134.375	150.375
2	130	134.625	150.625
3	131	134.875	150.875
4	132	135.125	151.125
5	133	135.375	151.375
6	134	135.625	151.625
7	135	135.875	151.875
8	136	136.125	152.125
9	137	136.375	152.375
10	138	136.625	152.625
11	139	136.875	152.875
12	140	137.125	153.125
13	141	137.375	153.375
14	142	137.625	153.625
15	143	137.875	153.875
16	144	138.125	154.125
17	145	138.375	154.375
18	146	138.625	154.625
19	147	138.875	154.875
20	148	139.125	155.125
21	149	139.375	155.375
22	150	139.625	155.625
23	151	139.875	155.875
24	152	140.125	156.125
25	153	140.375	156.375
26	154	140.625	156.625
27	155	140.875	156.875
28	156	141.125	157.125
29	157	141.375	157.375
30	158	141.625	157.625
31	159	141.875	157.875
32	160	142.125	158.125
33	161	142.375	158.375
34	162	142.625	158.625
35	163	142.875	158.875
36	164	143.125	159.125
37	165	143.375	159.375
38	166	143.625	159.625
39	167	143.875	159.875
40	168	144.125	160.125
41	169	144.375	160.375
42	170	144.625	160.625
43	171	144.875	160.875
44	172	145.125	161.125
45	173	145.375	161.375
46	174	145.625	161.625
47	175	145.875	161.875
48	176	146.125	162.125
49	177	146.375	162.375
50	178	146.625	162.625
51	179	146.875	162.875
52	180	147.125	163.125
53	181	147.375	163.375
54	182	147.625	163.625
55	183	147.875	163.875
56	184	148.125	164.125
57	185	148.375	164.375
58	186	148.625	164.625
59	187	148.875	164.875
60	188	149.125	165.125
61	189	149.375	165.375
62	190	149.625	165.625
63	191	149.875	165.875
64	192	150.125	166.125
65	193	150.375	166.375
66	194	150.625	166.625
67	195	150.875	166.875
68	196	151.125	167.125
69	197	151.375	167.375
70	198	151.625	167.625
71	199	151.875	167.875
72	200	152.125	168.125
73	201	152.375	168.375
74	202	152.625	168.625
75	203	152.875	168.875
76	204	153.125	169.125
77	205	153.375	169.375
78	206	153.625	169.625
79	207	153.875	169.875
80	208	154.125	170.125
81	209	154.375	170.375
82	210	154.625	170.625
83	211	154.875	170.875
84	212	155.125	171.125
85	213	155.375	171.375
86	214	155.625	171.625
87	215	155.875	171.875
88	216	156.125	172.125
89	217	156.375	172.375
90	218	156.625	172.625
91	219	156.875	172.875
92	220	157.125	173.125
93	221	157.375	173.375
94	222	157.625	173.625
95	223	157.875	173.875
96	224	158.125	174.125
97	225	158.375	174.375
98	226	158.625	174.625
99	227	158.875	174.875
100	228	159.125	175.125
101	229	159.375	175.375
102	230	159.625	175.625
103	231	159.875	175.875
104	232	160.125	176.125
105	233	160.375	176.375
106	234	160.625	176.625
107	235	160.875	176.875
108	236	161.125	177.125
109	237	161.375	177.375
110	238	161.625	177.625
111	239	161.875	177.875
112	240	162.125	178.125
113	241	162.375	178.375
114	242	162.625	178.625
115	243	162.875	178.875
116	244	163.125	179.125
117	245	163.375	179.375
118	246	163.625	179.625
119	247	163.875	179.875
120	248	164.125	180.125
121	249	164.375	180.375
122	250	164.625	180.625
123	251	164.875	180.875
124	252	165.125	181.125
125	253	165.375	181.375
126	254	165.625	181.625
127	255	165.875	181.875

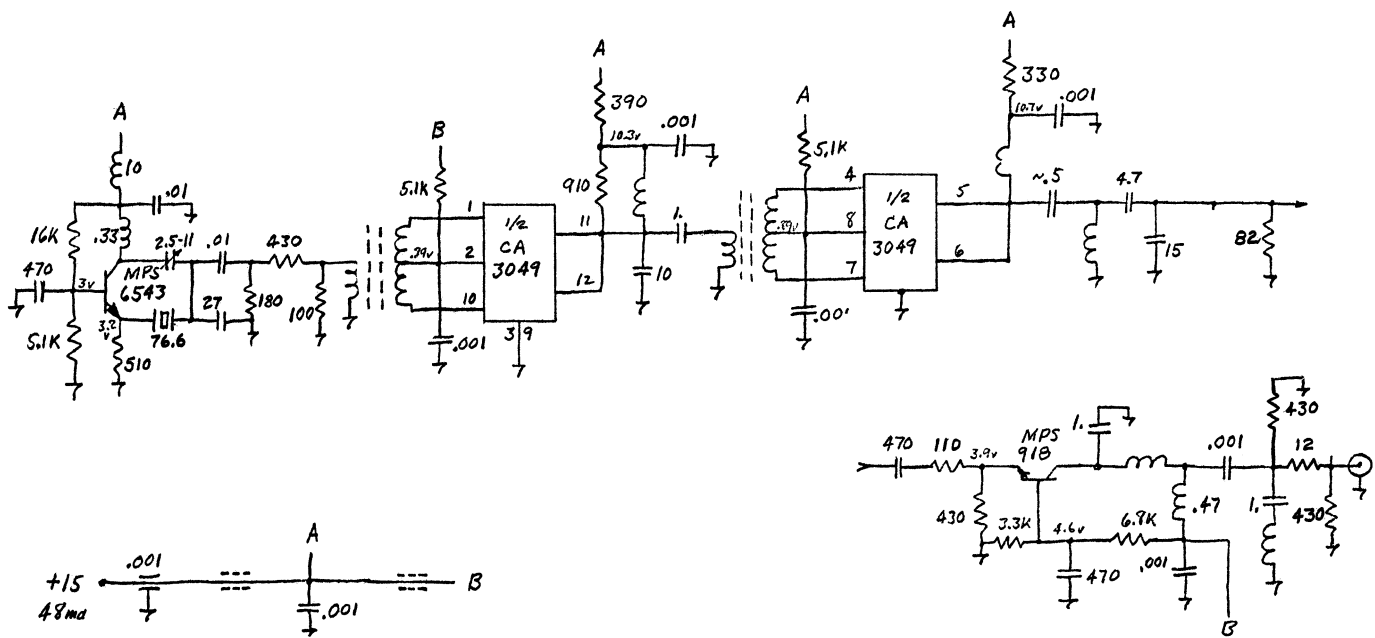
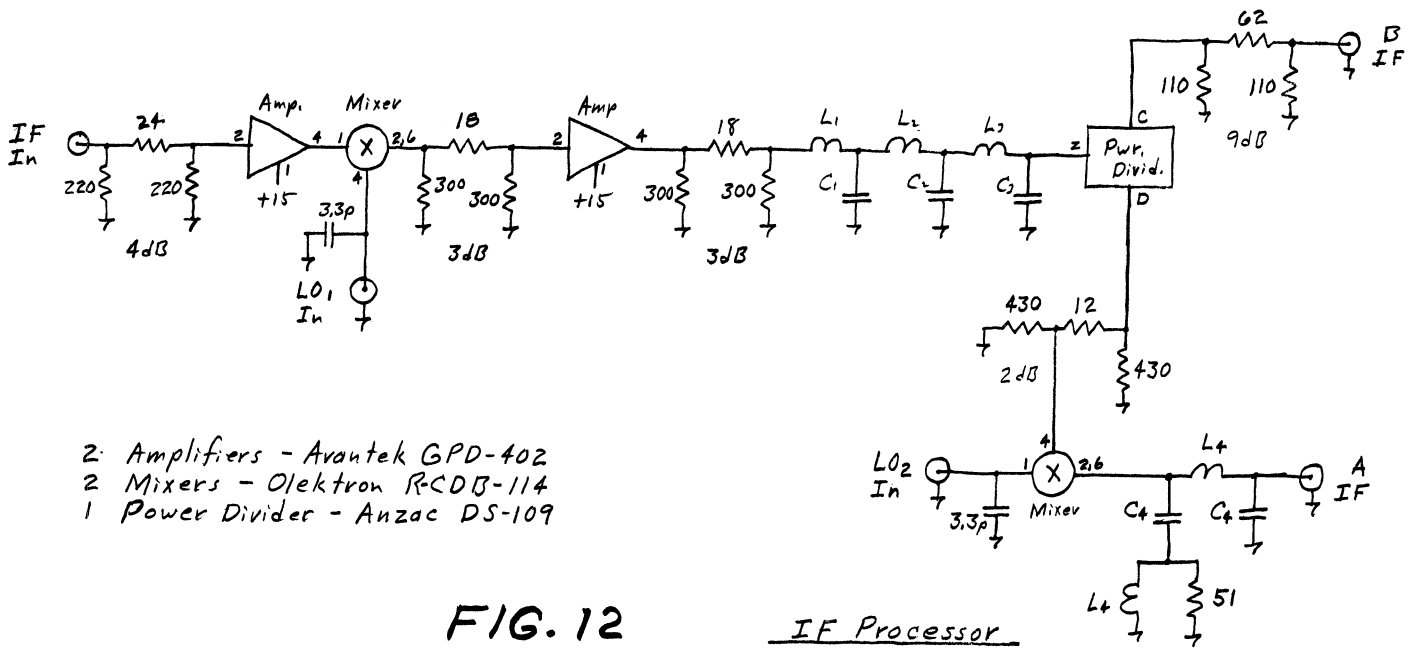
FIG. 11C

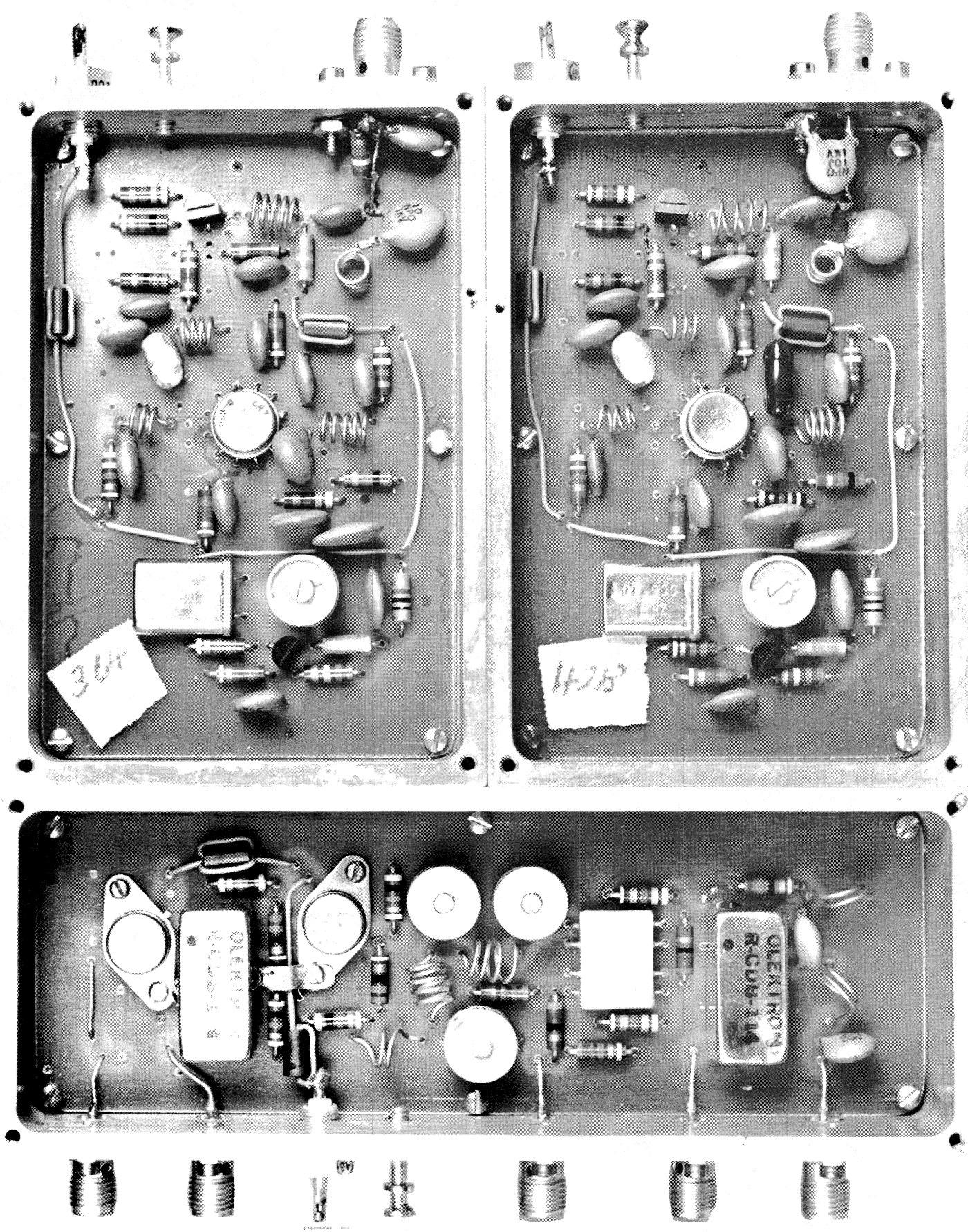
256 CHANNEL FILTER RECEIVER
 INCREMENT = 0.100
 100kHz/Channel

FREQUENCY CHART

CHANNEL NO.		SERIES	
REC-A	REC-B	A	B
0	128	143.650	150.050
1	129	143.750	150.150
2	130	143.850	150.250
3	131	143.950	150.350
4	132	144.050	150.450
5	133	144.150	150.550
6	134	144.250	150.650
7	135	144.350	150.750
8	136	144.450	150.850
9	137	144.550	150.950
10	138	144.650	151.050
11	139	144.750	151.150
12	140	144.850	151.250
13	141	144.950	151.350
14	142	145.050	151.450
15	143	145.150	151.550
16	144	145.250	151.650
17	145	145.350	151.750
18	146	145.450	151.850
19	147	145.550	151.950
20	148	145.650	152.050
21	149	145.750	152.150
22	150	145.850	152.250
23	151	145.950	152.350
24	152	146.050	152.450
25	153	146.150	152.550
26	154	146.250	152.650
27	155	146.350	152.750
28	156	146.450	152.850
29	157	146.550	152.950
30	158	146.650	153.050
31	159	146.750	153.150
32	160	146.850	153.250
33	161	146.950	153.350
34	162	147.050	153.450
35	163	147.150	153.550
36	164	147.250	153.650
37	165	147.350	153.750
38	166	147.450	153.850
39	167	147.550	153.950
40	168	147.650	154.050
41	169	147.750	154.150
42	170	147.850	154.250
43	171	147.950	154.350
44	172	148.050	154.450
45	173	148.150	154.550
46	174	148.250	154.650
47	175	148.350	154.750
48	176	148.450	154.850
49	177	148.550	154.950
50	178	148.650	155.050
51	179	148.750	155.150
52	180	148.850	155.250
53	181	148.950	155.350
54	182	149.050	155.450
55	183	149.150	155.550
56	184	149.250	155.650
57	185	149.350	155.750
58	186	149.450	155.850
59	187	149.550	155.950
60	188	149.650	156.050
61	189	149.750	156.150
62	190	149.850	156.250
63	191	149.950	156.350
64	192	150.050	156.450
65	193	150.150	156.550
66	194	150.250	156.650
67	195	150.350	156.750
68	196	150.450	156.850
69	197	150.550	156.950
70	198	150.650	157.050
71	199	150.750	157.150
72	200	150.850	157.250
73	201	150.950	157.350
74	202	151.050	157.450
75	203	151.150	157.550
76	204	151.250	157.650
77	205	151.350	157.750
78	206	151.450	157.850
79	207	151.550	157.950
80	208	151.650	158.050
81	209	151.750	158.150
82	210	151.850	158.250
83	211	151.950	158.350
84	212	152.050	158.450
85	213	152.150	158.550
86	214	152.250	158.650
87	215	152.350	158.750
88	216	152.450	158.850
89	217	152.550	158.950
90	218	152.650	159.050
91	219	152.750	159.150
92	220	152.850	159.250
93	221	152.950	159.350
94	222	153.050	159.450
95	223	153.150	159.550
96	224	153.250	159.650
97	225	153.350	159.750
98	226	153.450	159.850
99	227	153.550	159.950
100	228	153.650	160.050
101	229	153.750	160.150
102	230	153.850	160.250
103	231	153.950	160.350
104	232	154.050	160.450
105	233	154.150	160.550
106	234	154.250	160.650
107	235	154.350	160.750
108	236	154.450	160.850
109	237	154.550	160.950
110	238	154.650	161.050
111	239	154.750	161.150
112	240	154.850	161.250
113	241	154.950	161.350
114	242	155.050	161.450
115	243	155.150	161.550
116	244	155.250	161.650
117	245	155.350	161.750
118	246	155.450	161.850
119	247	155.550	161.950
120	248	155.650	162.050
121	249	155.750	162.150
122	250	155.850	162.250
123	251	155.950	162.350
124	252	156.050	162.450
125	253	156.150	162.550
126	254	156.250	162.650
127	255	156.350	162.750

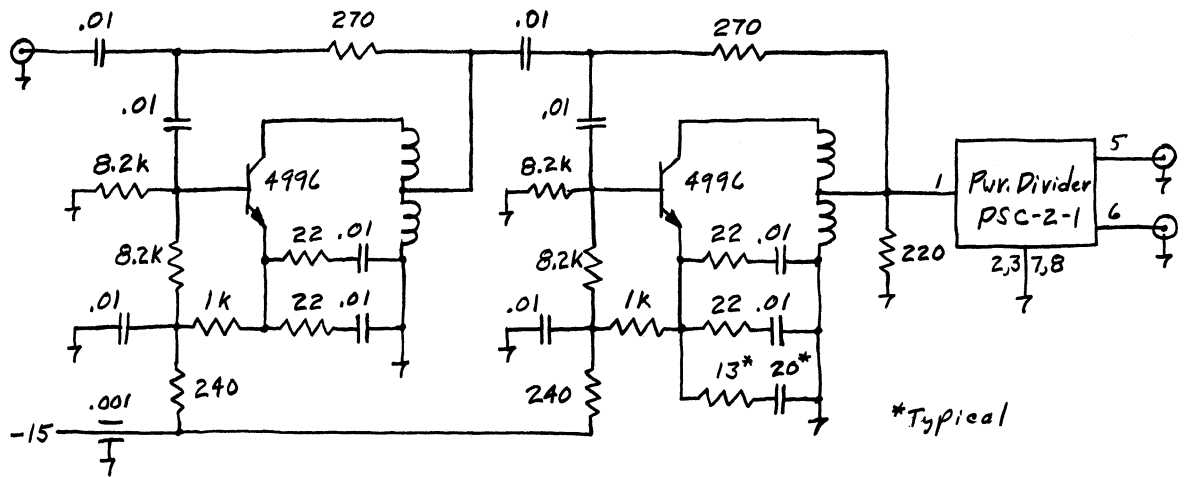
FIG. 11D





IF PROCESSOR AND OSCILLATOR-MULTIPLIERS

FIGURE 14



Amplifier-Splitter

50 to 250 MHz

FIG. 15

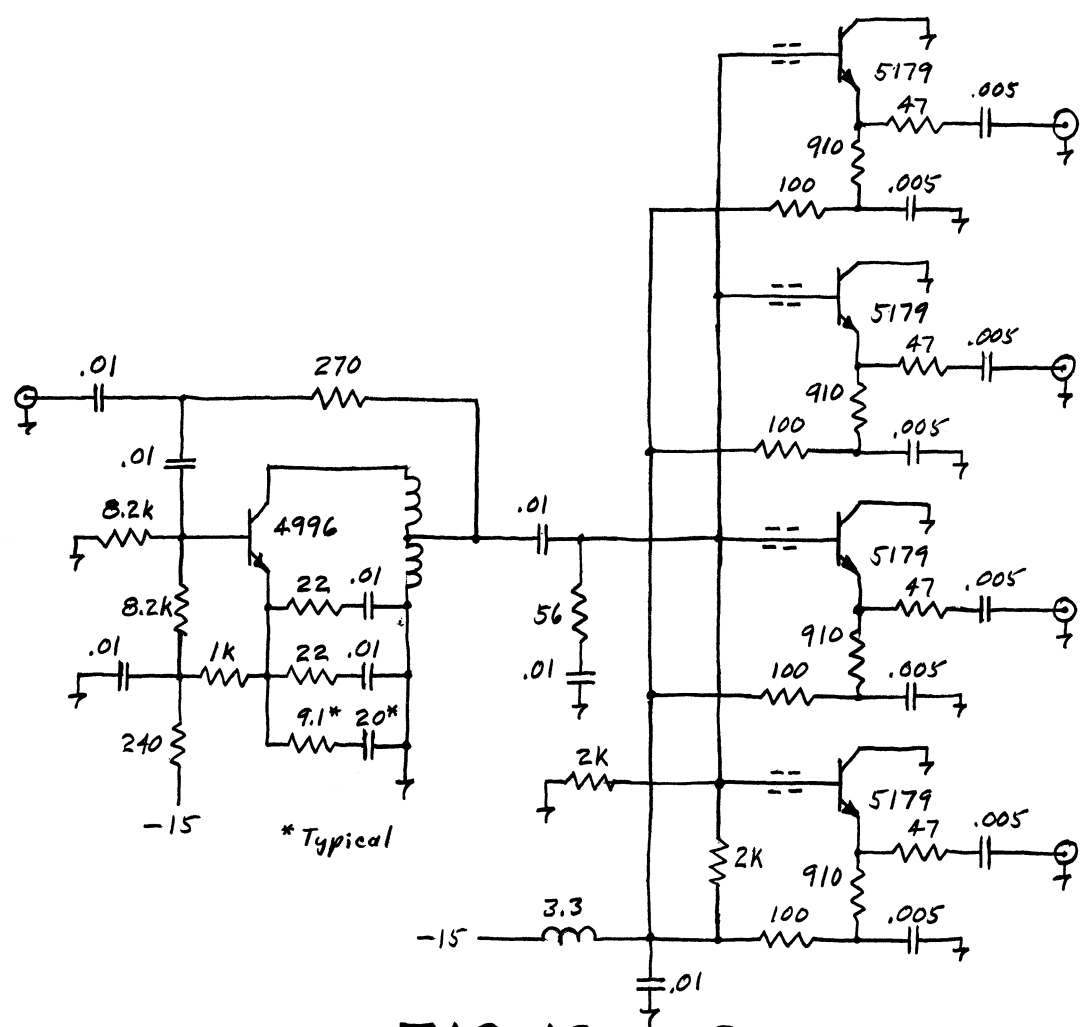


FIG. 16 Splitter

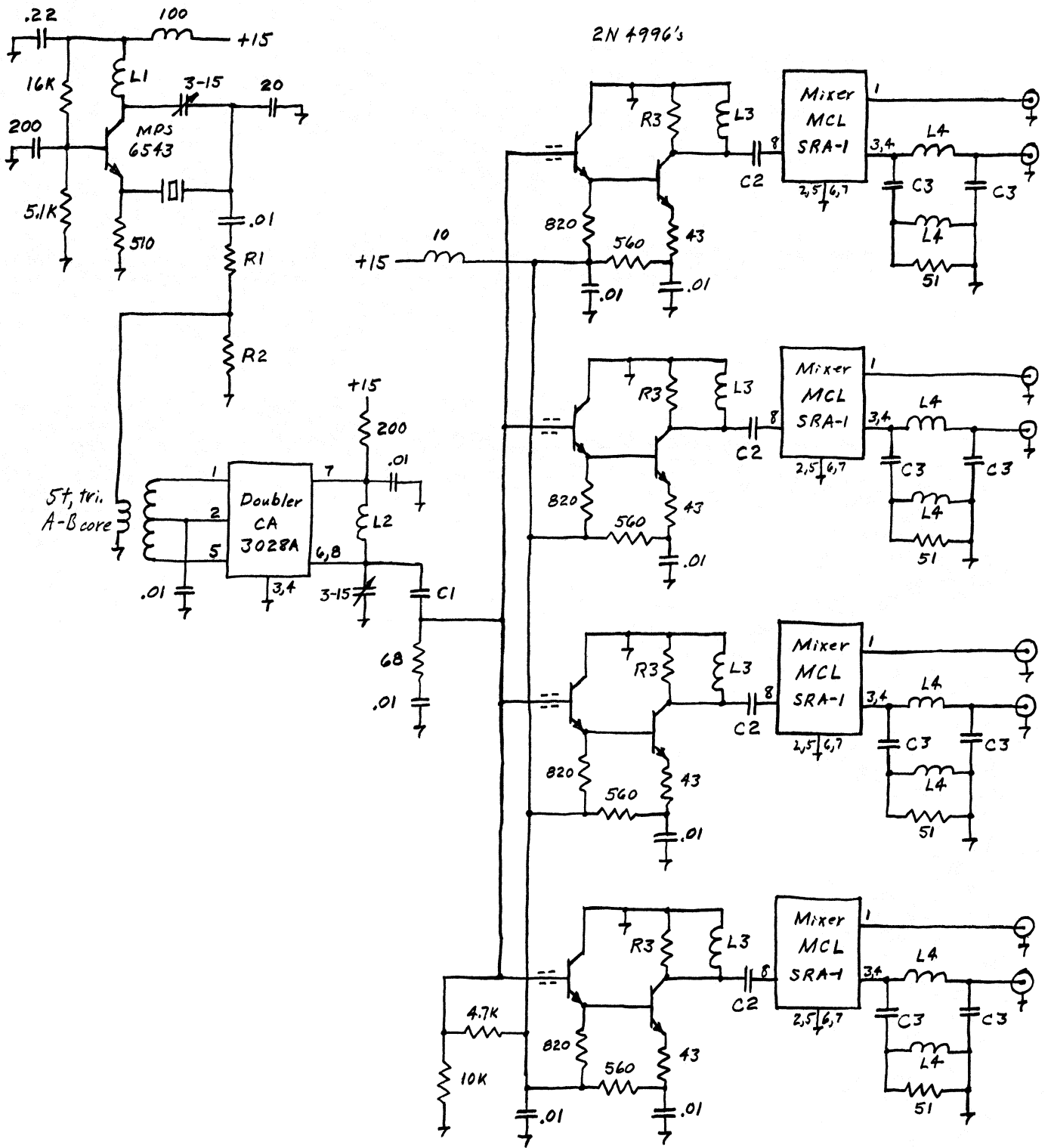


FIG. 17

Oscillator-Mixer

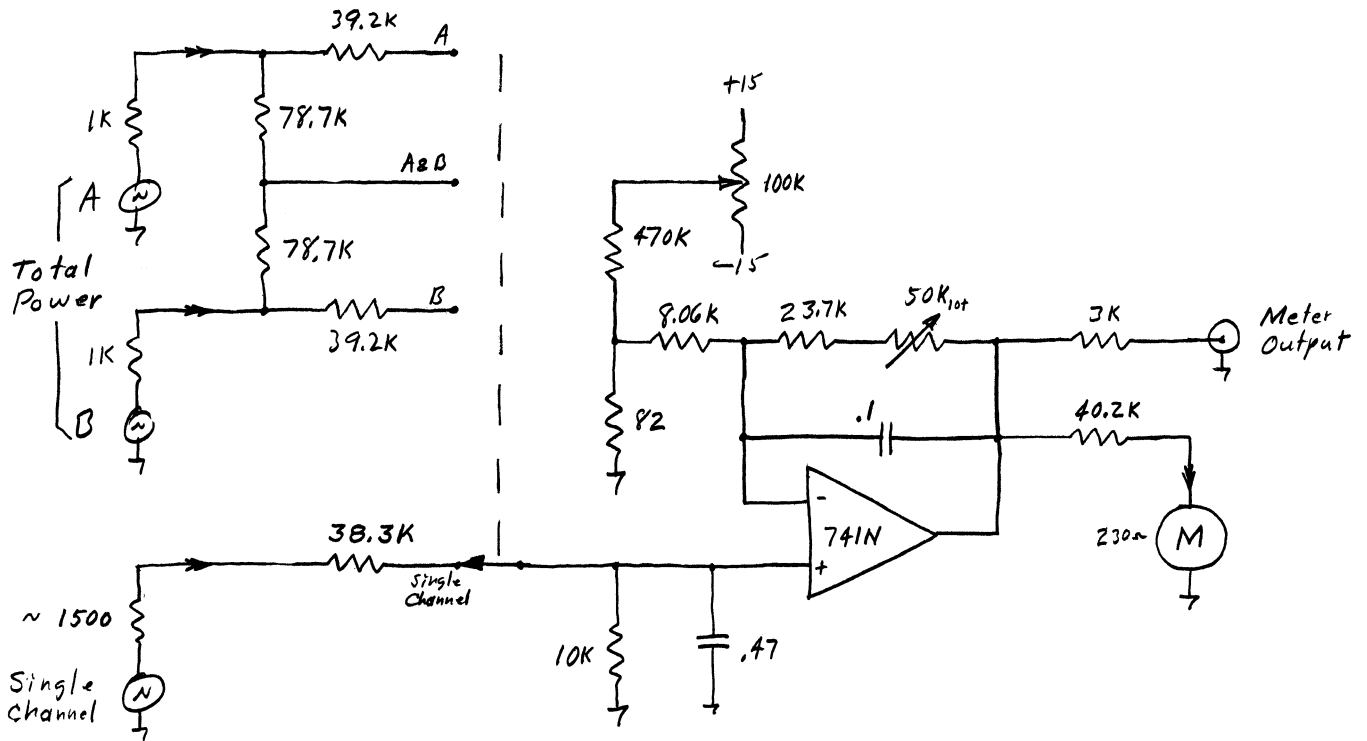


FIG. 18 Power Monitor

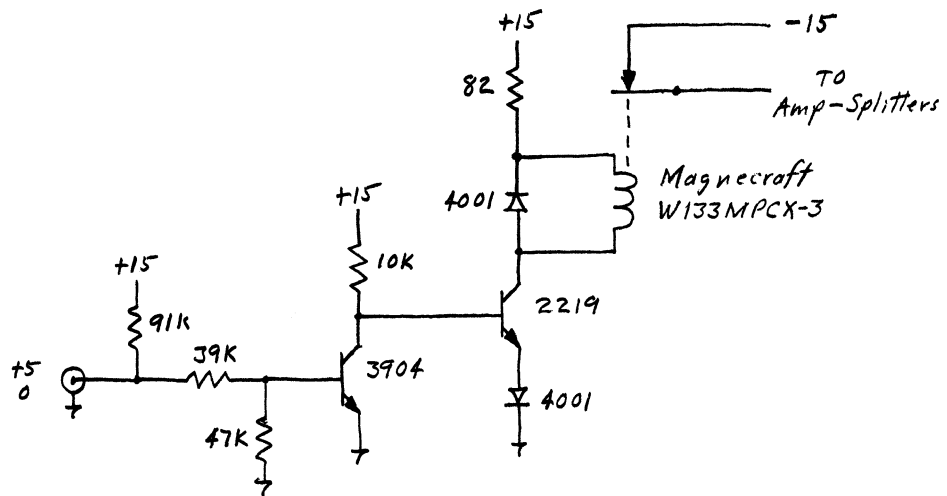
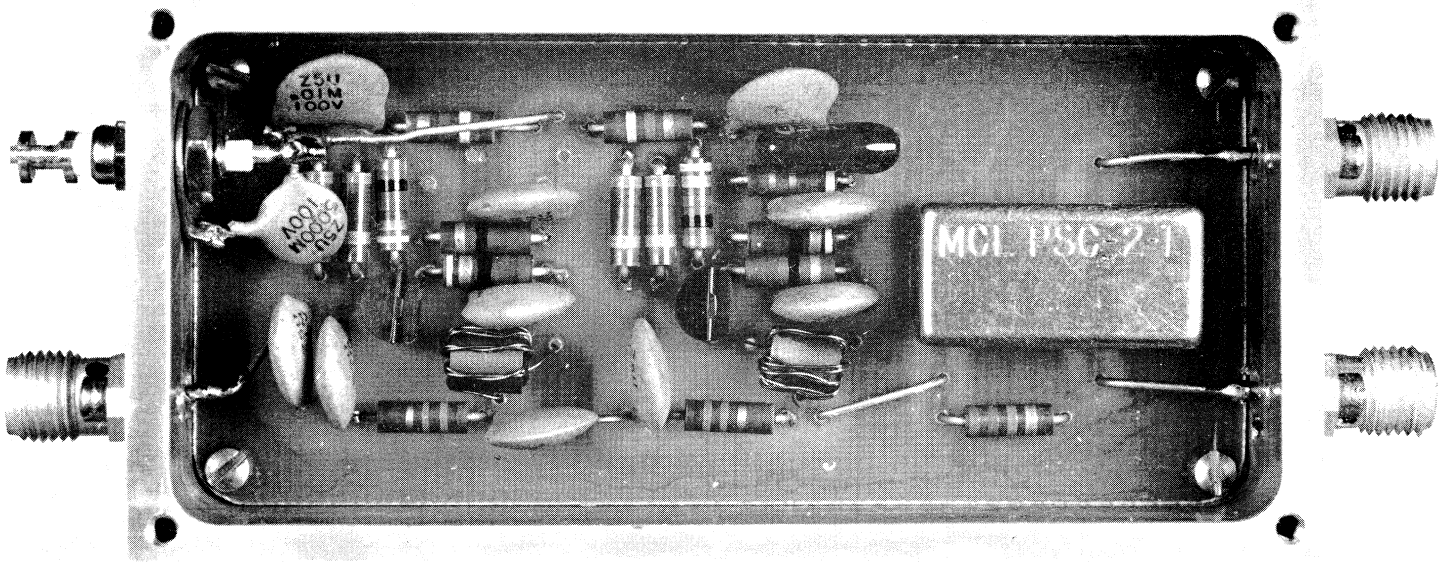
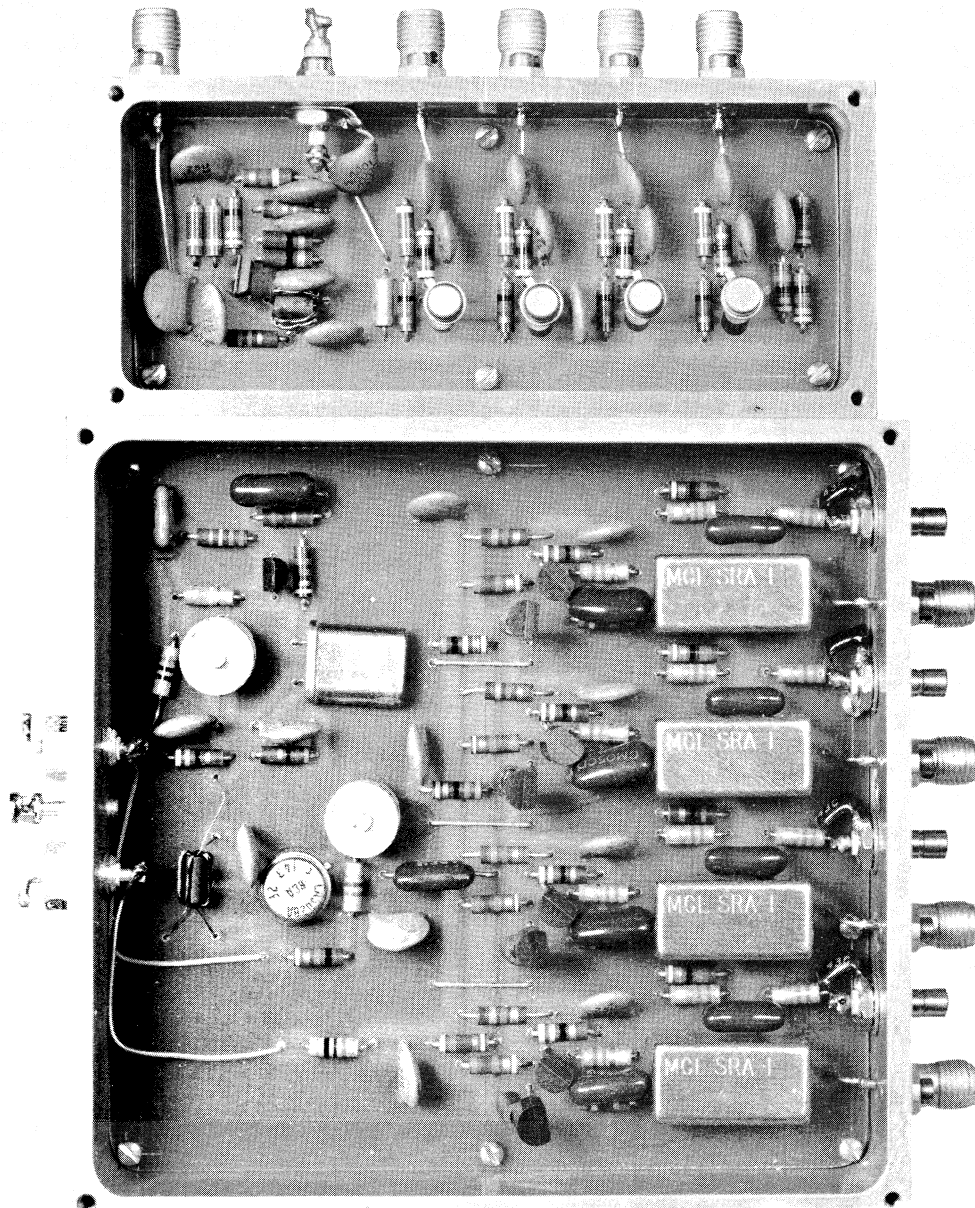


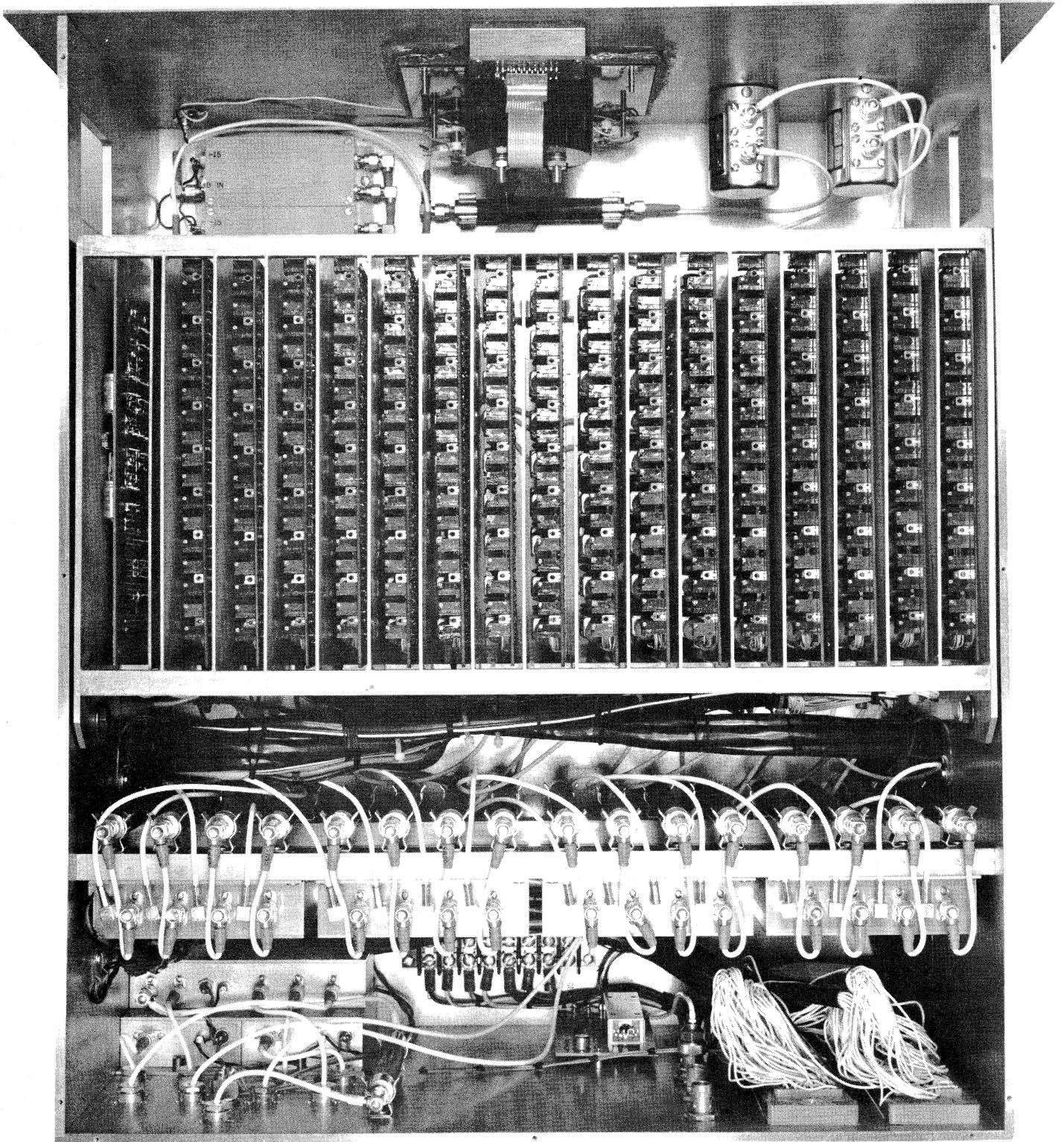
FIG. 19 Zero Check Ckt.



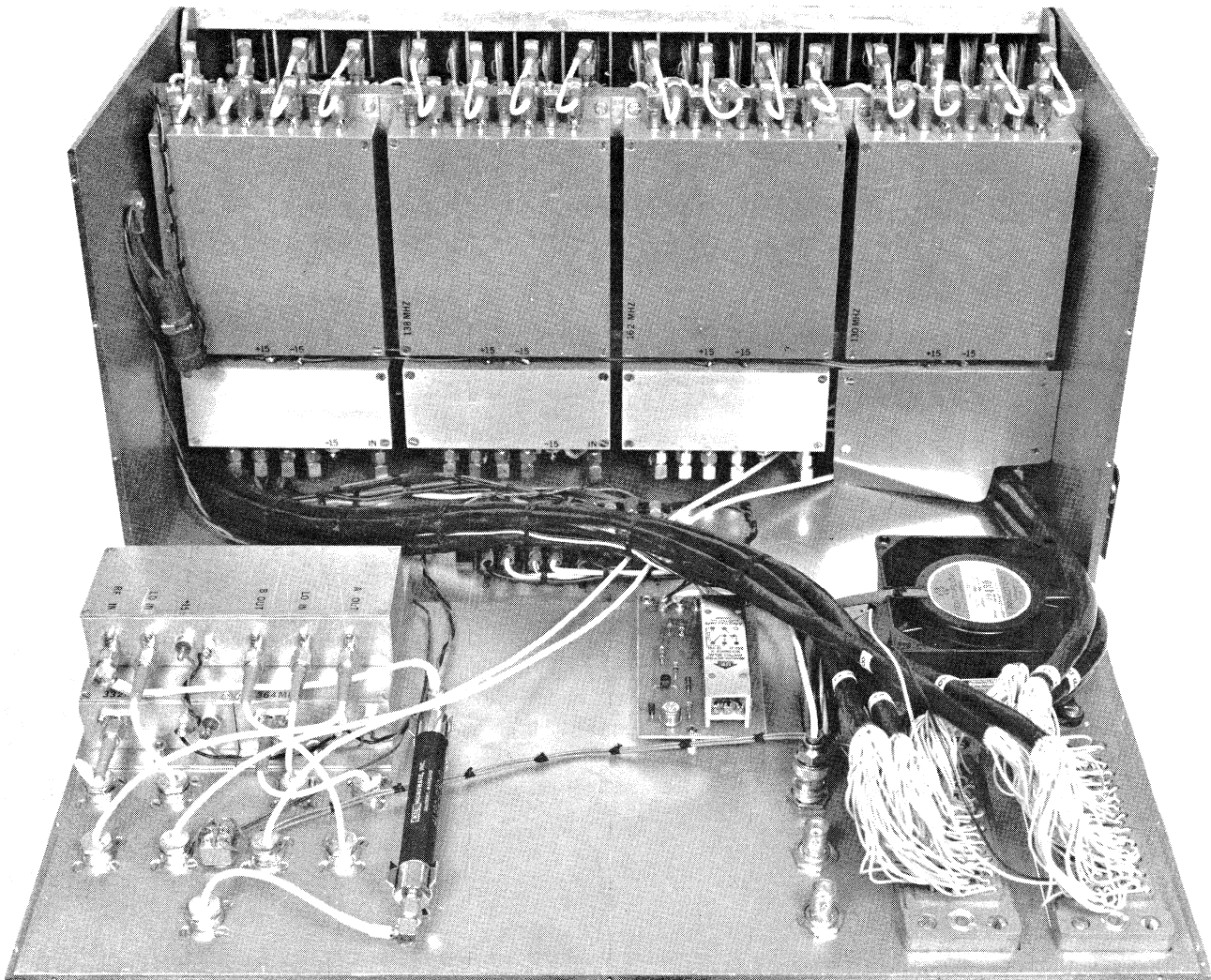
AMPLIFIER-SPLITTER
FIGURE 20



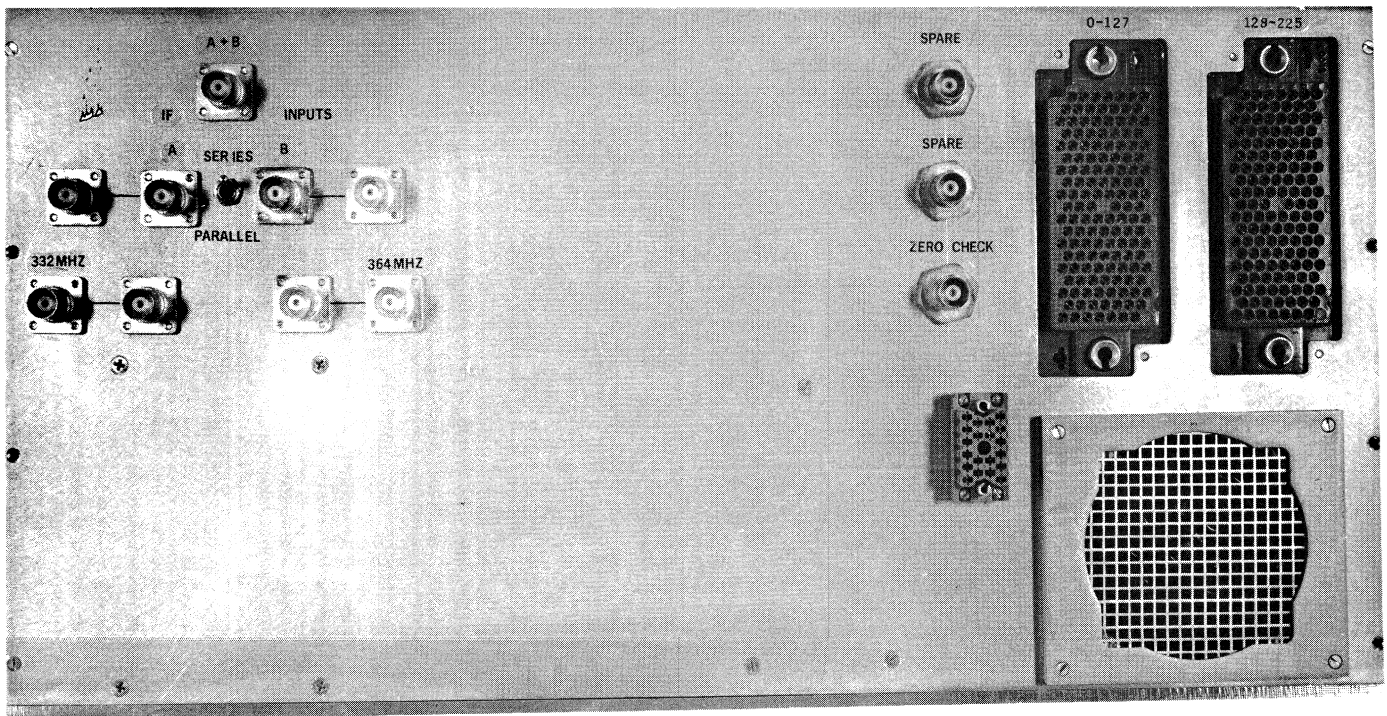
OSCILLATOR-MIXER AND SPLITTER
FIGURE 21



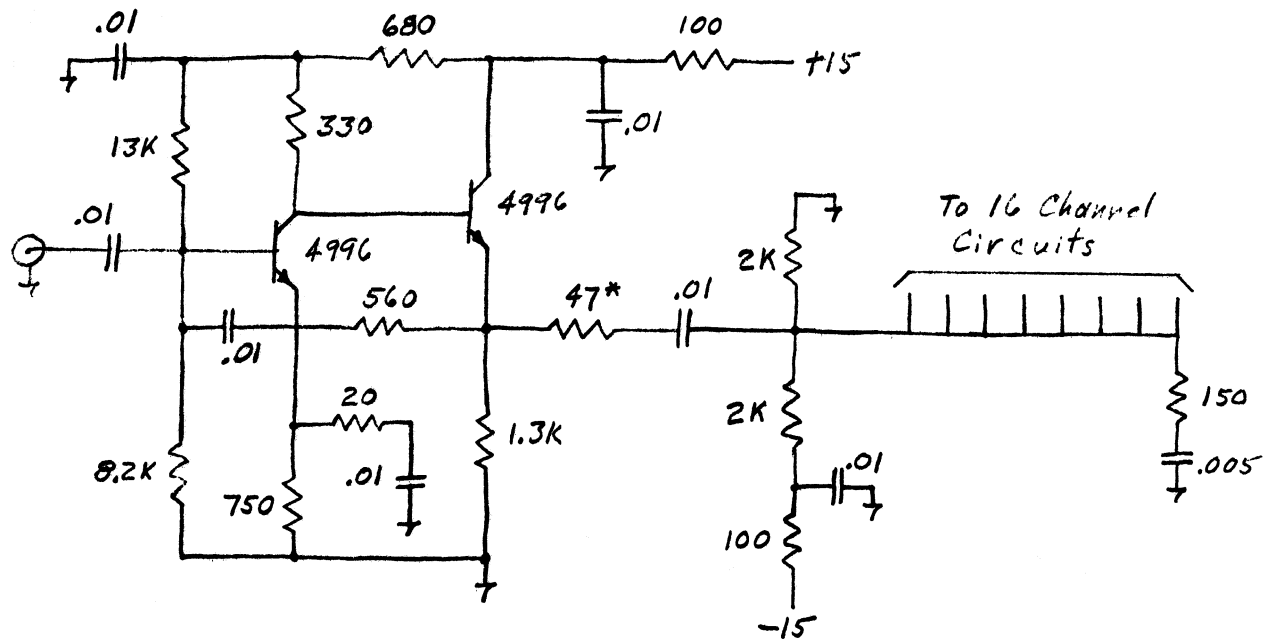
TOP VIEW
FIGURE 22



INSIDE BACK
FIGURE 23



BACK PANEL
FIGURE 24



* May vary for gain adjustment

Filter Board Input Amp

FIGURE 25