NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WEST VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 144

COMPUTER CONTROL OF THE UNIVERSAL LOCAL OSCILLATOR

DWAYNE SCHIEBEL

JULY 1974

NUMBER OF COPIES: 150

COMPUTER CONTROL OF THE UNIVERSAL LOCAL OSCILLATOR

Dwayne Schiebel

TABLE OF CONTENTS

FIGURES

COMPUTER CONTROL OF THE UNIVERSAL LOCAL OSCILLATOR

1. Introduction

This report describes the new computer control system for the Universal Local Oscillator. The system also provides a means for checking four frequency synthesizers in the IF Processor rack and control signals for the Cassegrain system.

2. Programming

The six least significant bits of the device address (bits 11-16) are selected by two digi-switches located in the digital drawer in the ULO rack. The following two addresses have been selected for ULO control:

31 Local Oscillator 1

32 Local Oscillator 2

The following commands are applicable to both ULO's. The only change would be in the six least significant bits of the address which will be represented by XX. Bit 7 of the address does not matter but it must be cautioned that when doing an INA it must be a "1" to clear the A register before doing the INA.

OTA $0XX_8$. This OTA can output 16 words of information; the first 9 words set the ULO, the 10th word is for the proposed Cassegrain system, words 11-13 are spare buffered words, and words 14-16 are unused. The format for the ULO is listed below. The ULO will only be updated at the next transition of the signal/reference signal. If the front panel switch is in manual it will be possible to do an OTA but the data will not be taken.

	Bits	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	
Words	1	100's MHz	10's MHz	1's MHz	100's kHz	
	2	10's kHz	1's kHz	100's Hz	10's Hz	F_{LO}
	3	1's Hz	.1 Hz			
	4					
	5		Same as	above.		$F_{REF\ 1}$
	6					
	7					
	8		Same as	above.		$F_{REF\ 2}$
	9					

Word 10 - Bits 1-14 are available as data and bits 15-16 are used to tell the Cassegrain system if $F_{REF\ 1}$ and $F_{REF\ 2}$ are greater or less than F_{LO}. Bit 15 is for $F_{REF\ 1}$ and bit 16 is for $F_{REF\ 2}$. The bit should be set to a "1" if it is greater.

INA $1XX_8$. This INA will input the frequency read by the counter in the ULO rack. (This counter measures the output of the multiplier.) An OCP $1XX_8$ must be executed before doing the INA's. There are two times the INA cannot be completed. One time is while a new counter reading is being stored (about 40 μsec). The other time is when the computer has read a set of readings. It will not be possible to take another reading until all three frequencies have been updated. This takes a maximum of 200 millisec, when switching at a 10 Hz rate. Listed below is the format for the input words.

	Bits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Words	1		MSD				---				---				---			F_{LO}
	2		---				---				LSD				BANDS*			
	3	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	4																	$F_{REF\ 1}$
	5						Same			as	above.							
	6																	
	7																	$R_{REF\ 2}$
	8						Same			as	above.							
	9																	

* Bands - Bits 13 = 1 = add 1700 MHz to counter reading.

14 = 1 = add 1300 MHz to counter reading.

15 = 1 = add 900 MHz to counter reading.

16 = 1 = take counter reading as it is.

Only one bit should be on at a time.

INA $2XX_8$. This INA reads the offset LO. At the 300-ft four LO's will be read. Only one will be read at the 140-ft. The input word will contain a count to tell the computer which LO was read. This count should be ignored at the 140-ft. Before reading a sequence of LO's, an OCP 2XX should be issued. This OCP will reset a counter to the first LO and cause the offset LO counter to count, after $\sim$ 1 sec the computer should be able to do two INA's. (It takes two INA's for each offset LO reading.) The system will then switch to another offset LO and count and the computer should be able to input two more words in $\sim$ 1 sec. The format for the input words is listed below.

	Bit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Word	1	10's kHz				1's kHz				LSD				BA*			
	2	100's MHz				10's MHz				1's MHz				100's kHz			

*BA contains a count to tell the computer which offset LO was read

B	A	LO#
0	0	A
0	1	B
1	0	C
1	1	D

INA $3XX_8$. This INA will input the status of the front panel rotary switch. The format is listed below.

Bits	13	14	15	16	
	0	0	0	1	Mod.
	0	0	1	0	$F_{REF\ 1}$
	0	0	1	1	F_{LO}
	0	1	0	0	$F_{REF\ 2}$
	0	1	1	1	Synth. in Local

SKS $4XX_8$. This SKS will skip if the front pane switch is in computer.

3. General Description

The new computer control system for the ULO contains four basic systems (see Figure 1). The first system is control and storage for the frequency synthesizer. The second system consists of a Balentine counter and storage for the computer. The third system controls an RF switch and a Systron Donner counter in the IF Processor rack for input into the computer. The fourth system is control and data for the Cassegrain system. The entire system uses wire-wrap cards and associated chassis designed by A. Shalloway.

4. Synthesizer Control (Figure 1A)

The heart of the synthesizer control is the synthesizer buffer card. Two digits are on one card. Five cards (slots 8-12) are required for each system. This card uses signals generated elsewhere in the system. These are described below.

DATA IN ..... This is the output bus of the computer buffered on control card 1 (slot 3).

$\overline{F_{REF\ 1}}$ & $\overline{F_{REF\ 2}}$ .. These signals are used to control the frequency switching. They are generated from the Sig./Ref. signal on control card 1 (slot 3).

MAN. ADV. ..... This is a level generated when a spring loaded toggle switch is pressed down on the front panel.

RESET A, B, & C .. Since the most signficant digit can only go to four, when in manual mode it is reset to zero by this signal. The reset signal is generated on control card 1 (slot 3).

STB A-C ..... These signals are generated on control card 2 (slot 4). When the computer does an OTA $0XX_8$ the "OTP" pulse gated with a decoded binary counter generates 16 strobe pulses, 9 of which are used for synthesizer control.

XFER ..... This signal is a pulse $\sim$ 500 nsec wide generated on control card 1 (slot 3). This pulse is generated at each transition of the signal/reference signal.

COMP/MAN ..... This is used to inhibit manually changing the synthesizer when in computer control.

ADVANCE ..... This signal is generated on control card 2 (slot 4). It is a 2.4 Hz signal with a 3 μsec pulse width.

ENABLE A & B .... The enable pulse is generated on control card 1 (slot 3). There is one enable pulse for each decade of the front panel display.

D_A & D_B ..... These two signals also generated on control card 1 (slot 3) are used to select which display is selected.

The synthesizer buffer card (slots 8-12) contains a buffer/counter, buffer, 4-line to 1-line switch and multiplexing for the display. The buffer/counter is the first buffer. Data from the computer (data in) is strobed (STB A-C) into the buffer. This buffer can also be advanced by MAN. ADV. going high and being in the manual mode. When in this manual mode, reset will go low when the most significant

digit steps from 4 to 5. This will only let the MSD get to four, which is required by the frequency synthesizer. The first buffer is strobed into the second buffer by XFER. This was done to insure that the frequency synthesizer changes frequency only during blanking time. The output of the second buffer goes to two 4-line to 1-line switches. One switch drives the decoder driver cards (slots 1 and 2). This is the switch that does the frequency switching; it is controlled by $\overline{F_{REF\ 1}}$ & $\overline{F_{REF\ 2}}$. The other switch is a Tri-State logic switch. It is used to multiplex the data to front panel displays. The Tri-State is enabled by one of the ten enable lines. This selects the decade to be displayed. Two control lines D_A & D_B are used to select which frequency is being displayed. Refer to control card 1 for these multiplexing signals. The only remaining circuitry on the buffer card is three circuits to decode a four in the most significant digit of each of the three frequencies $F_{REF\ 1}$, $F_{REF\ 2}$, and F_{LO}. This four decode is used by reset circuitry on control card 1.

The switched frequency from the synthesizer buffer card goes to the decoder driver card (slots 1 and 2). The decoder driver contains a 4-line BCD to 10-line decoder. The ten lines are level converted by optical-isolators to levels usable by the frequency synthesizer.

A table below lists which synthesizer buffer card and which decoder driver is used for each decade of the frequency synthesizer.

		Buffer Card	Decoder Card
100's	MHz	Slot 8	Slot 1
10's	MHz	Slot 8	Slot 1
1's	MHz	Slot 9	Slot 1
100's	kHz	Slot 9	Slot 1
10's	kHz	Slot 10	Slot 1
1's	kHz	Slot 10	Slot 2
100's	Hz	Slot 11	Slot 2
10's	Hz	Slot 11	Slot 2
1's	Hz	Slot 12	Slot 2
.1's	Hz	Slot 12	Slot 2

5. ULO Counter Control and Storage (Figure 1B)

Two logic cards are required for control and storage of the ULO counter. The first card is memory control (slot 6). This card resets the counter and generates read and write addresses, and write control signals for the solid state memory. The second card is the memory. This memory card contains a 16-word, 16-bit memory, 16-pole, 3-position switch and two clocks: 100 kHz and 5 kHz.

A counter reset pulse is generated 1 millisec after the transition of the signal/reference signal. After the counter has finished its count a store cycle is initiated. This store cycle causes three store pulses (write $\overline{ENB}$) to be sent to the memory.

The address for the memory can be generated in three ways; all three ways are described below.

Write Address. The write address is generated through the use of 4-line to 1-line switches. Each frequency requires 3 addresses. Two switches are used for each frequency. These two switches are enabled by $\overline{F_{LO}}$, $\overline{F_{REF\ 1}}$, or $\overline{F_{REF\ 2}}$. The two selected switches are then controlled by a shift register which is also used to generate store pulses.

Read Address. The read address is generated by a binary counter which is reset by an OCP, then incremented each time the computer does an INA.

Memory Test Address. A test address can be generated by setting a toggle switch to memory test and selecting the address in a digi-switch. It should be cautioned that this test cannot be used while the computer is running since the input bus will be hung up while in memory test.

All three addressing possibilities are selected by two 4-line to 1-line switches. The switches will be in the read position most of the time. During a store cycle it will switch to the write position.

The computer is prevented from reading the memory during an update of the memory or if it has already read the counter reading.

The memory card stores information received from the counter. Three words are stored for each frequency. The first two words are used for the counter; the third word is a spare. The output of the memory (7489) is the complement of the information that was stored in it. This information inverted is gated with the decoded address (AD-1) and applied to a sub-input bus. On this sub-input bus a ground is a one. This sub-input bus goes to control card 2. Control card 2 will drive the cable to the computer.

Also contained on the memory card is a circuit to input the front panel rotary switch and two clocks. The 5 kHz is for the front panel display and the 100 kHz is for memory control.

6. IF Processor Counter Control (Figure 1C)

Control of the IF Processor requires one logic card. This logic card is called "Control Card 3". This card contains an INA counter, LO select counter and decoder (used at 300-ft), counter reset control, and a 16-pole 2-position switch.

The first step the computer should take is to issue an OCP to reset the INA counter and LO select counter. This OCP will also reset the frequency counter after a delay of 300 millisec. After the counter has finished its count, a flip-flop will be set enabling the DRL line. When the computer does an INA, the INA flip-flop will be toggled. This changes the 16-pole switch for the second INA. When the computer does the second INA, the INA flip-flop will be toggled again. This causes the LO select counter to step one count and reset the frequency counter after a delay of 300 millisec. When the counter has finished its count the computer can do two more INA's.

The state of the INA flip-flop controls a 16-pole 2-position switch. This switch controls which part of the counter reading the computer will input. The first word contains the three least significant digits of the counter plus a count to tell the computer which LO was read. The second word is the four most significant digits of the counter.

7. Control and Data for the Cassegrain System (Figure 1D)

The Cassegrain system requires a signal to tell it which direction the LO frequency will be going at the next frequency switch time. It also requires a buffer which can be set by the computer to drive a D/A converter.

The frequency direction signal is generated on control card 3. This circuit uses a 4-line to 1-line switch. The inputs to this switch are two data bits from the computer. These two bits are used to tell if $F_{REF\ 1}$ and $F_{REF\ 2}$ are greater or less than F_{LO}. If the frequency is greater than F_{LO} the bit is set to a one.

The data for the Cassegrain system is stored on a buffer card (slot 13). This card also contains 3 spare 16-bit buffers.

8. DDP-116 I/O Buffers

Since the cable had to be quite long going to the ULO, all I/O lines were buffered. This buffering was done on "Cambion Cards" and installed in the block that contains the level conversion system.

9. Installation of Second ULO

A second LO can be connected to the system by connecting two cables from LO #2 to LO #1. Connect a cable from J2 in LO #2 to J4 in LO #1. Connect a cable from J3 in LO #2 to J5 in LO #1. It will also be necessary to change the address of LO #2 to the correct address (32).

10. Credits

Credit should be given to the following people for their help in this project: Doreen Morris, G. Runion, A. Shalloway, J. Turner, W. Vrable and the Green Bank Machine Shop. Thanks also should be given to Ron Weimer for his help in this project.

11. MNEMONIC LIST

Name	Origin	Destination
ADBXX+	J2	Slot 4
ADD. SEL. $\overline{A}$-$\overline{B}$	Slot 6	Slot 7
AD-0 - AD-7	Slot 4	Slots 3, 5, 6 & 7
ADVANCE	Slot 4	Slots 8-12
A4D, B4D, C4D	Slot 8	Slot 3
BCD COUNT	Slot 3	J13-15
CLOCK TO DISPLAY	Slot 3	J13-15
COMP/MAN	J19	Slots 3, 4, 8-12
COUNTER RESET ±	Slot 5	J7
COUNTER RESET	Slot 6	J6
DATA OUT/DATA IN	Slots 8-12	Slots 1 & 2 (Data In)
D_A & D_B	Slot 3	Slots 8-12
DIGIT A-E	Slots 1 & 2	J1
DISPLAY CLK/MAN CLK	Slot 7	Slots 3 & 4
DISPLAY DATA SEL.	Slot 3	Slots 8-12
DISPLAY DIGIT SEL.	Slot 3	Slots 8-12
DRL-A	Slot 5	J3
DRL 3	Slot 6	Slot 5
DRL 4	Slot 4	Slot 5
END OF COUNT	J6	Slot 6
$\overline{F_{LO}}$	Slot 3	Slot 6, J19
$\overline{F_{REF\ 1}}$	Slot 3	Slots 6, 8-12, J19
$\overline{F_{REF\ 2}}$	Slot 3	Slots 6, 8-12, J19
FREQ. DIR. $F_{REF\ 1}$ & $F_{REF\ 2}$	Slot 13	Slot 5
FREQ. DIR. ±	Slot 5	J8
F STEERING	Slot 3	Slot 5
INBO1-THRU 16-	Slots 5 & 7	Slot 4
INB-1A-16A	Slot 4	J3
INPUT WORD A_1-A_{16} & B_1-B_{16}	J7	Slot 5
LOCAL/REMOTE	J1	Slot 3
MAN. ADV. A, B, C	Slot 8	Slot 3
MEMORY ADDRESS 1, 2, 4, 8	Slot 6	Slot 7
MEMORY CLK.	Slot 7	Slot 6
MEMORY TEST 1, 2, 4, 8	Digi-Switch	Slot 6
MEM. TEST	Toggle Switch	Slot 6
MSTCL ±	J3	Slot 5
MSTCL + A	Slot 5	Slots 3, 6 & 13
OCP ±	J3	Slot 4
OCP + A	Slot 4	Slots 3, 5, 6
OFFSET LO SEL. A-D	Slot 5	J7
OTB-	J2	Slot 3
OTB + A	Slot 3	Slots 8-12 (Data In)
		Slot 13
OTP ±	J2	Slot 4
OTP + A	Slot 4	(Not used)
OUTPUT A 1-14	Slot 13	J8
OUTPUT A 15 & 16	Slot 13	Slot 5
OUTPUT B-D	Slot 13	(Spare)
OUSTB 0-15	Slot 4	Slots 8-13
PRINT COMMAND	J7	Slot 5
REF ±	J9	Slot 3
RESET A-C	Slot 3	Slot 8
RRL ±	J3	Slot 5
RRL + A	Slot 5	Slot 6
S_A - S_D	J19	Slots 3 & 7
SIG/REF ±	Slot 3	J8
SIG/REF A	Slot 3	Slots 5 & 6
TO PANEL BUS	Slots 8-12	J13-15
WORD IN A_1-A_{16} & B_1-B_{16}	J6	Slot 7
WRITE $\overline{ENB}$	Slot 6	Slot 7
XFER	Slot 3	Slots 8-12

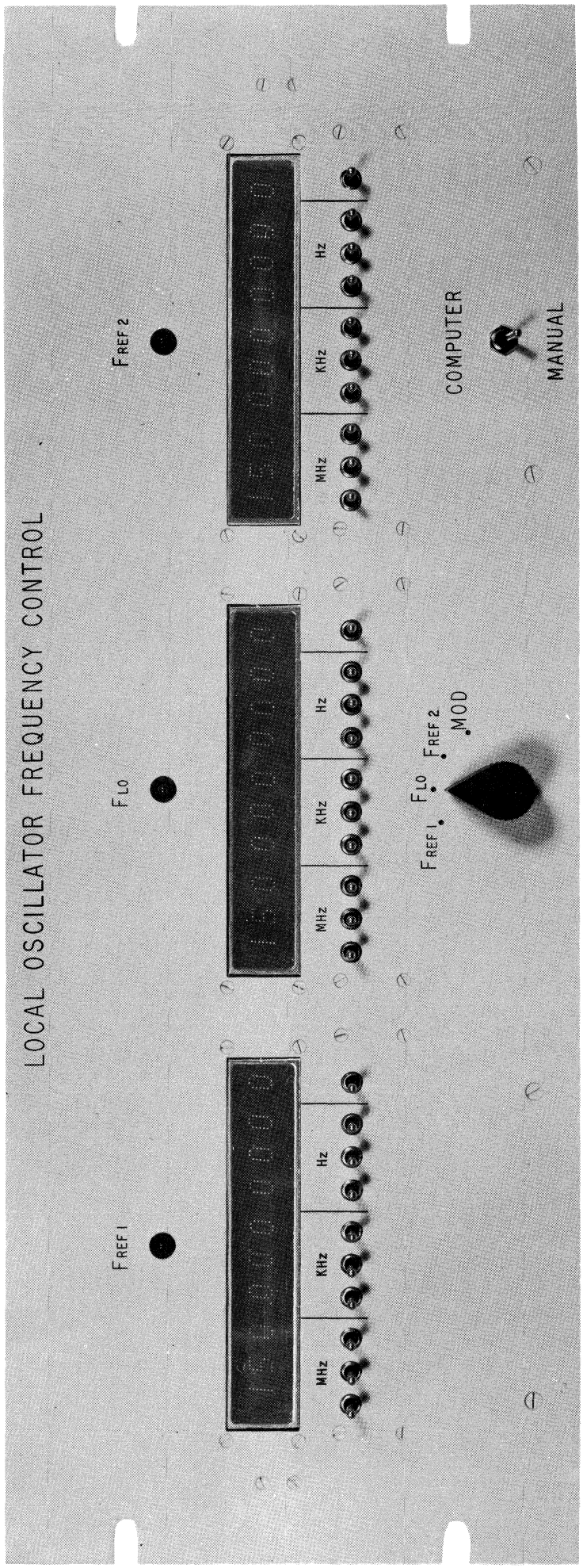
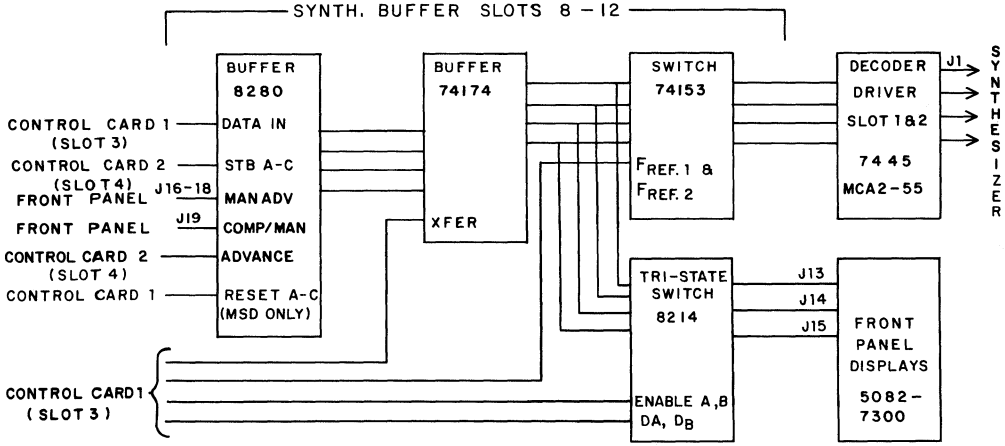
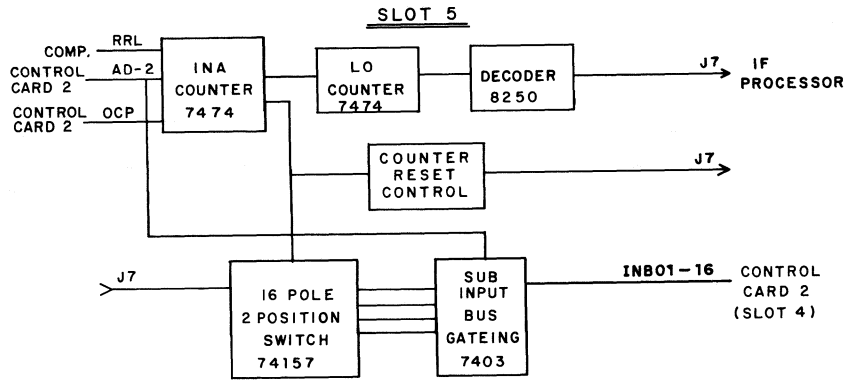


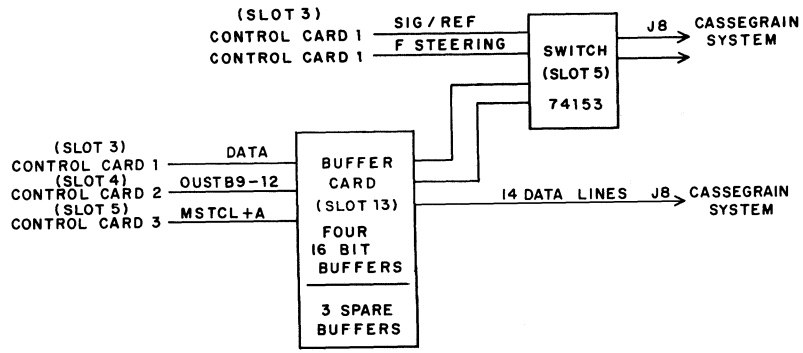
Figure 1 — Photograph of the Digital System



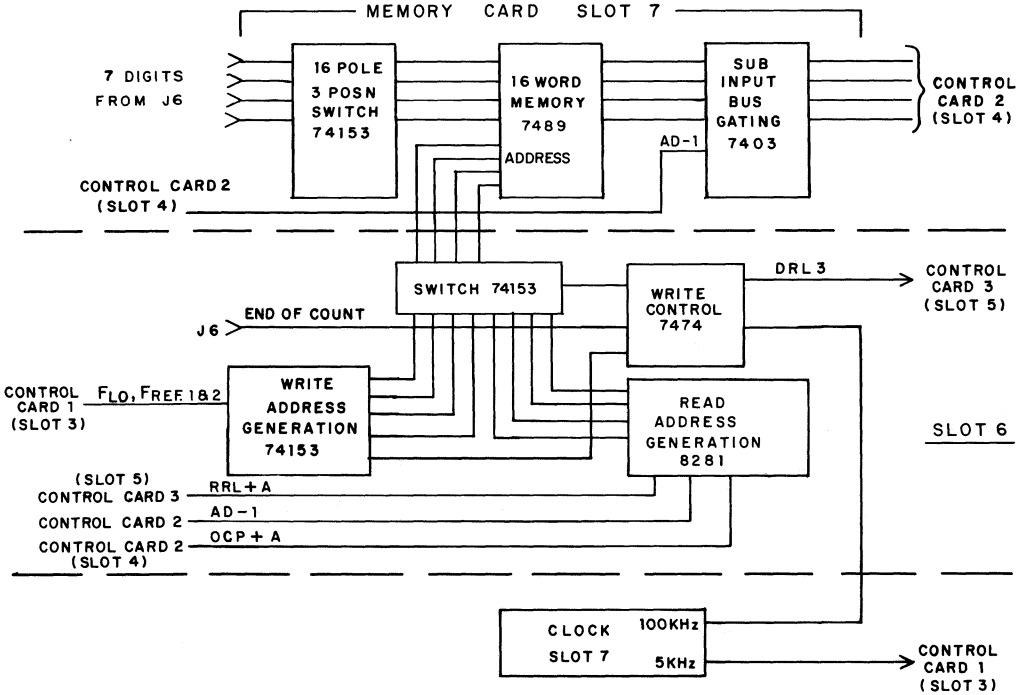
SYNTHESIZER CONTROL FIG. 1A



IF PROCESSOR COUNTER CONTROL FIG. 1C

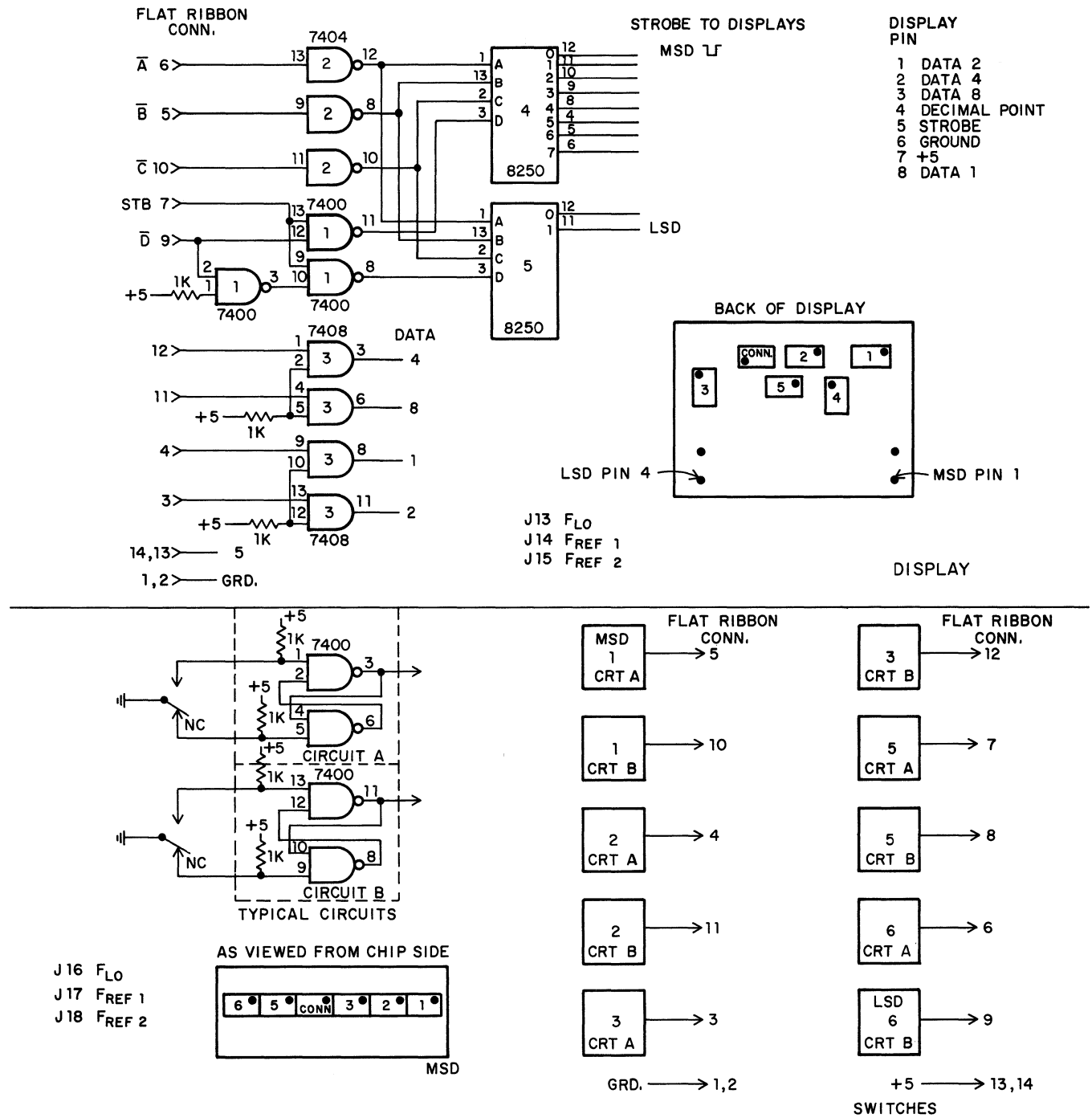


CONTROL & DATA FOR CASSEGRAIN SYSTEM FIG. 1D



ULO COUNTER CONTROL & STORAGE FIG. 1B

Figure 2 — Block Diagram



FRONT PANEL CIRCUITS

Figure 3

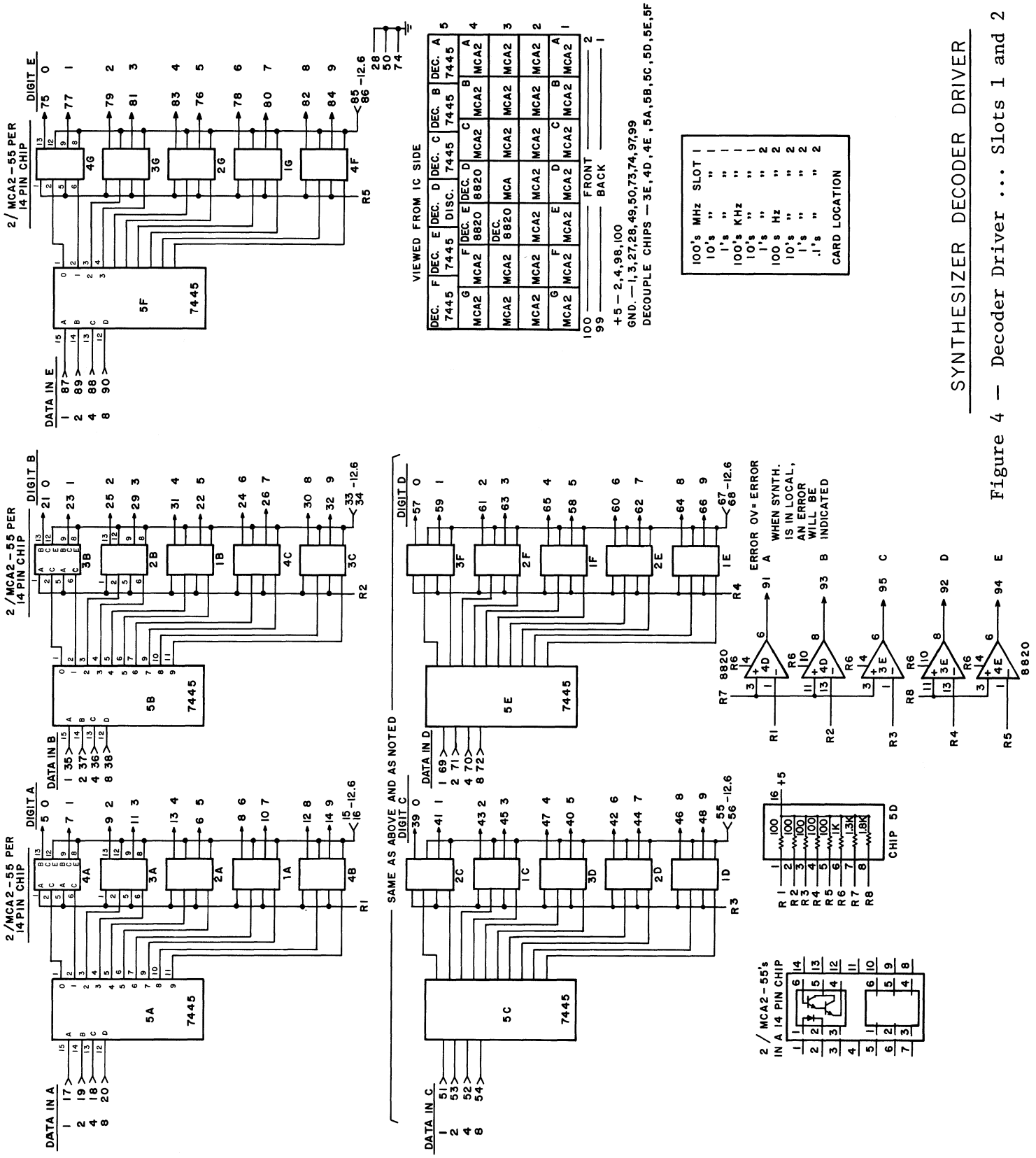


Figure 4 — Decoder Driver ... Slots 1 and 2

SYNTHESIZER DECODER DRIVER

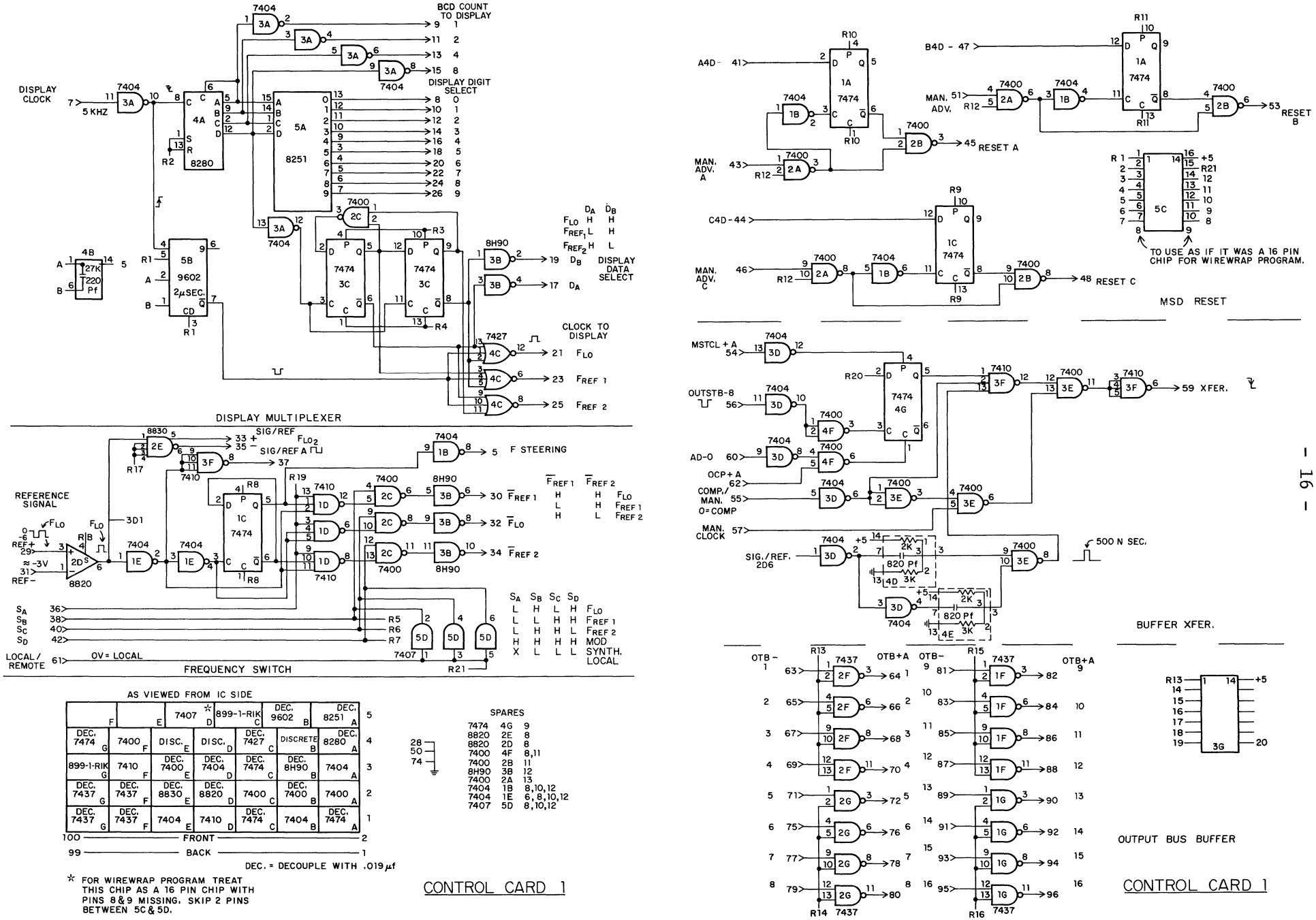
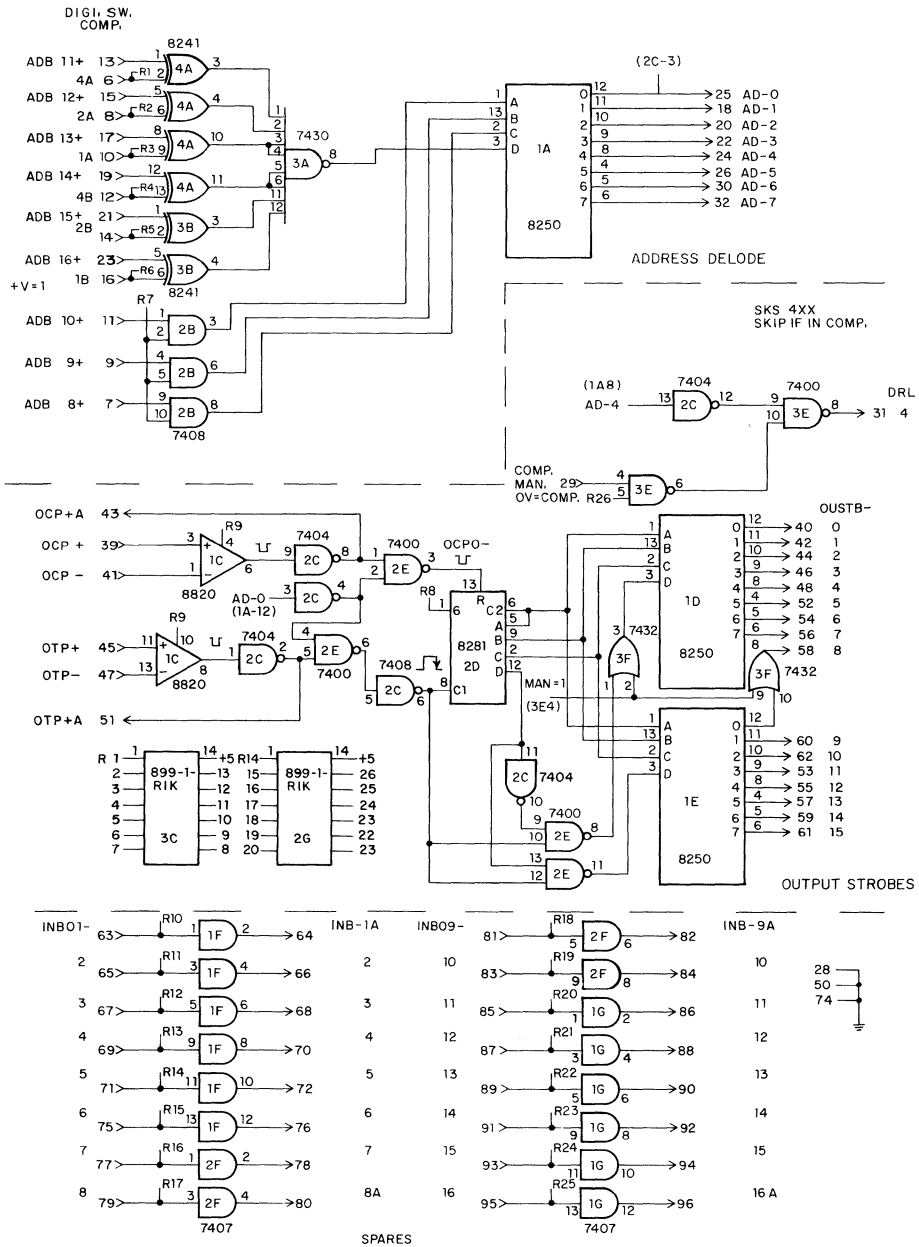


Figure 5 — Control Card 1 ... Slot 3

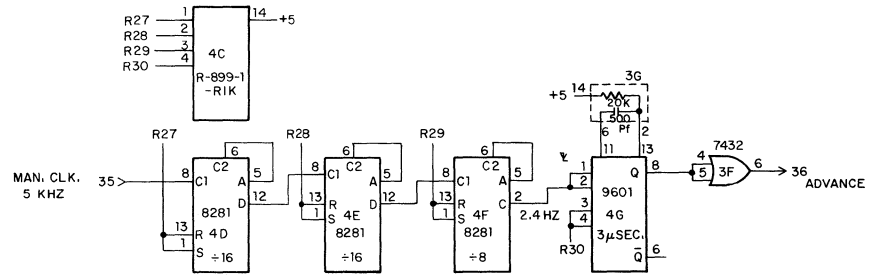


CONTROL CARD 2

						5
DEC. 9601	DEC. 8281	DEC. 8281	DEC. 8281	899-1-RIK		DEC. 8241	4
DISC.	DEC. 7432	DEC. 7400		899-1-RIK	DEC. 8241	DEC. 7430	3
899-1-RIK	DEC. 7407	DEC. 7400	DEC. 8281	DEC. 7404	DEC. 7408		2
DEC. 7407	DEC. 7407	DEC. 8250	DEC. 8250	DEC. 8820		DEC. 8250	1

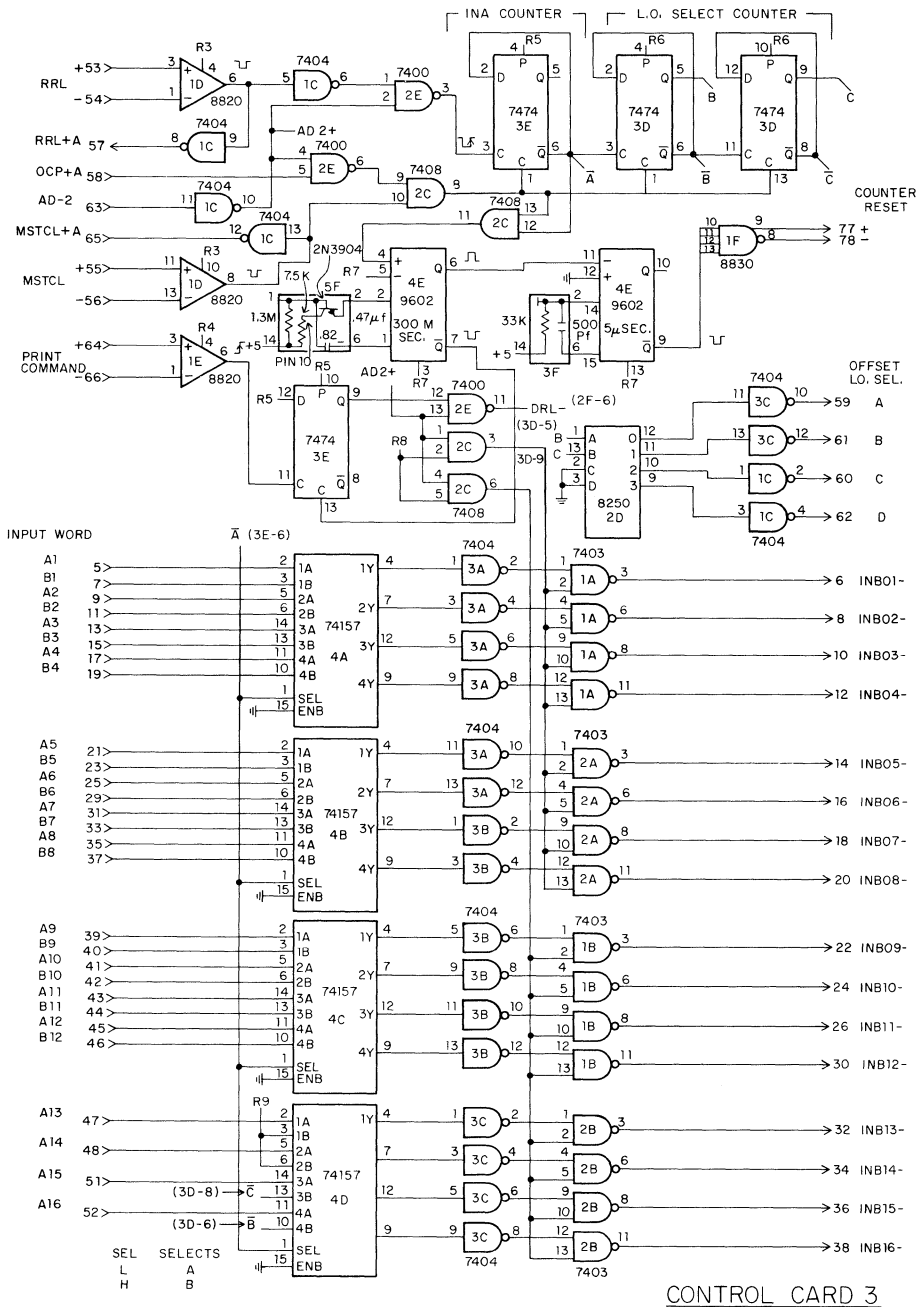
100 — FRONT — 2
99 — BACK — 1

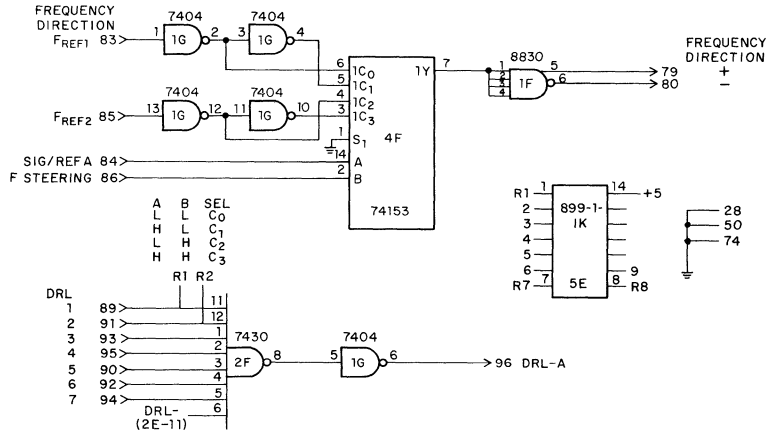
+5 2,4,98,100
GRD. 1,3,27,28,49,50,73,74,97,99
DEC= DECOUPLE WITH .019 μf



CONTROL CARD 2

Figure 6 — Control Card 2 ... Slot 4





	DISC.	899-1-1K					5
DEC. 74153	DEC. 9602	DEC. 74157	DEC. 74157	DEC. 74157	DEC. 74157		4
	DISC.	DEC. 7474	DEC. 7474	DEC. 7404	7404	7404	3
	DEC. 7430	7400	DEC. 8250	7408	DEC. 7403	7403	2
DEC. 7404	DEC. 8830	DEC. 8820	DEC. 8820	7404	7403	DEC. 7403	1

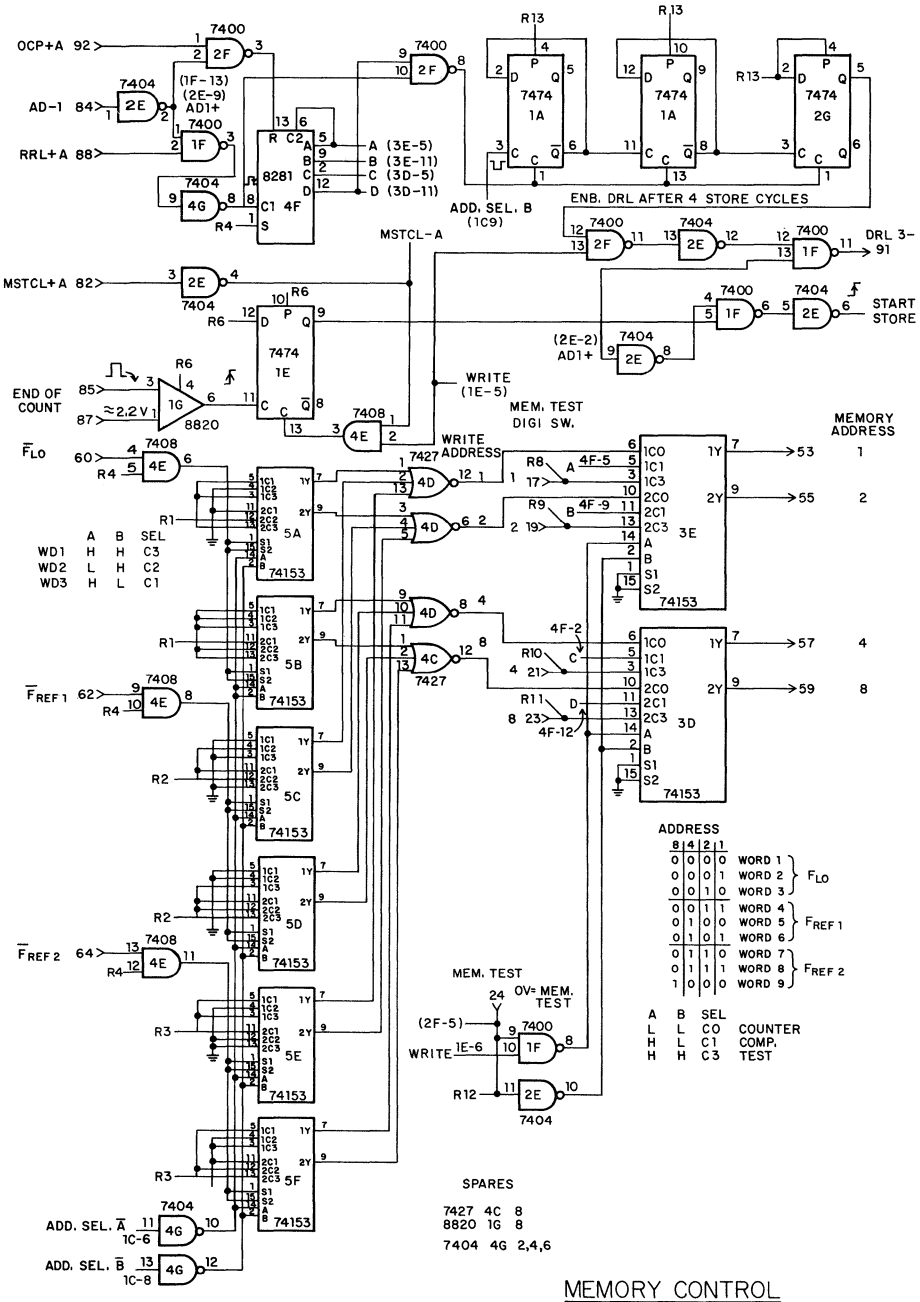
100 FRONT 2
99 BACK 1

DEC = DECOUPLE WITH .019μf

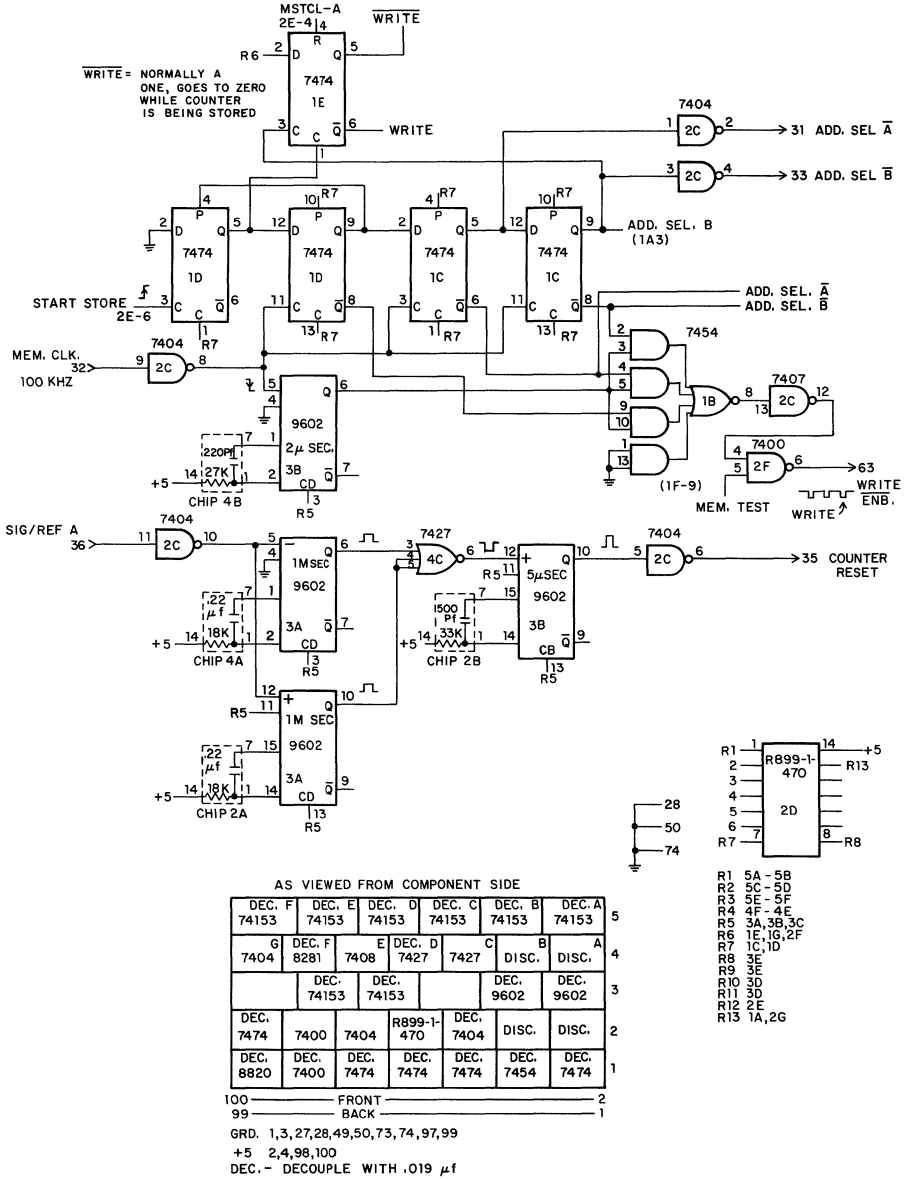
SPARES
7404 1G 8
74153 4F 9
8820 1E 8
7400 2E 8

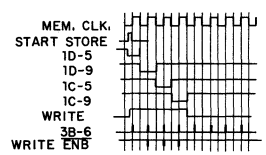
CONTROL CARD 3

Figure 7 — Control Card 3 ... Slot 5



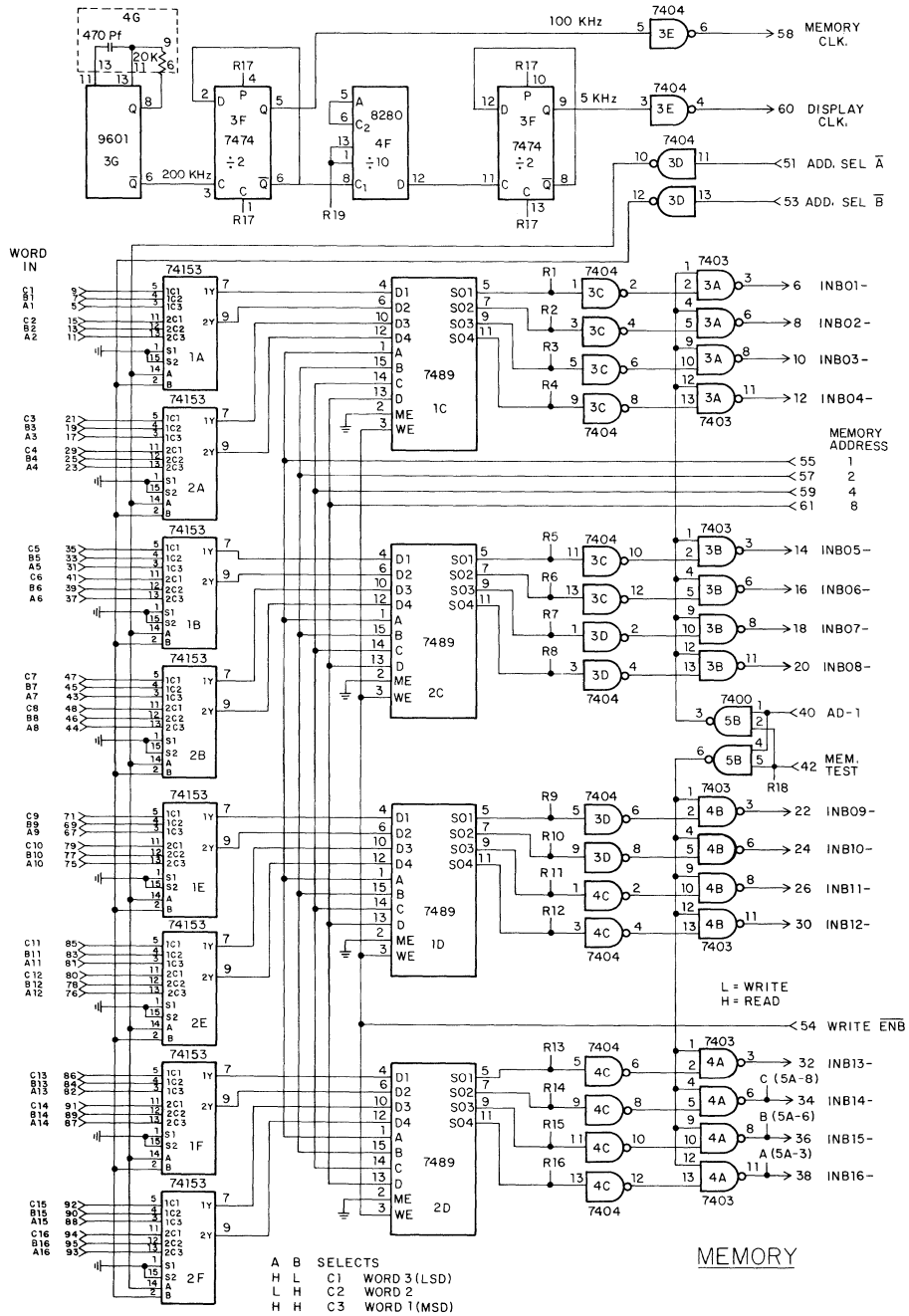
MEMORY CONTROL

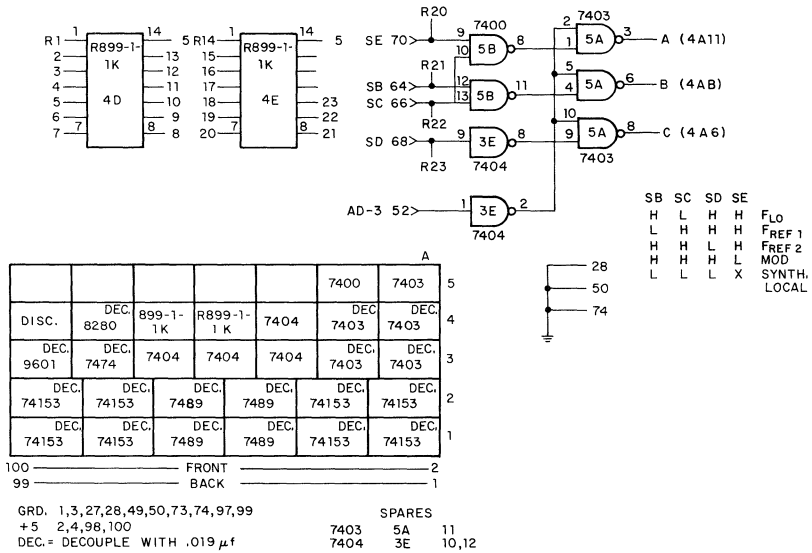




MEMORY CONTROL

Figure 8 — Memory Control ... Slot 6





					A		
					7400	7403	5
DISC.	DEC. 8280	899-1-1K	R899-1-1K	7404	DEC. 7403	DEC. 7403	4
DEC. 9601	DEC. 7474	7404	7404	7404	DEC. 7403	DEC. 7403	3
DEC. 74153	DEC. 74153	DEC. 7489	DEC. 7489	DEC. 74153	DEC. 74153		2
DEC. 74153	DEC. 74153	DEC. 7489	DEC. 7489	DEC. 74153	DEC. 74153		1

100 — FRONT — 2
99 — BACK — 1

GRD. 1,3,27,28,49,50,73,74,97,99
+5 2,4,98,100
DEC. = DECOUPLE WITH .019 μf

SPARES
7403 5A 11
7404 3E 10,12

MEMORY

Figure 9 — Memory ... Slot 7

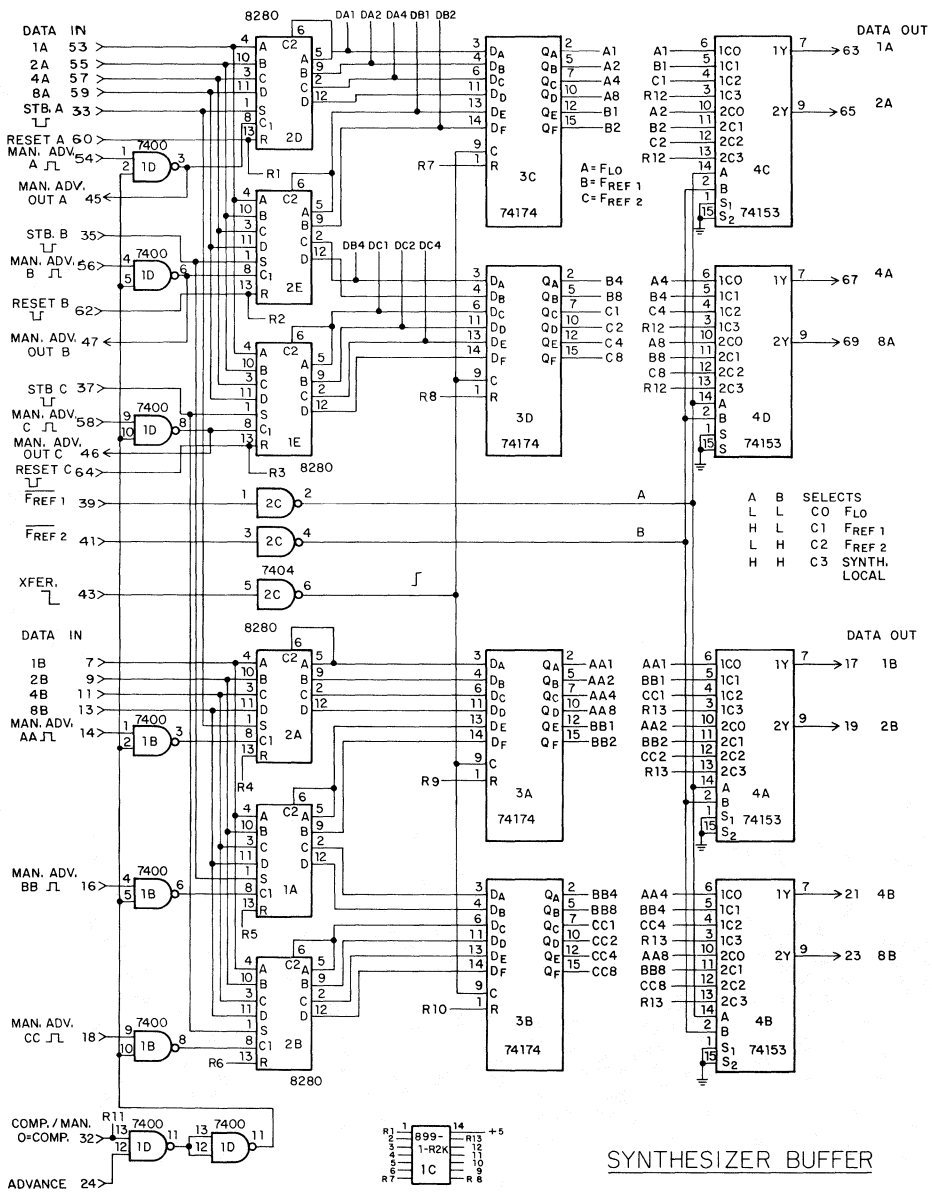
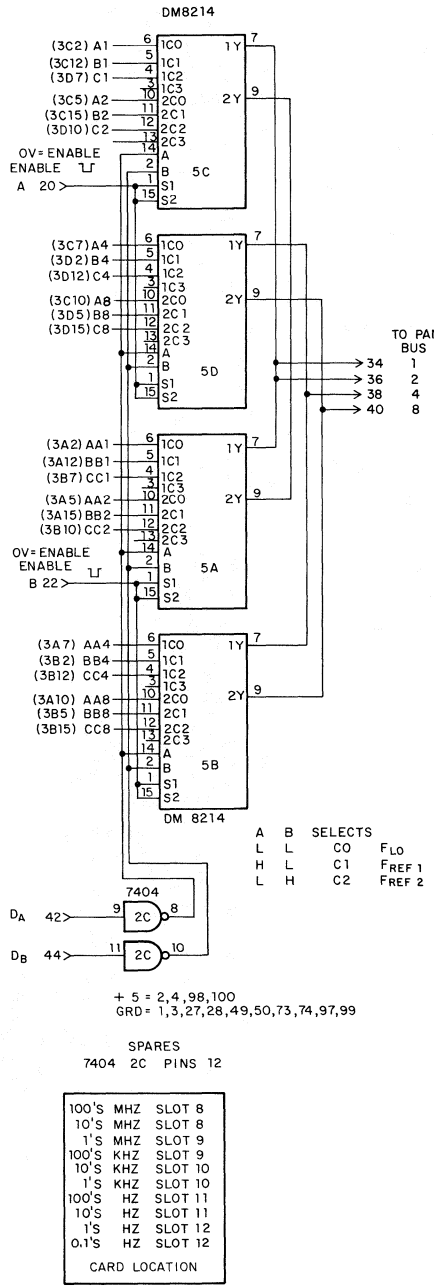
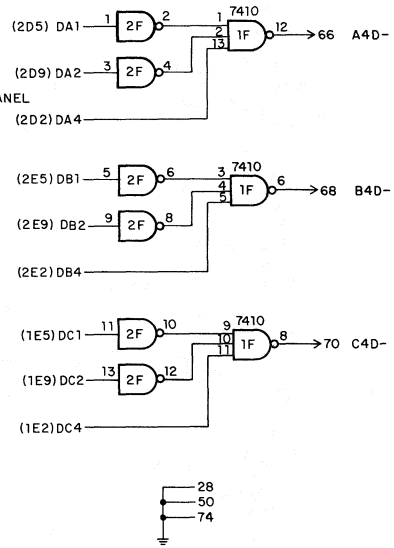
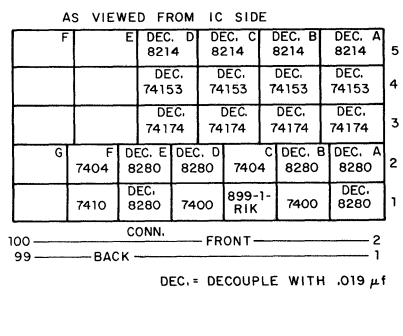


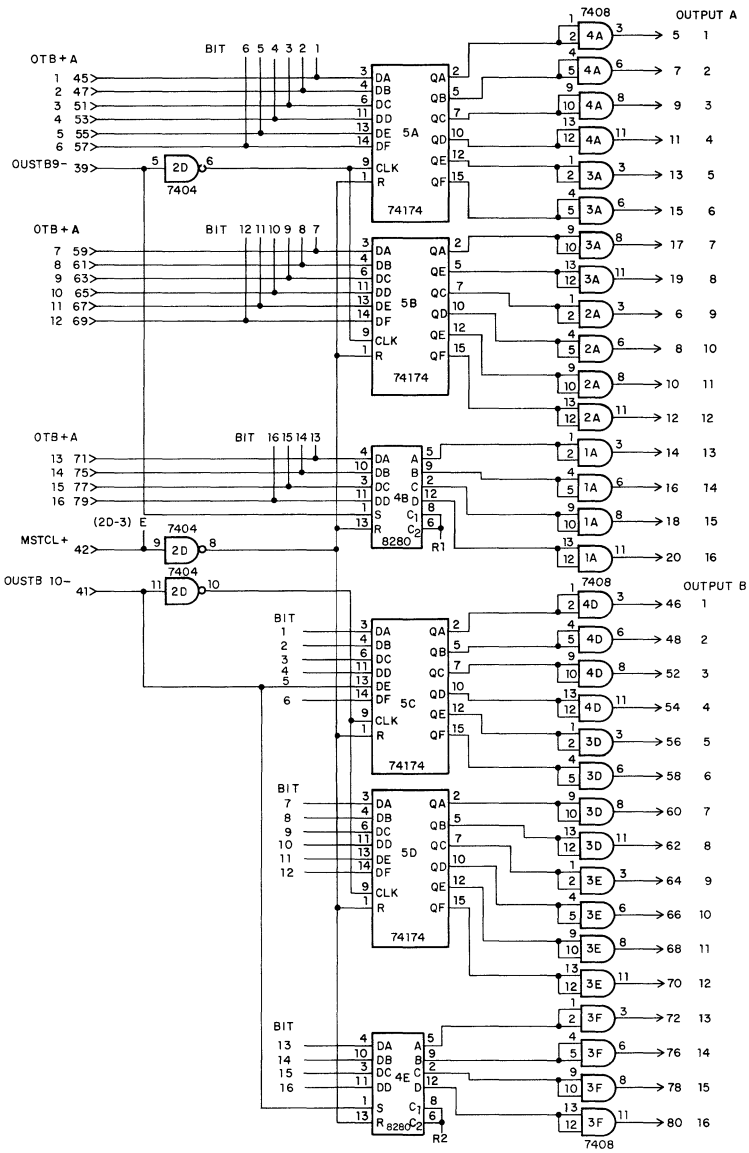
Figure 10 — Synthesizer Buffer ... Slots 8-12

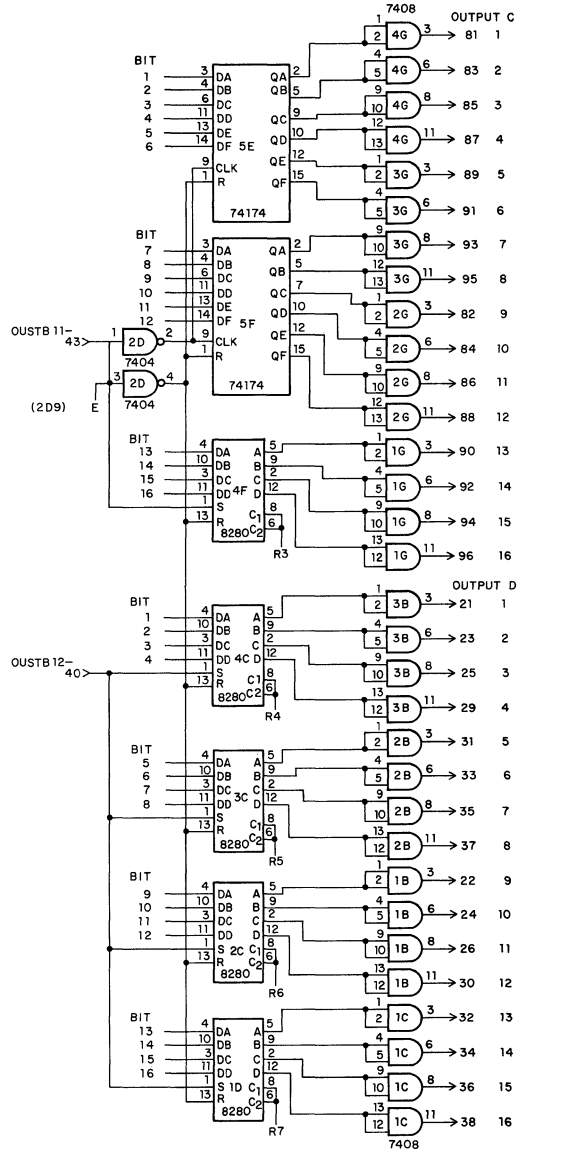


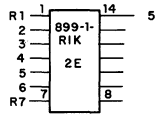




SYNTHESIZER BUFFER







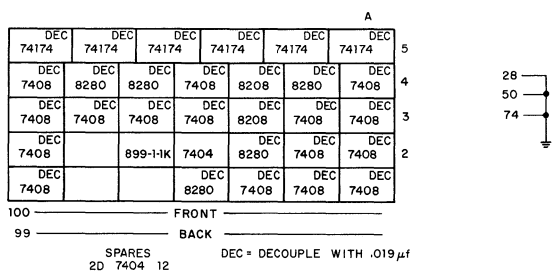
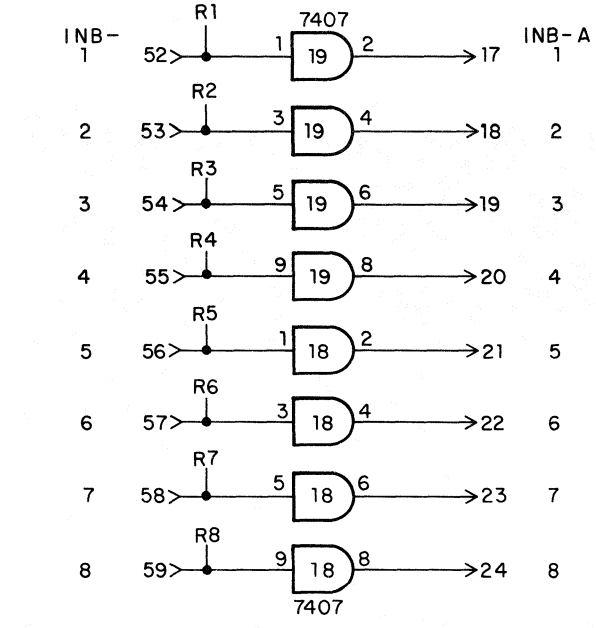
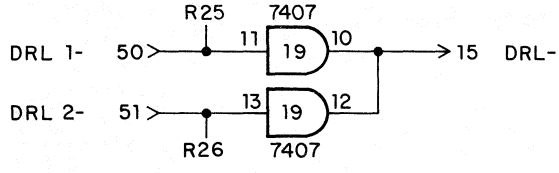
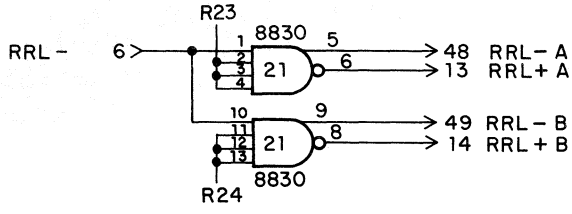
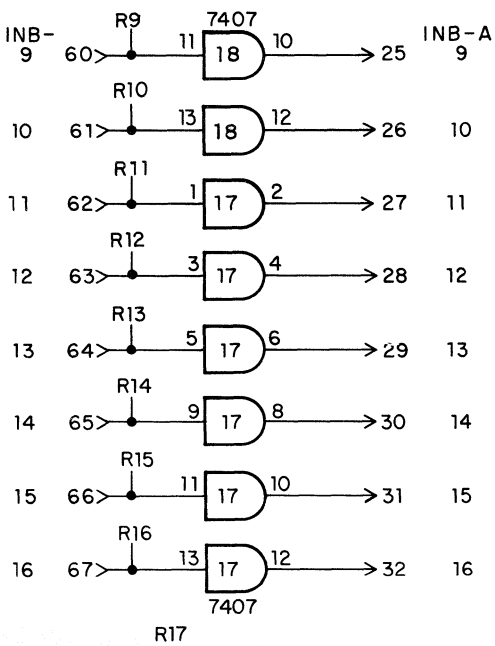


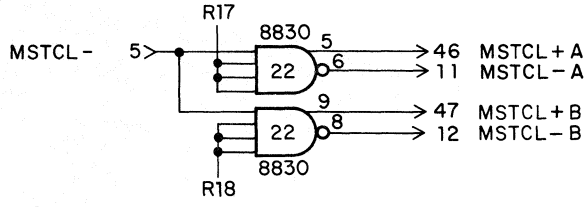
Figure 11 — Buffer Card ... Slot 13

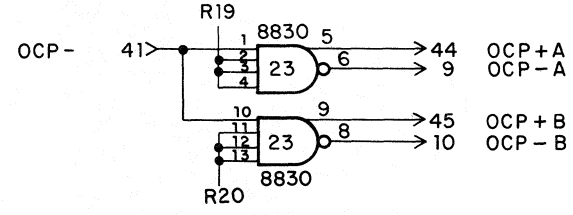


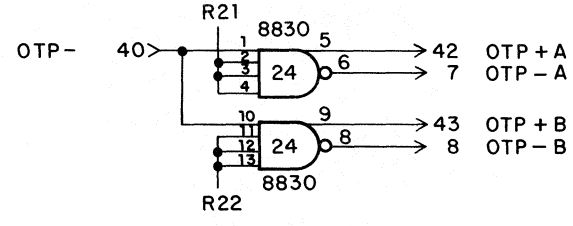


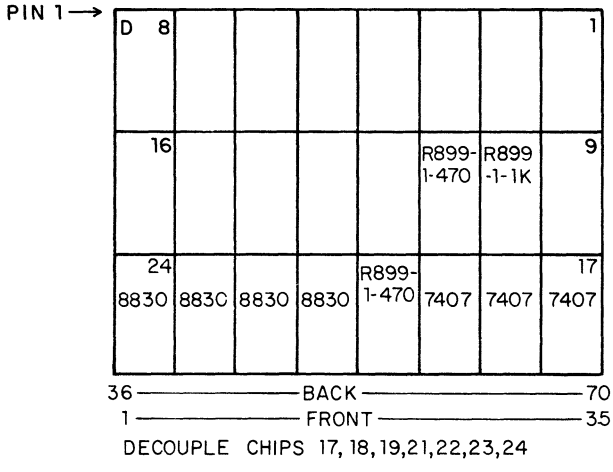












CARD LOCATION

140′ SLOT 3

300′ SLOT 6

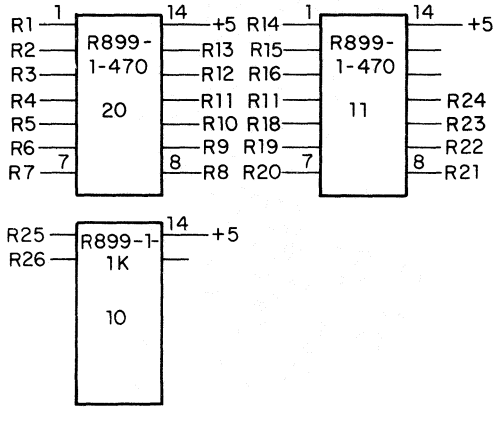
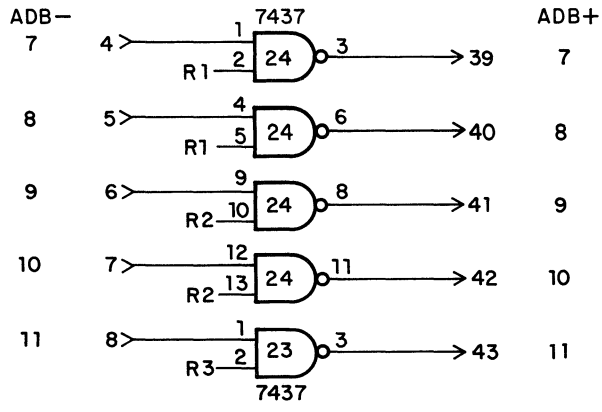


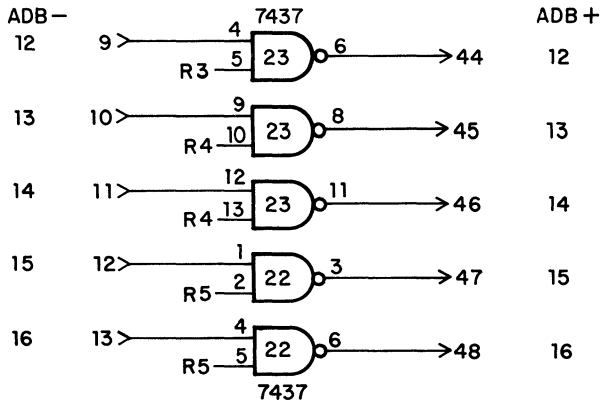
Figure 12

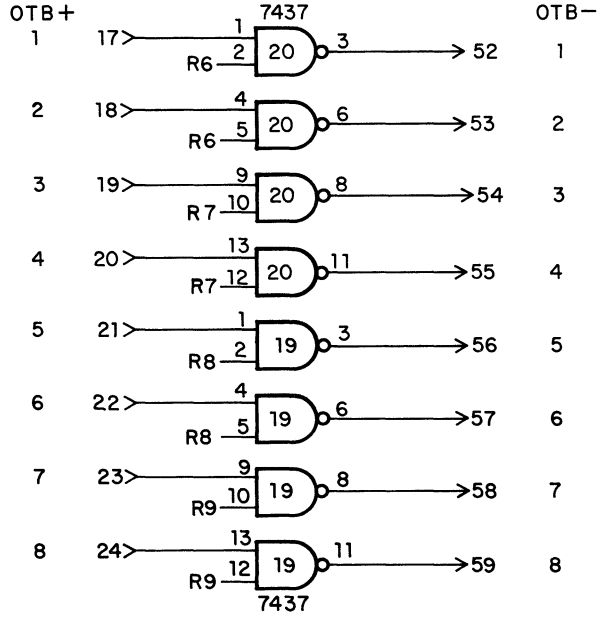
DDP 116 I/O BUFFER 1

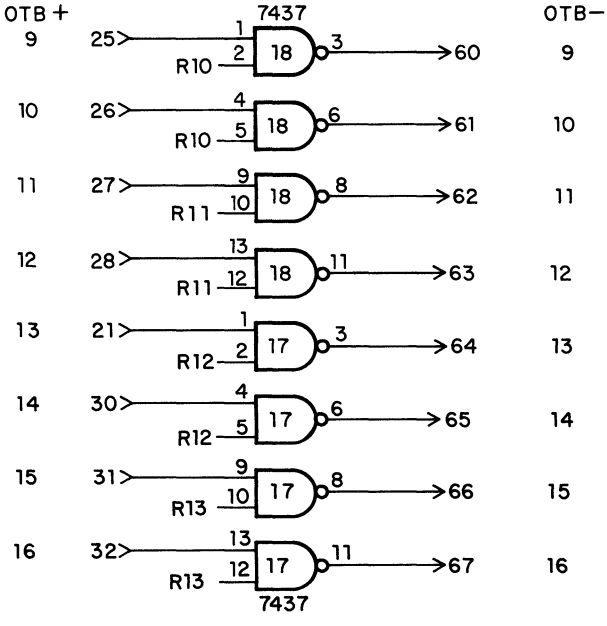
ULO BUFFER FOR

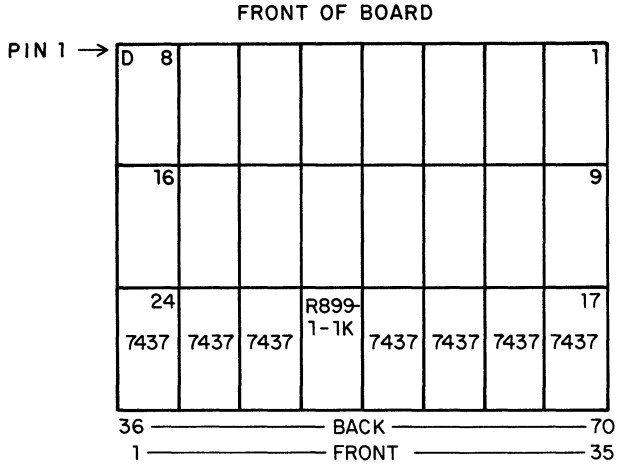
INB, MSTCL, OCP, OTP, DRL, RRL











DECOUPLE CHIPS 17, 18, 19, 20, 22, 23, 24
WITH .22μf

CARD LOCATION

140′ SLOT 2
300′ SLOT 5

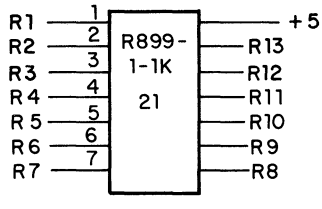


Figure 13

DDP 116 I/O BUFFER 2

ULO BUFFER FOR
ADB & OTB