NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia

Electronics Division Internal Report No. 134

A 512-CHANNEL INTEGRATOR AND MULTIPLEXER

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OCTOBER 1973

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1.0 Introduction

This report describes the interface between the newly developed 256 channel filter receivers and the PDP-11 computer. The same general principles are used as in previous systems (E.D. Internal Report #101) but because of the greater number of channels a more compact form of construction is used.

2.0 Principle of Operation

A block diagram of the interface is shown in Figure 1.

The analog inputs from each channel of the filter receiver are first buffered to reject common mode signals then integrated with a true integrator for an exact period. This period is adjustable and will be set to about 90 ms. At the end of the integration period the integrators are switched to a hold mode, the output of each integrator is sampled, converted to 14 bit binary number and fed to the computer. This scanning, converting and read in process takes about 8 ms for the 512 channels. The integrators are then reset and another integration period begins.

The data flow between the multiplexer and the PDP-11 is controlled by a general purpose direct memory access interface to the PDP-11 unibus. This interface (the DR11-B), rather than using program controlled data transfers, operates directly to the memory, moving data to and from the multiplexer.

A typical read out sequence would take place in the following way. The address of the first channel to be converted is loaded into the channel select counter (this is to permit read outs of banks of channels other than 512). At the start of the hold period the first channel is converted by the 14 bit A/D converter. The end of conversion (E.O.C.) signal from the converter is used to request a data transfer from the DR-11B interface and also to advance the channel select counter to the next channel. When the transfer is complete the DR-11B issues an end of cycle signal that starts the next conversion. This data exchange continues until the prescribed number of transfers has taken place. This is indicated by the overflow of a register internal to the DR-11B that has previously

been loaded by the program with the desired number of data transfers. At the end of a block transfer the program may check that the final channel selected by the channel select counter is the correct one.

A feature is included to permit testing of the A/D converter under computer control by providing it with a variable input from a DAC.

DAT 14 IN is used to indicate if the data being sampled is the result of a signal or reference integration. Signals are also provided that indicate if the filter receivers are being used in the serial or parallel mode.

The multiplexer is also used as an interface between the computer and the radiometer. The computer may provide the signal/reference waveform rather than the internal timing generator in the multiplexer. Also provided by the computer are calibration and zero check signals to the front end and filter receivers.

The timing generator provides the integrate/hold and reset signals to the integrator cards, and also the signal/reference waveform to the front end (or L.O.). The signal reference squarewave is available at 5 Hz, 2.5 Hz and 1.25 Hz so that a signal or reference period may consist of one, two or three integration periods. The timing generator may be synchronized to an external 5 Hz signal (for use with a chopper wheel or nutating subreflector). A 1 MHz clock internal to the timing generator is normally used for generating the various waveforms but provision is made for an external 1 MHz clock.

Manual scanning of integrator outputs is useful for checking correct operation of the filter receivers and multiplexer. A V.C.O. is used to drive the channel select counter up or down at whatever rate is desired. The channel number is displayed both in binary and decimal form. The channel output is displayed on a moving coil meter, the value at the end of an integration period being stored in a sample/hold circuit.

The system timing diagram is shown in Figure 2.

3.0 Integrator Multiplexer Card

The basic printed circuit card used in the integrator/multiplexer consists of 16 channels, each channel being made up of a buffer amplifier, and a true integrator with hold and reset capability. Also on the card is a 16 channel multiplexer integrated circuit. Thirty two of these cards are used to give the 512 channel capability.

A circuit diagram of two channels, together with the 16 channel multiplexer and output amplifier is shown in Figure 3 and an assembly drawing of two channels is shown in Figure 3A.

3.1 Buffer Amplifier

The buffer amplifier used was a Sprague ULN 2157. Two of these amplifiers are packaged in a 14 pin dual in line plastic package. The relevant performance specifications of this amplifier are as follows:

	TYP	MAX
Input offset voltage	$\pm$1.5 mV	$\pm$5.0 mV
Input offset current	$\pm$5 nA	$\pm$25 nA
Input bias current	70 nA	250 nA
Input offset voltage/ temperature		10μV/°C max

3.2 Integrate/Hold Switch

To perform the switching functions in the integrate/multiplexer we made extensive use of the CMOS analog switches that have become available over the last year. The switch used for performing the integrate/hold function is a DG 200 manufactured by Siliconix, Inc. The DG 200 has two independent analog switches, each switching function being controlled directly from TTL logic. The "on" resistance is <100 ohms and is not very dependent on input signal level or

temperature. The switch operated from ±15V power supplies and will switch analog signals of ±15V.

3.3 Integrator

The operational amplifier used for the integrator is a ULN 2177 manufactured by Sprague. The time constant of integration of 100 ms was satisfied with a 1 MΩ input resistor and a 0.1μF polystyrene capacitor. The input offset currents are critical in this case and the important specifications of the amplifier are listed below:

	TYP	MAX
Input Offset Voltage	±1.5 mV	±5 mV
Input Offset Current	±0.4 nA	±1 nA
Input Bias Current	0.8 nA	2 nA
Open Loop Voltage Gain	150 V/mV	

A polystyrene capacitor was used for low leakage and low dielectric absorption.

A junction F.E.T. was used for resetting the integrator because the discharge current would be slightly too high for CMOS device. A CDR5 level shifter is common to all reset transistors on a card and serves to change the TTL input signal to ±15 suitable for switching the F.E.T.s.

3.4 Multiplexer Chip

To sample the output of each integrator while in the "hold" mode a 16 channel CMOS multiplexer with 4 line binary addressing is used. This multiplexer chip, a DG 506, is manufactured by Siliconix and enjoys the same advantages as CMOS analog switches in general. Resistors were included in series with each analog input to the device to limit the input current needed to charge the common drain capacitance when switching between analog inputs of different levels. This current should be limited to avoid burning out the F.E.T. switches and also to avoid overloading the integrator. A later

version of this chip (produced by Harris Semiconductor) includes these resistors. The additional time constant introduced by these resistors is not significant.

3.5 Output Amplifier

The output amplifier associated with the multiplexer is used in a unity gain non-inverting mode to give a high input impedance. This is important to avoid errors introduced by variations in "on" resistance of the different channels of the DG 506.

3.6 Performance of Integrator/Multiplexer Card

All gain determining components on the card are ±1%. Tests on the prototype card gave a highest channel gain of 1.005 and lowest gain of 0.992. The variations in gain for different channels with temperature over the range of 0-45°C were $\frac{\Delta G}{\Delta T}$ = +1.0 x 10^{-4}/°C minimum and $\frac{\Delta G}{\Delta T}$ = +3.5 x 10^{-4}/°C maximum. The rise time at the output of the card was measured and found to correspond to a time constant of 0.4μs. To permit settling to within one bit of the 14 bit A/D converter a 4μs delay between selection of a channel and the start of the conversion is used.

The zero offset voltage of each channel may be adjusted to zero by means of the offset potentiometer associated with the buffer amplifier.

3.7 Cost Per Channel

The cost per channel is as follows:

Component cost per channel	$15.38
Printed circuit card cost per channel	1.38
Construction cost per channel	2.50
	$19.26

This cost refers just to integrator multiplexer cards and does not include the control logic or A/D converter.

4.0 Control Logic

4.1 Timing Logic

The readout, reset, integrate signals are generated by the 1 MHz internal oscillator or 1 MHz external oscillator. A 5 Hz squarewave from the computer, sub-reflector (sync input) or the internal 5 Hz gives the starting pulse (SYNC A) (Fig. 4) for the generation of the readout, reset, integrate cycle.

The readout, an 8 ms positive pulse, is generated by dividing the 1 MHz clock.

The reset is a 1 ms positive pulse and is used to reset all integrators to zero. When in the TEST mode the reset is used to reset the channel select counter (CSC). At the end of reset the 1 MHz clock is divided by decade counters to generate the integrate period, Fig. 4. This is a variable time period and can be varied from 70-90 ms by selector switches behind the front panel.

4.2 Signal/Reference

Signal/reference can come from three sources, internal, computer and external (Fig. 4).

Internal signal/reference is generated from the 1 MHz and can be varied by a front panel switch for 1.25 Hz, 2.5 Hz or 5 Hz operation. This signal also available on BNC connectors on the back panel in either 3C or TTL logic.

External signal/reference comes from a BNC on the back panel and can be either 3C or TTL logic input. It should be no higher frequency than 5 Hz.

The computer signal reference is generated by Data Out 14 from the computer and should be no higher frequency than 5 Hz.

An external sync must also be supplied when in the external or computer position. This signal generates Sync "A" and should be a 5 Hz TTL signal. When in external position J21 on the back panel is used and the sync output of the nutating

subreflector can generate Sync "A". When in the computer position Data Out 15 is switched at a 5 Hz rate to generate Sync "A". Sync "A" is used to start the readout cycle.

4.3 Channel Select Counter

Channels can be selected in two ways manual or computer. In the manual mode the clock pulses (Clock M) to advance the CSC are generated by a VCO, the frequency of the VCO is controlled by the manual channel advance pot on the front panel (Fig. 5).

An up-down counter is used and the manual advance can make the channels advance up or down to the desired channel.

In the computer mode the end of cycle from the A/D (Clock A) advances the counter. It only allows the counter to count up. When the test-normal switch is in normal the CSC is loaded by the computer.

The four least significant bits of the CSC are buffered because they drive the DG 506's (A) on the 32 integrator boards. The next five bits select which board is displayed or sent to the computer by driving DG 506 (B) on Board W. The MSB 2^8 is an enable that selects channels 0-255 or 256-511 by enabling the DG 506 (B) on Card W.

The load lines from the computer load the CSC when in computer-normal mode. The load command is generated by the "GO" command from the computer.

A one shot is used to reset the CSC when switching from computer to manual mode.

The binary output of the CSC is displayed by L.E.D.s on the front panel. This output is also converted to BCD and is displayed on the Numeric Display (Fig. 5).

4.4 Interface

Inputs from computer to multiplexer

GO is used to generate the load data pulse for CSC. The $\overline{GO}$ bit triggers a N8162A one shot that produces the load pulse (Fig. 5).

END of cycle from the computer (EOC computer) along with the readout produce the trigger for the A/D and reset the S/H mode control F/F (Fig. 5).

Data Out 13 is used to generate the cal "on" signal. A F/F used as a latch stores the data until it is updated.

Data Out 12 is used to generate the zero check.

Data Out 15 is used to generate Sync "A" computer.

Data Out 14 is used to generate Sig/Ref computer.

Funct #1 - This computer output is used to select what type of data will go to the computer either channel data or the last count in the CSC (Fig. 5).

Funct #2 - This is used to test the calibration of the A/D. Funct 2 allows either channel voltages or a cal voltage from the computer to be applied to the A/D (Fig. 5).

Output of Multiplexer to Computer

Cycle REQ A is generated on the falling edge of the EOC from the A/D. It is a .5 μsec pulse and is generated by a one shot (Fig. 5).

DATA IN LINES 0→13 can either contain the data from the various channels or the final count of the CSC. These are selected by function 1 (Fig. 5).

STATUS B&C. These inputs come from the filter banks and by a switch closure select the parallel or serial mode of operation.

4.5 A/D Converter

The A/D converter is an Analogic MP2914A (Fig. 5). It has 14 bit output with 10 μsec conversion time. The MSB is Bit 1 and LSB is Bit 14. The input to the A/D is buffered by an Analog Devices SHA-2A Sample Hold Amplifier. To insure that the input to the A/D does not change during the conversion of data the SHA-2A is put into the hold mode before the A/D starts conversion.

Input to A/D

The input to the A/D can come from two sources - computer or integrators. When the input comes from the integrators Funct 2 is in a "Hi" state. This means that normal data transfer between the computer and multiplexer is taking place. When Funct 2 is low

a calibration output from the computer can be fed into the A/D to check its calibration. The cal voltage input must be positive.

Calibration of A/D

Refer to the enclosed data sheet on the MP2914A.

Logic Inputs & Outputs A/D

The trigger input to the A/D is generated by the readout or the end of cycle from the computer. The A/D trigger is a 4 μsec positive pulse and conversion takes place on the NEGATIVE edge of this pulse. The trigger also generates the mode control for the SHA-2A.

End of Cycle from A/D (EOC)

This is a 10 μsec pulse that goes positive during conversion and negative when conversion is finished. The EOC pulse is used to advance the CSC and send a request A to the computer and clocks the mode control F/F for the SHA-2A.

5.0 Front Panel Meter Circuit

The input of the A/D is buffered and this signal is the input to the meter circuit (Fig. 5).

A CAG 30 is used to control this input and is only closed when in manual mode. The LH 0043 is a sample Hold module and its hold mode is controlled by readout. When in readout the input is sampled. The input to the meter circuit is also connected to an isolated BNC on the front panel.

The gain of the meter circuit can be varied by a switch on the front panel. The ranges are 20 mV, 200 mV, 2V, 20V full scale.

6.0 Power Supplies

The multiplexer requires ±15 volts at 2.5 amps and +5V at 3 amps. The power supplies are mounted in a separate chassis with current and voltage metering as shown in Figure 6.

7.0 Constructional Details

A total of 36 cards are used in the multiplexer, 32 integrator boards, 3 wirewrap logic boards and one A/D printed circuit board.

The chassis used to house these boards was designed by Arthur Shalloway and Gene Runion and was found to be ideal for this purpose.

A specially designed power plane distributes power to the board connectors. Wirewrap connectors are used throughout. Moulded plastic card guides and a simple constructional technique make the chassis inexpensive and simple to produce. Two large quiet fans insure adequate air flow over the circuit boards.

Connections are made to the filter receivers via four 140 pin Elco connectors and two 56 pin Elco connectors are used for the computer interface. BNC connectors are used for connections to the standard receiver and front end.

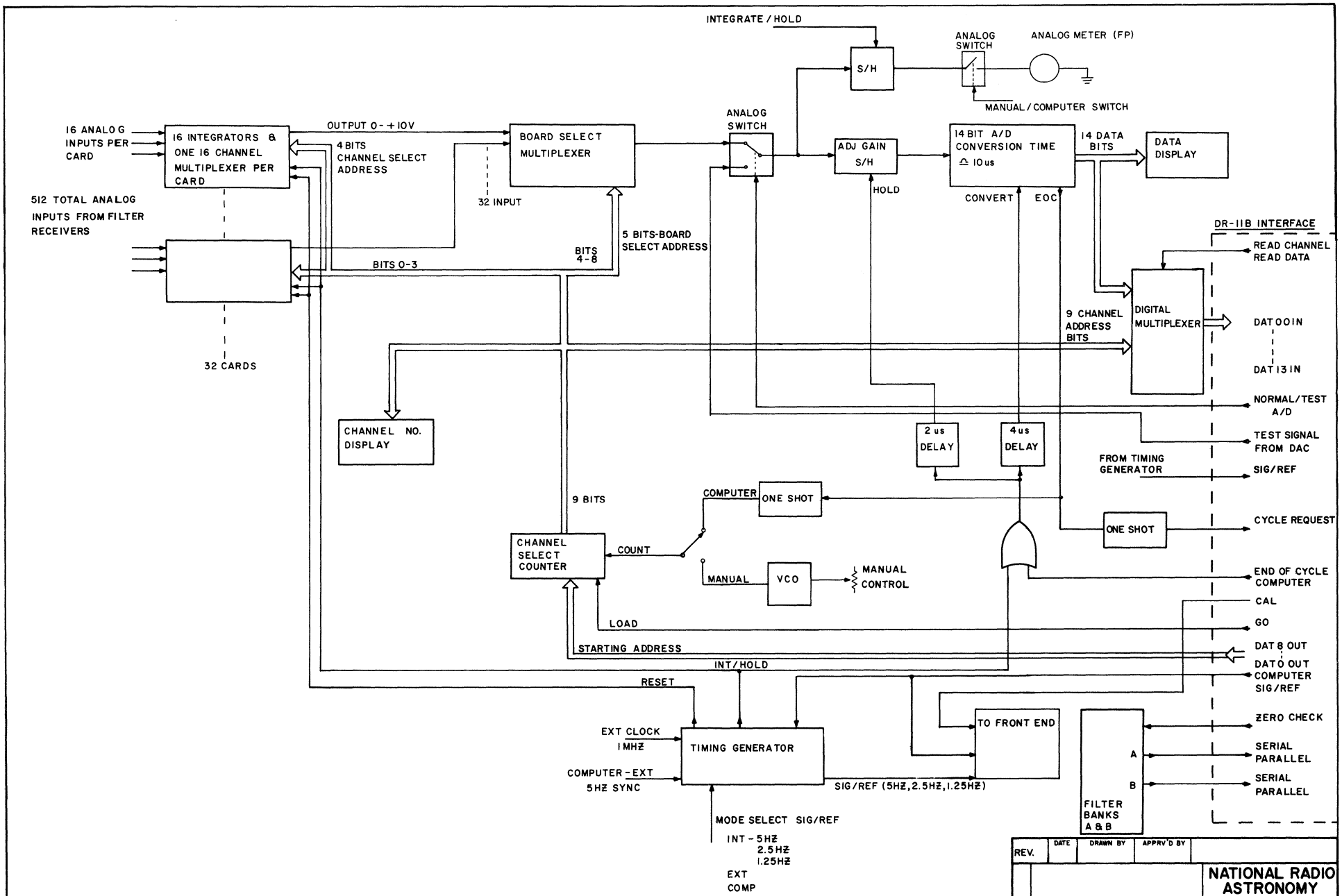


FIGURE 1

REV.	DATE	DRAWN BY	APPRV'D BY

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, Va., 22901

512 LINE MULTIPLEXER BLOCK DIAGRAM

DRAWN BY C PACE
DESIGNED BY
APPROVED BY

DATE 9-19-73	SHEET NUMBER	DRAWING NUMBER C 2579 BI	REV.	SCALE

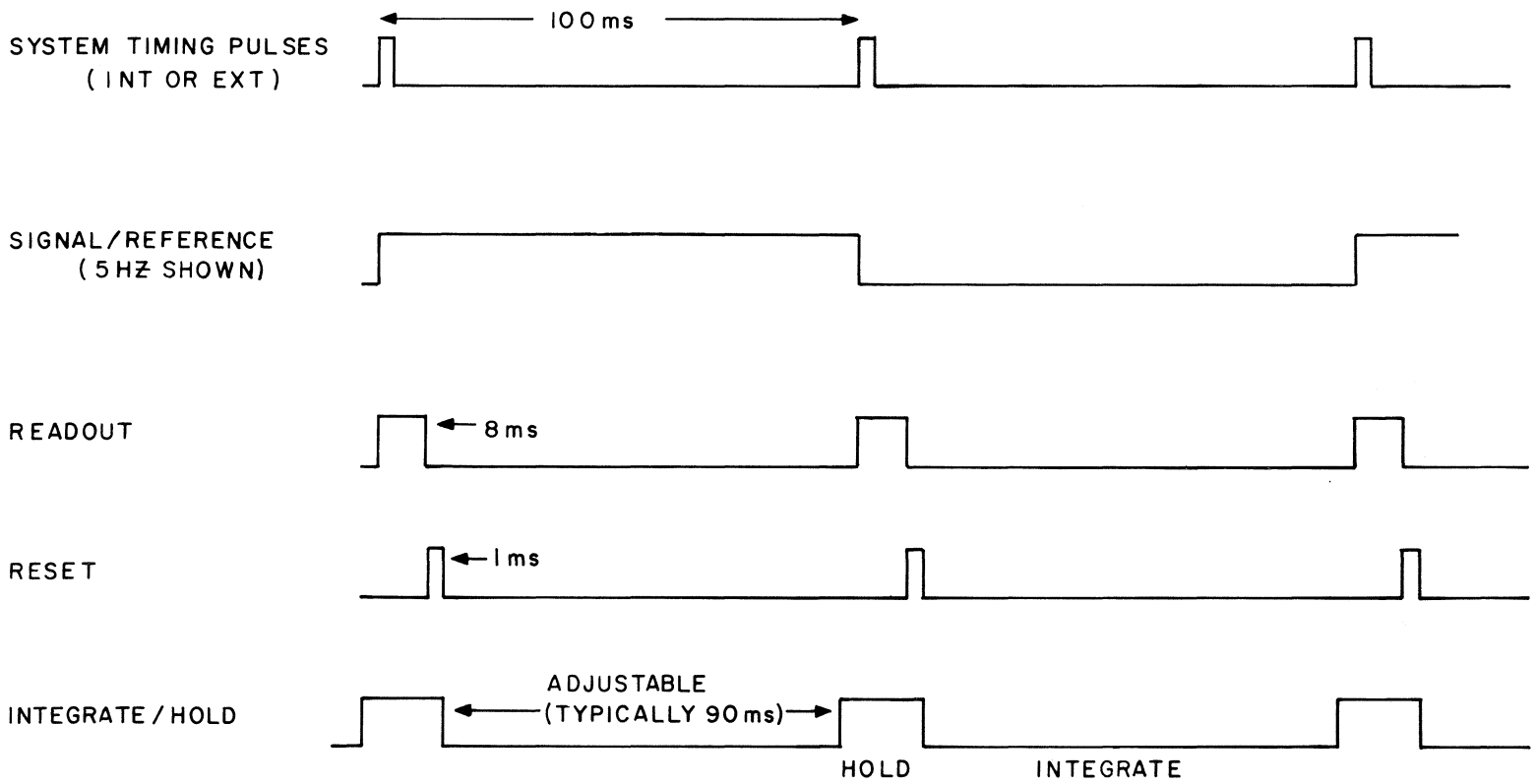
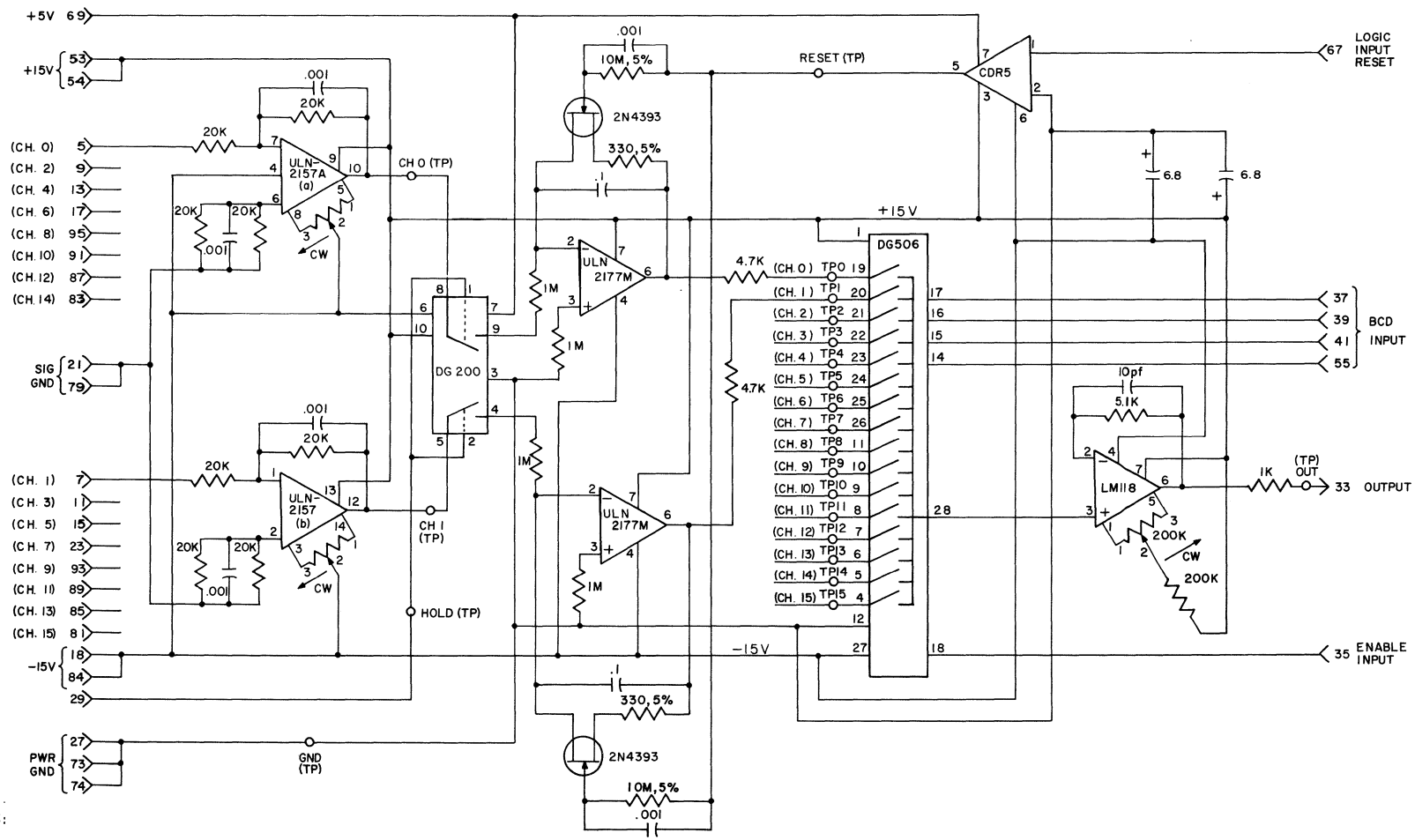


FIGURE 2

512 LINE MULTIPLEXER
SYSTEM TIMING

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, Va., 22901
DRAWN BY C PACE
DESIGNED BY
APPROVED BY

DATE	SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
10-3-73		A 2579 B2		



NOTES:

1. ALL CAPS IN UF UNLESS OTHERWISE NOTED.
2. DG200 + ULN2157 TWO UNITS IN ONE PACKAGE.
3. ALL RESISTORS 1% UNLESS OTHERWISE NOTED.
4. TESTPOINT COLOR CODE:
   - BLUE - MULTIPLEXER INPUTS AND BUFFER OUTPUT
   - BROWN - HOLD
   - GRAY - RESET
   - RED - BUFFER AMP OUTPUT FROM ULN2157 TO DG200
   - YELLOW - GROUND

FIGURE 3

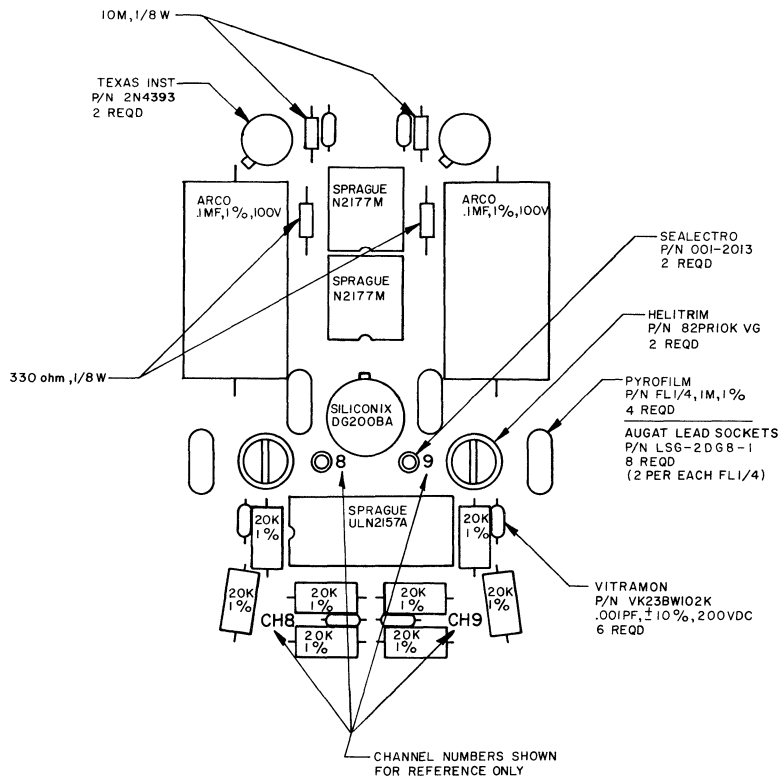
REV.	DATE	DRAWN BY	APPRV'D BY	
A	9-18-73	C. PACE		SW-DG506

SCHEMATIC
2 CHANNELS OF
16 CHANNEL MULTIPLEXER

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA., 22901
DRAWN BY John Cannest
DESIGNED BY
APPROVED BY C. Pace

DATE 4-13-73 | SHEET | DRAWING C2579SI | REV

DWG NO C2579SI



NOTES:

1. SCALE: 2/1.
2. COMPONENTS ARE SHOWN FOR TWO CHANNELS WHICH ARE TYPICAL FOR ALL CHANNELS.
3. FOR SCHEMATIC SEE DRAWING #C2579S1.

FIGURE 3 A

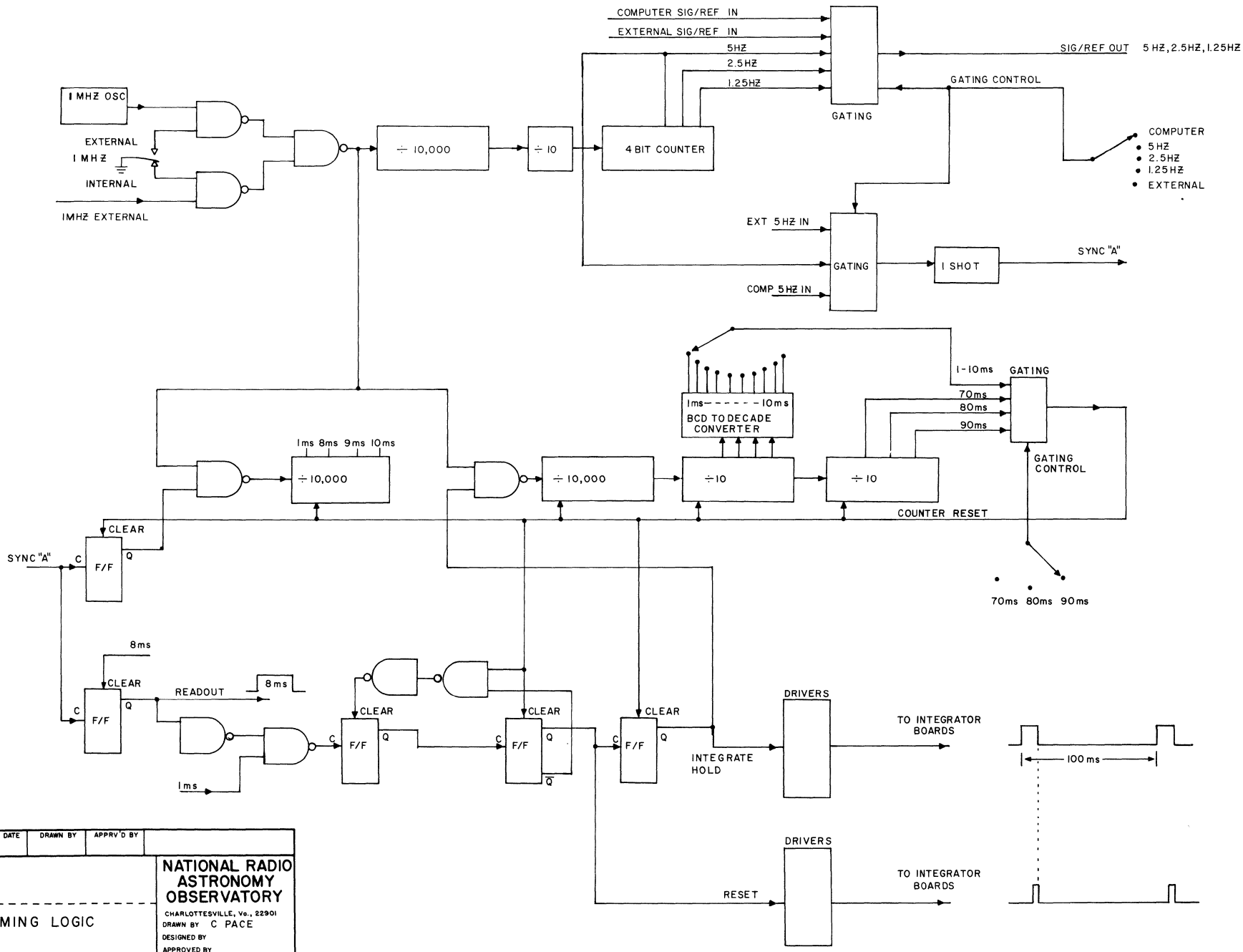
REV.	DATE	DRAWN BY	APPRV'D BY	

ASSEMBLY DRAWING
2 CHANNELS OF
16 CHANNEL MULTIPLEXER

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, Va., 22901
DRAWN BY John Earnest
DESIGNED BY
APPROVED BY C Pace

DATE	SHEET NUMBER	DRAWING NUMBER	REV.
4-10-73		B2579M2	

DWG. NO. B2579M2



REV.	DATE	DRAWN BY	APPRV'D BY	

TIMING LOGIC

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, Va., 22901
DRAWN BY C PACE
DESIGNED BY
APPROVED BY

DATE	SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
10-3-73		C 2579 L3		

FIGURE 4

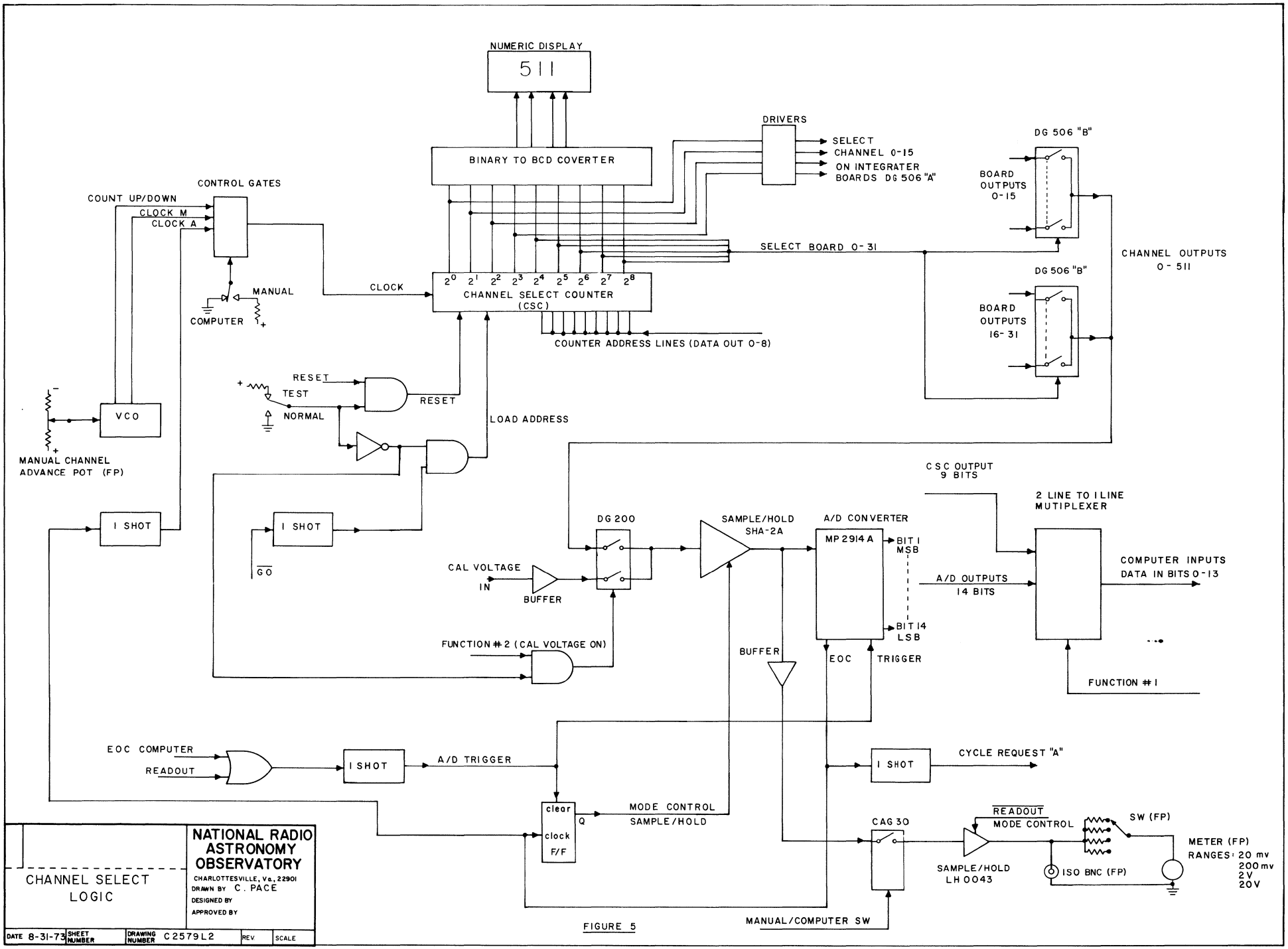


FIGURE 5

CHANNEL SELECT LOGIC	NATIONAL RADIO ASTRONOMY OBSERVATORY CHARLOTTESVILLE, Va., 22901 DRAWN BY C. PACE DESIGNED BY APPROVED BY
DATE 8-31-73 / SHEET NUMBER	DRAWING NUMBER C2579L2 / REV / SCALE

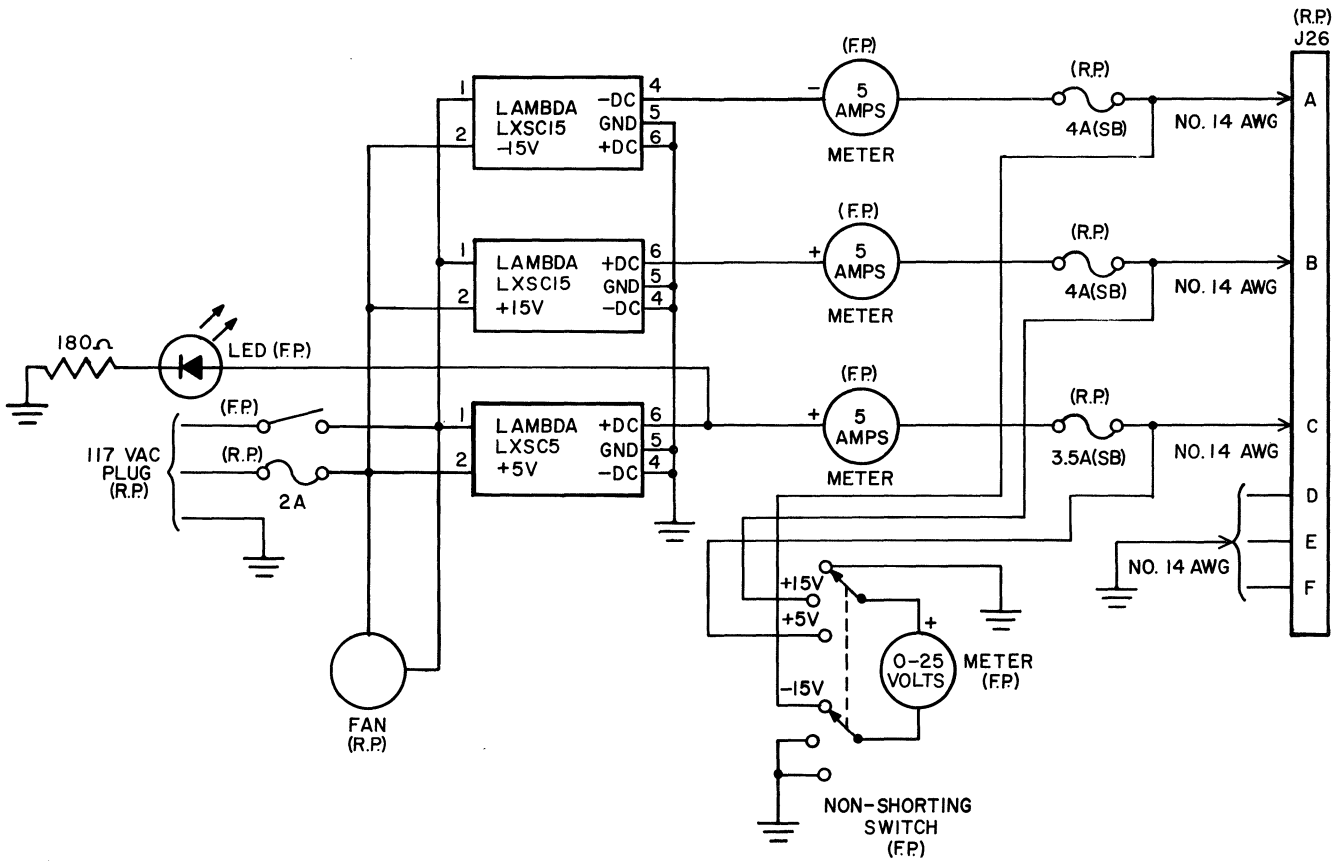


FIGURE 6

REV.	DATE	DRAWN BY	APPRV'D BY	
A	7-17-73	John Barnett	C Pace	RELOCATED "0-25 VOLT" METER LEADS; 4A(SB) WAS 2A; 3.5(SB) WAS 3A.

512 CHANNEL MULTIPLEXER POWER SUPPLY

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, Va., 22901
DRAWN BY John Barnett
DESIGNED BY C Pace
APPROVED BY C Pace

DATE	SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
6/12/73		B2579S2	A	

DWG. NO. B2579S2

Preliminary Data, January 1972

MILITARY (A SUFFIX) −55 to +125°C
INDUSTRIAL (B SUFFIX) −20 to +85°C

DG200

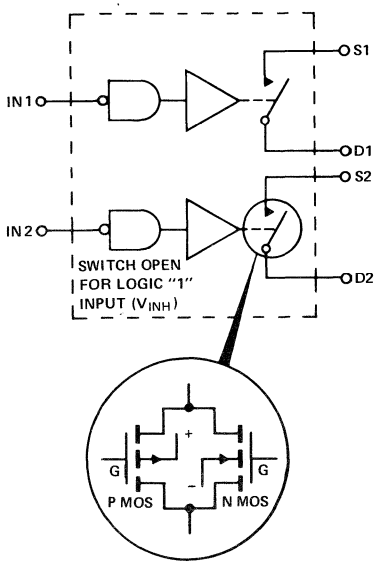
Type	Package
DG200AA	TO-100
DG200BA	TO-100

DUAL SPST CMOS ANALOG TRANSMISSION GATE

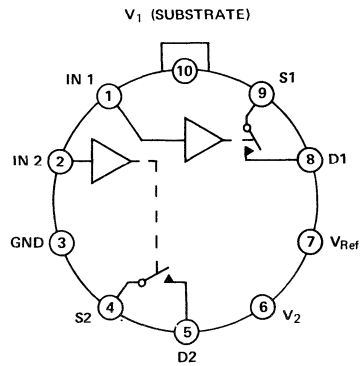
MONOLITHIC CMOS SWITCH WITH DRIVER

- ±15 V Analog Signal Range
- ±15 V Supplies
- r_{DS} < 100 Ohms Over Full Temperature and Signal Range
- Break-Before-Make Switching Action
- TTL, DTL, and CMOS Direct Control Interface Over Military Temperature Range Without Need For Interface Components

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



Siliconix incorporated

DG200

ABSOLUTE MAXIMUM RATINGS

V_{IN} and V_{Ref} to Ground ..... -0.3 V, V_1
V_S or V_D to V_1 ..... 0, -32 V
V_S or V_D to V_2 ..... 0, 32 V
V_1 to Ground ..... 16 V
V_2 to Ground ..... -16 V
Current, Any Terminal Except S or D ..... 30 mA
Current, S or D ..... 5 mA
Operating Temperature ..... -55 to 125°C
Storage Temperature ..... -65 to 150°C
Power Dissipation (Package)* ..... 450 mW

*All leads welded or soldered to PC board. Derate 6 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and to assure conformance with specifications.

		Characteristic	Typ 25°C	Max Limits DG200AA -55°C	DG200AA 25°C	DG200AA 125°C	DG200BA -20°C	DG200BA 25°C	DG200BA 85°C	Unit	Test Conditions (Unless Otherwise Noted) V_1 = 15 V, V_2 = -15 V, Gnd = 0, V_{Ref} = Open***	
1	INPUT	I_{INH}			-0.01	-10		-0.01	-10	µA	V_{IN} = 2 V	
2					0.01	10		0.01	10		V_{IN} = 15 V	
3		$I_{IN(Peak)}$	-120									
4		I_{INL}			-0.01	-10		-0.01	-10		V_{IN} = 0.8 V	
5	OUTPUT	$r_{DS(ON)}$	65	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = 1 mA
6			65	70	70	100	80	80	100		V_D = -10 V	
7		$I_{S(OFF)}$	0.1		2	1000		5	500	nA	V_S = 15 V, V_D = -15 V	V_{IN} = 2 V
8			-0.1		-2	-1000		-5	-500		V_S = -15 V, V_D = 15 V	
9		$I_{D(OFF)}$	0.1		2	1000		5	500		V_D = 15 V, V_S = -15 V	
10			-0.1		-2	-1000		-5	-500		V_D = -15 V, V_S = 15 V	
11		$I_{D(ON)}$*	0.1		2	1000		5	500		V_D = V_S = 15 V	V_{IN} = 0.8 V
12			-0.1		-2	-1000		-5	-500		V_D = V_S = -15 V	
13	POWER	I_1	2.5		3			3		mA	Both Channels "ON", V_{IN} = 0	
14		I_2	-2.5		-3			-3				
15		I_1 Standby	1.7		2			2			Both Channels "OFF", V_{IN} = 5 V	
16		I_2 Standby	-1.7		-2			-2				
17	DYNAMIC	t_{on}	400		1000			1000		ns	See Switching Circuit	
18		t_{off}	230		500			500				
19		$C_{S(OFF)}$	8.5							pF	V_S = 0, V_{IN} = 5 V	f = 140 kHz to 1 MHz
20		$C_{D(OFF)}$	8.5								V_D = 0, V_{IN} = 5 V	
21		$C_{ds(off)}$	1								V_D = V_S = 0, V_{IN} = 5 V	
22		$C_{D(ON)}$	22								V_D = V_S = 0, V_{IN} = 0 V	
23		"OFF" Isolation**	65							dB	V_{IN} = 5 V, R_L = 1 kΩ, C_L = 10 pF, V_S = 3 VRMS, f = 100 kHz	

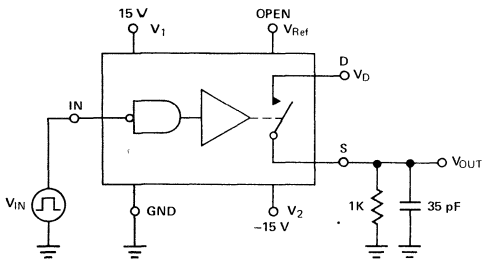
*$I_{D(ON)}$ is leakage from driver into "ON" switch.

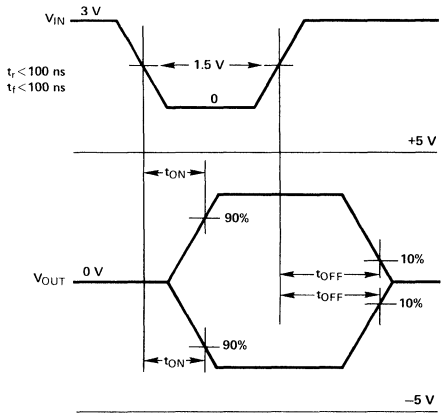
**"OFF" Isolation ≙ 20 log $\frac{|V_A|}{|V_B|}$, A = output terminal of "OFF" switch, B = any other switch terminal.

*** Functional operation is possible for 10 V ≤ V_{DD} − V_{SS} ≤ 15 V, but the input logic threshold will shift. To maintain TTL threshold voltage compatibility a reference voltage of 1.5 V may be applied to the V_{Ref} terminal. The V_{Ref} terminal has R_{IN} ≅ 13 KΩ.

ICAE

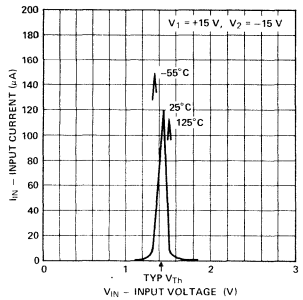
SWITCHING CIRCUIT AND DEFINITIONS



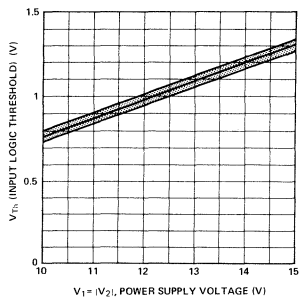


TYPICAL CHARACTERISTICS

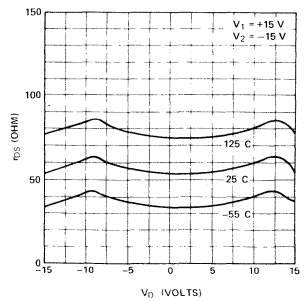
I_{IN} vs V_{IN}



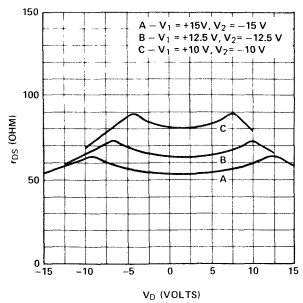
V_{Th} (Input Logic Threshold) vs Power Supply Voltage



r_{DS} vs V_D and Temp

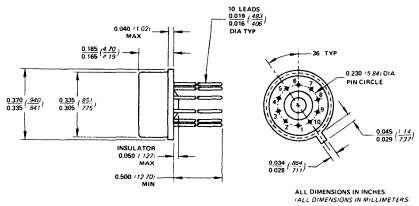


r_{DS} vs V_D and Power Supply Voltage



DG200

MECHANICAL DATA



TO-100
DG200AA, BA

Preliminary Data, January 1972

MILITARY (A SUFFIX) −55 to +125°C
INDUSTRIAL (B SUFFIX) −20 to +85°C

DG506

Type	Package
DG506AR	MO-015
DG506BR	MO-015

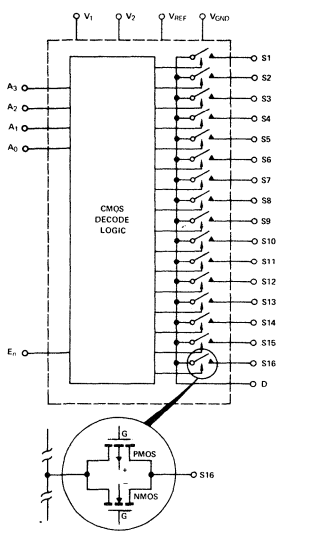
16-CHANNEL ANALOG MULTIPLEXER COMPLEMENTARY MOS (CMOS)

MONOLITHIC CMOS MULTIPLEXER WITH 4-LINE BINARY DECODE

- ±15 V Analog Signal Range
- r_{ON} < 500 Ohms Over Full Temperature and Signal Range
- Break-Before-Make Switching Action
- TTL, DTL, and CMOS Direct Control Interface Over Military Temperature Range Without Need For Interface Components
- 4-Line Binary Input Selects 1 of 16 Channels
- 5th Line Binary Input (En) Allows Output Line To Be Common To Several Other Units
- 36 mW Typical Standby Power

The DG506 is a single-pole 16-position (plus OFF) electronic switch array which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF condition each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 4-bit binary word input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 16 switch positions, provided a positive logic "1" is present at the Enable input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between -0.3 and 0.8 V as logic "0" voltages, and voltages between 2 and 15 V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS, and certain special P-MOS circuits. Switch action is break-before-make.

FUNCTIONAL DIAGRAM



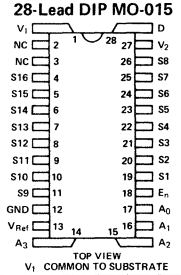
DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	E_n	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

LOGIC "1" = $V_{AH} \geq 2$ V
LOGIC "0" = $V_{AL} \leq 0.8$ V

PIN CONFIGURATION

28-Lead DIP MO-015



TOP VIEW
V_1 COMMON TO SUBSTRATE

Siliconix incorporated

DG506

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En, or V_{Ref}) to Ground ..... -0.3 V, V_1
V_S or V_D to V_1 ..... 0, -32 V
V_S or V_D to V_2 ..... 0, 32 V
V_1 to Ground ..... 16 V
V_2 to Ground ..... -16 V
Current (Any Terminal, Except Analog Source/Drain) . 30 mA
Current (Analog Drain) ..... 10 mA
Current (Analog Source) ..... 1 mA
Operating Temperature ..... -55 to 125°C
Storage Temperature ..... -65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Max Limits A Suffix -55°C	A Suffix 25°C	A Suffix 125°C	B Suffix -20°C	B Suffix 25°C	B Suffix 55°C	Unit	Test Conditions (V_1 = 15 V, V_2 = -15 V, Ground = 0, V_{Ref} = Open***)	
SWITCH	1	$r_{DS(ON)}$	S to D	16	250	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = -100 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2 V
	2			16	250	400	400	500	450	450	550		V_D = -10 V, I_S = -100 μA	
	3	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVE}}\right)$, -10 V ≤ V_S ≤ 10 V	
	4	$I_{S(OFF)}$	S	16	-0.05		±1	±50		±5	±50	nA	V_S = 10 V, V_D = -10 V	V_{En} = 0
	5			16	-0.05		±1	±50		±5	±50		V_S = -10 V, V_D = 10 V	
	6	$I_{D(OFF)}$	D	1	-0.3		±10	±500		±20	±500		V_D = 10 V, V_S = -10 V	
	7			1	-0.3		±10	±500		±20	±500		V_D = -10 V, V_S = 10 V	
	8	$I_{D(ON)}$*	D	16	-0.3		±10	±500		±20	±500		$V_{S(All)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2 V
	9			16	-0.3		±10	±500		±20	±500		$V_{S(All)}$ = V_D = -10 V	
INPUT	10	I_{AH}	A_0, A_1, A_2, A_3, En	5			-10	-30		-10	-30	μA	V_A = 2.4 V	
	11			5			10	30		10	30		V_A = 15 V	
	12	$I_{A(Peak)}$		5	-60								See Curve "I_A vs V_A"	
	13	I_{AL}	A_0, A_1, A_2, A_3	4			-10	-30		-10	-30		V_{En} = 2 V	All V_A = 0
	14		En	1			-10	-30		-10	-30		V_{En} = 0	
DYNAMIC	15	$t_{transition}$	D		0.6		1					μs	See Fig. 1	
	16	t_{open}	D		0.2								See Fig. 2	
	17	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	18	$t_{off(En)}$	D		0.3		1							
	19	"OFF" Isolation**	D		60							dB	V_{En} = 0, R_L = 200 Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	20	$C_{S(OFF)}$	S	16	5							pF	V_S = 0	V_{En} = 0, f = 140 kHz to 1 MHz
	21	$C_{D(OFF)}$	D	1	40								V_D = 0	
	22	$C_{ds(off)}$	D to S	16	1								V_S = 0, V_D = 0	
SUPPLY	23	I_1	V_1	1	5.2	14	10	7		10		mA	V_{En} = 5 V	All V_A = 0
	24	I_2	V_2	1	-5.2	-14	-10	-7		-10				
	25	I_1 Standby	V_1	1	1.2	3.5	2.5	2		2.5			V_{En} = 0	
	26	I_2 Standby	V_2	1	-1.2	-3.5	-2.5	-2		-2.5				

* $I_{D(ON)}$ is leakage from driver into "ON" switch.

**"OFF" isolation $\triangleq$ 20 log $\left|\frac{V_D}{V_S}\right|$, V_S = input to "OFF" switch, V_D = output due to V_S.

***Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For $V_1 = -V_2 = 10$ V, 1.5 V may be applied to the V_{Ref} terminal. The V_{Ref} terminal has $R_{IN} \cong 13$ KΩ.

ICAB-A

SWITCHING INFORMATION

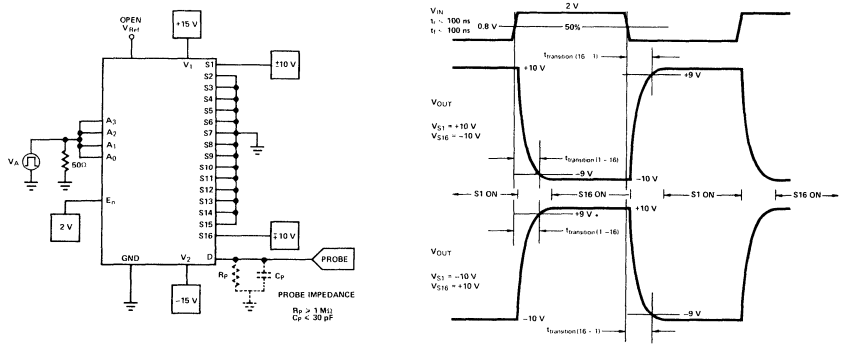
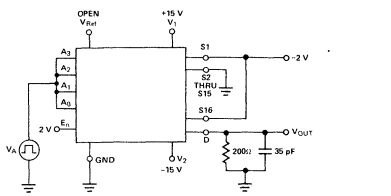


Figure 1



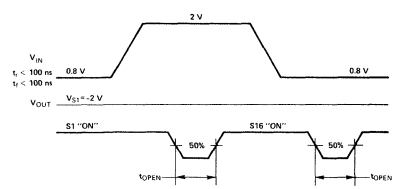
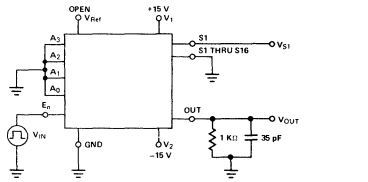


Figure 2



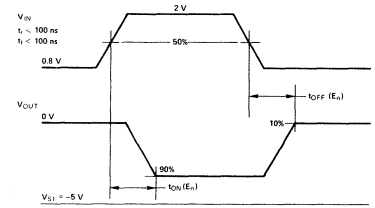
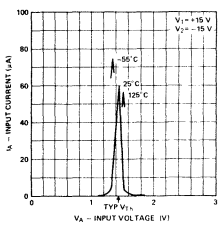


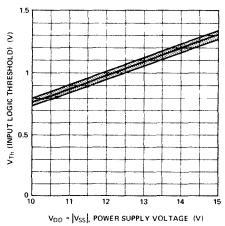
Figure 3

TYPICAL CHARACTERISTICS

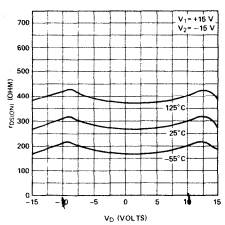
I_A vs V_A (Terminals A_0, A_1, A_2, E_n)



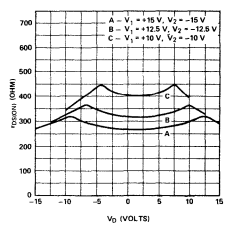
V_{Th} (Input Logic Threshold) (V)



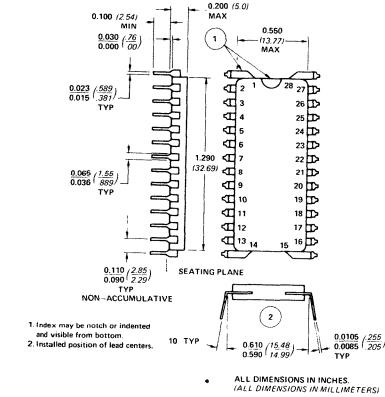
$r_{DS(on)}$ vs V_D and Temp



$r_{DS(on)}$ vs V_D and Power Supply Voltage

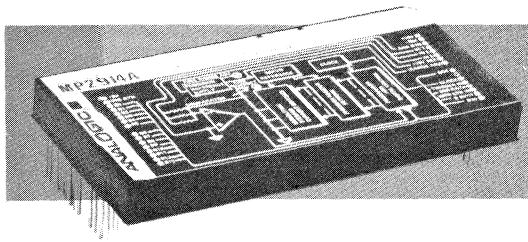


MECHANICAL DATA



MO-015
28-Pin Dual-In-Line Package
DG506AR, BR

Siliconix incorporated 2201 Laurelwood Road, Santa Clara, California (408) 246-8000



MP2913A and MP2914A very high speed 13-bit & 14-bit A/D CONVERTER

GENERAL DESCRIPTION

Analogic's MP2913A and MP2914A are the fastest 13 and 14 bit analog-to-digital converters available at lowest cost in the smallest package. Housed in a 2" x 4" x 0.4" MODUPAC ™, these extremely fast and highly precise ADC's (10 microseconds for 14 bits) provide substantial space and cost economies in high speed-high resolution digitizing systems. The high accuracy and differential linearity (.006%) plus the high stability (gain tempco is 7 PPM/°C and differential linearity tempco is 3 PPM/°C) of these units assure true 13 and 14 bit resolution.

PERFORMANCE ACHIEVEMENTS

The high digitizing rate of 100,000 conversions per second with an accuracy and differential linearity of .006% of the MP2913A and MP2914A is achieved by incorporating three separate ground planes and a unique strobing comparator. While accelerating the conversion process, these design innovations virtually eliminate major electrical interferences thus minimizing noise. Implementing these and similar techniques with the optimum components available assures that the MP2913A and MP2914A have the high accuracy and linearity consistent with high speed 14 bit conversion.

Combining the MP2914A with Analogic's AN4716 Multiplexer and MP270 Sample and Hold modules will provide analog-to-digital conversions of more than 75,000 per second.

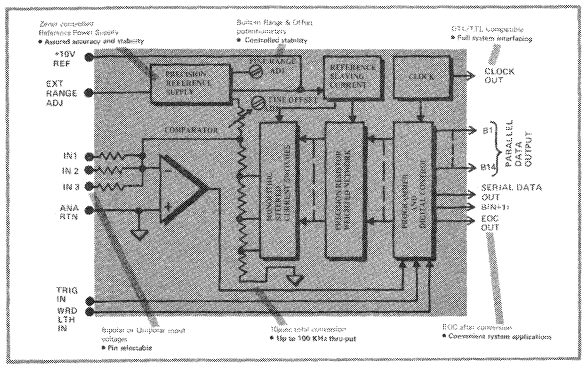


Figure 1. MP2914A Functional Block Diagram

FEATURES

- Extremely Fast Conversion to 14 bits....
  ---10μsec
- Highly Accurate and Linear....
  ---within .006%
- Highly Stable....
  ---3 PPM/°C Differential Linearity Tempco
- Small Shielded Module....
  ---2" x 4" x 0.4"
- Low Cost

APPLICATIONS

- Fast thru-put Systems
- High Speed Computer Interfacing
- Wide Band Data Digitizing
- Multi-channel Process Control

ANALOGIC®
. . . The Digitizers

Audubon Road ■ Wakefield, Massachusetts 01880

Tel (617) 246-0300 TWX (710) 348-0425

MP2913A & MP2914A SPECIFICATIONS

ANALOG INPUT	
Input Voltage (Full Scale Range)	-10V to +10V, 0V to +10V, -5V to +5V, 0V to +5V (pin selectable. See Fig. 5)
Input Impedance	Depends on FSR. See Fig. 5
ACCURACY (@ 23°C)	
Absolute Accuracy	Same as relative accuracy after calibration
Relative Accuracy	.006% FSR
Differential Linearity	.006% FSR
Quantizing Error	±1/2 LSB
3σ-Noise (Includes Reference Noise)	.005% FSR P-P referred to input
Monotonicity	Guaranteed
STABILITY	
Tempco of Differential Linearity	<±3 PPM/°C FSR
Tempco of Gain	<±7 PPM/°C Reading
Tempco of Offset	<±12 PPM/°C FSR
Clock Stability	±0.1%°C
Power Supply Sensitivity	±0.0012% change in supply voltage
Recommended Recalibration Interval	6 months
Repeatability	Defined by Noise and Accuracy
CONVERSION TIME	
Total Conversion	10μsec
DIGITAL SIGNALS	
Compatibility	Standard TTL Compatible
Parallel Output	Binary, B1, B1 to B13 or B14. 2 unit loads/line
Serial Output	Negative pulses simultaneous with clock pulse for "0". Max load 30pF
Trigger Input	Neg. going pulse from binary "1", 50 nsec min. duration at binary "0", must have been at binary "1" for 1 μsec min.
Trigger Input Transition	<200 nsec (90% to 10%)
End of Conversion, EOC	"1" to "0" level transition, nominally 100 nsec after LSB data pulse. 8 unit loads
EOC Transition	<20 nsec (10% to 90%)
Clock Output	Standard TTL compatible
Clock Output External Capacitance	30 pF maximum allowable
Selectable Word Length	2 to 13 bits (MP2913A), 2 to 14 bits (MP2914A)
POWER SUPPLY	
+15V ±3%	60mA
-15V ±3%	60mA
+5V ±5%	300mA
ENVIRONMENTAL, PHYSICAL, & RELIABILITY	
Maximum Input Without Damage	±200% Full Scale Range
Missing Codes	None
Warm-up Time to Stated Accuracy	5 minutes
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	5% to 95% (non-condensing)
Electrical Shielding	RFI 6 sides; EMI 5 sides
Mechanical Protection	6 sides
Packaging MP29XXA	2" x 4" x 0.39" Modupac
Packaging AN29XXA	MP29XXA on plug-in P.C. card

Binary Output Coding

The particular output binary code desired can be selected in accordance with the accompanying table. *

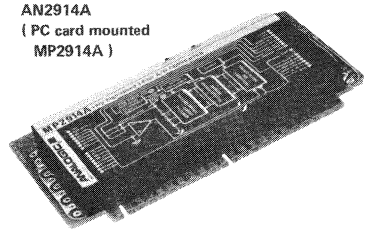
14 BIT RESOLUTION	13 BIT RESOLUTION
Unipolar binary :	**Unipolar binary :**
+9.9994V = 11 111 111 111 111 0.0000V = 00 000 000 000 000 Pin Label = B1, B2.....B14	+9.9988V = 1 111 111 111 111 0.0000V = 0 000 000 000 000 Pin Label = B1, B2.....B13
Offset binary:	**Offset binary:**
+9.9988V = 11 111 111 111 111 0.0000V = 10 000 000 000 000 -10.0000V = 00 000 000 000 000 Pin Label = B1, B2.....B14	+9.9976V = 1 111 111 111 111 0.0000V = 1 000 000 000 000 -10.0000V = 0 000 000 000 000 Pin Label = B1, B2.....B13
Two's compliment :**	**Two's complement** :**
+9.9988V = 01 111 111 111 111 0.0000V = 00 000 000 000 000 -10.0000V = 10 000 000 000 000 Pin Label = $\overline{B1}$, B2.....B14	+9.9976V = 0 111 111 111 111 0.0000V = 0 000 000 000 000 -10.0000V = 1 000 000 000 000 Pin Label = $\overline{B1}$, B2.....B13

*10 volt unit only. For 5 volt units divide input voltage by 2.

** To change to offset binary, use B1 instead of $\overline{B1}$.

Figure 2. Input/Output Coding Table

AN2914A
(PC card mounted MP2914A)



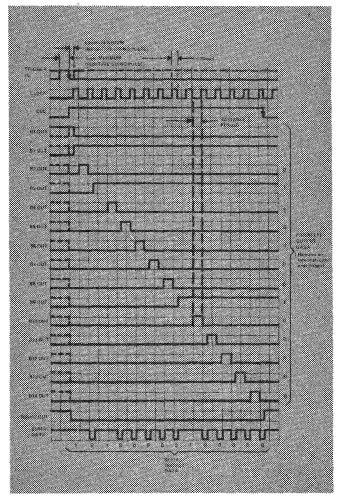


Figure 3. Timing Diagram for MP2914A

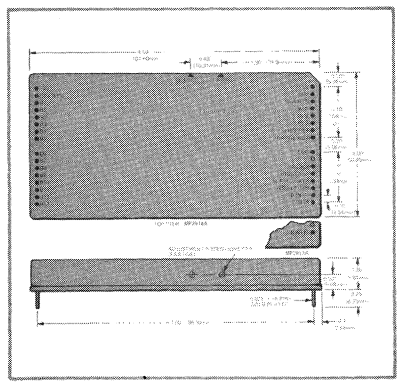


Figure 4. MP2913A/MP2914A Outline Drawing

Input Voltage Range Selection

Three input pins are provided to allow user selection of one of four standard input voltage ranges. " IN 1 ", " IN 2 " and " IN 3 " must be connected in accordance with the following tables to select the full scale range desired.

MODUPAC MP2913A & MP2914A

Range	Input Impedance	IN 1	IN 2	IN 3
−10V to +10V	5000Ω	to ANA RTN	to ANA INPUT	to +10V REF
0V to +10V	2500Ω	to ANA RTN	to ANA INPUT	to ANA INPUT
−5V to +5V	2500Ω	to ANA INPUT	to ANA RTN	to +10V REF
0V to +5V	1250Ω	to ANA INPUT	to ANA INPUT	to ANA INPUT

P.C CARD AN 2913A & AN 2914A

Range	Input Impedance	Terminals on Card		
−10V to +10V	5000Ω	E29 to E28	E30 to E35	E31 to E32
0V to +10V	2500Ω	E29 to E28	E30 to E35	E33 to E34
−5V to +5V	2500Ω	E36 to E35	E30 to E28	E31 to E32
0V to +5V	1250Ω	E29 to E28	E30 to E35	E34 to E333

Figure 5. Range Selection Tables Showing the Jumper Connections Needed for FSR Required

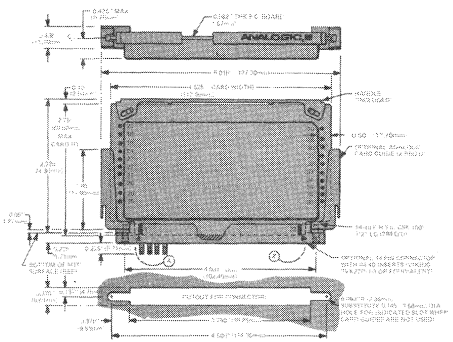
HOW TO ORDER

Simply specify ——— [ ]

Configuration FOR	ENTER
13 Bit Modupac	MP2913A
MP2913A on a PC card	AN2913A*
14 Bit Modupac	MP2914A
MP2914A on a PC card	AN2914A*

* For OEM quantities or as part of a system order, FSR connections (See Fig.5) are made at the factory. The part number should be changed as follows: For 0 to +10V, add -1; -10V to +10V, add -2; -5V to +5V, add -3; 0V to +5V, add -4. For example a AN2914A-2 is a 14 bit ADC with -10V to +10V FSR.

Outline Drawing



* For AN2914A only. For AN2913A pin V and terminal E24 are B(N+1), pin 17 and terminal E23 are at binary "0".

Terminal Designation	Pin Designation			
	TRIGGER IN	A	1	EOC
		B	2	
	WRD LTH IN	C	3	B13 OUT
		D	4	
E18 WRD LTH IN	B2 OUT	E	5	B1 OUT
E19 WRD LTH IN	B4 OUT	F	6	B3 OUT
E20 WRD LTH IN	B12 OUT	H	7	B6 OUT
E21 WRD LTH IN	B5 OUT	J	8	B8 OUT
E22 WRD LTH IN	B7 OUT	K	9	
E23 (BN+1)*	CLOCK	L	10	SERIAL DATA
E24 B14*	+5V	M	11	+5V
E25 B13	DIG RTN	N	12	DIG RTN
E26 B11	B11 OUT	P	13	B10 OUT
E27 B9	$\overline{B1}$	R	14	B9 OUT
E28 ANA RTN	SIG RTN	S	15	ANA RTN
E29 IN 1	INPUT	T	16	INPUT
E30 IN 2	*B14 OUT	U	17	B (N+1)*
E31 IN 3	ANA RTN	V	18	
E32 +10V REF	−15V	W	19	ANA RTN
E33 ANA INPUT	+15V	X	20	−15V
E34 IN 3	+10V REF OUT	Y	21	+15V
E35 ANA INPUT		Z	22	RANGE ADJ
E36 IN1				

Figure 6. AN29XXA Outline Drawing, Jumper Terminal and Connector Pin Diagram.

CALIBRATION

Zero Offset Calibration

To recalibrate the OFFSET: 1. Apply the input voltage shown in accompanying table and, 2. Adjust the OFFSET control so that the LSB of the output codes listed in the table alternate equally between "1" and "0". Offset should be readjusted whenever the selected full scale range is changed.

Full Scale Range	MP2913A or AN2913A Input voltage	MP2913A or AN2913A Output Code ($B_1, B_2, \ldots B_{13}$)	MP2914A or AN2914A Input voltage	MP2914A or AN2914A Output Code ($B_1, B_2 \ldots B_{14}$)
-10V to +10V	+0.0012	1 000 000 000 000/1	+0.00061	10 000 000 000 000/1
0V to +10V	+0.0006	0 000 000 000 000/1	+0.00031	00 000 000 000 000/1
-5V to +5V	+0.0006	1 000 000 000 000/1	+0.00031	10 000 000 000 000/1
0V to +5V	+0.0003	0 000 000 000 000/1	+0.00015	00 000 000 000 000/1

Figure 7. Offset Calibration Table

Range Calibration **Zero offset should be calibrated before recalibrating RANGE.**

Internal: A built-in 0.1% adjustment of the full scale voltage is provided. To recalibrate the RANGE: 1. apply the input voltage shown in the accompanying table and, 2. adjust the RANGE control so that the LSB of the output code, 111...110/1 ($B_1, \ldots B_{(N)}$), alternates equally between "1" and "0". RANGE should be readjusted whenever the selected full scale range is changed.

External: A wider range adjustment may be implemented by connecting a 20KΩ potentiometer between "+10V REF" and "ANA RTN;" and connecting a resistor, R, between the wiper area of the 20KΩ potentiometer and "RANGE ADJ". The adjustment range will be +.5% to −.3% for R=470KΩ and +5% to −2.8% for R=47KΩ.

Full Scale Range	MP2913A or AN2913A Input Voltage	MP2914A or AN2914A Input Voltage
−10V to +10V	+9.9963	+9.9982
0 to +10 V	+9.9982	+9.9991
−5V to +5V	+4.9982	+4.9991
0 to +5V	+4.9991	+4.9995

Figure 8. Range Calibration Table

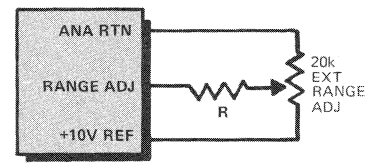
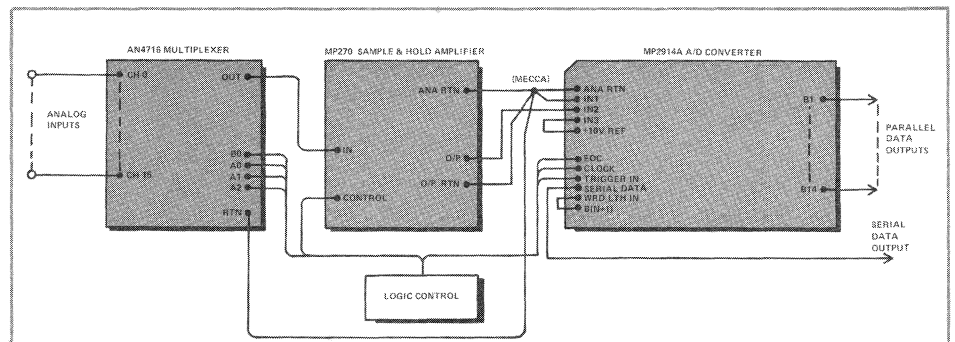


Figure 9. External Connection for Range Adjustment

Output Word Length Selection

The number of bits in the output word is pin selectable. To operate the ADC at its full capacity B (N+1) must be connected to WRD LTH IN. This connection is factory installed on the PC card for all AN versions ordered and must be removed when operating at less than full capacity. To operate the converter at less than its full digital output capacity WRD LTH IN must be connected only to the terminal identified as one bit more than the desired number of bits out.

EXAMPLE: When the ADC is operated as an 8-bit converter, connect WRD LTH IN to B9 only.



MP2914A Analog-toDigital Converter is shown connected in a high speed-high resolution multiplexed data conversion subsystem. The subsystem provides 14 bit data conversion at thru-put rates up to 75000 conversions per second.

Figure 10. 16 Channel High Speed-High Resolution Digitizing System

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