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RFI SURVEILLANCE COMPUTER INTERFACE

Joseph Greenberg

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RFI SURVEILLANCE COMPUTER INTERFACE

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INTRODUCTION

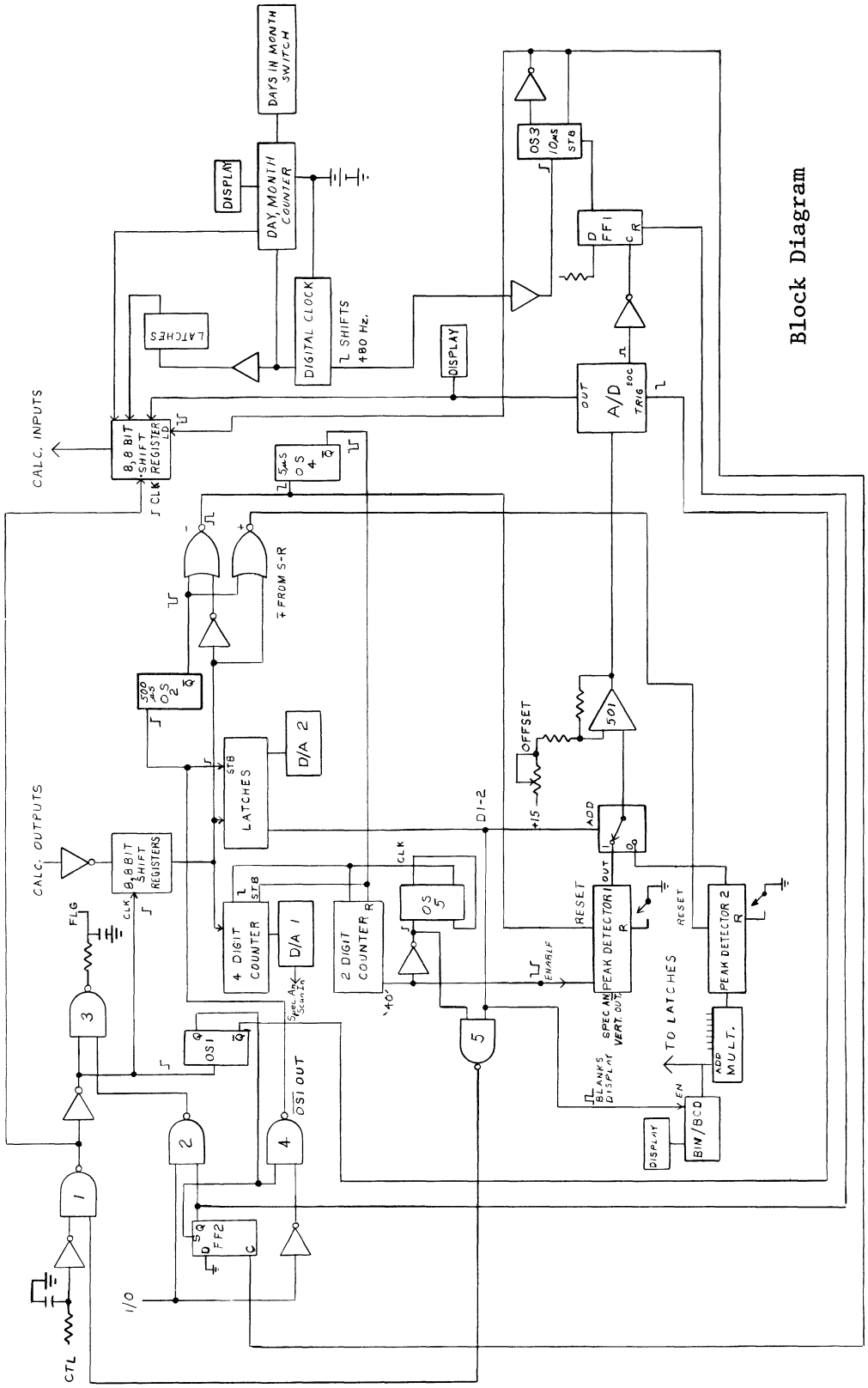
A Hewlett Packard Model 9810A calculator is used to monitor up to sixteen receivers and a spectrum analyzer. The calculator is equipped with a plotter and a tape memory unit.

The output portion of the interfacing logic contains two D/A converters and ten additional digital latches. One D/A converter provides an external scanning voltage to the spectrum analyzer. A voltage range of 0 to 8.000 volts corresponds to the frequencies displayed on the spectrum analyzer CRT. When a voltage is output, the logic automatically scans through an additional 0.040 volt. Since the spectrum analyzer output is fed into a peak detector, the automatic scanning effectively broadens the spectrum analyzer's bandwidth to $1/200^{th}$ of the screen width.

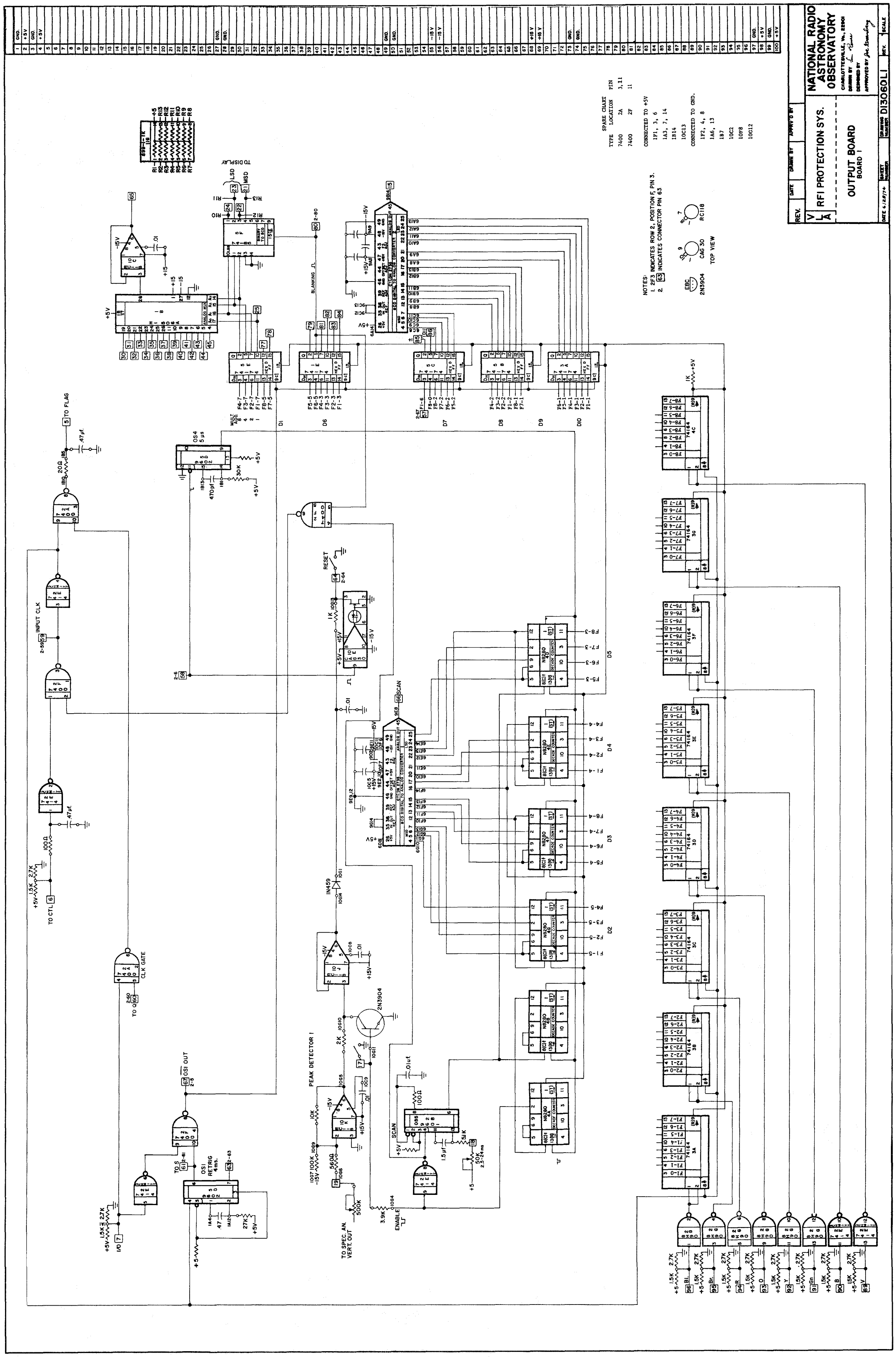
An address is output to determine which source will be multiplexed to the A/D converter. Up to sixteen receivers can be connected to the sixteen-to-one multiplexer. The output of this is fed into a separate peak detector. The outputs of the two peak detectors are multiplexed to the A/D converter. Since there are two peak detectors, one of the receivers and the spectrum analyzer can be monitored simultaneously.

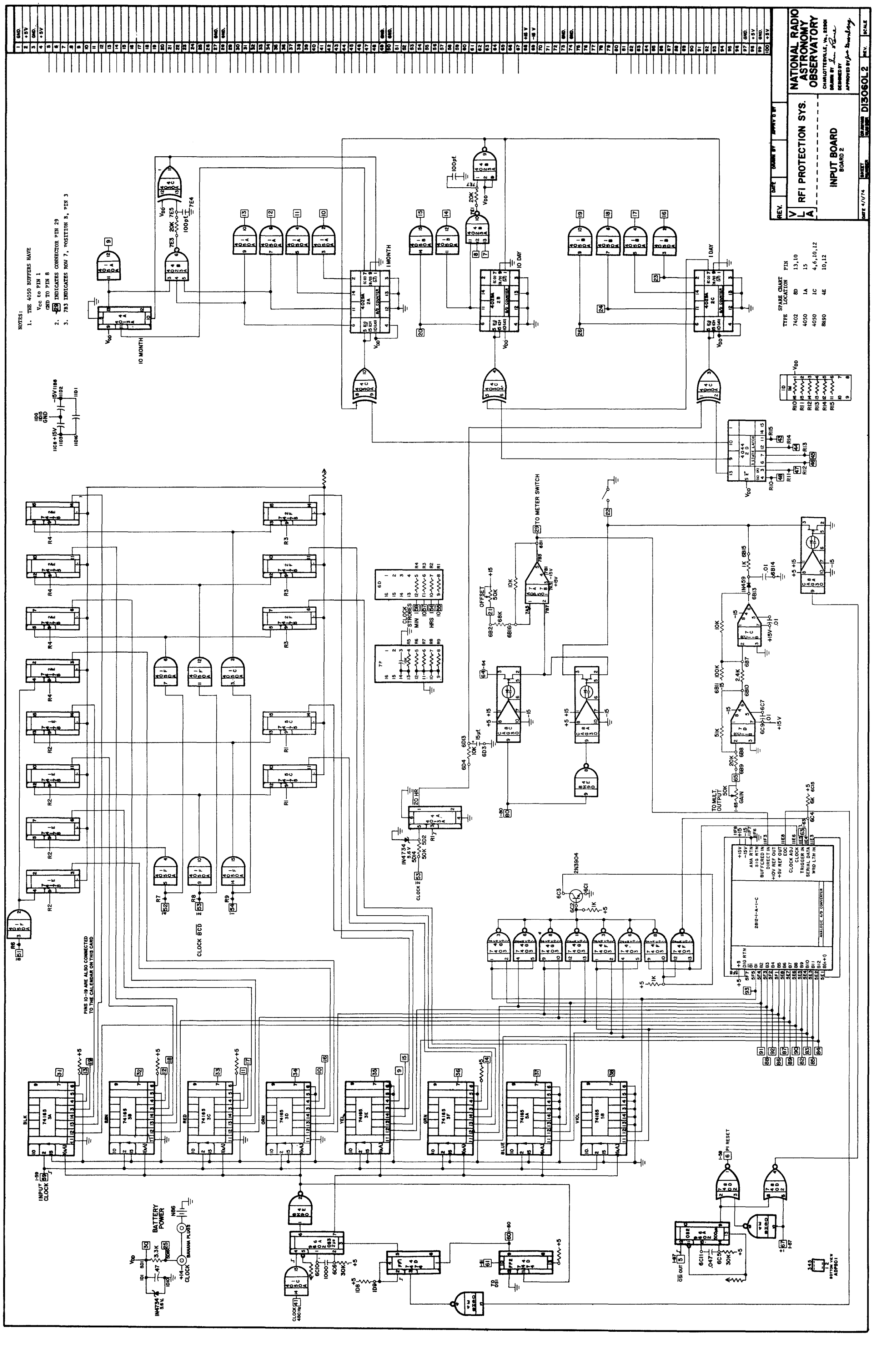
A clock-calendar is also interfaced with the calculator. It is constructed from CMOS logic for lowest power consumption and has a NiCad battery back-up in case of power failure.

An input operation yields the month, day, hour, minute, and the output of the A/D converter.

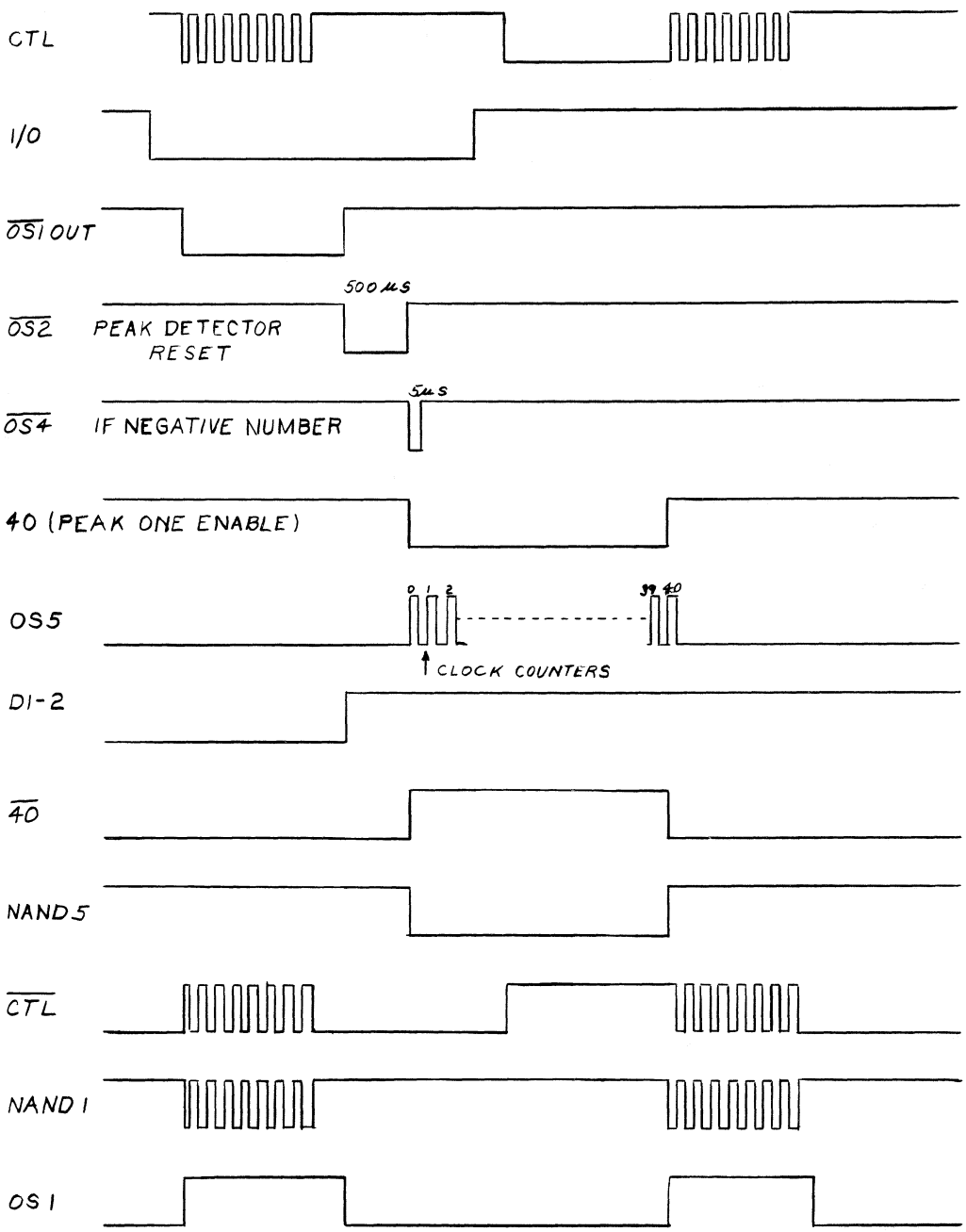


Block Diagram

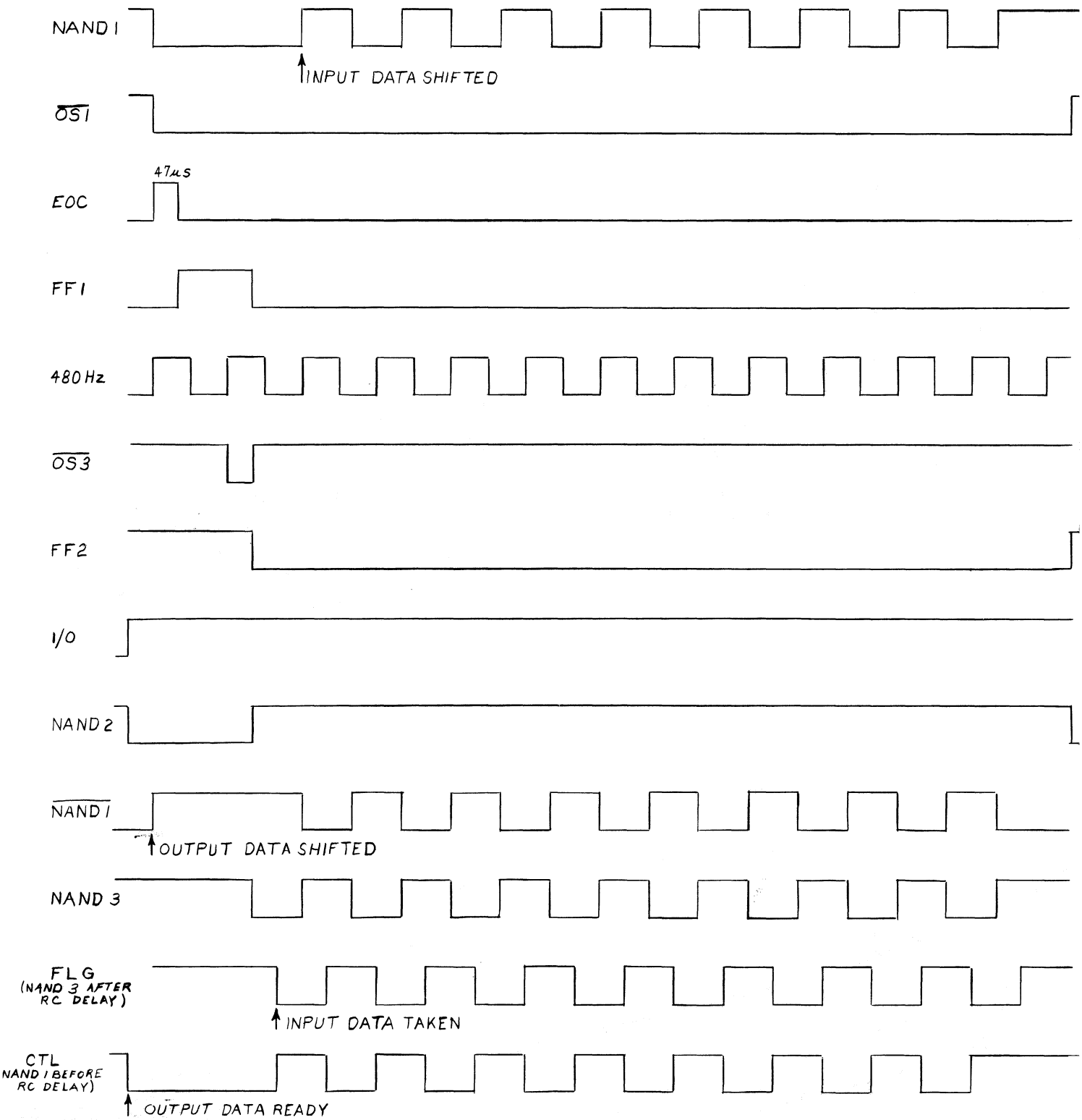

NATIONAL RADIO ASTRONOMY OBSERVATORY
RFI PROTECTION SYS.
OUTPUT BOARD
BOARD I
D13060L1
PEAK DETECTOR I
INPUT CLK
CLK GATE
TO FLAG
TO DISPLAY
BLANKING
RESET
SCAN
ENABLE
TOP VIEW


NOTES:
1. THE 4050 BUFFERS HAVE Vcc to PIN 1 GND TO PIN 8
2. [29] INDICATES CONNECTOR PIN 29
3. 7E3 INDICATES ROW 7, POSITION E, PIN 3
NATIONAL RADIO ASTRONOMY OBSERVATORY
RFI PROTECTION SYS.
INPUT BOARD
BOARD 2
D13060L2

TIMING DIAGRAM I



TIMING DIAGRAM 2



LOGIC DESCRIPTION

Refer to the block diagram, the individual board schematics, and the timing diagrams as an aid to understanding.

The calculator is interfaced with the logic via an HP 11202A I/O TTL Interface. For a full description of the interface refer to the 11202A I/O TTL Interface Preliminary User's Manual.

Board 1 contains the basic timing logic of the system. The "Control" line from the calculator is received by a resistor-capacitor filter and a Schmitt trigger. This was necessary to eliminate noise problems and also provide a delay. The resistor pull-up is necessary since the calculator outputs are open collector. A high to low transition of "Control" indicates the calculator is ready for input or output.

The "Flag" line gives control back to the calculator when returned in a low state. During output, it signals that the data has been accepted. During input, it tells the calculator the data is ready.

Control goes through 4 gates, another RC delay, and is then received as the "Flag" by a Schmitt trigger in the 11202A Interface. The "Flag" is acknowledged by "Control" returning high (see bottom of timing diagram 2).

During an output operation initiated by the command FMT 4 2 XTO, "Control" goes low eight times. During each cycle, one bit is output from each of the eight output lines; thus, a number from the X-register is output in a 64-bit block.

To store this 64-bit block, eight 8-bit shift registers are used, one for each output line. The data is shifted on the positive edge of $\overline{\text{NAND1}}$, which is a delayed consequence of "Control" going low.

The number $-1.23456789012 \times 10^{12}$ would be output in a 64-bit block as follows:

$-1.23456789012 \times 10^{12}$

'128'	'64'	'32'	'16'	'8'	'4'	'2'	'1'
0	0	0	0	1	1	0	0
0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	1	0	1	0	0
0	1	0	1	0	1	1	0
0	1	1	1	1	0	0	0
1	0	0	1	0	0	0	0
0	0	0	1	0	0	1	0
'8'	'4'	'2'	'1'	'8'	'4'	'2'	'1'
V	B	G	Y	O	R	Br	Bl

Each row represents one cycle. Each column represents one output wire as identified at the bottom by its color. Note it is the resistor color code from right to left. The first row output is the exponent in binary. Negative exponents are represented by two's compliment. The second row represents the sign. A "+" sign is all zeros. The last six rows represent, in order, the twelve digits of the number in BCD, two digits per row.

The data formats in the output and input blocks are as shown below.

INPUT FORMAT

Chip Pin	V	B	G	Y	O	R	Br	Blk	
6	0	0	0	0	0	1	1	1	
5	0	0	0	0	0	0	0	0	
4	0	0	1	Mo. 10	-------- Mo. 1 ----------				
3	0	0	--- Day 10 ---		-------- Day 1 ----------				
14	0	0	--- Hr. 10 ---		-------- Hr. 1 ----------				
13	0	------ Min. 10 ----			-------- Min. 1 ----------				
12	--------- A/D 1 ----------				-------- A/D 2 ----------				
11	--------- A/D 3 ----------				0	0	0	0	
	5B	5A	3F	3E	3D	3C	3B	3A	Chip Position

OUTPUT FORMAT

Chip Pin	V	B	G	Y	O	R	Br	Blk	
13	X	X	X	X	------- Mult. Address ------				
12	X	X	X	X	X	X	X	Latch	
11	-------- Latches ---------				------------ D1 ------------				
10	---------- D2 ----------				------------ D3 ------------				← D/A 1
6	---------- D4 ----------				--------- Latches ---------				
5	---------- D1 ----------				------------ D2 ------------				← D/A 2
4	---------- D3 ----------				------------ D4 ------------				
3	X	X	X	Latch	X	X	X	X	
	4C	3G	3F	3E	3D	3C	3B	3A	Chip Position

X indicates an unused output.

The '2' bit of the first digit in the input block is wired high. This is because erroneous results will occur if the first digit were zero, as in months earlier than October. The two bit may be later subtracted away. Also note the exponent input is seven. This allows easy separation of the date and A/D output. This is seen in the example below:

> Suppose the time is 23:59 on December 31, and the A/D output is 999. Pressing FMT 3 2 XFR will input the number 32312359.999 into the X register. The last 9 will not be displayed since it is only a ten digit display. Pressing UP INT - results in the A/D output being in the Y register in the form 0.999. Now pressing UP 2 EEX 7 - will result in 0.999 in the Z register and 12312359 in the Y register.

The output lines have been inverted to get them into positive logic. When outputing a number, it is the order of the digits not the exponent, that is important. The first digit cannot be zero, since then the other digits would be left-justified over one space. Example:

> The X register contains -3.796011234 x 15. To output this number, press FMT 4 2 XTO. The '_' sign strobes and starts D/A 1 scanning from 7.960 to 7.999 volts. The 7.960 volts is the largest permissible value to output to start D/A 1 scanning. Voltages greater than 8.000 cause errors in the spectrum analyzer. The '2' bit of the first digit, 3, sets the multiplexer to Peak Detector 1. The other bits of the first digit, '3', the four bits of the sixth digit, '1', and the '1' bit of the eleventh (undisplayed) digit are stored on latches for user applications. D/A 2 outputs 1.234 volts. Peak Detector 2 inputs from receiver fifteen due to the exponent.

Refer now to the Block Diagram and Timing Diagram 1.

OS1 triggers on the positive edge of $\overline{\text{NAND1}}$. It has a period about ten times the cycle rate. Since it is retriggerable, it stays high until about four milliseconds after the last cycle.

I/O is a calculator signal that goes low before an output operation and high before an input. OS1 is gated with $\overline{\text{I/O}}$ to give $\overline{\text{OS1}}$ out. The positive edge of $\overline{\text{OS1}}$ OUT occurs only after an output operation. It is used to strobe, from the shift registers onto latches, the input to D/A 2, the multiplexer addresses, and other bits. This positive edge also triggers OS2 for a 500 microsecond pulse. $\overline{\text{OS2}}$ is then demultiplexed through two NOR gates and an inverter to reset one or the other peak detector. The address is obtained from the $\pm$ bit stored in the shift registers. A positive number output resets Peak Detector 2, which is driven by the receiver multiplexer. A negative number resets Peak Detector 1, which is driven by the spectrum analyzer.

When Peak Detector 1 is reset, the negative edge of the positive resetting pulse triggers OS4 for a 5 microsecond pulse. $\overline{\text{OS4}}$ then strobes digits two through five from the shift registers onto the four decimal counters whose outputs go to D/A 1. The output of D/A 1 scans the spectrum analyzer. Note this value changes only after a negative number has been output. Also, $\overline{\text{OS4}}$ resets a separate, two-digit counter. This counter was previously set at 40. The $\overline{40}$ bit of the counter is fed into an AND, trigger input of OS5. The output of OS5 goes through an RC delay and into an inverted-AND input of OS5. Thus, the negative edge of OS5, after a slight delay, triggers OS5 again, as long as the $\overline{40}$ bit remains high. The negative edge of $\overline{\text{OS5}}$ clocks both the two-digit and four-digit counters. Thus, OS5 will give 41 pulses before the 40 bit goes high, disabling it. Note that the counters will not advance from the first pulse of OS5, since the strobe $\overline{\text{OS4}}$ is still low. The net result is that when a number is output to D/A 1, the output will start at that number and scan through an additional 0.040 volt.

The 40 bit is also used as an enable command for Peak Detector 1, causing it to be sensitive only while the D/A is scanning.

The duration of OS5 can be varied by the scan rate control on the front panel. Thus, the time for a 0.040 volt scan can be varied from one-tenth to one second.

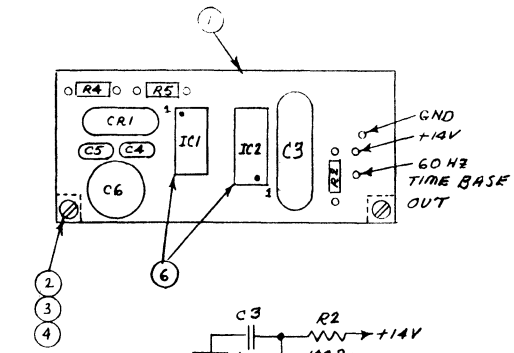
Using the command FMT 3 2 XFR, data is input into the calculator in the 64 bit block. The exponent is input first.

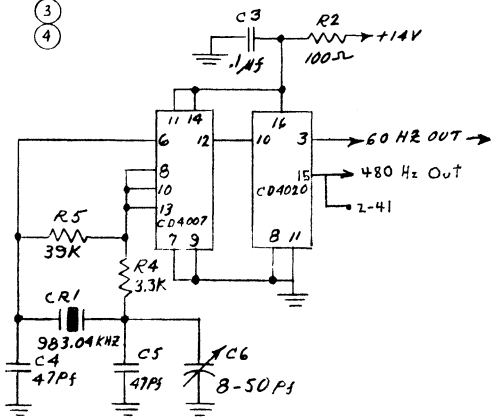
Refer to the Block Diagram and Timing Diagram 2. When an input operation is made, first I/O goes high, then Control goes low. This, in turn, drives $\overline{\text{NAND1}}$ high and triggers OS1. $\overline{\text{OS1}}$ going low triggers the A/D converter. Forty-seven microseconds later, the EOC signal going low indicates a conversion complete. $\overline{\text{EOC}}$ clocks Flip-Flop 1 high. The digital clock used advances its counters on the falling edge of its clock. Thus, the rising edge is a safe time to load the time into the shift registers. The 480 Hz signal from the clock is buffered and triggers OS3 on its positive edge. Flip Flop 1 is connected to the inhibit of OS3. With Flip Flop 1 now high, the first rising edge of the clock signal will trigger it and load the shift registers. The positive edge of $\overline{\text{OS3}}$ clocks FF2 low which resets FF1.

The calculator must wait for the shift registers to be loaded. To accomplish this FF2 is normally high, since it is set when OS1 is low. NAND2 gates FF2 with I/O. Thus, NAND2 is low in the beginning of an input operation. NAND3 gates $\overline{\text{NAND1}}$ with NAND2 and outputs through an RC to Flag. Thus, Flag cannot go low, telling the calculator to take the data, until NAND2 goes high. This occurs when FF2 is clocked low. Note the total delay must be less than the duration of OS1. New data is shifted when NAND1 goes high again.

The digital clock is an Aries AR-730 Fluorescent Clock with an AR-723 crystal time base. It uses a National MM5311 clock chip.

This chip's outputs are multiplexed seven-segment and $\overline{\text{BCD}}$. Since the chip is CMOS all the outputs except the strobes need a buffer to go to TTL. The clock's outputs are strobed on to latches which go to the shift registers.

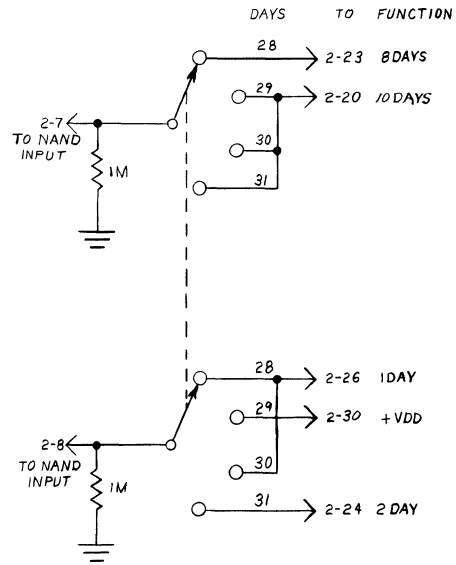




ITEM	DWG NO	DESCRIPTION	QTY
1	A1072	PC BOARD	
2		SCREW 4-40 X 1/4 LG	2
3		NUT 4-40	2
4		BRACKET	2
C3		CAPACITOR .1 Mf	1
C4		" 47Pf	1
C5		" 47Pf	1
C6		CAPACITOR 8-50 Pf	1
CR1		CRYSTAL 983.04KHZ	1
IC1		IC CD4007 AE	1
IC2		" CD4020 AE	1
R2		RESISTOR 100Ω	1
R4		" 3.3K	1
R5		" 39K	1
5		WIRE 2'	
6		MOLEX CONN 3½"	

NOTE: TO INSTALL IN AR730
1. REMOVE R2 + CONNECT 60HZ TIME BASE TO JUNCTION OF C4 + D9
2. CONNECT GND
3. CONNECT +14V TO JUNCTION OF R4 + D3

Crystal Time Base



DAYS IN MONTH

The digital clock's multiplexing rate is determined by an RC on the clock. It must cycle through all six digits in less than the time of one-half the 480 Hz cycle. Erroneous data could otherwise be strobed into the shift registers, since the data is loaded one-half cycle after the clock's counters have been advanced. Making the multiplexing rate too fast will render the displays illegible. The multiplexing frequency used updates all six digits at a rate of 1360 Hz.

Board 2 contains a COSMOS day and month calendar. The COSMOS and the clock run off the clock's power supply which has a battery back-up. The N86 NiCa battery floats directly across the output of the power supply. The current is limited by a series resistor in the power supply. The displays will be dim if the battery is not fully charged. There is a zener diode to limit the voltage if the battery is disconnected. The battery will trickle charge at about 30 mA.

The supply voltage to the COSMOS logic is lowered from 14 to 5.6 volts by a zener diode so that the clock strobe outputs will trigger the logic.

The clock's twenty hour bit goes to a COSMOS flip-flop in addition to the TTL one. The data to this flip-flop is clipped by a 5.6 volt zener to make it compatible with the COSMOS. This flip-flop advances the day counter. When the day counter reads one plus the number set on the rear-panel, DAYS IN MONTH switch, a NAND gate advances the month counter and strobes the day counter to 01. There is an RC delay present to assure all flip-flops are clocked.

Have the DAYS IN MONTH switch set to the number of days in the current month.

When the month counter reads 13, it is strobed to 01.

The time is set by the front panel controls, HOURS SLEW, MINUTES SLEW, and HOLD. The date is set by means of a one day, ten day, and one month switch. Depressing the date switches advances the respective number one digit. Using the ten day switch can result in a date between 34 and 00 if the reset date was skipped. Note the '40' and '80' day bits are not displayed.

The 7403 gates on the A/D converter provide the necessary feedback to get BCD output.

Peak Detector 1 can be seen on the schematic of Board 1. It inputs the zero to -0.75 volt vertical output of the spectrum analyzer. Zero volts corresponds to no signal. This goes to a summing junction where a 1.5 volt offset is added so that the diode used will always be in the active region. The GAIN control is adjusted so as to give a 1.5 to 11.5 volt signal. The 2K resistor on the output prevents the Enable transistor from overloading the op-amp. A '1' to the base turns on the transistor, disabling the peak-detector. Since the '40' signal controls Enable, the peak detector is only on when the counters are scanning. The peak detector can also be turned on by the ENABLE switch on the front panel. Make sure the switch is in the center off position when the system is in program control. The voltage follower op-amp provides a low output impedance to the diode-capacitor peak storer. The CAG-30 or the front panel RESET switch discharges the capacitor.

Peak Detector 2 on Board 2 takes a positive pulse from the receiver multiplexer. The full-scale value for this pulse can be varied from 0.94 to 3.29 volts by the GAIN control on the front panel. This pulse is amplified and has a 1.5 volt offset added to give a 1.5 to 11.5 volt output to a diode-capacitor peak detector as in Peak Detector 1. There are identical resetting facilities also.

The outputs of the two peak detectors are multiplexed by two CAG30's. The two bit of the first digit controls the address, with high indicating Peak Detector 1.

The output of this multiplexer goes to a 501 FET op-amp which subtracts what remains of the added offset after going through the diode. The front panel A/D INPUT OFFSET control varies the offset. To set this, first set the front panel, SCAN RATE control at the value to be used in the program. Enter the program 2 4 CHS FMT 4 2 XTO GTO 0 END. Short the VERTICAL OUTPUT input to ground. Execute the program. Starting with minimum offset, adjust the A/D INPUT OFFSET until the A/D OUPTUT just reads 000.

Note the offset is independent of the gain controls when the input voltage is zero. The A/D INPUT OFFSET should be adjusted before either GAIN control. The op-amp outputs to the A/D input. The response time of the peak detectors is determined by the RC time constant of the diode and the 0.01 mFd capacitor. Since the voltage-current curve of a diode is non-linear, the resistance of the diode is small for a diode voltage above 0.7 volt, but grows very large as the voltage goes to zero. Thus, the longer the duration of a pulse of set amplitude, the higher the voltage that will be stored in the peak detector. The OFFSET and GAIN controls should be set using a pulse of the expected duration.

To set Peak Detector 1's GAIN, first run the same program that was used in setting the A/D INPUT OFFSET. Have the spectrum analyzer set up so that a pulse which extends to full scale is centered in the screen. Switch the spectrum analyzer to external scan. Connect the rear panel VERTICAL OUTPUT and SCAN IN to the spectrum analyzer. Vary the spectrum analyzer's frequency so that the full scale pulse is included in the logic's 0.04 volt scan. Advance the SPECTRUM ANALYZER PEAK DETECTOR GAIN control until the A/D OUTPUT just reads 999. If the SCAN RATE control is changed, the OFFSET and GAINS should be readjusted.

The exponent of the X register number is the address for the 16 receiver multiplexer. It is output and latched in binary. A 74185 converts the address to BCD which goes to the front panel display as a number from zero to fifteen. If the '2' bit of the first digit is on, indicating Peak Detector 1's address, the address display will show '1' 'blank'. For receiver 1, the display will show '0' '1'.

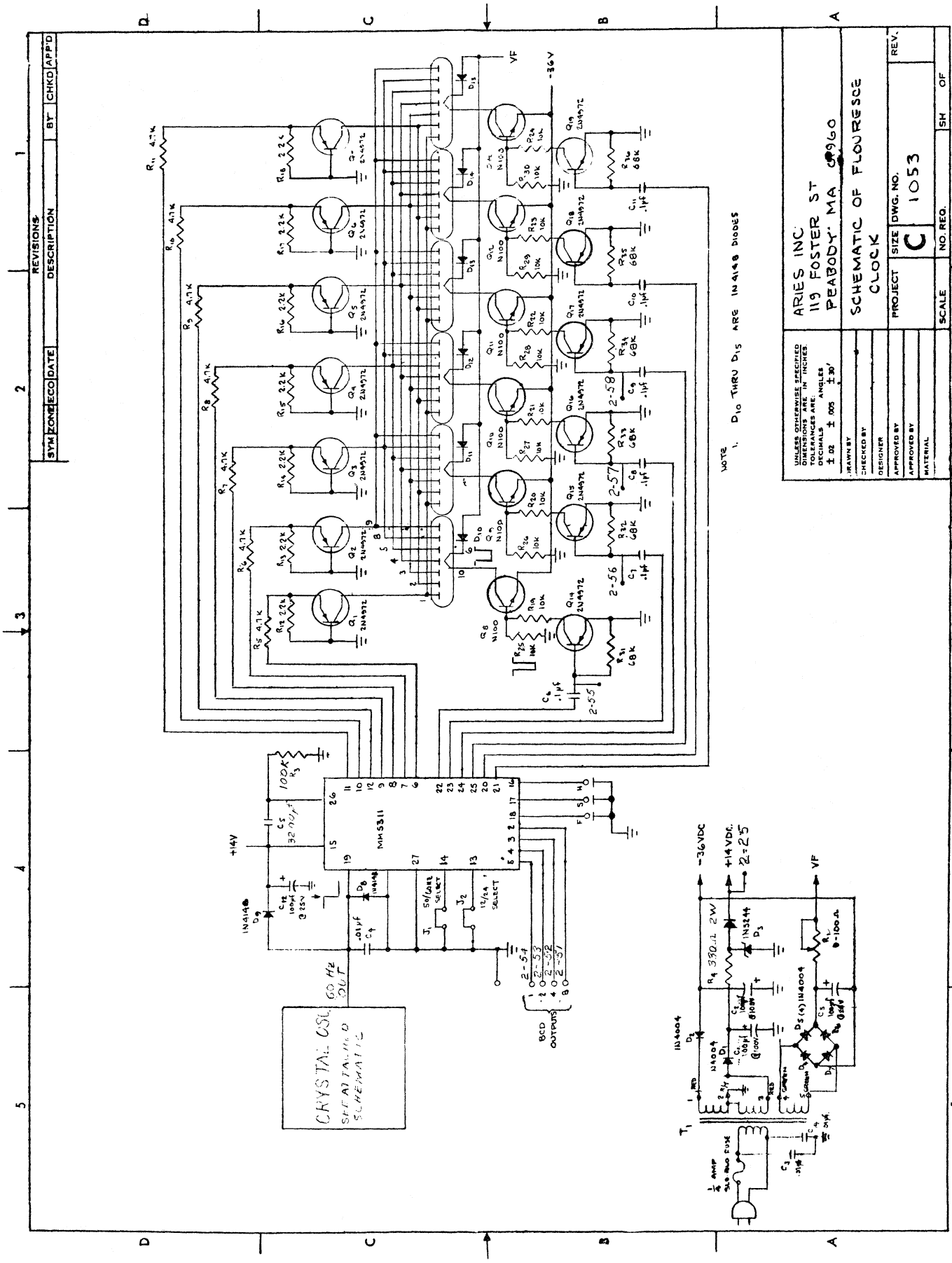
Additional front panel functions are a fault light and reset button for the 5 volt power supply, BNC's for the last four multiplexer inputs, and displays for the A/D OUTPUT, TIME, MONTH, and DAY.

A typical input-output sequence is as follows:

1. Output a positive number to reset Peak Detector 2, with the exponent telling what receiver it should look at.
2. Output a negative number to reset Peak Detector 1, strobe a number to D/A 1, and start it scanning.
   The exponent should be the same as above to keep Peak Detector 2 looking at the same receiver. Have digit one equal 1.
3. Perform an input operation. This brings in the month, day, time, and output of Peak Detector 2.
4. Output a positive number to reset Peak Detector 2, with the exponent telling what receiver it should look at. Have digit one equal 1.
5. After a wait, perform an input operation to again bring in the output of Peak Detector 2.

Any number of observations of the various receivers can be made in the manner of steps four and five. During this time, D/A 1 can still be scanning the spectrum analyzer. When it is desired to look at Peak Detector 1, output a positive number with the two bit of digit one high. Have the exponent set to the receiver Peak Detector 2 is currently looking at. Now, perform an input operation. If D/A 1 is not done scanning, the logic will wait until it is. To maximize efficiency, adjust the SCAN RATE control to make the program and scan time equal. The output of Peak Detector 1 will be input. The program can now cycle back to step 2, with the number strobed to D/A1, 40 units larger than the previous one.

Do not have an input and output operation back-to-back since an error may result due to OS1 not going low.



Schematic of Flourescent Clock

CONNECTOR LIST FOR

HP 9810A CALCULATOR TO "RFI SURVEILLANCE COMPUTER INTERFACE"

Type: HP 11202A I/O TTL Interface to Elco 56 Pins; Panel: E; Cable: P

Pin	To		Function	Pin	To		Function
A				a	2-33	I2	Red
B				b	1-95	01	Brown
C				c	1-96	00	Black
D				d	2-36	I5	Green
E	912			e	2-35	I4	Yellow
F	907			f	1-93	03	Orange
H	906			h	1-94	02	Red
J	908			j	1-7	I/O	
K	905			k	1-6	Control	
L				l			
M				m	1-91	05	Green
N	GND	ECH		n	1-92	04	Yellow
P		STP		p	1-5	Flag	
R	2-38	I7	Violet	r			
S	2-37	I6	Blue	s	1-89	07	Violet
T				t	1-90	06	Blue
U	GND	GND					
V	2-31	I0	Black				
W	GND	GND					
X	2-32	I1	Brown				
Y							
Z	2-34	I3	Orange				

Abbreviations: Board Connectors: 1, 2, 3, etc.
Pin Numbers: -3, -x, -B, -22, etc.

WIRE LIST (6 DIGIT DISPLAY HARNESS - 3 AUGAT PLUGS)
AB, CD, EFH

Function	To			Origin
20 h	Augat AB	Pin 14	(Red)	GND
10 h		1		2-9
40 h		13		GND
+5 volts		2		+5
80 h		12		GND
Colon		3		N.C.
D.P.		11		N.C.
Ground		4		GND
2 h		10		2-12
1 h		5		2-13
4 h		9		2-11
+5 volts		6		+5
8 h		8		2-10
Ground		7		GND
20 m	Augat CD	Pin 14	(Red)	2-14
10 m		1		2-15
40 m		13		GND
+5 volts		2		+5
80 m		12		GND
Ground		3		GND
2 m		11		2-18
1 m		4		2-19
4 m		10		2-17
+5 volts		5		+5
8 m		9		2-16
+5 volts		6		+5
2 s		8		GND
Ground		7		GND
4 s	Augat EFH	Pin 14	(Red)	GND
1 s		1		1-21
8 s		13		GND
Ground		2		GND
D.P.		12		N.C.
10 s		3		N.C.
0.2 s		11		1-24
0.1 s		4		1-25
0.4 s		10		1-23
40 s		5		N.C.
0.8 s		9		1-22
Ground		6		GND
80 s		8		N.C.
20 s		7		N.C.

WIRE LIST (A/D DISPLAY CABLE - 1 AUGAT PLUG)

Function	To	Origin
H-8	Augat Pin 14 (Red)	2-93
H-1	1	2-92
H-4	13	2-91
T-1	2	2-90
T-2	12	2-89
H-2	3	2-88
T-4	11	2-87
+5 volts	4	+5
T-8	10	2-86
GND	5	GND
U-2	9	2-85
U-1	6	2-84
U-4	8	2-83
U-8	7	2-82

Abbreviations: E-p indicates Elco connector, pin p, 2-67 indicates Board 2, pin 67.

OUTPUT BOARD - BOARD 1

Pin	To	From
1		GND
2		PWR
3		GND
4		PWR
5	E-p	Flag
6	E-k	Control
7	E-j	I/O
8		
9		
10		
11		
12		
13		
14		
15		D/A 2 out
16		
17		Peak 1 Enable
18	Scan Time Pot 50 K	9601
19	V.O. Pot 500 ohm	Peak Detector - Gain
20		
21	Mult. D1-1	EFH Pin 1
22	Add. D2-8	9
23	Display 4	10
24	2	11
25	1	4
26		
27		GND
28		GND
29		
30		0
31	BNC	Multiplexer 1
32	Connectors	Inputs 2
33		3
34		4
35		5
36		6
37		7
38		8
39		9
40		10
41		11
42		12
43		13
44		14
45		15
46		
47		
48		
49		GND
50		GND

OUTPUT BOARD - BOARD 1

Pin	To	From
51		
52		
53		
54		
55		-15 volts
56		-15 volts
57	2-67	± S-R
58	2-6	OS2
59	2-59	Input Clock
60	Q 2-60	Clock Gate
61	S 2-61	OS1
62		
63	A/D Trig 2-63	$\overline{OS1}$
64	501 2-64	Peak 1 Output
65	50K Gain Pot	Multiplexer Out
66	Scan In	D/A 1 Out
67	2-5	$\overline{OS1}$ Out
68		+15 volts
69		+15 volts
70		
71		
72		
73		GND
74		GND
75		
76		
77		Latches: D1-8
78		-4
79		-1
80	Mult. Add. 2-80	-2
81		D6-8
82		-4
83		-2
84		-1
85		±
86		D11-1
87		
88		
89	E-s	CALC V
90	E-t	OUTPUT B
91	E-m	PINS: G
92	E-n	Y
93	E-f	O
94	E-h	R
95	E-b	Br
96	E-c	B1
97		GND
98		PWR
99		GND
100		PWR

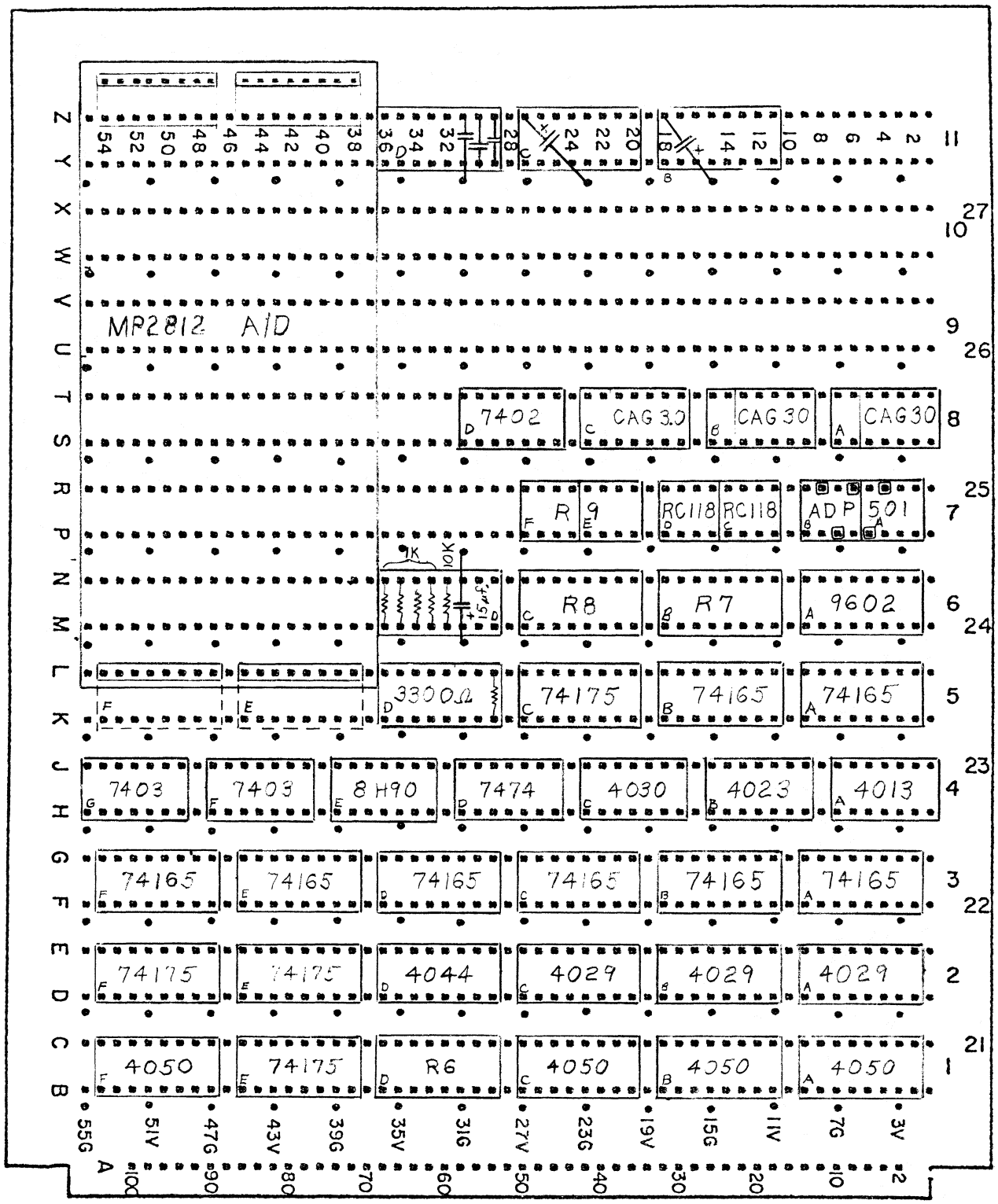
Abbreviations: E-p indicates Elco connector, pin p; 2-67 indicates Board 2, pin 67.

INPUT BOARD - BOARD 2

Pin	To	From
1		GND
2		PWR
3		GND
4		PWR
5	1-67 $\overline{OSI}$ out	9602 Trig
6	1-58 Peak 1 reset	NOR
7	Month Switch	Month NAND
8	Month Switch	Month NAND
9	AB Pin 1	M10
10	Date 8	M8
11	Display 9	M4
12	10	M2
13	5	M1
14	CD Pin 14	D20
15	1	D10
16	9	D8
17	10	D4
18	11	D2
19	4	D1
20	Month Switch	D10 Unbuffered
21	Offset Pot	501
22	Peak 2 Reset	CAG 30
23	Month Switch	D8 Unbuffered
24	Month Switch	D2 Unbuffered
25	Battery	V_{DD}
26	Month Switch	D1 Unbuffered
27		GND
28		GND
29	Meter Switch	A/D Input
30	Month Switch	5.6 V from Battery
31	CALC Blk E-V	Shift
32	Inputs Br E-X	Registers
33	R E-a	
34	O E-Z	
35	Y E-e	
36	G E-d	
37	B E-S	
38	V E-R	
39		
40		
41	480 Hz Clock	Buffer
42		
43	Date Setting	M1-S
44	Switches	M1-R
45		D10-S
46		D10-R
47		D1-S
48		D1-R
49		GND
50		GND

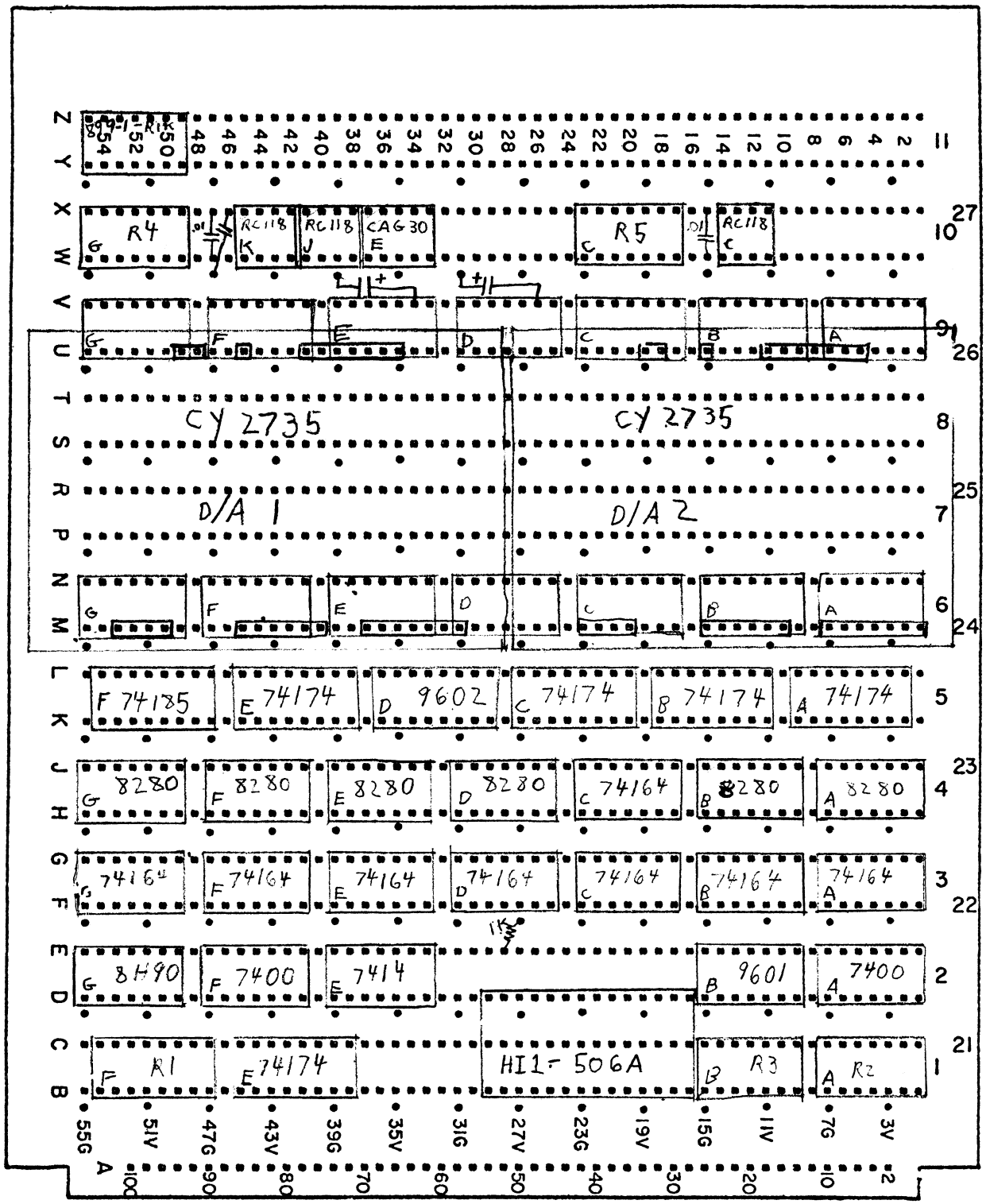
INPUT BOARD - BOARD 2

Pin	To	From
51	Clock $\overline{8}$	Buffers
52	Output $\overline{4}$	
53	$\overline{2}$	
54	$\overline{1}$	
55	Clock 10H	
56	Strobes 1H	
57	10M	
58	1M	
59	Input Clock 1-59	
60	1-60	Q
61	1-61	S
62		
63	1-63	A/D Trig
64	1-64	501 Mult.
65	50K Gain Pot	RC 118
66		
67	$\pm$ SR 1-57	NOR Add
68		+15 volts
69		-15 volts
70		
71		
72		
73		GND
74		GND
75		
76		
77		
78		
79		
80	1-80 D5-1	Mult. Add.
81		
82	Pin 7	A/D U-8
83	8	Output U-4
84	6	U-1
85	9	U-2
86	A/D 10	T-8
87	Display 11	T-4
88	3	H-2
89	12	T-2
90	2	T-1
91	13	H-4
92	1	H-1
93	14	H-8
94		
95		
96		
97		GND
98		PWR
99		GND
100		PWR



Input Board Chip Placement

Pin 1 in upper right-hand corner.



Output Board Chip Placement