NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 132

A READ-ONLY MEMORY PROGRAMMER/VERIFIER

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READ-ONLY MEMORY PROGRAMMER/VERIFIER

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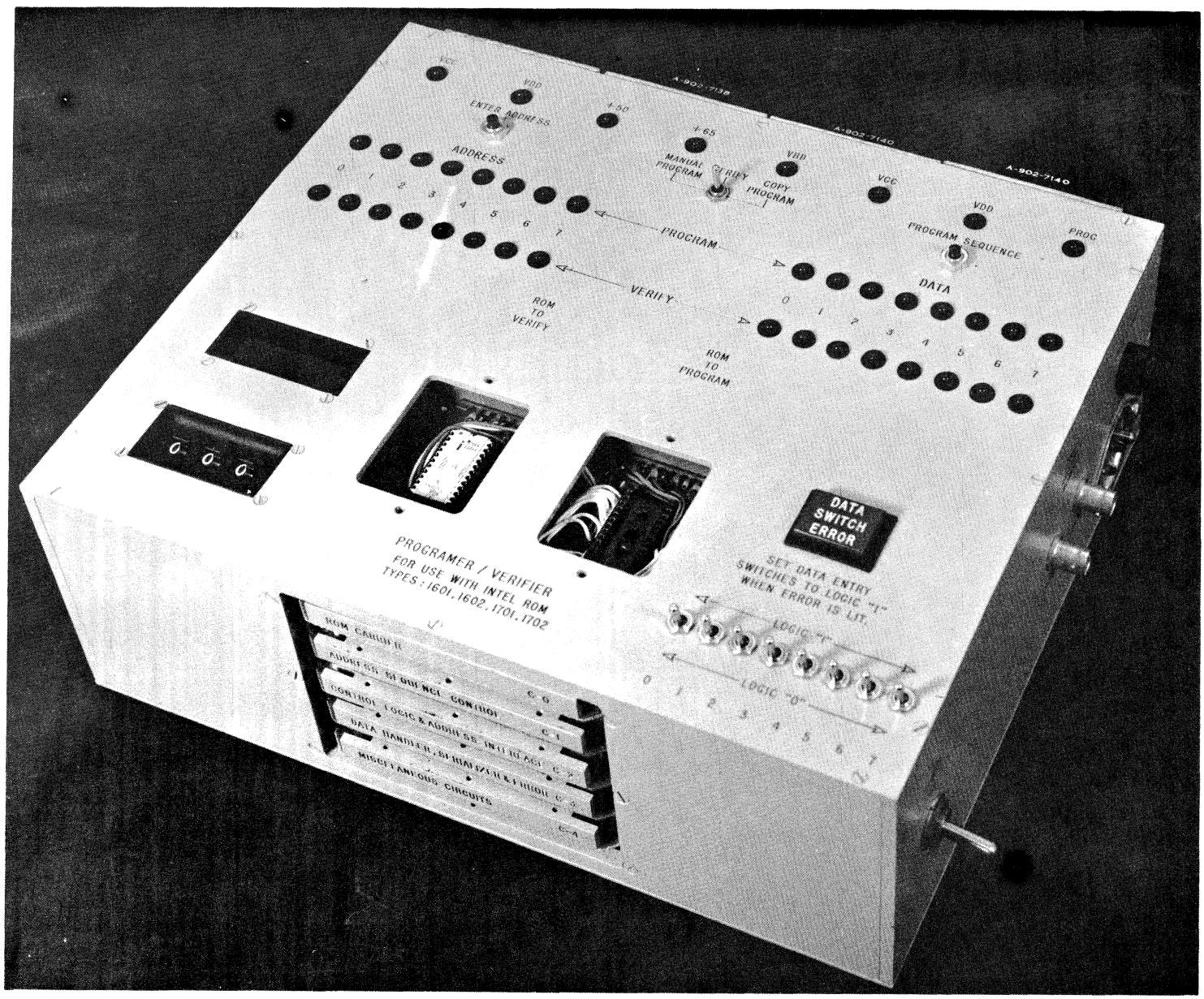
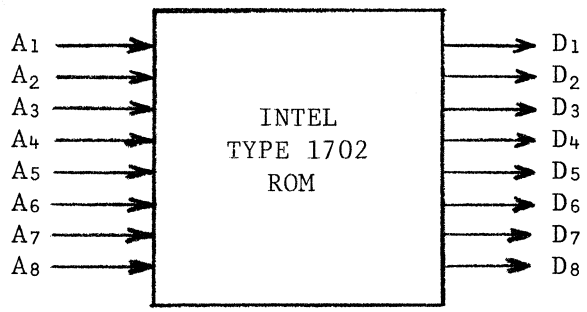
Technological achievement has provided us with the programmable/erasable read-only memory! A programmer for this type of memory has been built and is shown in the picture.



The ROM (Read Only Memory) operates by means of the stored charge principle and will retain data for up to ten years. Or, the ROM may be erased with intense ultra-violet light which discharges the small gate capacitance of the memory cell field effect transistors.

The ROM provides an easy and compact means for code conversion. Any combination and number (up to eight for a single ROM) of binary input lines may be translated to any other combination and number (up to eight for a single ROM) of output binary lines:



Thus, the Intel ROM Type 1702 is an 8 x 8 array of memory cells which is 2048 bits in size. It is anticipated that the ROM system will find many uses in many areas of digital design where complex combinatorial logic comprising multi-gate trees are employed. The advantages are a saving in electronic P.C. board real estate, cost and offer the ability to reconfigure an electronic system by simply unplugging a ROM and plugging in a new one. The 1702 ROM may then be erased for reuse in about 5 minutes with the model UVS-11 ultra-violet light source manufactured by Ultra Light Products, Inc.

Operation

1. Turn off power switch.
2. Plug in ROM in verify socket (pin - 1 key in upper left corner).
3. Turn on power.
4. Move mode selector toggle to "Verify".
5. Advance through all 256 addresses and verify clear memory (all zeros) by using the thumbwheels and address entering push-button.

6. Turn off power.
7. Transfer ROM to program socket.
8. To copy a ROM go to step 18, otherwise go to next step.
9. Turn on power.
10. Move mode selector toggle to "manual program".
11. Set thumbwheels to desired starting address.
12. Push "enter address" and verify that correct address has been entered into the display. (Thumbwheels are notorious mechanical beasts and hence sometimes a little shaking is necessary to get the correct address entered.)
13. Set up the data with the "data entry" switches according to your truth table.
14. Push the "program sequence" push-button. (Verify that faint flickering of the selected address and data bits V_{GG}, Prog, and V_{DD} occurs. V_{DD} is rather bright.)
15. After about 5 seconds the machine will stop with the next address displayed.
16. When 256 is reached, turn off power and go to step 27.
17. Repeat back to step 13 if the next memory address is to be programmed. If not, repeat back to step 11.
18. Move mode selector toggle to "copy program".
19. Insert master ROM in verify socket.
20. Turn on power.
21. Set thumbwheels to 000.
22. Push "program sequence" push-button.
23. Do step 14 and then step 24.
24. In about 20 minutes the machine will stop with 256 displayed in the address display.

25. Turn off power.

26. Remove master ROM from verify socket.

27. Transfer programmed ROM to verify socket.

28. Move mode switch to "verify".

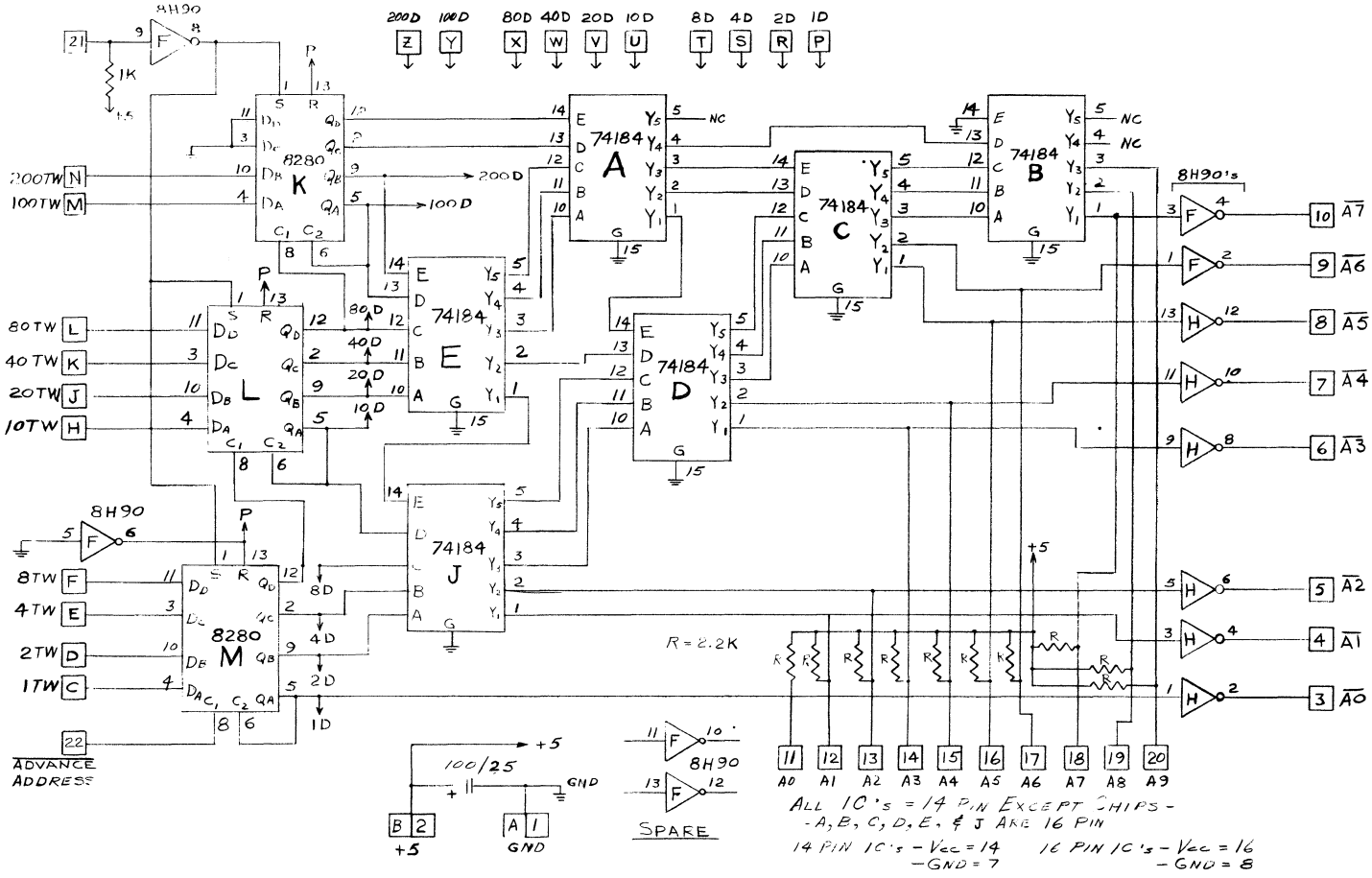
29. Turn on power.

30. Advance through all 256 addresses and verify data according to your truth table.

31. End.

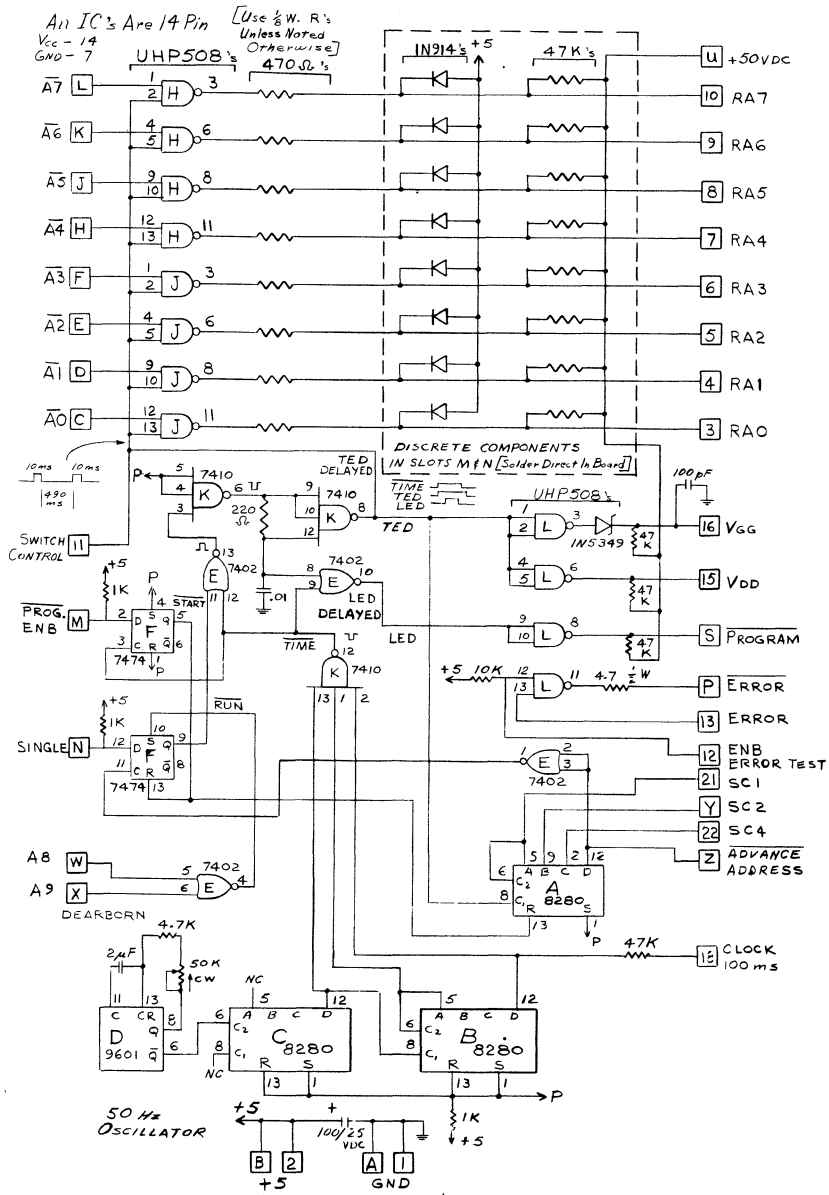
Circuit Description

The ROM programmer comprises address sequence control, program data handling, high voltage program power supply control, and various displays and switches to interface with humans. Circuit card 1 contains a 3-decade address counter-latch (chips K, L, and M) with inputs connected to the thumbwheels (see schematic).



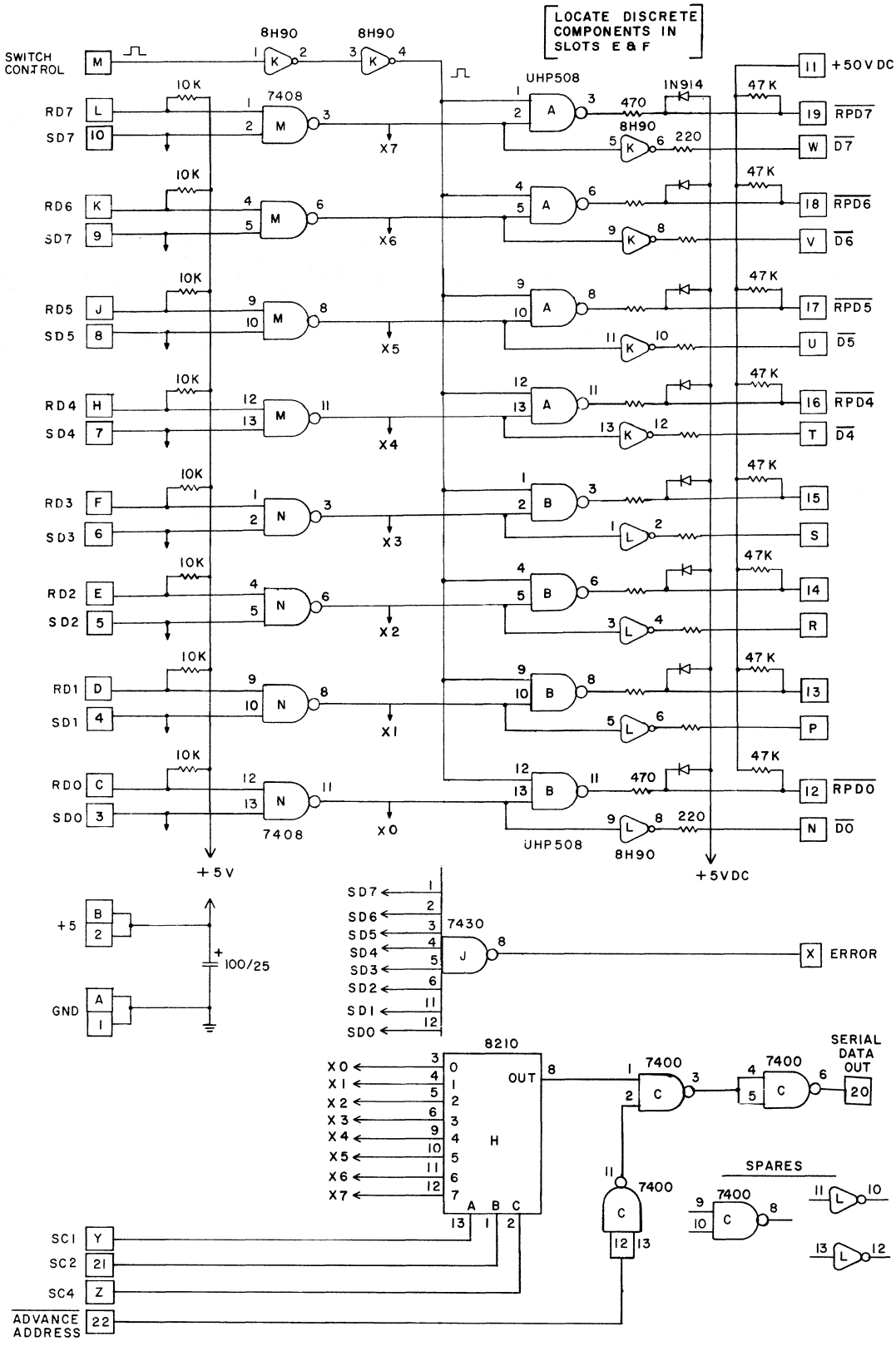
ROM PROGRAMMER/VERIFIER
ADDRESS SEQUENCE CONTROL C1

The "enter address" push-button grounds pin F-9 when pushed which "latches in" the thumbwheel preset address to the counters. The counter outputs drive the displays (card output pins P-Z) and "BCD" to binary code converter chips A, B, C, D, E, and J. The code converter provides binary sequence outputs to inverters F and H and "verify" ROM address inputs. The inverters drive the address (verify) LED's and are also connected to card C-2 high voltage driver inputs (chips H and J). See schematic for card C-2. The driver outputs are connected to the "programmed" ROM address inputs. This ROM "sits up" at +50 volts so that the driver outputs provide negative pulses to the ROM. The 10 ms pulses occur in



ROM PROGRAMER/VERIFIER
CONTROL LOGIC & ADDRESS C-2

groups of ten with a 2% duty factor so that 5 seconds of time is required for each address. This sequence is controlled by the rest of the logic on card C-2. The oscillator (chip D) sets the speed. Decade dividers (chips C and B) provide timing to gate K-12 which provides a 2% duty factor waveform ($\overline{time}$) which enables ultimately the address and data high voltage drivers. Gate K-8 delays the trailing edge of $\overline{time}$ whereas gate E-10 delays the leading edge of $\overline{time}$. These gates operate in such a way that the program pulse occurs fully inside the time span between set-up and release time of all other logic and signals applied to the programmed ROM. This precludes the possibility of spikes occurring internal to the ROM due to race conditions yielding erroneous results. Flip-flops (F) maintain the run status of the machine. Divider (chip A) counts the sequence of ten program pulses and stops and/or advances the address accordingly. The outputs of this counter also drive the serializer comprising chips H and C on card C-3 which provide serial data to a chart recorder for recording. See card schematic C-3. Data entry switch data and "verify" ROM data are both connected to chips M and N which provide program data to the high voltage drivers (chips A and B) providing appropriate negative voltage pulses to the programmed ROM. Chips K and L drive the verify data LED's for display purposes. The "program" address and data display LED's are series connected with the appropriate programmed ROM terminals which provides a monitor of current flow from the ROM. If the ROM is shorted the corresponding LED will light brightly; if open, it will not light at all. Normally during program sequence the LED's flicker dimly according to logic status of the high voltage signals driving the "programmed" ROM. Diodes 1N914 and 470 ohm resistors provide a clamping to -45 V action to the high voltage drivers, thus limiting the negative amplitude according to Intel specification. The error gate J-8 checks the status of the data entry switches and provides a logical zero signal to gate L-11 on card C-2 when all data toggles are set to 1. This is a necessary condition to operate the programmer in the "copy" mode. When the

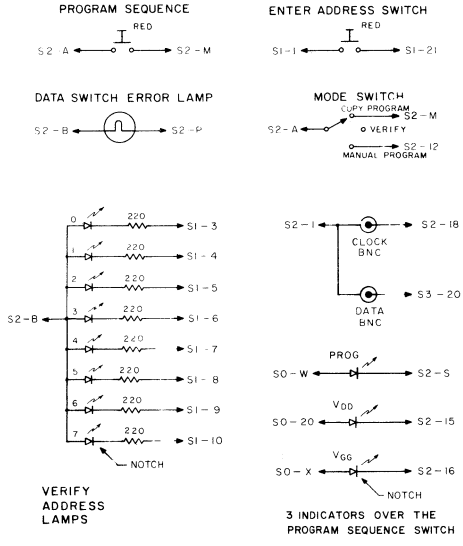


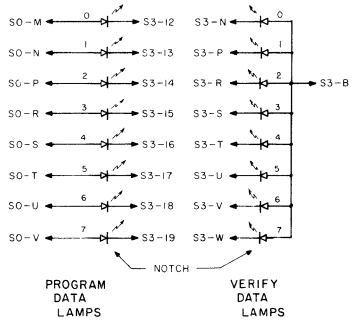
ROM PROGRAMER / VERIFIER

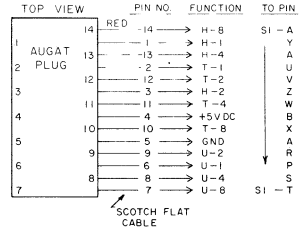
DATA HANDLER, SERIALIZER, & ERROR CHECK LOGIC C-3

mode toggle is placed in the "copy ROM' position, gate L-11 is enabled which drives the error indicator accordingly.

The following schematic presents the various interface, display, and power supply circuits.

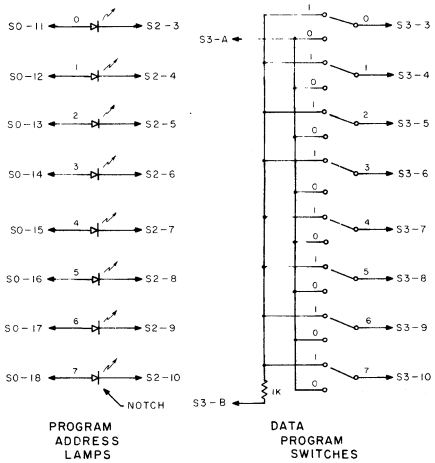


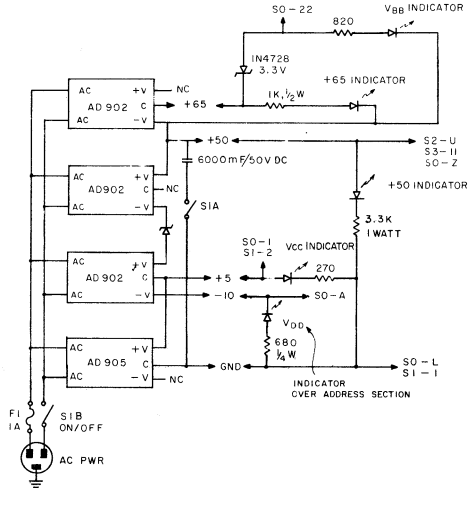




FOR: 3 DIGIT GENERAL PURPOSE DISPLAY —
INDEPENDENT / PARALLEL BCD DATA
NO DEC. POT OR STROBE

14 PIN AUGAT / SCOTCH CABLE FAN OUT —
FOR ADDRESS DISPLAY

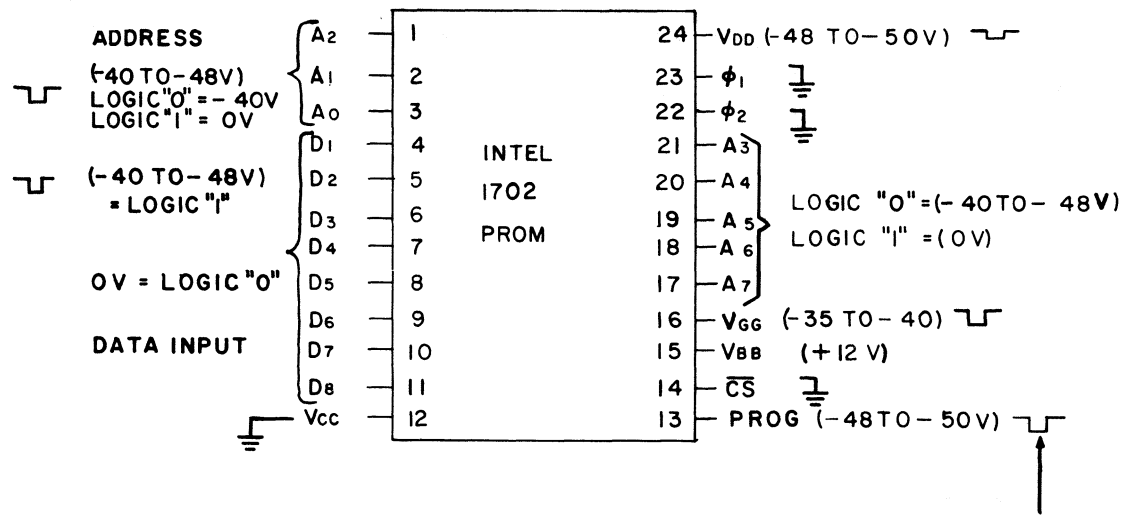




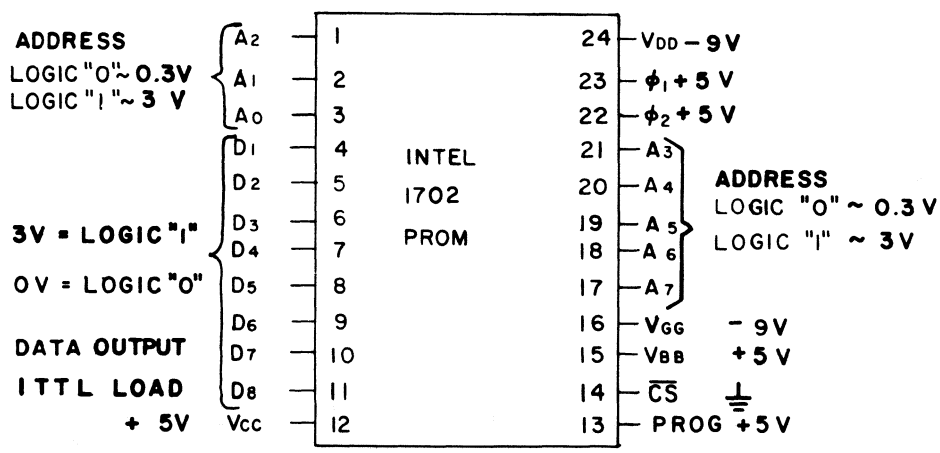
The next three pages provide specifications for the Intel series ROM's. Some specifications vary in the data (i.e., program time of 2 minutes instead of 20) since some older, low serial number ROM's required more relaxed variables. The programmer should remain timed to provide 20 minute programming time to accommodate the older ROM's. The last pages provide pictures and wire lists of the equipment.

ROM PROGRAMER/VERIFIER

PROGRAM:



VERIFY:



2048 BIT ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

1602A -- ELECTRICALLY PROGRAMMABLE

1702A -- ERASABLE & ELECTRICALLY REPROGRAMMABLE

- **Fast Programming -- 2 minutes for all 2048 bits**
- **All 2048 bits guaranteed * programmable -- 100% factory tested**
- **Fully Decoded, 256x8 organization**
- **Static MOS -- No Clocks Required**
- **Inputs and Outputs DTL and TTL compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip select input lead**

The 1602A and 1702A are 256 word by 8 bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A and 1702A undergo complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

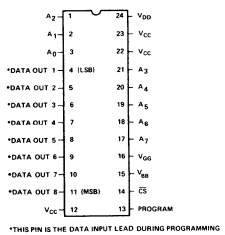
The 1602A and 1702A use identical chips. The 1702A is packaged in a 24 pin dual in-line package with a transparent quartz lid. The transparent quartz lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. This procedure can be repeated as many times as required. The 1602A is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A/1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the 1602A or 1702A.

The 1602A/1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



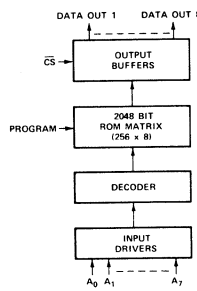
*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

See page 3-8 for operational connection.

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONNECTIONS

The external lead connections to the 1602A/1702A differ, depending on whether the device is being programmed[1] or used in read mode. (See following table)

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = −9V±5%, V_{GG}[2] = −9V±5%, unless otherwise noted.

SYMBOL	TEST	MIN.	TYP.[3]	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2, I_{OL} = 0.0mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0, I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

Continuous Operation

Note 1: In the programming mode, the data inputs 1–8 are pins 4–11 respectively. $\overline{CS}$ = GND.
Note 2: V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} increases in proportion to V_{GG} duty cycle. (See p. 5)
Note 3: Typical values are at nominal voltages and T_A = 25°C.

A.C. Characteristics

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5% unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		.700	1	μs
t_{DVGG}	Clocked V_{GG} set up	0			μs
t_{CS}	Chip select delay			100	ns
t_{CO}	Output delay from $\overline{CS}$			900	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	μs

Note 1. The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Capacitance* T_A = 25°C

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	V_{IN} = V_{CC}, $\overline{CS}$ = V_{CC}, V_{OUT} = V_{CC}, V_{GG} = V_{CC} — All unused pins are at A.C. ground
C_{OUT}	Output Capacitance		10	15	pF	
$C_{V_{GG}}$	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

*This parameter is periodically sampled and is not 100% tested.

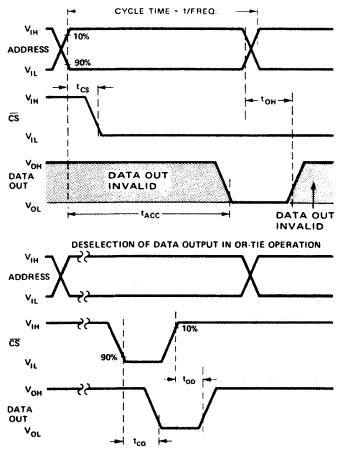
Switching Characteristics

Conditions of Test:

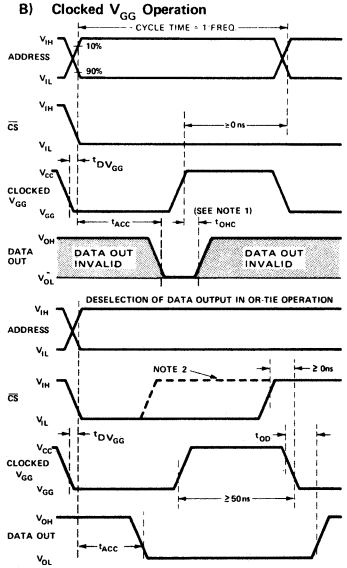
Input pulse amplitudes: 0 to 4V; t_R, t_F ≤50 ns

Output load is 1 TTL gate; measurements made at output of TTL gate (t_{PD}≤15 ns)

A) Constant V_{GG} Operation



B) Clocked V_{GG} Operation



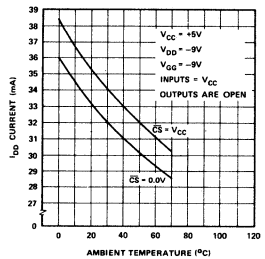
NOTE 1: The output will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

NOTE 2: If $\overline{CS}$ makes a transition from V_{IL} to V_{IH} while clocked V_{GG} is at V_{GG}, then deselection of output occurs at t_{OD} as shown in static operation with constant V_{GG}.

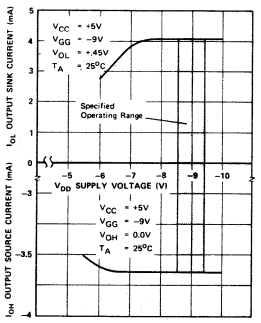
intel® Silicon Gate MOS **1602A/1702A** ROMs

Typical Characteristics

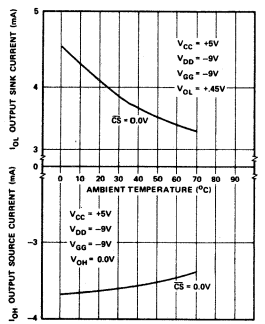
I_{DD} CURRENT VS. TEMPERATURE



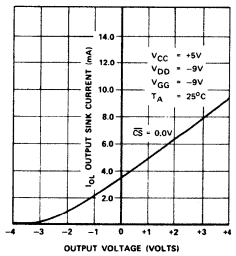
OUTPUT CURRENT VS. V_{DD} SUPPLY VOLTAGE



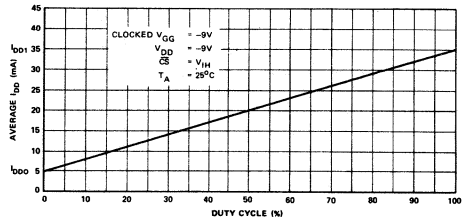
OUTPUT CURRENT VS. TEMPERATURE



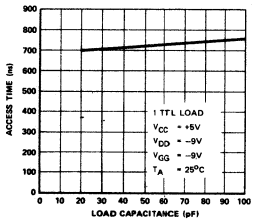
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



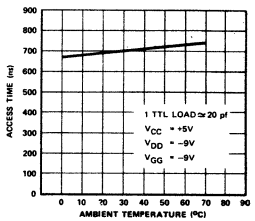
AVERAGE CURRENT VS. DUTY CYCLE FOR CLOCKED V_{GG}



ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. TEMPERATURE



PROGRAMMING OPERATION

D.C. and Operating Characteristics for Programming Operation

T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = −48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = −48V
I_{BB}	V_{BB} Supply Load Current		.05		mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{prog} = −48V V_{GG} = −35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300 mA for greater than 100 μsec. Average power supply current I_{DDP} is typically 40 mA at 20% duty cycle.

A.C. Characteristics for Programming Operation

$T_{AMBIENT}$ = 25°C, V_{CC} = 0V, V_{BB} = + 12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle (V_{DD} , V_{GG})			20	%	
$t_{\phi PW}$	Program Pulse Width			3	ms	V_{GG} = −35V, V_{DD} = V_{prog} = −48V
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD} , V_{GG} Set Up	100			μs	
t_{VD}	V_{DD} , V_{GG} Hold	10		100	μs	
t_{ACW} (2)	Address Complement Set Up	25			μs	
t_{ACH} (2)	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

Note 2. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.

Switching Characteristics for Programming Operation

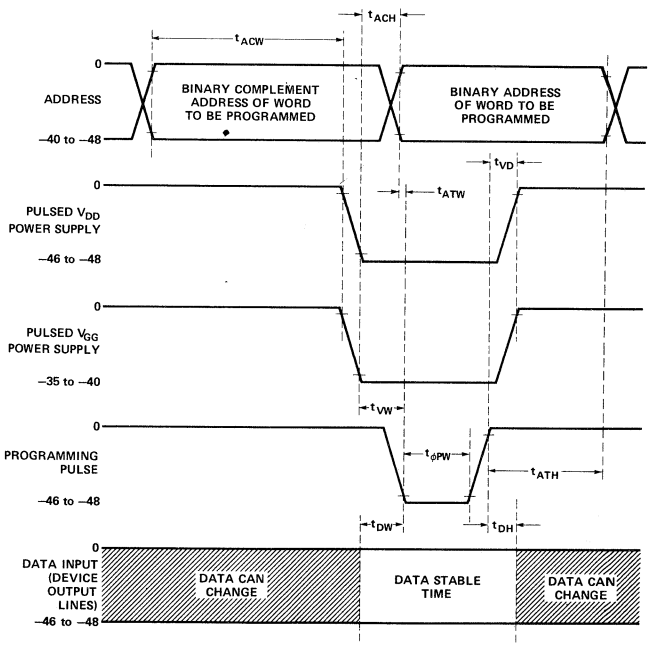
PROGRAM OPERATION

Conditions of Test:

Input pulse rise and fall times ≤ 1μsec

$\overline{CS}$ = 0V

PROGRAM WAVEFORMS



Programming Operation of the 1602A/1702A

When the Data Input for the Program Mode is:	Then the Data Output during the Read Mode is:
V_{ILIP} = ~−48V pulsed	Logic 1 = V_{OH} = 'P' on tape
V_{IHP} = ~ 0V	Logic 0 = V_{OL} = 'N' on tape

WORD	ADDRESS A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|
255	1	1	1	1	1	1	1	1

Address Logic Level During Read Mode: Logic 0 = V_{IL} (~.3V) Logic 1 = V_{IH} (~3V)

Address Logic Level During Program Mode: Logic 0 = V_{IL2P} (~−40V) Logic 1 = V_{IHP} (~0V)

A ROM VERIFY

From		To
A2	1	4
A1	2	3
A0	3	2
RD0	4	B
RD1	5	C
RD2	6	D
RD3	7	E
RD4	8	F
RD5	9	H
RD6	10	J
RD7	11	K
	12	

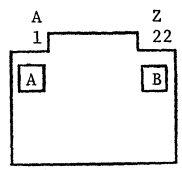
From	To	
13		
14	L	
15		
16		
17	9	A7
18	8	A6
19	7	A5
20	6	A4
21	5	A3
22		
23		
24		

1N914

1N914

1
(+5)

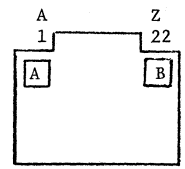
A
(-10)



B ROM PROGRAM

From			To	From	To	Program
A2	1		13	13	W	
A1	2		12	14		
A0	3		11	15	22	V_{BB} + 12
D0	4	LSB	M	16	X	V_{GG}
D1	5		N	17	18	A7
D2	6		P	18	17	A6
D3	7		R	19	16	A5
D4	8		S	20	15	A4
D5	9		T	21	14	A3
D6	10		U	22		
D7	11	MSB	V	23		
	12			24	20	V_{DD}

Z
(+50)



CARD SLOT WIRING LIST

FOR: BOX ROM Programmer/Verifier CARD C-1

Slot 1 —

Y Buss
X Buss
1 K

Address Select Thumb-wheels

	From	To	From	To
A	Gnd		1	GNd
B	+5		2	+5
C	1 - TW		3	S2-C
D	2 - TW		4	S2-D
E	4 - TW		5	S2-E
F	8 - TW		6	S2-F
H	10 - TW		7	S2-H
J	20 - TW		8	S2-J
K	40 - TW		9	S2-K
L	80 - TW		10	S2-L
M	100 - TW		11	SO-2
N	200 - TW		12	SO-3
P			13	SO-4
R			14	SO-5
S			15	SO-6
T			16	SO-7
U			17	SO-8
V			18	SO-9
W			19	S2-W
X			20	S2-X
Y			21	
Z			22	S2-Z

Abbreviations:

Ex: S 25-22
Slot 25, Pin 22

J9-MM
Elco J9, Pin MM

BNC Connectors: B1, B2, B3, etc.
Elco Connectors: J1, J2, J3, etc.
Slot Connectors: S1, S2, S3, etc.
Pin No.'s -3, -X, -B, -22, etc.

USE BUSS WIRE WHENEVER POSSIBLE TO NAME CONNECTIONS TO ADJACENT CARDS.

CARD SLOT WIRING LIST

FOR: BOX ROM Programmer/Verifier CARD C-2

Slot 2 —

	From	To	From	To
A	Gnd		1	Gnd
B	+5		2	+5
C			3	
D			4	
E			5	
F			6	
H			7	
J			8	
K			9	
L			10	
M			11	S3-M
N			12	
P			13	S3-X
R	NC		14	NC
S			15	SO-20
T	NC		16	SO-X
U	+50 V DC		17	NC
V	NC		18	
W			19	NC
X			20	NC
Y	S3-21		21	S3-Y
Z	S3-22		22	S3-Z

Abbreviations:

Ex: S 25-22
Slot 25, Pin 22

J9-MM
Elco J9, Pin MM

BNC Connectors: B1, B2, B3, etc.
Elco Connectors: J1, J2, J3, etc.
Slot Connectors: S1, S2, S3, etc.
Pin No.'s -3, -X, -B, -22, etc.

CARD SLOT WIRING LIST

FOR: BOX ROM Programmer/Verifier CARD C-3

Slot 3 —

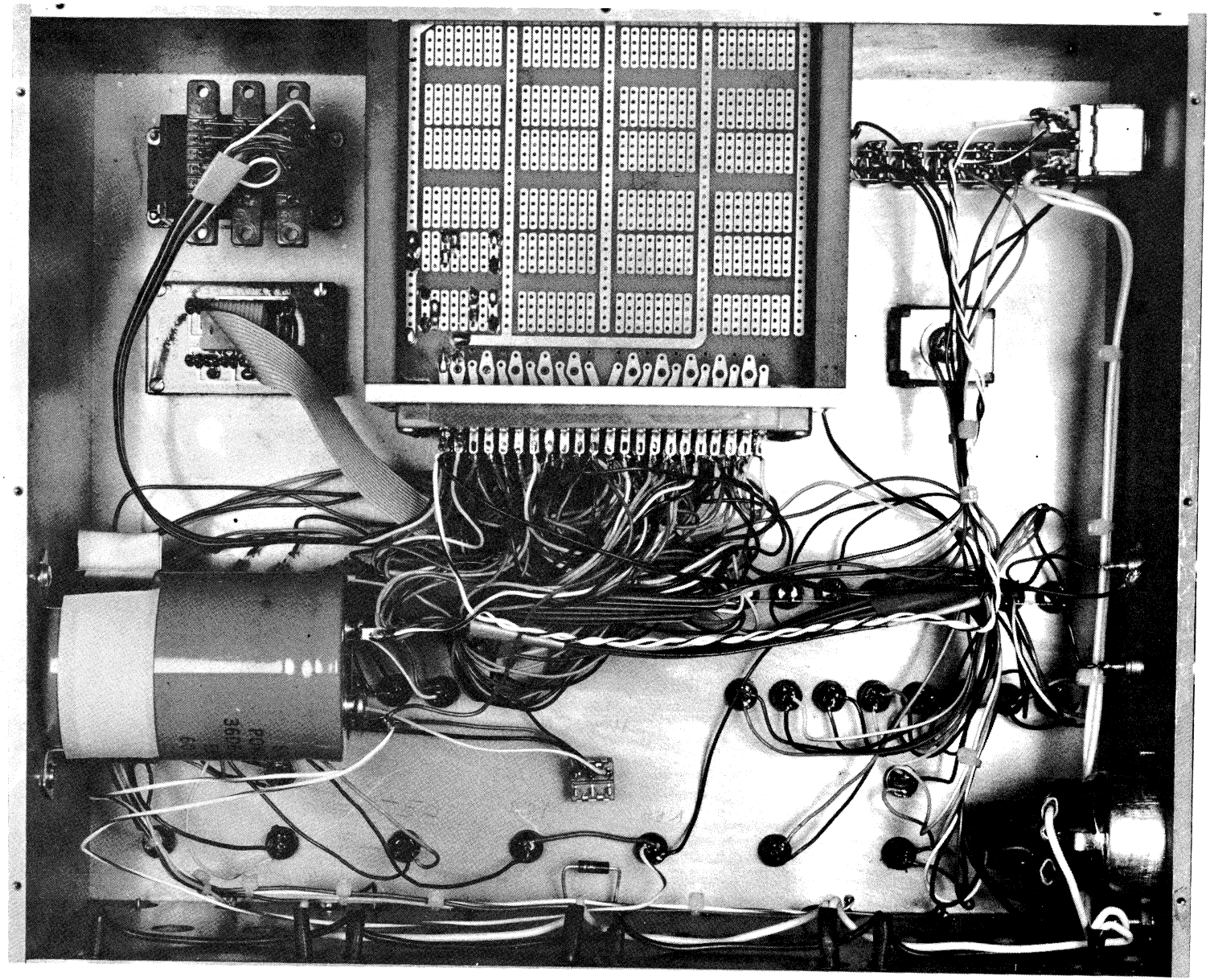
	From	To	From	To
A	Gnd		1	Gnd
B	+5		2	+5
C	SO-B		3	
D	SO-C		4	
E	SO-D		5	
F	SO-E		6	
H	SO-F		7	
J	SO-H		8	
K	SO-J		9	
L	SO-K		10	
M			11	+50 V DC
N			12	
P			13	
R			14	
S			15	
T			16	
U			17	
V			18	
W			19	
X			20	
Y			21	
Z			22	

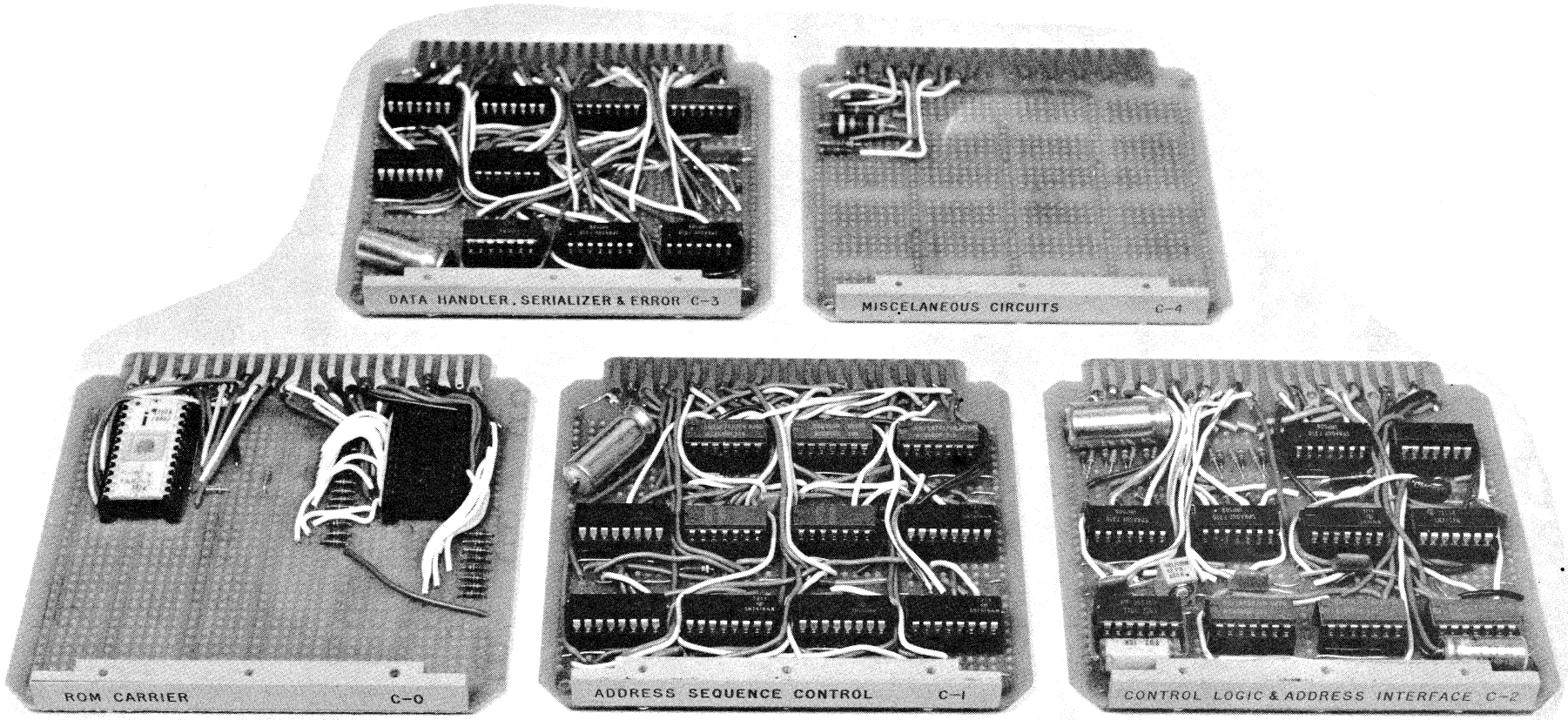
Abbreviations:

Ex: S 25-22
Slot 25, Pin 22

J9-MM
Elco J9, Pin MM

BNC Connectors: B1, B2, B3, etc.
Elco Connectors: J1, J2, J3, etc.
Slot Connectors: S1, S2, S3, etc.
Pin No.'s -3, -X, -B, -22, etc.




DATA HANDLER, SERIALIZER & ERROR C-3
MISCELANEOUS CIRCUITS C-4
ROM CARRIER C-0
ADDRESS SEQUENCE CONTROL C-1
CONTROL LOGIC & ADDRESS INTERFACE C-2