NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia 24944

Electronics Division Internal Report No. 130

PULSE PERIOD GENERATOR

Michael Hersman

AUGUST 1973

NUMBER OF COPIES: 150

PULSE PERIOD GENERATOR

Michael Hersman

General Description

An accurate pulse period generator, with adjustable analog delay and width features, has been completed for use in the new 0.5-1 GHz pulsar receiver system. Periods of up to 10 seconds are available with resolution of 1 microsecond and accuracy to within a few parts in 10^7. A zero to ten second delay stage allows pulse placement anywhere within the selected period. Pulse width is adjustable from less than 0.1 ms to 10 seconds. The delay and width stages are accurate to within 3% of setting and stable to within 0.01% of setting. The output is a TTL compatible, positive or negative logic pulse.

Physically, the generator consists of two power supplies and four printed circuit boards with associated hardware mounted in a standard 3 1/2 inch rack drawer. (See the attached photograph.) The circuit boards are: (1) a seven decade, CMOS programmable down counter, (2) the delay and the width circuitry, (3) the oscillator and some interface circuitry, and (4) the output stage.

Functional Description

The Clock

The internal clock for the period generator is a Vectron Laboratories temperature-compensated (no oven required) crystal oscillator model CO-251 with TTL compatible output, operating at 5 MHz. The oscillator has an advertised stability of 10^{-8} per day and 10^{-6} per year. Five megahertz was chosen as the clock frequency to facilitate the use of 5 MHz from the hydrogen maser if greater accuracy than that provided by the internal clock is desired.

The internal clock frequency is adjustable, and a monitor output is provided on the rear panel.

The "EXTERNAL 5 MHz" input is designed for use with a 1 V to 2 V rms sine wave.

The 5 MHz is divided to 1 MHz and the logic level is shifted from 0-5 V TTL to the 0-15 V CMOS level needed to drive the divider.

The Divider

The divider stage (Figure 2) uses seven Motorola MC 14522CL programmable down counters cascaded to provide maximum counting capability of 10^7 - 1 which, at the 1 MHz clock speed, gives a maximum period of 9.999999 seconds. BCD digiswitches, with separate true and not true commons, are used to set in the period.

Occasionally, when changing period settings or when the counter sees all zeros, the counting sequence is disrupted and the counter must be reset. A button is provided for this purpose on the front panel.

The period pulse out of the divider is inverted to provide a negative going edge for the delay stage.

The Delay-Width Section

The delay and width stages (Figure 3) use Signetics NE 555 integrated circuit timers with external, variable R-C networks (Figure 4) to generate periods from less than 0.1 ms to 10 seconds. The input circuit passes only the negative going edge of the input pulse to trigger the timer. The panel LED's are driven from the timers through 24 ohm dropping resistors.

The delay and the width durations are set with a turns-counting dial and a switched multiplier. The turns-counting dial may be set as low as 0.10. On extremely low settings (e.g., 0.01) the timing period is no longer accurate and the timer may oscillate.

The delay and width stages may be used either with the internal period generator or with an external period introduced as a + or - TTL logic edge at the appropriate "EXTERNAL EDGE IN" input.

With the delay multiplier switch set in the zero delay position, the period pulse from the divider is applied to the input of the width stage and the delay stage is bypassed.

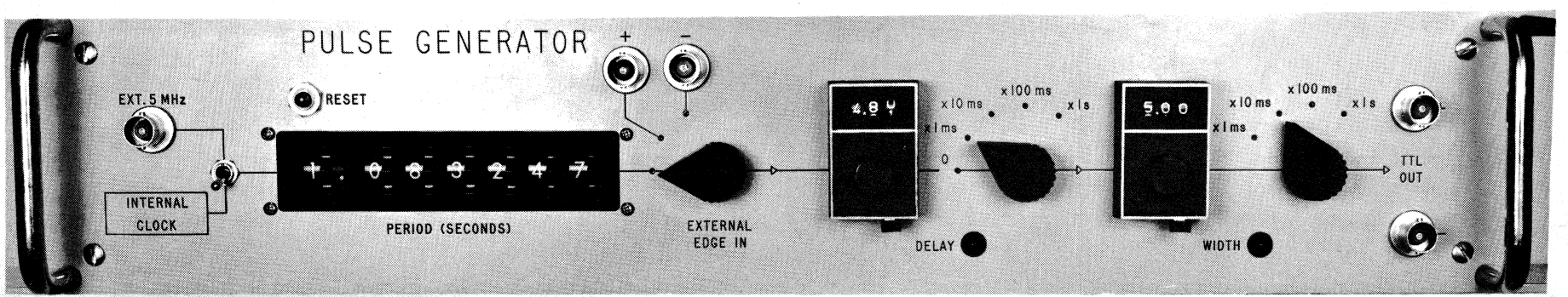
The delay and width durations were calibrated during construction by careful selection of capacitors for the R-C networks. After a nominally correct capacitor combination was found, other capacitors of the same value were tried until the desired accuracy was achieved.

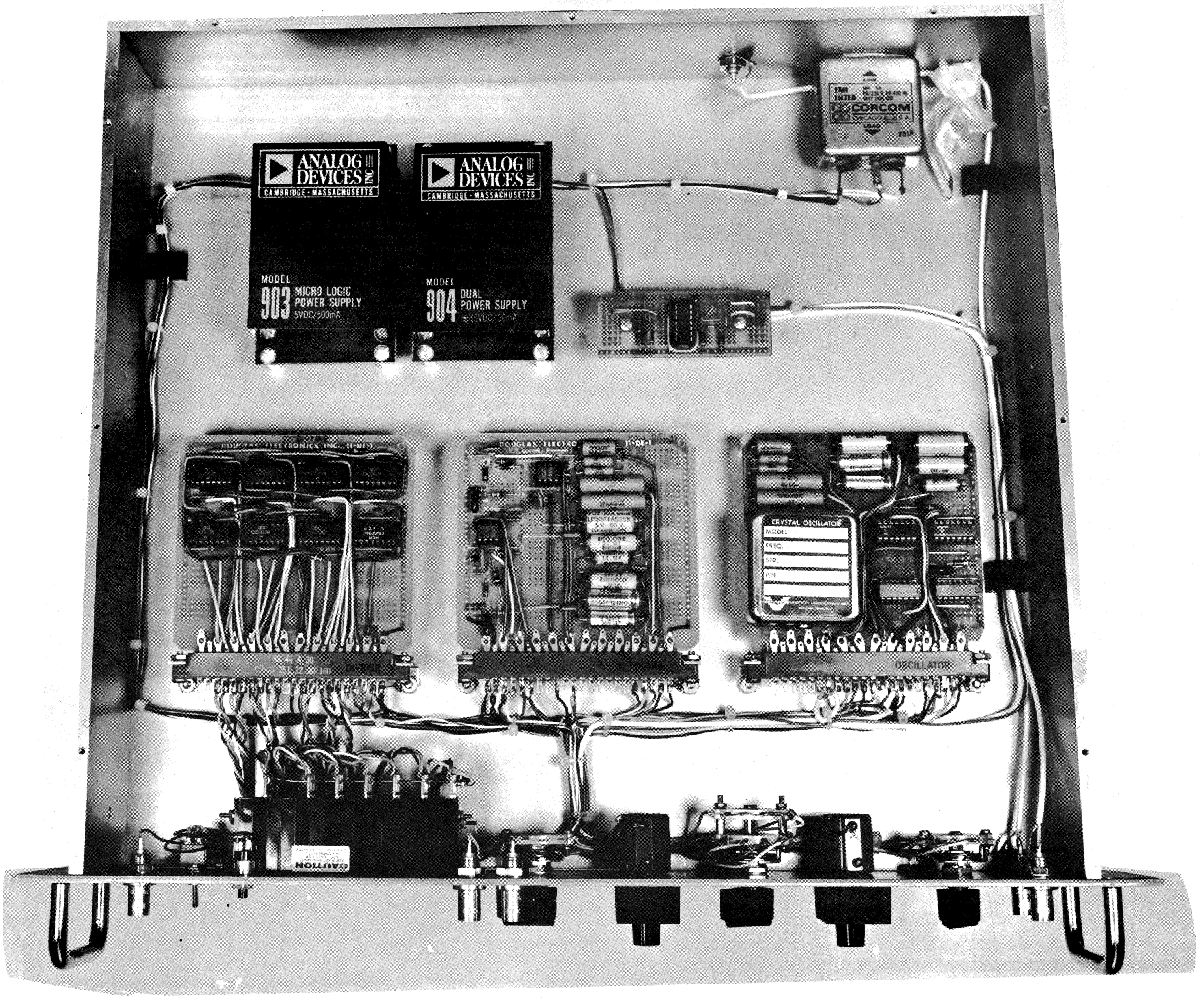
The accuracy of the delay and width stages is better than $\pm$ 3% of dial setting. The timing accuracy from pulse to pulse is better than 0.01% of dial setting. This variation can cause an output pulse jitter of 0.01% of the delay stage setting. If a jitter free pulse is needed, the delay stage should be bypassed and the real time pulse placement could then be set by a hit or miss method using the counter reset button. However, it is not expected that this small amount of jitter will cause any problems.

The Output

The output stage (Figure 6) consists of one SN 7406 hex open collector buffer. It is located on its own small board with filtered power supply line and with extra care taken to insure good grounding to eliminate noise on the output. Originally, unused portions of the SN 5406 and SN 5407 chips on the oscillator board were used for output, but excessive noise levels were encountered (0.3 volt peak to peak at 1 MHz) and the output was moved to its own board, which solved the problem.

The output is TTL compatible, with a maximum fan out of 25 for both TTL + and - outputs.


PULSE GENERATOR
+
−
EXT. 5 MHz
RESET
INTERNAL
CLOCK
+ . 0 0 0 2 4 7
PERIOD (SECONDS)
EXTERNAL
EDGE IN
4.8 Y
x 10 ms
x 100 ms
x 1 s
x 1 ms
0
DELAY
5.0 0
x 10 ms
x 100 ms
x 1 s
x 1 ms
WIDTH
TTL
OUT


ANALOG DEVICES INC
CAMBRIDGE - MASSACHUSETTS
MODEL
903 MICRO LOGIC POWER SUPPLY
5VDC/500mA
ANALOG DEVICES INC
CAMBRIDGE - MASSACHUSETTS
MODEL
904 DUAL POWER SUPPLY
±15VDC/50mA
EMI FILTER
CORCOM
CHICAGO, ILL. U.S.A.
DOUGLAS ELECTRONICS, INC. 11-DE-1
DOUGLAS ELECTRO 11-DE-1
CRYSTAL OSCILLATOR
MODEL
FREQ
SER
PIN
DIVIDER
OSCILLATOR
CAUTION

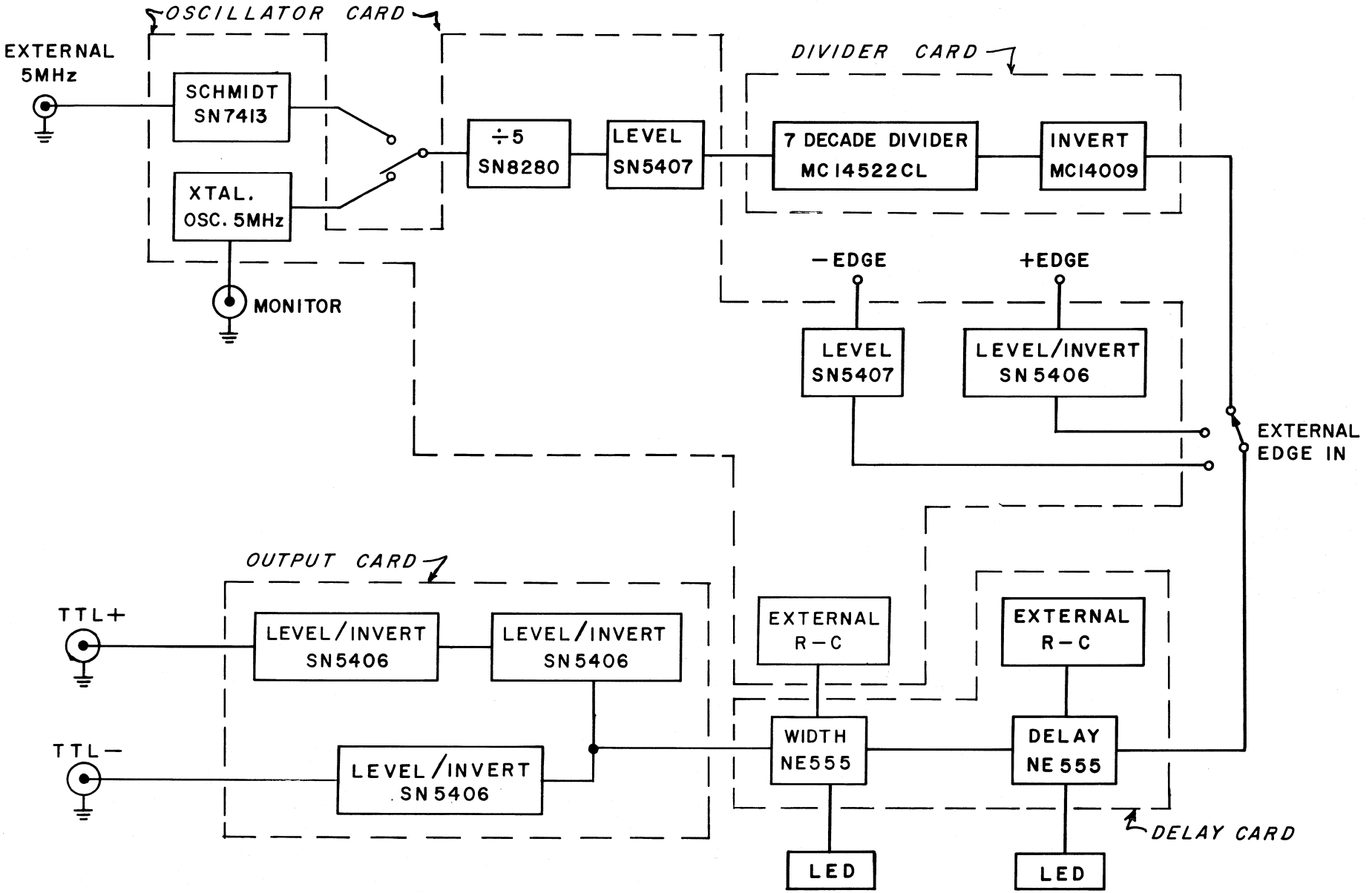
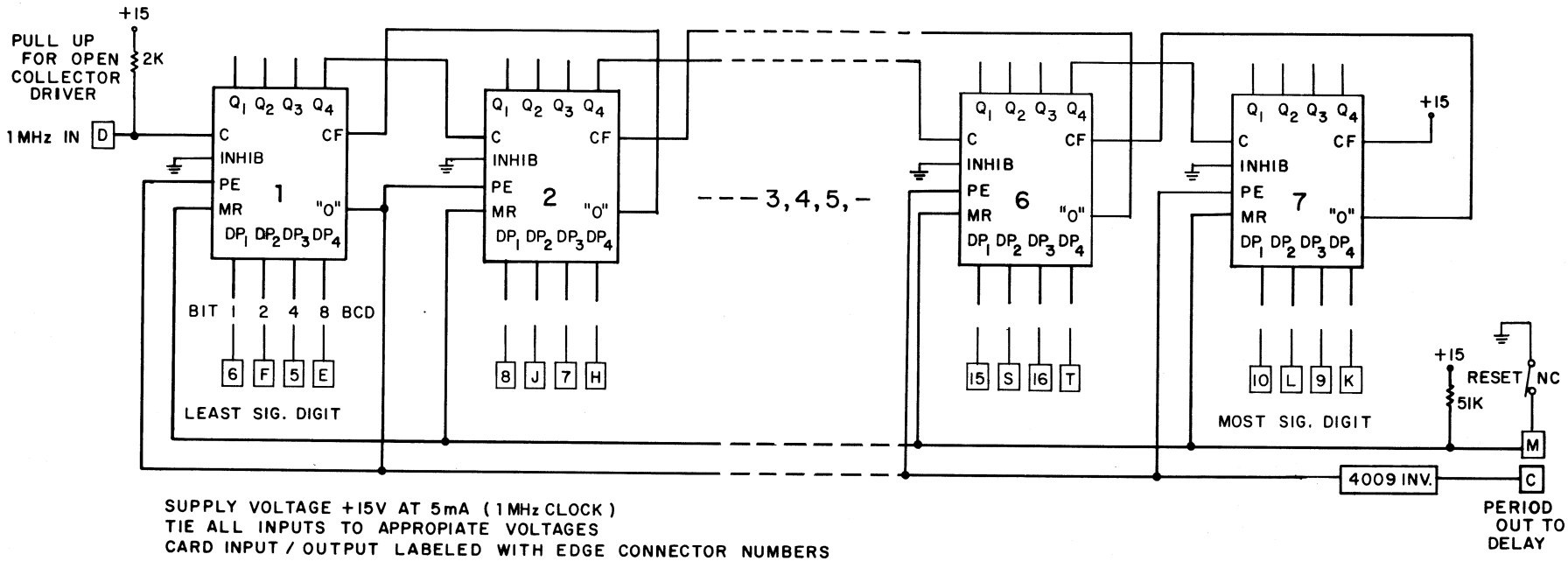
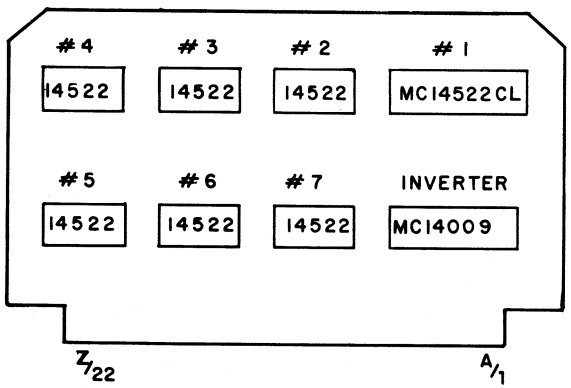
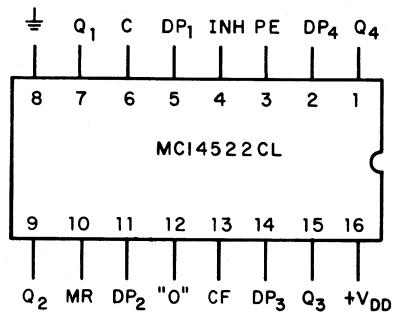


FIG. 1 BLOCK DIAGRAM





DIVIDER CARD LAYOUT



PIN LAYOUT FOR DIVIDER CHIP

FIG. 2 7 DECADE DIVIDER CHAIN

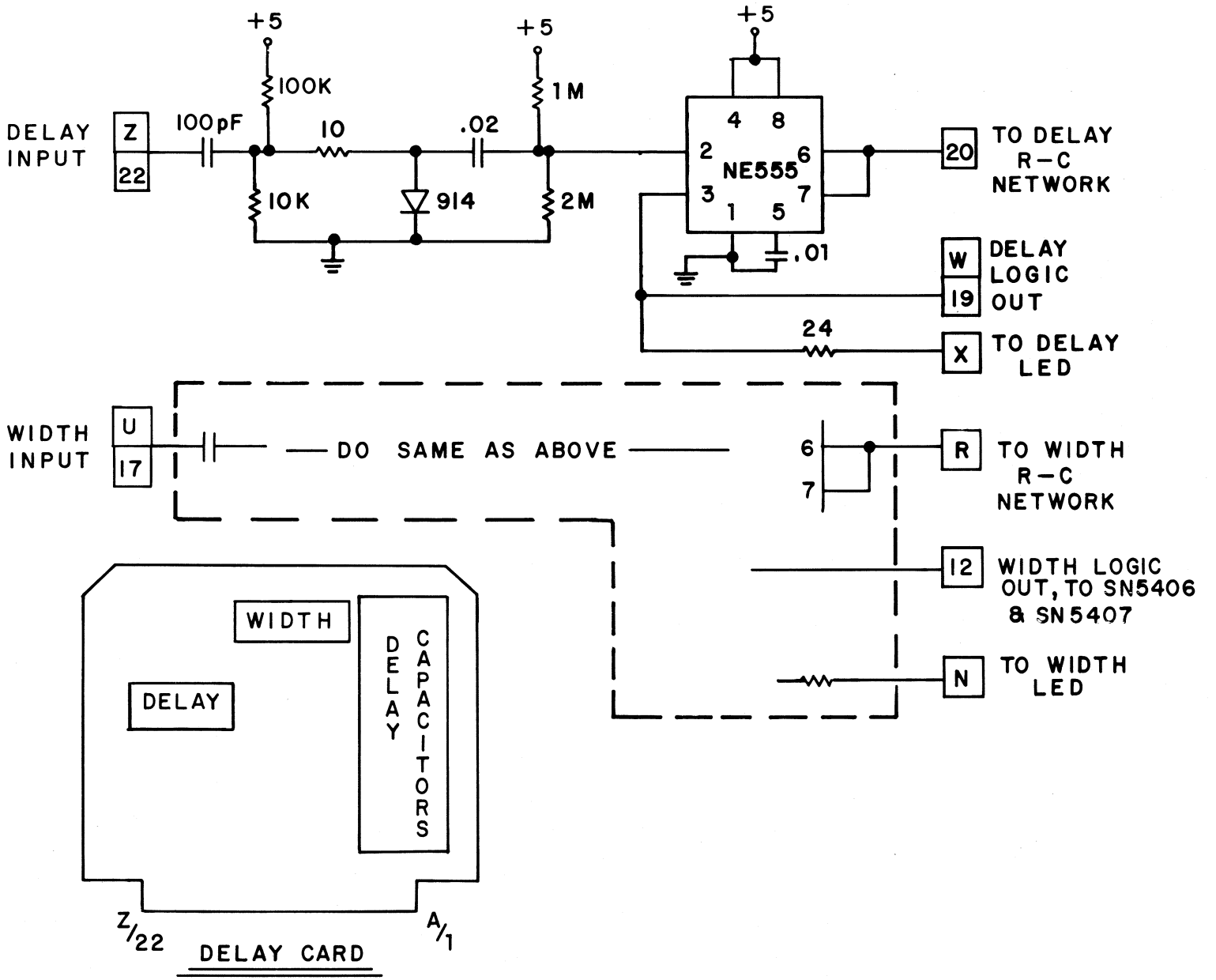


FIG. 3 DELAY WIDTH CIRCUITS

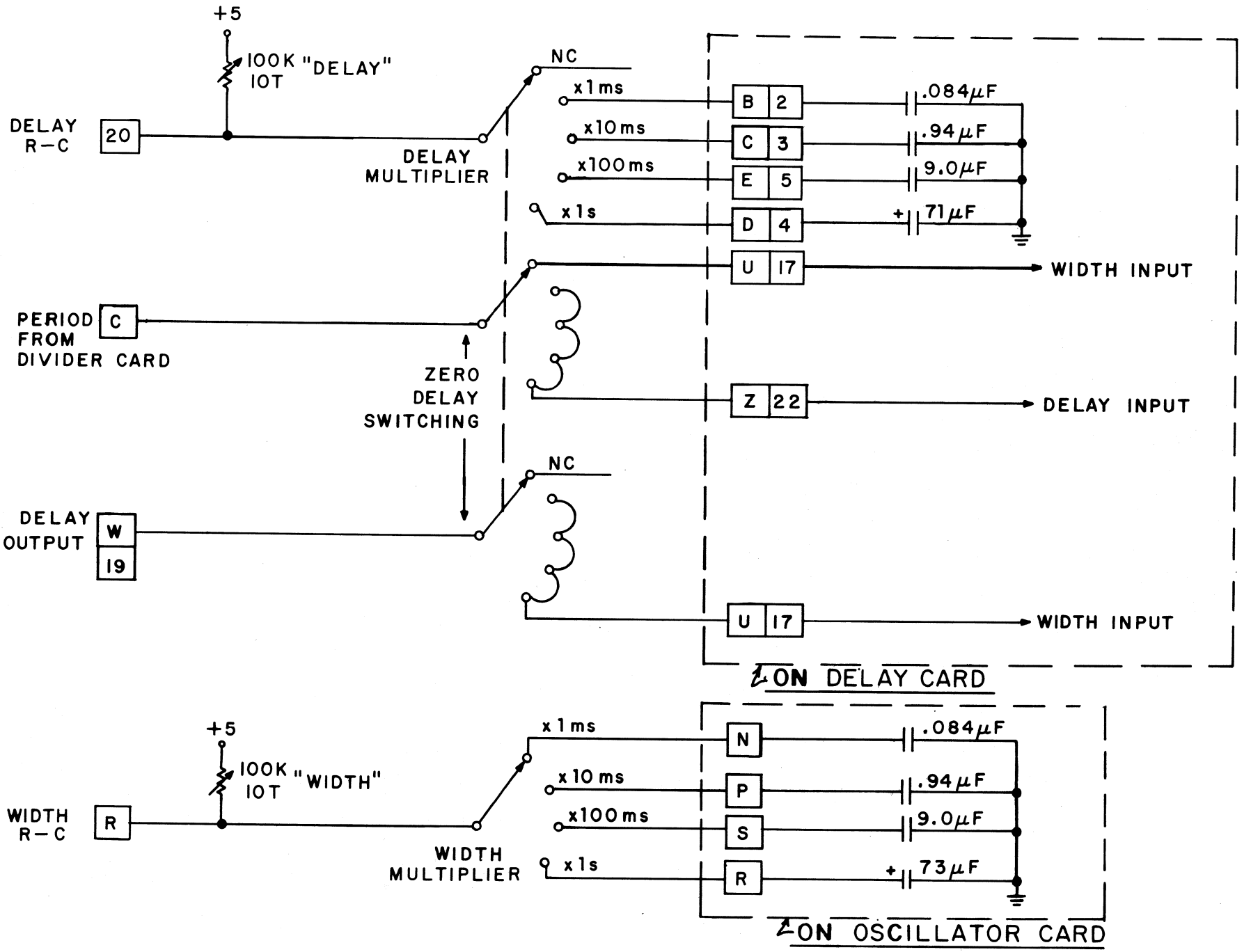
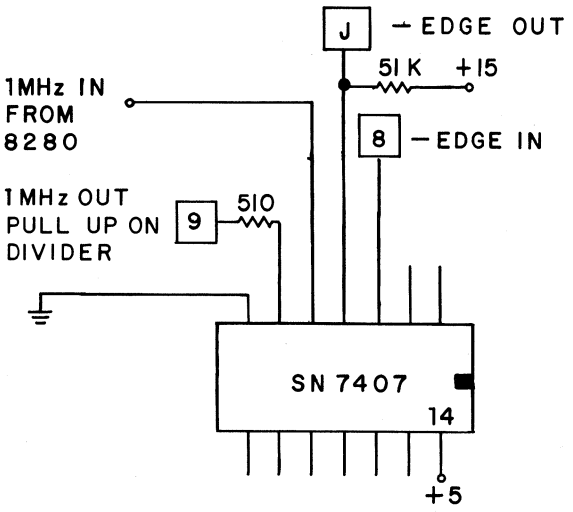
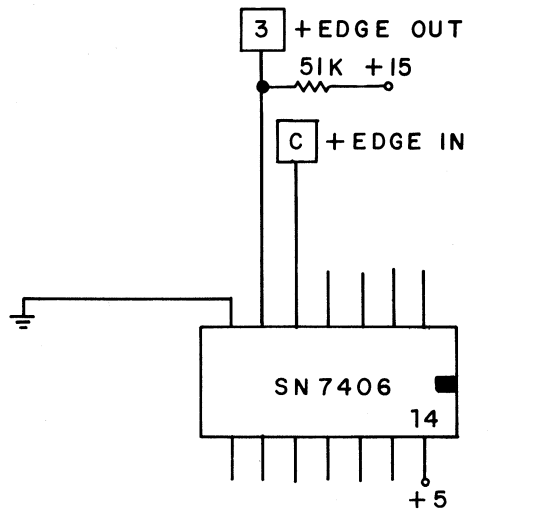


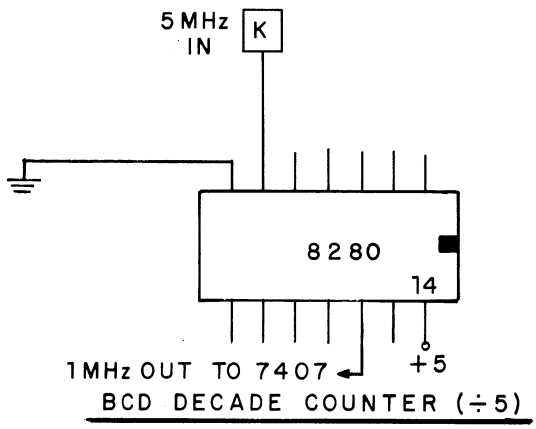
FIG. 4 DELAY & WIDTH CONTROLS



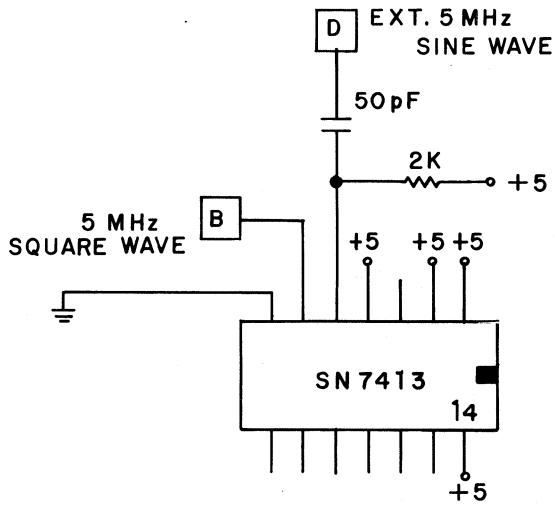
HEX OPEN COLLECTOR BUFFER



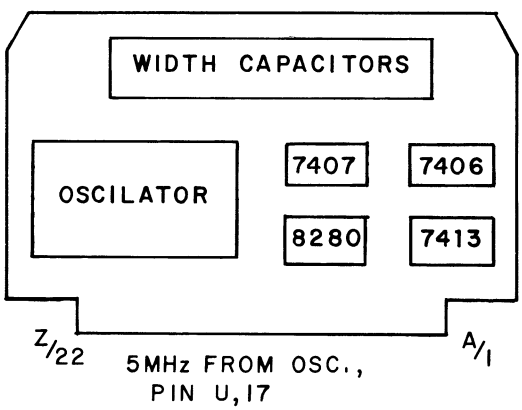
HEX OPEN COLLECTOR INVERTER



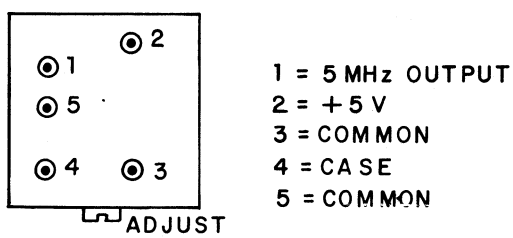
BCD DECADE COUNTER (÷5)



FOUR INPUT NAND SCHMIDT



OSCILLATOR CARD



OSCILLATOR – BOTTOM VIEW

FIG. 5 OSCILLATOR CARD

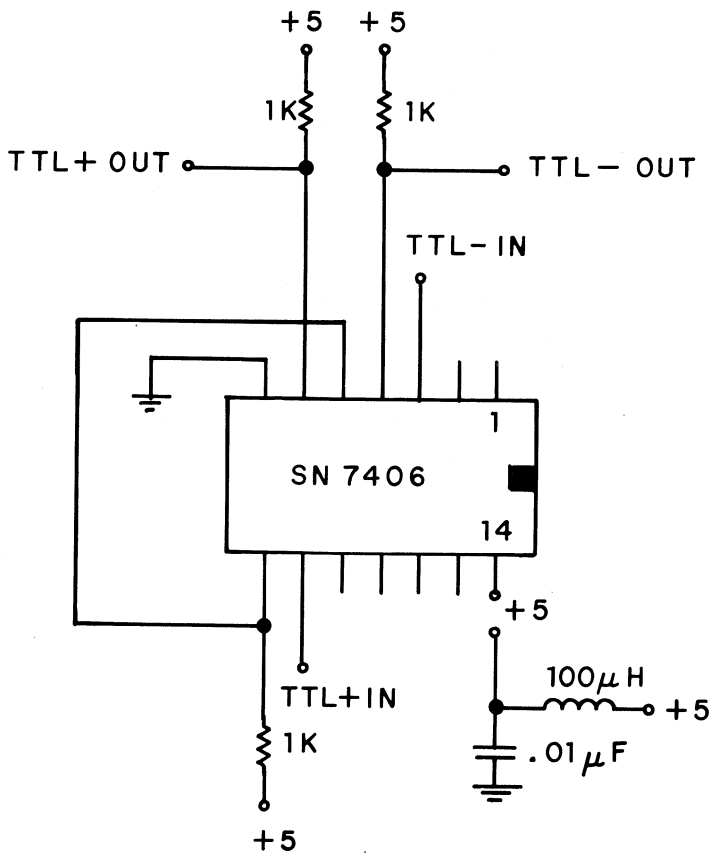


FIG. 6 OUTPUT CARD