NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

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# INTERFEROMETER EXPANSION: (1) AUTOCORRELATION INTERFACE, (2) 16-OUTPUT WORD BUFFERS, AND (3) FREQUENCY SYNTHESIZER DRIVER UNIT

Dwayne Schiebel

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## I. Introduction

This report describes the following three systems:

### 1. Autocorrelator Interface

This interface was designed using 3-C cards and utilizing as much of the present input system as possible. This is located in row H of the option bay.

### 2. 16-Output Word Buffer

This system was built using integrated circuits. It provides 16 output word buffers and two D/A converters to drive a memory scope. This is contained in a card file in the bottom of the memory expansion rack.

### 3. Frequency Synthesizer Driver

This system was built using IC's and discrete components. It is located in the equipment room.

## II. Autocorrelator Interface

This interface is similar to the interface that was installed in the 300-foot and 140-foot computers.

The address that was selected for the A/C input is '0065. To input from the auto-correlator an INA 1065 would be executed. By outputing an OCP 0065 a sync pulse would be generated for the Model III correlator. The correlator will interrupt the computer on Interrupt Line 8; this is interrupt location $37_8$ in the computer.

### A/C Address Decode and OCP (Figure 1)

This interface was tied into the existing interface wherever it was possible. The address is decoded in slot 14, then power amplified in slot 15, and called 0065 + $A/\overline{B}$. The OCP pulse is gated with 0065 + B to trigger a one shot for the A/C sync pulse.

DRL and PIL (Figure 2)

Whenever the A/C is ready to dump data into the computer, it sends an interrupt to the interface (PIL A/C). This will set flip flop B in slot 17 which will bring PIL 08 to ground. This will interrupt the computer and be reset by the priority interrupt system (ACK 08-). The A/C will generate a DRL A/C every time it has a data word on the line. This will set flip flop A in slot 17 and gated with 0065 + A generate a ready indication called DSE 0065-. This signal will generate a DRL- to the computer via the old input interface. When the computer inputs the data an RRL will be sent from the computer signifying that it has taken the data. This signal will reset flip flop A and generate $\overline{\text{RRL A/C}}$ to signal the A/C that the data has been taken.

Input Bus (Figure 3)

The data coming from the A/C is such that ground = "1" and -6 V = 0. This is inverted and then gated with 0065 + A=B to generate IBxxx- which is ORed with the old input system to put data on the input bus of the computer.

All signals going to and from the old input system can be found on the 116 computer drawing "Voltage Input Lines", L.B.D. 01-09.

III. Output Word Buffer

Program Information

Listed below are the new OTA's and their function:

| | |
|---|---|
| OTA 0063 | $F_1$ 16 Bit Absolute Value |
| OTA 0163 | $F_2$ 16 Bit Absolute Value |
| OTA 0263 | $F_3$ 16 Bit Absolute Value |
| OTA 0363 | Bit 1 = Sign $F_1$ |
| | Bit 2 - 11 = $\phi_1$ |
| OTA 0463 | Bit 1 = Sign $F_2$ |
| | Bit 2 - 11 = $\phi_2$ |
| OTA 0563 | Bit 1 = Sign $F_3$ |
| | Bit 2 - 11 = $\phi_3$ |
| OTA 0663 | Frequency Synthesizer |
| | Bits 9 - 16 = 100 MHz and 10 MHz in BCD |
| OTA 0763 | Frequency Synthesizer |
| | 1 MHz, 100 kHz, 10 kHz, 1 kHz in BCD |

| | |
|---|---|
| OTA 1063 | Frequency Synthesizer |
| | 100 Hz, 10 Hz, 1 Hz, .1 Hz in BCD |
| OTA 1163 | Horiz. D/A, Bits 1-10 ± 10 V |
| | Bit 15 = Blanking = 0 |
| | Bit 16 = Erase = 1 |
| OTA 1263 | Vert. D/A, Bits 1-10 ± 10 V |
| OTA 1363 | Spare |
| OTA 1463 | Spare |
| OTA 1563 | Spare |
| OTA 1663 | Spare |
| OTA 1763 | Spare |

Output Buffer Address Decode (Figure 5)

This card level converts the address bus to TTL levels through the use of DM 8820's and decodes the address. Chip 9 on this card decodes the "63" part of the address and after a double inversion this signal (ADxx63-) is level converted back to 3C levels on chip 17. The level converted signal is DRL; this signal being at ground signals the computer that it is ready to take data.

Chips 11 and 12 are binary to octal decoder which decodes bits 7 thru 10 of the address into 16 addresses, AD0063+ thru AD1763+. These signals go to +5 when they are selected.

Master clear and OTP are also level converted and amplified on this card for use by the buffer cards.

Output Bus Level Conversion (Figure 6)

This card level converts the output bus in the same manner as the address bus and is then amplified through the use of 8H90's. This level conversion is such that for a "1" out of the computer (0 volt) the output of the card (OTBxx+A) is at a "1" (+5 volts).

Output Buffer (Figure 7)

This card contains two 16 bit buffers. The buffers consist of four 8281's for each computer word. At this time it must be cautioned that 8281 DC must be used. This is a later version of the 8281. The earlier version had a strobing problem that I will not go into in this report. The buffers are loaded using the parallel inputs and a

strobe. This strobe is generated by gating the decoded address ADxxx + A/B and the OTP pulse. The output of the buffers go through exclusive OR gates. The advantage of exclusive OR gates gives an option of inverting or not inverting the output of the buffers. If an inversion is desired, the other input to the gate should be tied to +5. This selection of inversion or no inversion is made on chips 6, 7 and 8. These programmed plugs must stay with a buffer slot. To replace a buffer card the programmed plugs would have to be removed and reinstalled on the new buffer card. See Table I for a wiring list of the programmed plugs. All buffers are reset when Master Clear is pressed, except the buffer card in slot 8. This is to keep the frequency synthesizer from going to zero when Master Clear is pressed.

D/A Converter (Figure 8)

This card contains two D/A converters to drive the horizontal and vertical axis of the CRT. It also contains two DIP relays to drive the erase and blanking on the CRT. Each relay must make a contact closure to erase or blank.

Termination Card (Figure 9)

This card is used to clamp each line going to the frequency synthesizer driving unit to +5 and ground. This was done to protect the buffer card from any induced spikes caused by driving 100 feet of cable.

## IV. Frequency Synthesizer Driving Unit (Figure 10)

This unit converts 10 groups of 4 BCD lines to 100 lines to drive the frequency synthesizer. Each card consists of a binary to decimal decoder (8251) and 10 drivers. The drivers are selected to a 0 V out of the decoder. This turns on $Q_1$ which turns on $Q_2$ and selects the digit. The frequency synthesizer driver unit is located below the frequency synthesizer in the equipment room. Tables III and IV are connector lists for this unit.

# TABLE I

Tie the following pins together to program the output of the buffers. Pin 14 is +V and pin 7 is Grd.

## Buffer for Slot 5

| Chip 6 | | Chip 7 | | Chip 8 | |
|---|---|---|---|---|---|
| 1 | to 7 | 1 | to 7 | 1 | to 7 |
| 2 | 14 | 2 | 7 | 2 | 7 |
| 3 | 14 | 3 | 7 | 3 | 7 |
| 4 | 14 | 4 | 7 | 4 | 7 |
| 5 | 14 | 8 | 7 | 5 | 7 |
| 6 | 14 | 9 | 7 | 6 | 7 |
| 8 | 14 | 10 | 7 | 8 | 7 |
| 9 | 14 | 11 | to 7 | 9 | 7 |
| 10 | 14 | | | 10 | 7 |
| 11 | 14 | | | 11 | 7 |
| 12 | 7 | | | 12 | 7 |
| 13 | to 7 | | | 13 | to 7 |

## Buffer for Slot 6

| Chip 6 | | Chip 7 | | Chip 8 | |
|---|---|---|---|---|---|
| 1 | to 7 | 1 | to 7 | 1 | to 7 |
| 2 | 7 | 2 | 7 | 2 | 14 |
| 3 | 7 | 3 | 7 | 3 | 14 |
| 4 | 7 | 4 | 14 | 4 | 14 |
| 5 | 7 | 8 | 7 | 5 | 14 |
| 6 | 7 | 9 | 7 | 6 | 14 |
| 8 | 7 | 10 | 7 | 8 | 14 |
| 9 | 7 | 11 | to 7 | 9 | 14 |
| 10 | 7 | | | 10 | 14 |
| 11 | 7 | | | 11 | 14 |
| 12 | 7 | | | 12 | 7 |
| 13 | to 7 | | | 13 | to 7 |

## Buffers for Slots 8, 9, 10 and 11

| Chip 6 | | Chip 7 | | Chip 8 | |
|---|---|---|---|---|---|
| 1 | to 7 | 1 | to 7 | 1 | to 7 |
| 2 | 7 | 2 | 7 | 2 | 7 |
| 3 | 7 | 3 | 7 | 3 | 7 |
| 4 | 7 | 4 | 7 | 4 | 7 |
| 5 | 7 | 8 | 7 | 5 | 7 |
| 6 | 7 | 9 | 7 | 6 | 7 |
| 8 | 7 | 10 | 7 | 8 | 7 |
| 9 | 7 | 11 | to 7 | 9 | 7 |
| 10 | 7 | | | 10 | 7 |
| 11 | 7 | | | 11 | 7 |
| 12 | 7 | | | 12 | 7 |
| 13 | to 7 | | | 13 | to 7 |

TABLE II

Output Buffer Connector List

| J1 | From | Name | J2 | From | Name |
|---|---|---|---|---|---|
| A | 11-6 | $F_1$ MSB | A | 11-28 | $F_2$ MSB |
| B | 11-7 | \| | B | 11-29 | \| |
| C | 11-8 | \| | C | 11-30 | \| |
| D | 11-9 | \| | D | 11-31 | \| |
| E | 11-41 | \| | E | 11-55 | \| |
| F | 11-42 | \| | F | 11-56 | \| |
| H | 11-43 | \| | H | 11-57 | \| |
| J | 11-44 | \| | J | 11-58 | \| |
| K | 11-45 | \| | K | 11-59 | \| |
| L | 11-46 | \| | L | 11-60 | \| |
| M | 11-47 | \| | M | 11-61 | \| |
| N | 11-48 | \| | N | 11-62 | \| |
| P | 11-49 | \| | P | 11-63 | \| |
| R | 11-50 | \| | R | 11-64 | \| |
| S | 11-51 | \| | S | 11-65 | \| |
| T | 11-52 | $F_1$ LSB | T | 11-66 | $F_2$ LSB |
| V | | -6 V | V | | -6 V |
| AA | 10-28 | $F_1$ Sign | AA | 9-6 | $F_2$ Sign |
| BB | 10-29 | $\phi_1$ MSB | BB | 9-7 | $\phi_2$ MSB |
| CC | 10-30 | \| | CC | 9-8 | \| |
| DD | 10-31 | \| | DD | 9-9 | \| |
| EE | 10-55 | \| | EE | 9-41 | \| |
| FF | 10-56 | \| | FF | 9-42 | \| |
| HH | 10-57 | \| | HH | 9-43 | \| |
| JJ | 10-58 | \| | JJ | 9-44 | \| |
| KK | 10-59 | \| | KK | 9-45 | \| |
| LL | 10-60 | \| | LL | 9-46 | \| |
| MM | 10-61 | $\phi_1$ LSB | MM | 9-47 | $\phi_2$ LSB |

Continued --

TABLE II (continued):

| J3 | From | Name |
|---|---|---|
| A | 10-6 | $F_3$ MSB |
| B | 10-7 | \| |
| C | 10-8 | \| |
| D | 10-9 | \| |
| E | 10-41 | \| |
| F | 10-42 | \| |
| H | 10-43 | \| |
| J | 10-44 | \| |
| K | 10-45 | \| |
| L | 10-46 | \| |
| M | 10-47 | \| |
| N | 10-48 | \| |
| P | 10-49 | \| |
| R | 10-50 | \| |
| S | 10-51 | \| |
| T | 10-52 | $F_3$ LSB |
| V | | -6 V |
| AA | 9-28 | $F_3$ Sign |
| BB | 9-29 | $\phi_3$ MSB |
| CC | 9-30 | \| |
| DD | 9-31 | \| |
| EE | 9-55 | \| |
| FF | 9-56 | \| |
| HH | 9-57 | \| |
| JJ | 9-58 | \| |
| KK | 9-59 | \| |
| LL | 9-60 | \| |
| MM | 9-61 | $\phi_3$ LSB |

---

| J8 | (Power) |
|---|---|
| 1 | +5 |
| 2 | +5 |
| 3 | Ground |

---

| J9 | |
|---|---|
| 3 | Blanking Com. |
| 4 | Blanking N.O. |
| 6 | Erase Com. |
| 7 | Erase N.O. |

| J4 | From | Name |
|---|---|---|
| A | 8-45 | 800 MHz |
| B | 8-46 | 400 MHz |
| C | 8-47 | 200 MHz |
| D | 8-48 | 100 MHz |
| E | 8-49 | 80 MHz |
| F | 8-50 | 40 MHz |
| H | 8-51 | 20 MHz |
| J | 8-52 | 10 MHz |
| R | 8-28 | 8 MHz |
| S | 8-29 | 4 MHz |
| T | 8-30 | 2 MHz |
| U | 8-31 | 1 MHz |
| W | 8-55 | 800 kHz |
| X | 8-56 | 400 kHz |
| Y | 8-57 | 200 kHz |
| Z | 8-58 | 100 kHz |
| a | 8-59 | 80 kHz |
| b | 8-60 | 40 kHz |
| c | 8-61 | 20 kHz |
| d | 8-62 | 10 kHz |
| e | 8-63 | 8 kHz |
| f | 8-64 | 4 kHz |
| h | 8-65 | 2 kHz |
| j | 8-66 | 1 kHz |
| p | 6-6 | 800 Hz |
| r | 6-7 | 400 Hz |
| s | 6-8 | 200 Hz |
| t | 6-9 | 100 Hz |
| u | 6-41 | 80 Hz |
| v | 6-42 | 40 Hz |
| w | 6-43 | 20 Hz |
| x | 6-44 | 10 Hz |
| y | 6-45 | 8 Hz |
| z | 6-46 | 4 Hz |
| AA | 6-47 | 2 Hz |
| BB | 6-48 | 1 Hz |
| CC | 6-49 | .8 Hz |
| DD | 6-50 | .4 Hz |
| EE | 6-51 | .2 Hz |
| FF | 6-52 | .1 Hz |
| KK | | Ground |
| LL | | Ground |
| MM | | Ground |
| NN | | Ground |

TABLE III

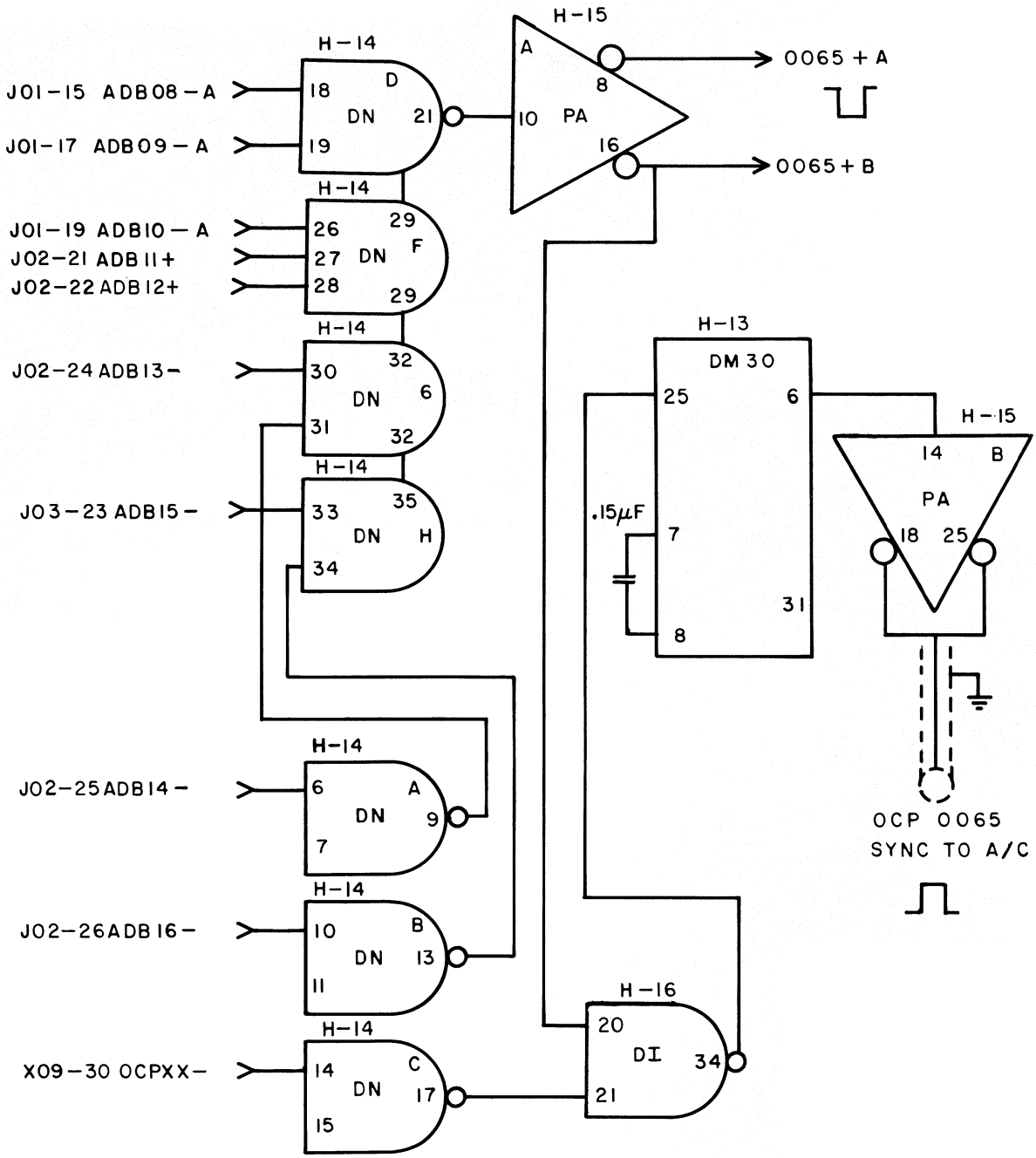
Frequency Synthesizer Driver Unit Connector List

| J1 | To | Name |
|---|---|---|
| A | 16-9 | 800 MHz |
| B | 16-10 | 400 MHz |
| C | 16-13 | 200 MHz |
| D | 16-12 | 100 MHz |
| E | 15-9 | 80 MHz |
| F | 15-10 | 40 MHz |
| H | 15-13 | 20 MHz |
| J | 15-12 | 10 MHz |
| R | 14-9 | 8 MHz |
| S | 14-10 | 4 MHz |
| T | 14-13 | 2 MHz |
| U | 14-12 | 1 MHz |
| W | 13-9 | 800 kHz |
| X | 13-10 | 400 kHz |
| Y | 13-13 | 200 kHz |
| Z | 13-12 | 100 kHz |
| a | 12-9 | 80 kHz |
| b | 12-10 | 40 kHz |
| c | 12-13 | 20 kHz |
| d | 12-12 | 10 kHz |
| e | 11-9 | 8 kHz |
| f | 11-10 | 4 kHz |
| h | 11-13 | 2 kHz |
| j | 11-12 | 1 kHz |
| p | 10-9 | 800 Hz |
| r | 10-10 | 400 Hz |
| s | 10-13 | 200 Hz |
| t | 10-12 | 100 Hz |
| u | 9-9 | 80 Hz |
| v | 9-10 | 40 Hz |
| w | 9-13 | 20 Hz |
| x | 9-12 | 10 Hz |
| y | 8-9 | 8 Hz |
| z | 8-10 | 4 Hz |
| AA | 8-13 | 2 Hz |
| BB | 8-12 | 1 Hz |
| CC | 7-9 | .8 Hz |
| DD | 7-10 | .4 Hz |
| EE | 7-13 | .2 Hz |
| FF | 7-12 | .1 Hz |
| KK | | Ground |
| LL | | Ground |
| MM | | Ground |
| NN | | Ground |

TABLE IV

Frequency Synthesizer Driver Unit Cable List

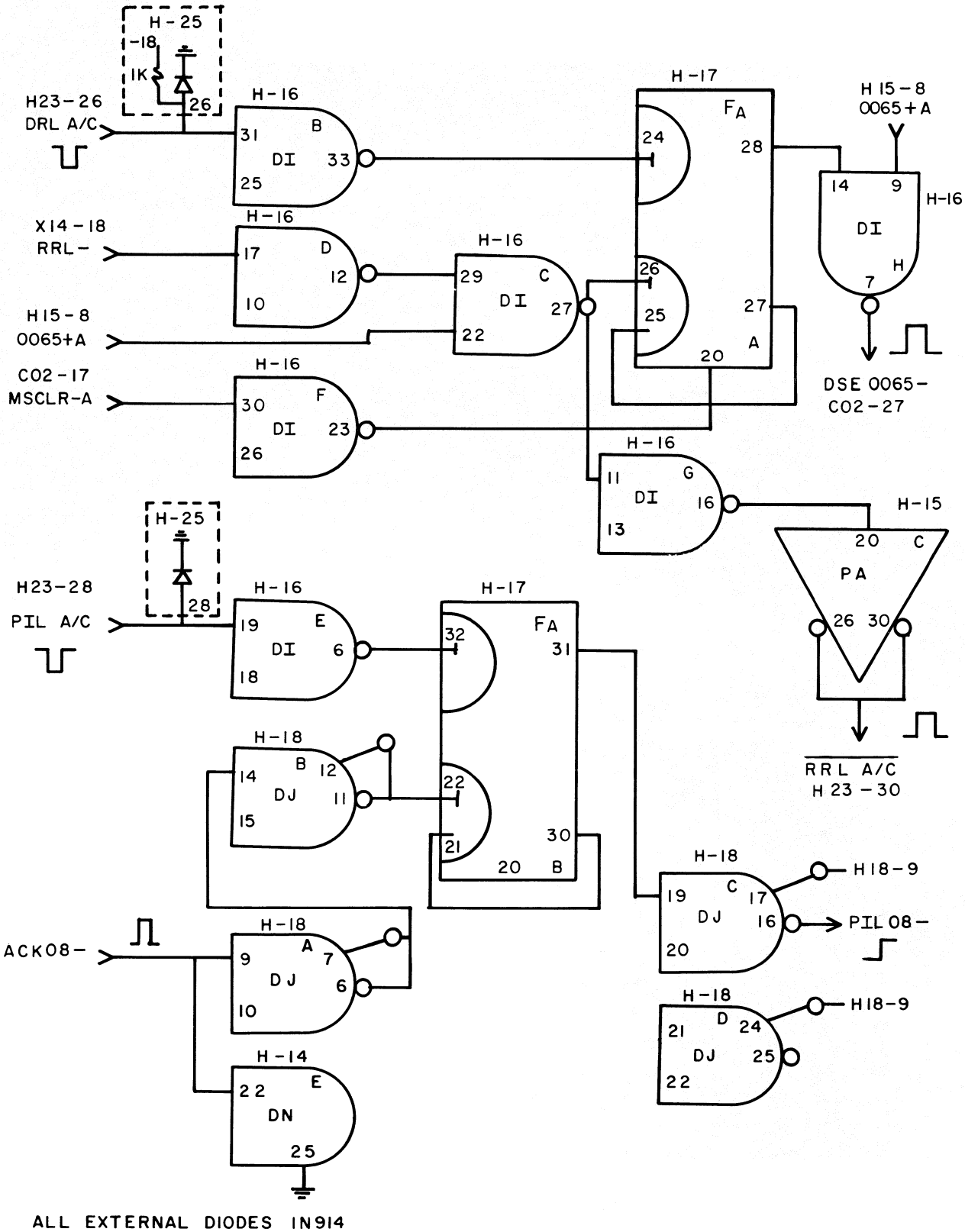
| P7 | From | P7 | From | P7 | From | P7 | From | P8 | From | P8 | From | P8 | From | P8 | From | P9 | From | P9 | From | Select |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 22 | 15-8 | 35 | 14-8 | 47 | 13-8 | 10 | 12-8 | 22 | 11-8 | 35 | 10-8 | 47 | 9-8 | 10 | 8-8 | 22 | 7-8 | 9 |
| | | 21 | 15-7 | 34 | 14-7 | 46 | 13-7 | 9 | 12-7 | 21 | 11-7 | 34 | 10-7 | 46 | 9-7 | 9 | 8-7 | 21 | 7-7 | 8 |
| | | 20 | 15-6 | 33 | 14-6 | 45 | 13-6 | 8 | 12-6 | 20 | 11-6 | 33 | 10-6 | 45 | 9-6 | 8 | 8-6 | 20 | 7-6 | 7 |
| | | 19 | 15-5 | 32 | 14-5 | 44 | 13-5 | 7 | 12-5 | 19 | 11-5 | 32 | 10-5 | 44 | 9-5 | 7 | 8-5 | 19 | 7-5 | 6 |
| | | 18 | 15-4 | 31 | 14-4 | 43 | 13-4 | 6 | 12-4 | 18 | 11-4 | 31 | 10-4 | 43 | 9-4 | 6 | 8-4 | 18 | 7-4 | 5 |
| 5 | 16-14 | 17 | 15-14 | 30 | 14-14 | 42 | 13-14 | 5 | 12-14 | 17 | 11-14 | 30 | 10-14 | 42 | 9-14 | 5 | 8-14 | 17 | 7-14 | 4 |
| 4 | 16-15 | 16 | 15-15 | 29 | 14-15 | 41 | 13-15 | 4 | 12-15 | 16 | 11-15 | 29 | 10-15 | 41 | 9-15 | 4 | 8-15 | 16 | 7-15 | 3 |
| 3 | 16-16 | 15 | 15-16 | 28 | 14-16 | 40 | 13-16 | 3 | 12-16 | 15 | 11-16 | 28 | 10-16 | 40 | 9-16 | 3 | 8-16 | 15 | 7-16 | 2 |
| 2 | 16-17 | 14 | 15-17 | 27 | 14-17 | 39 | 13-17 | 2 | 12-17 | 14 | 11-17 | 27 | 10-17 | 39 | 9-17 | 2 | 8-17 | 14 | 7-17 | 1 |
| 1 | 16-18 | 13 | 15-18 | 26 | 14-18 | 38 | 13-18 | 1 | 12-18 | 13 | 11-18 | 26 | 10-18 | 38 | 9-18 | 1 | 8-18 | 13 | 7-18 | 0 |
| $10^8$ | | $10^7$ | | $10^6$ | | $10^5$ | | $10^4$ | | $10^3$ | | $10^2$ | | $10^1$ | | $10^0$ | | $10^{-1}$ | | |




| ROW H | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DM30 | DA30 | PA30 | DI30 | FA30 | DJ30 | SI69 | SI79 | SI69 | SI79 | CONN. | | SPECAL |

ADDRESS DECODE AND OCP

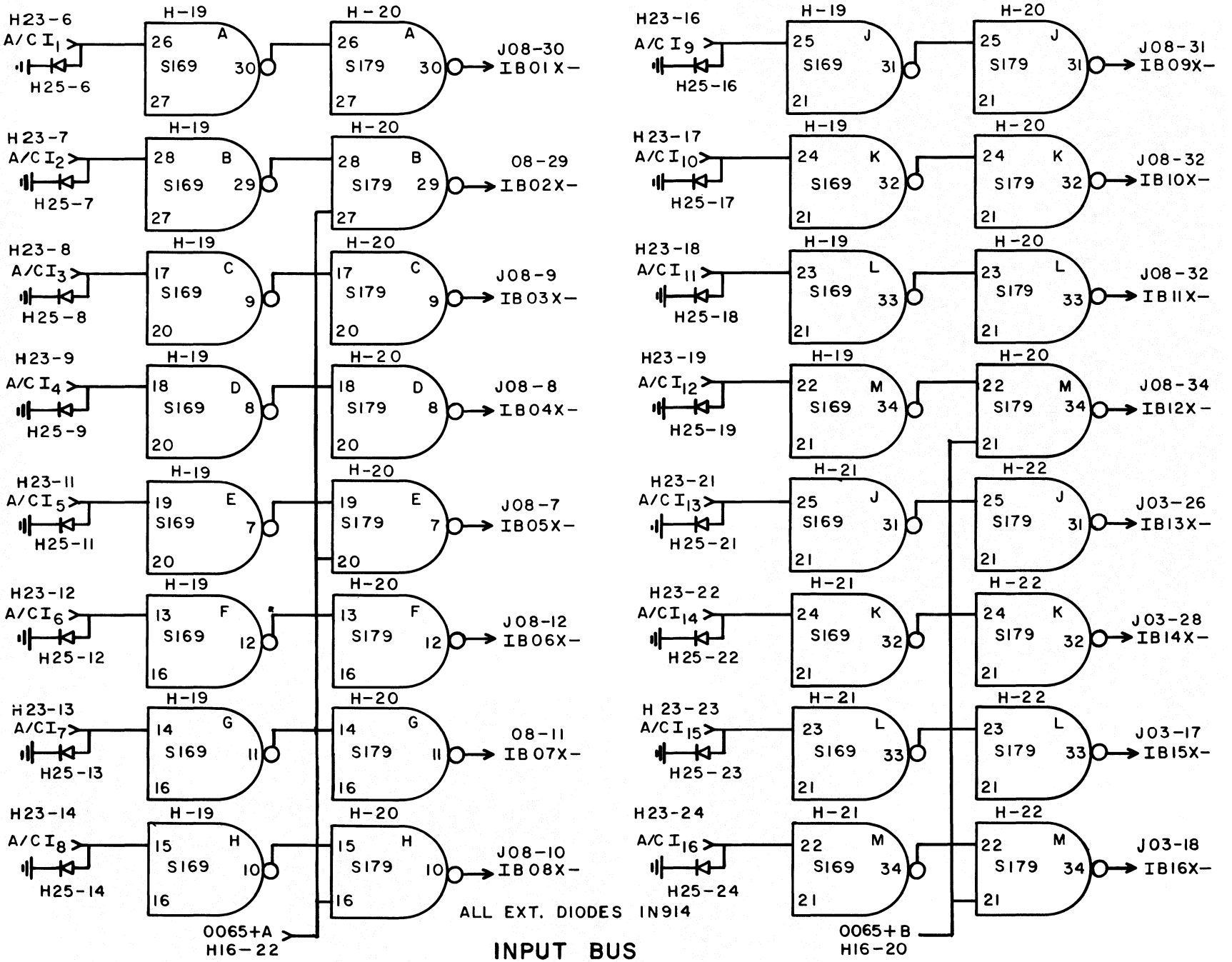
FIG. 1




ALL EXTERNAL DIODES IN914

DRL & PIL

FIG. 2




INPUT BUS

FIG. 3

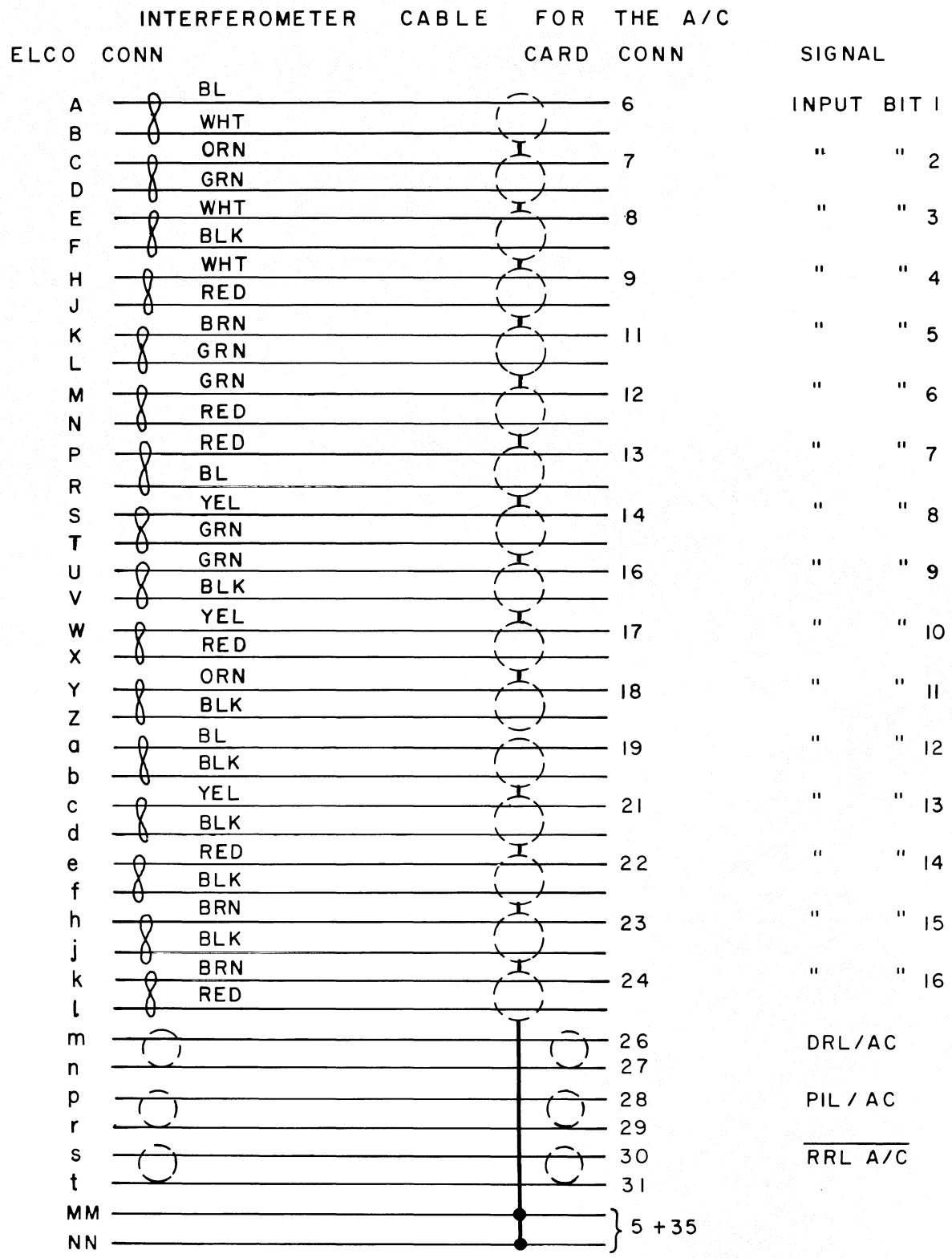
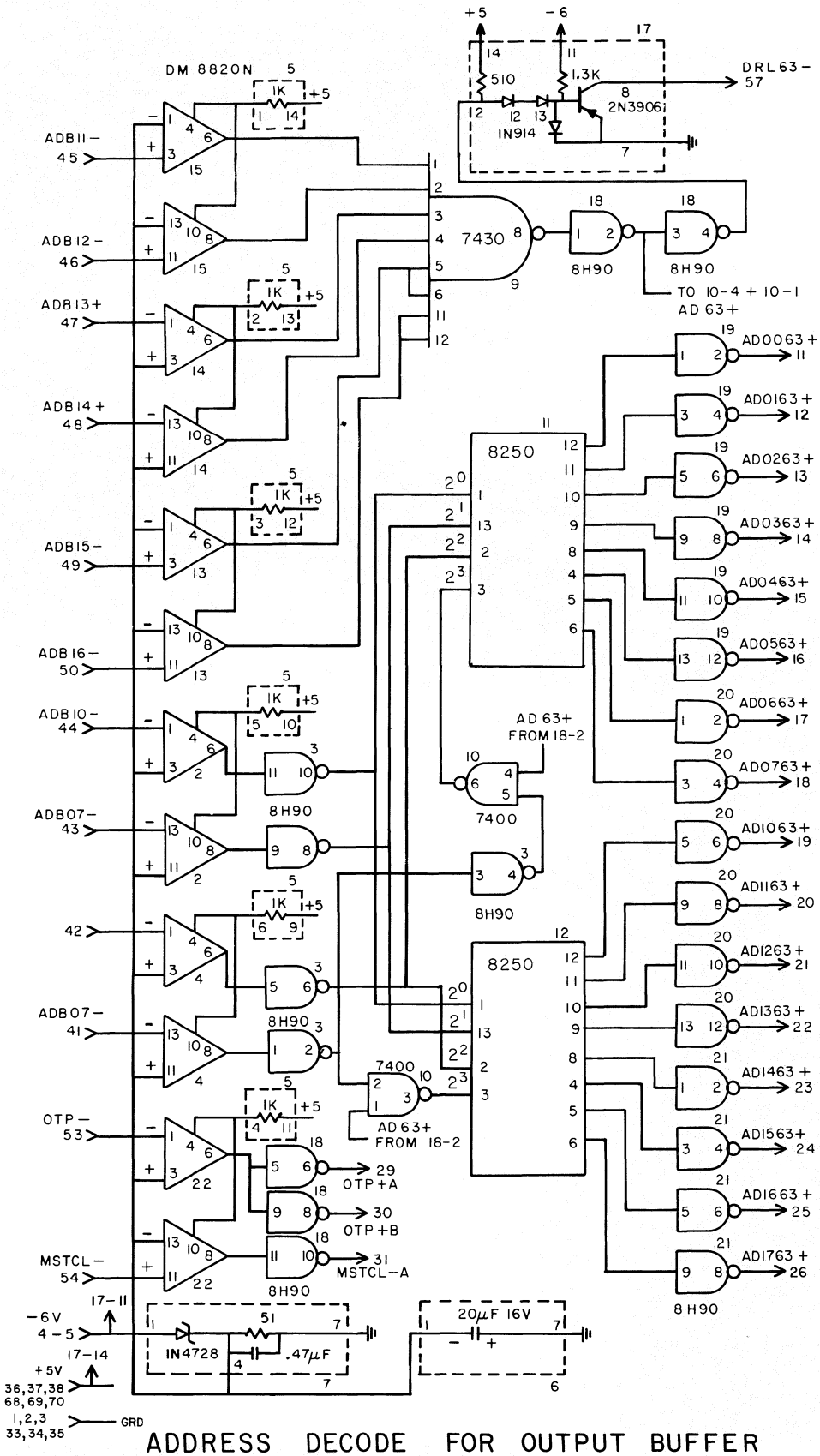
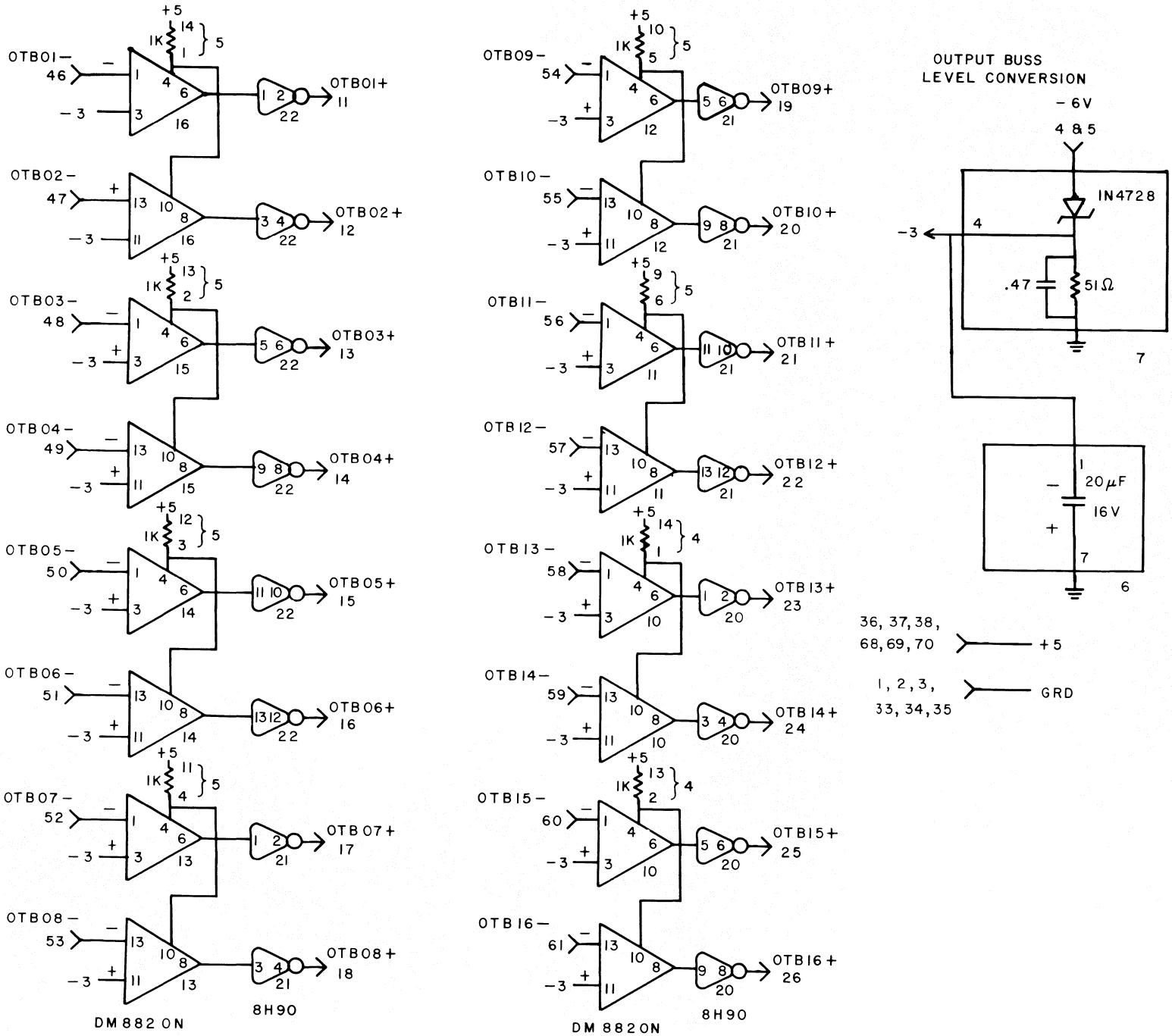

INTERFEROMETER CABLE FOR THE A/C
ELCO CONN
CARD CONN
SIGNAL
A BL
B WHT
6
INPUT BIT 1
C ORN
D GRN
7
" " 2
E WHT
F BLK
8
" " 3
H WHT
J RED
9
" " 4
K BRN
L GRN
11
" " 5
M GRN
N RED
12
" " 6
P RED
R BL
13
" " 7
S YEL
T GRN
14
" " 8
U GRN
V BLK
16
" " 9
W YEL
X RED
17
" " 10
Y ORN
Z BLK
18
" " 11
a BL
b BLK
19
" " 12
c YEL
d BLK
21
" " 13
e RED
f BLK
22
" " 14
h BRN
j BLK
23
" " 15
k BRN
l RED
24
" " 16
m
n
26
27
DRL/AC
p
r
28
29
PIL/AC
s
t
30
31
RRL A/C
MM
NN
5 +35
56 PIN ELCO
WITH
PROTECTED PINS

FIG. 4



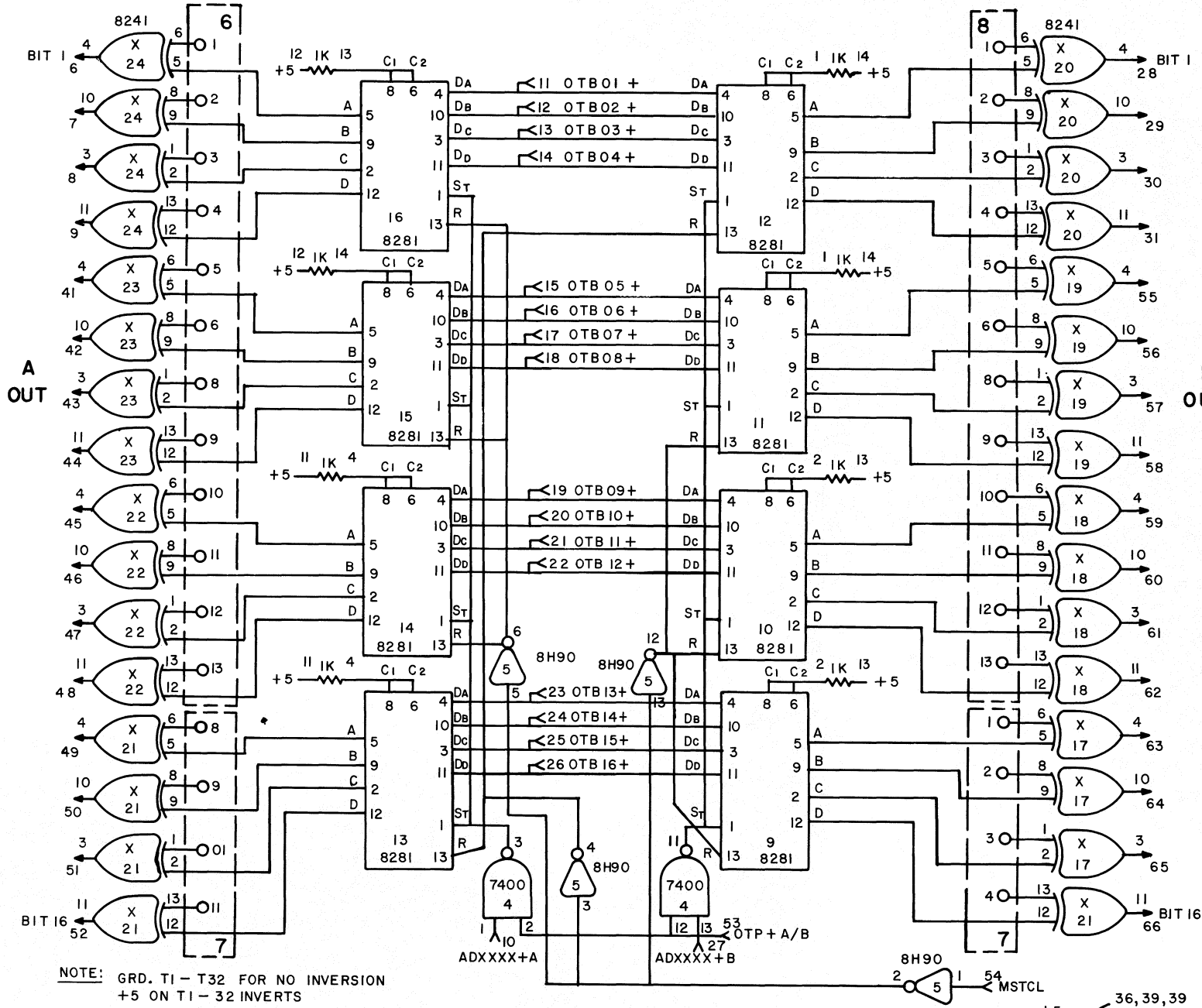

ADDRESS DECODE FOR OUTPUT BUFFER

FIG. 5



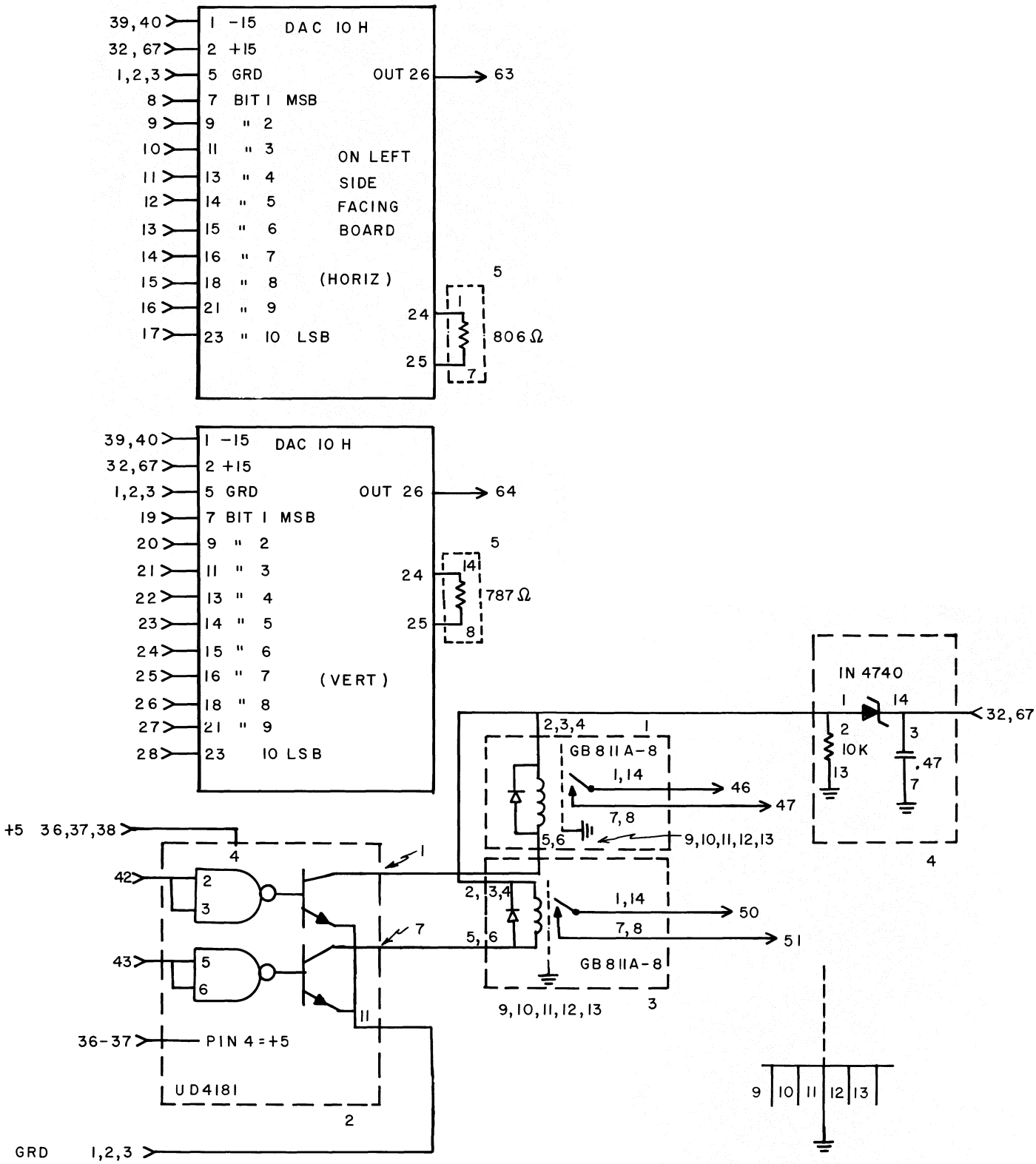

OUTPUT BUS LEVEL CONVERSION

FIG. 6



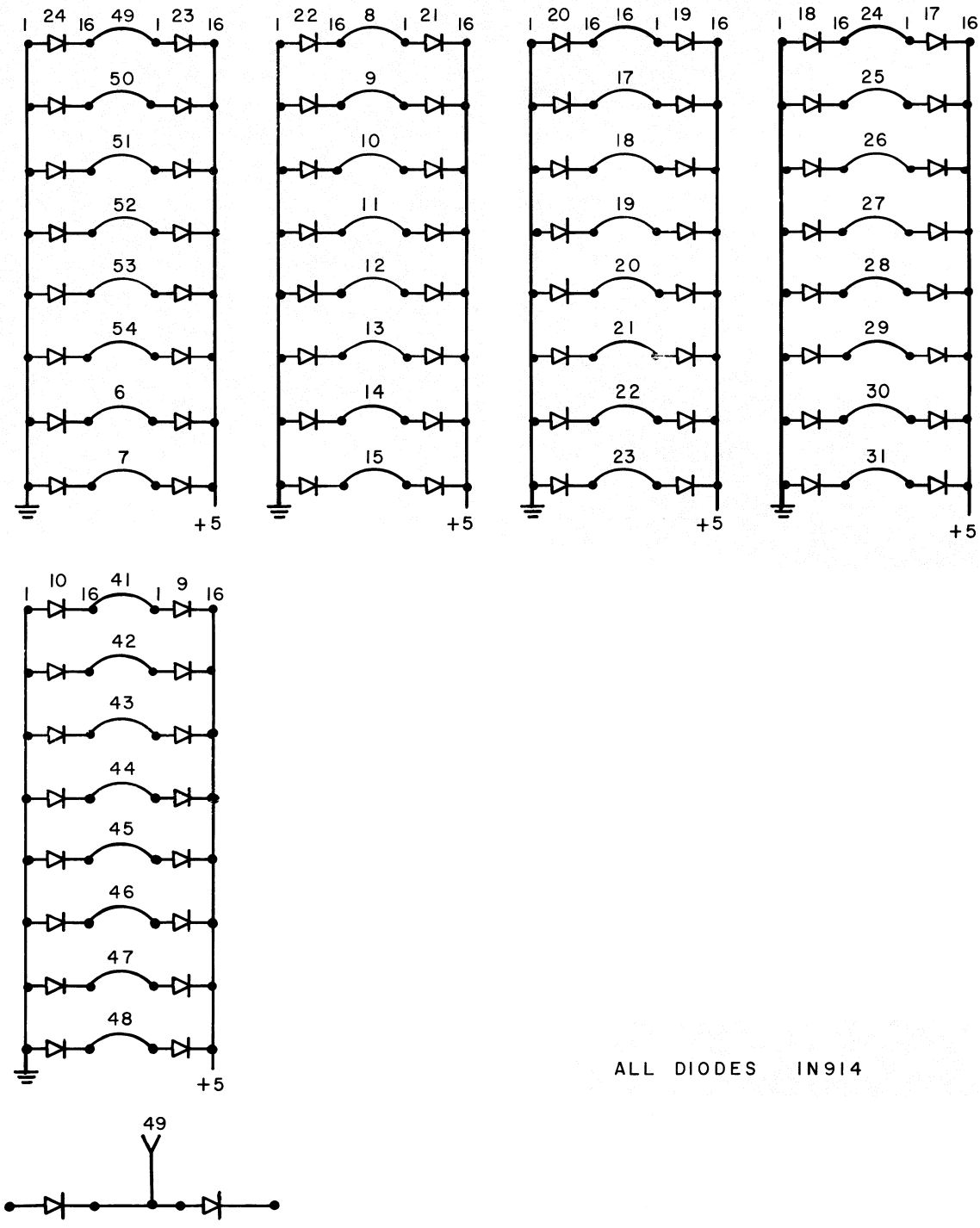

OUTPUT BUFFER

FIG. 7


39,40
1 -15
DAC 10 H
32, 67
2 +15
1,2,3
5 GRD
OUT 26
63
8
7 BIT 1 MSB
9
9 " 2
10
11 " 3
ON LEFT
11
13 " 4
SIDE
12
14 " 5
FACING
13
15 " 6
BOARD
14
16 " 7
15
18 " 8
(HORIZ)
16
21 " 9
24
806 Ω
17
23 " 10 LSB
25
5
1
7
39,40
1 -15
DAC 10 H
32,67
2 +15
1,2,3
5 GRD
OUT 26
64
19
7 BIT 1 MSB
20
9 " 2
21
11 " 3
24
787 Ω
22
13 " 4
23
14 " 5
25
24
15 " 6
25
16 " 7
(VERT)
26
18 " 8
27
21 " 9
28
23 10 LSB
5
14
8
IN 4740
1
14
32,67
2
10K
13
3
.47
7
4
2,3,4
1
GB 811A-8
1,14
46
47
7,8
5,6
9,10,11,12,13
+5
36,37,38
4
42
2
3
1
7
43
5
6
11
36-37
PIN 4 = +5
UD4181
2
GRD
1,2,3
2,3,4
1,14
50
7,8
51
5,6
GB 811A-8
9,10,11,12,13
3
9
10
11
12
13

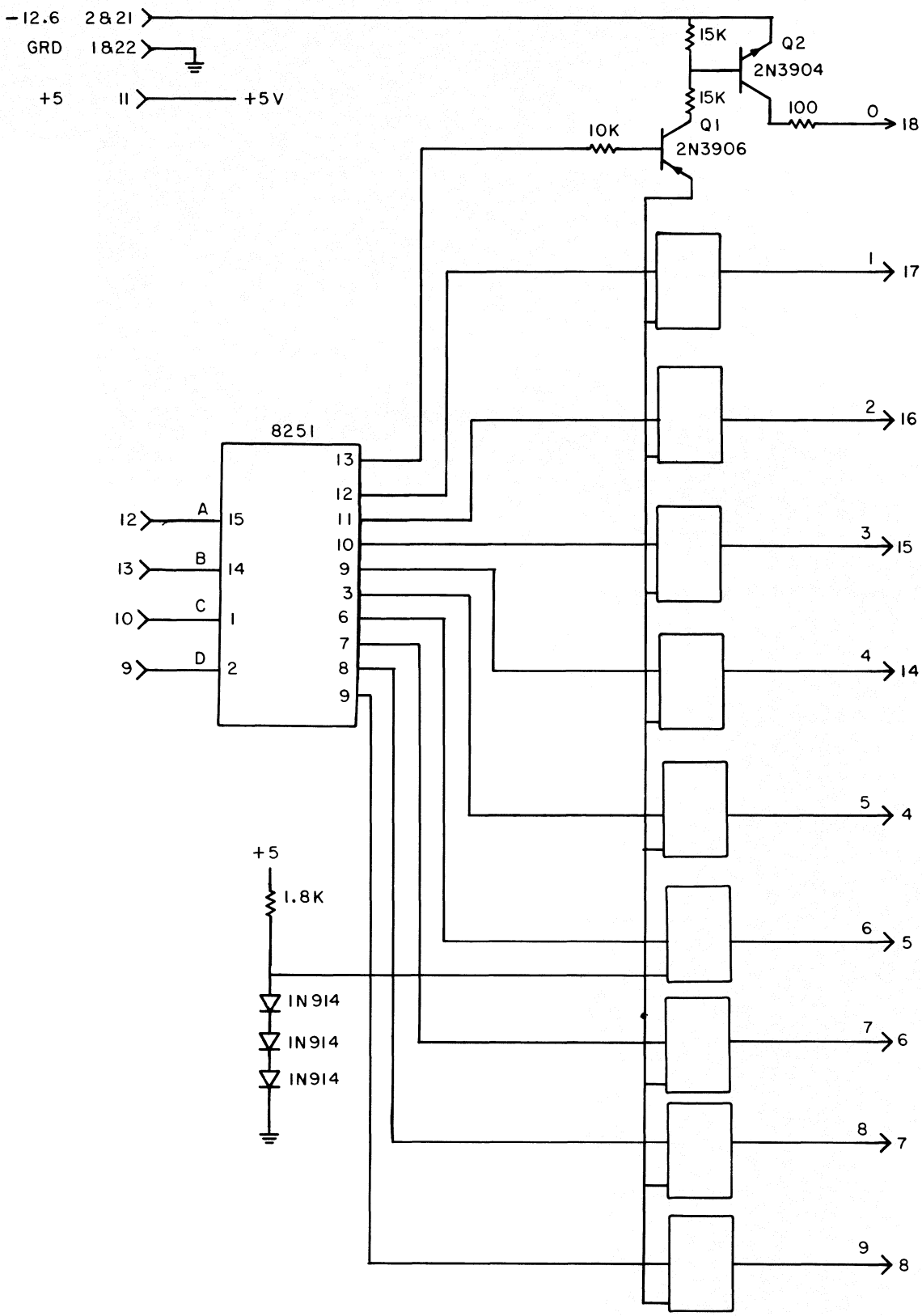
D/A CARD

FIG. 8



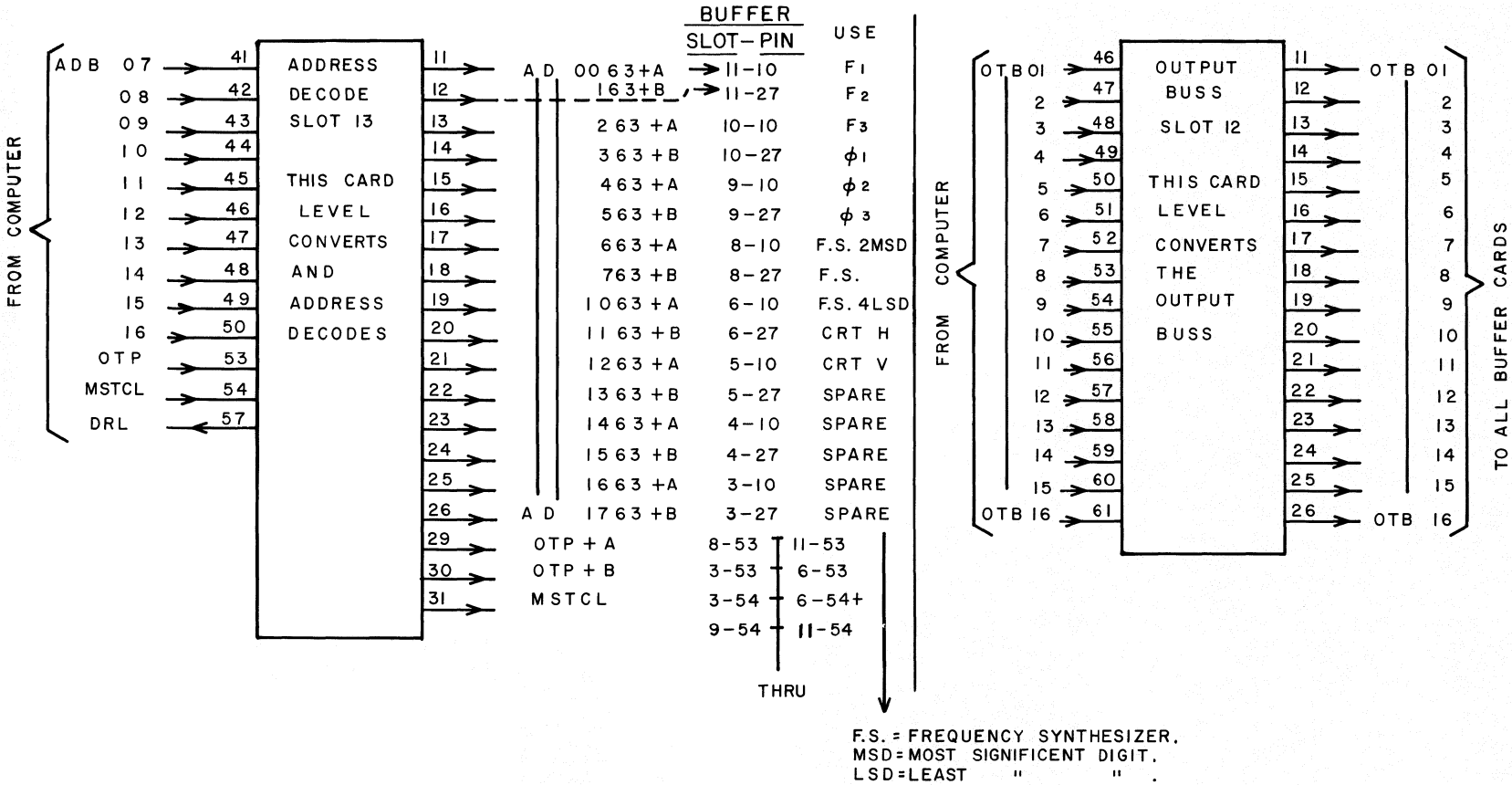

TERMINATION CARD

FIG. 9



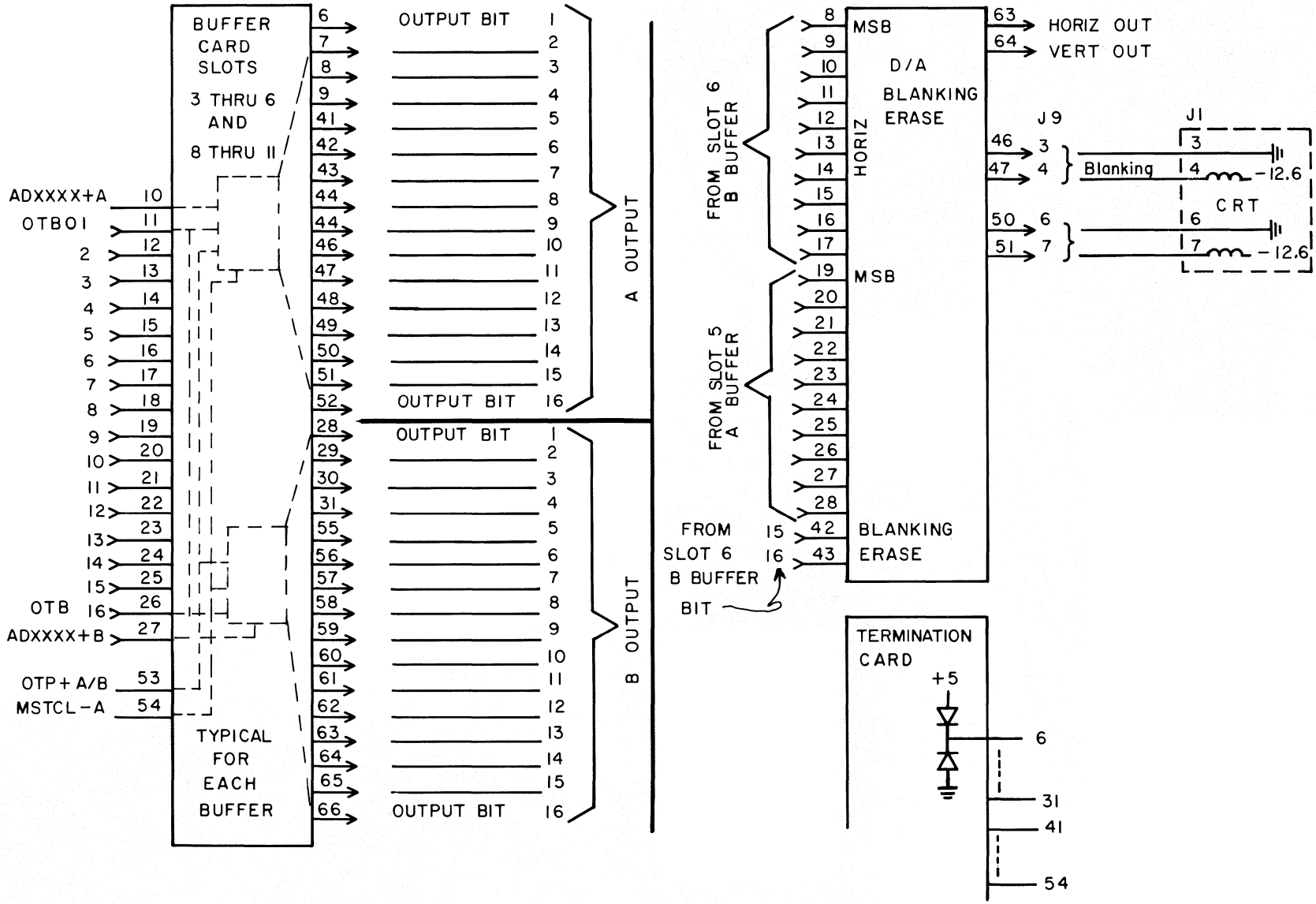

FREQUENCY SYNTH. DRIVER

FIG. 10




ADDRESS DECODE OUTPUT BUSS

FIG. 11




BUFFER D/A TERMINATION

FIG. 12