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A LOBE ROTATOR SYSTEM FOR RADIO INTERFEROMETERS

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1. Abstract

A lobe rotator system, comprising a crystal oscillator coupled to a high-speed synchronous counter producing a reference phase output, herein designated REF, coupled to one input of a phase comparator and, further, a low frequency synthesizer connected by suitable means to a presettable low speed counter producing a variable phase and frequency with respect to REF, coupled to the other input of the phase comparator producing a phase and frequency modulated output, herein designated LR, has been developed and built at NRAO for radio interferometers. The lobe rotator may be employed to reduce the interference fringe rate to zero by proper programming and by heterodyning the REF and LR with the two corresponding element local oscillators with suitable filtering means. The NRAO system produces one REF and three LR signals, herein designated LR-1, LR-2 and LR-3, for interferometers of up to four elements.

2. Introduction

The following report is intended to completely describe the NRAO 4-element interferometer digital lobe rotation system. All information that is required to build, use, and repair the system is contained herein.

The lobe rotator output is defined as follows:[1]

$$e_k = \sqrt{2} \sin [2\pi t (f_c \pm f_k) + \phi_k + \Theta_k + f_k \tau_k]$$

where

k = 0, 1, 2, or 3.

t = 0 when a reset signal is applied (every 10 seconds from the sidereal clock).

f_c = Carrier frequency, 30 MHz or 10 kHz.

f_k = Fringe frequency as specified by a 16-bit binary word from the DDP-116 computer with $f_0 \equiv 0$. The $\pm$ preceding f_k is selected by an additional bit.

Θ_k = An arbitrary phase angle which is stable to within 0.1 degree over several hours.

ϕ_k = Phase relative to e_0 when $t = 0$. It is variable from 0 to 360° in $360°/2^{10} \approx 0.36°$ steps as specified by a 10-bit computer output word with $\phi_0 \equiv 0$.

τ_k = Constant group delay in each channel. This can be any value of 0 to 3 milliseconds. It must be measured and stable to within 30 microseconds.

3. Specification

k = number of interferometer elements = a maximum of 4.

f_k = 0 to 4.88278 Hz, specified by a 16-bit binary word with the most significant bit = 2.44141 Hz and the least significant bit = .0000372529 Hz.

ϕ_k = 0 to 359.648 degrees specified by a 10-bit binary word with the most significant bit = 180 degrees and the least significant bit = .352 degree.

REF output is greater than 2 volts peak to peak, AC coupled into 50 ohm load with rise and fall times approximately 300 nanoseconds. f_0 = 10 kHz stable to within 4 parts in 10^6.

LR output is the same as REF except $f_0 = f \pm f_k$.

All control inputs from the computer are TTL compatible positive logic definitions. Twenty-seven bits are required to define a lobe rotator channel output.

Update strobe is accepted by a differential line receiver with minimum signal differential of 2 volts and common mode of ± 15 volts. Maximum update strobe rate is 1000 Hz but is usually at a 0.1 Hz rate. A minimum rate of 0.04 Hz is allowable before 1/2 least significant bit of phase error results between updates.

System power consumption is about 20 watts.

The computer control instructions are as follows:

OTA 63	f_1	16 bit absolute value, MSB = bit 1
OTA 163	f_2	" " " " "
OTA 263	f_3	" " " " "
OTA 363	f_1	Sign = bit 1
	ϕ_1	10 bits, MSB = bit 2, LSB = bit 11
OTA 463	f_2	Sign = bit 1
	ϕ_2	10 bits, MSB = bit 2, LSB = bit 11
OTA 563	f_3	Sign = bit 1
	ϕ_3	10 bits, MSB = bit 2, LSB = bit 11

4. Physical Description

The radio interferometer lobe rotator system described herein has been designed and constructed by relying entirely upon digital technology. By virtue of this, a system of well-defined behavior has resulted. Digital integrated circuits (TTL) in 14 and 16 pin dual, in-line packages and some discrete circuits have been incorporated, yielding a system that is small and reliable. All circuits are on six Douglas type 11-DE-5 plug-in circuit cards containing up to 36 integrated circuits each. There are only 3 different cards so that only 3 spare cards are required for easy replacement, allowing short down times. Ten card slots are provided, slots 1-6 containing active cards, slot 7 containing the card extender, and slots 7-10 containing the spares. The system power is provided by an Acopian model 5R10 supply capable of 5 volts at 10 amps. The system requires only 2.7 amps. However, the supply also powers some computer output interface requiring about 4 amps at present. A rear mounted connector and ammeter is provided for output interface. On the front panel, a voltmeter and ammeter are provided for monitoring the power to the lobe rotator digital circuit. A power on/off switch is provided to control the lobe rotator power only, the AC power being applied to the 10 amp supply at all times as well as output power to the computer interface. Refer to section 10 for pictures of the system.

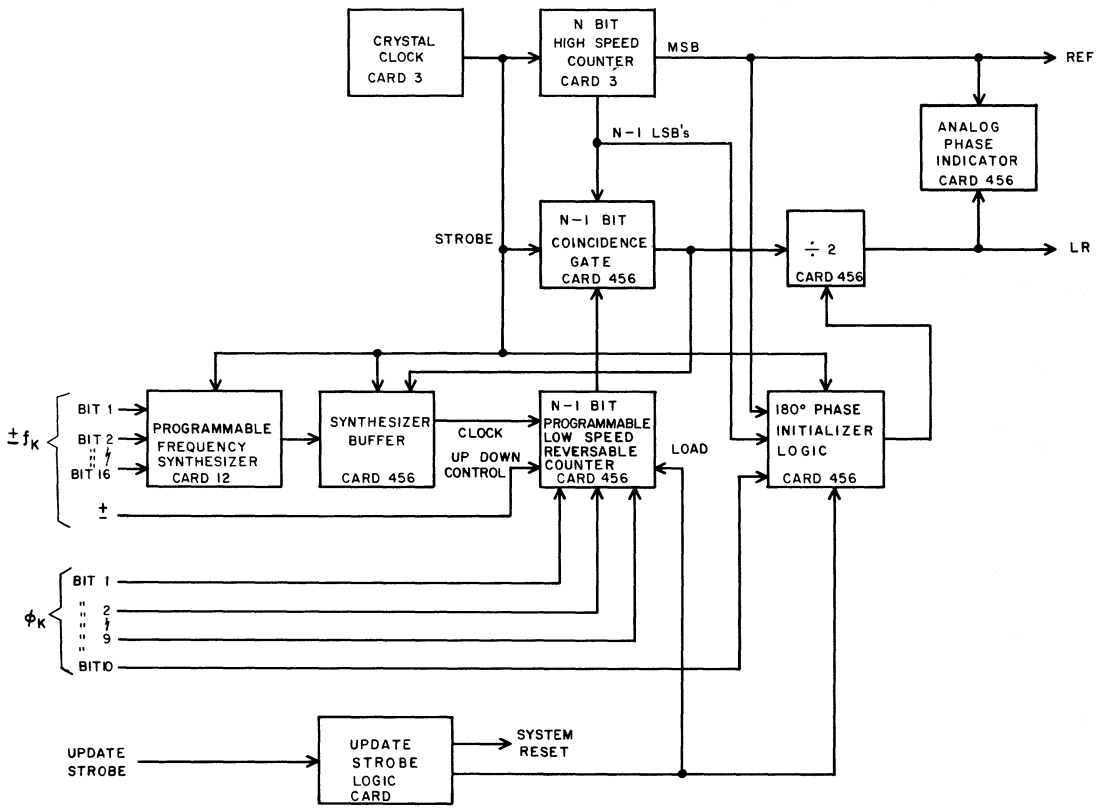
The front panel is divided into five sections, namely, power monitor and control, REF generator and test points, and three variable output sections (LR-1, LR-2, and LR-3), the lobe rotator monitor phase meters and test points. These phase meters indicate in two ranges that are switch-selectable from the front panel, low range from 0 to 360 degrees and high range from 0 to 16 π radians. The indicated phase is the corresponding LR output relative to the REF output. Four front panel BNC connectors in parallel with four corresponding rear panel connectors provide the 50 ohm outputs of the lobe rotator system. These outputs are connected via coax cables to the respective crystal filters and local oscillators of the interferometer system. Refer to section 13 for a list of the front panel test points.

Three cables connecting the lobe rotator to the computer provide the 26-bit control word inputs to the three variable LR output generators.

The 10 1/2 x 19 inch lobe rotator chassis is rack mounted on chassis slides for easy servicing in the DDP-116 computer memory expansion bay.

5. Short Electronic Description

The digital portion of the lobe rotator system is shown in Figure 1. The block diagram presents the REF channel and only one of the three LR channels, the other two being identical to the one shown. Each block represents a subsystem and will be discussed individually. The actual card location of each block is shown in each block, i.e., card 12, card 3, card 456, etc. Card 12 functions in slot 1 or 2 and is the same for both. The other two cards follow a similar scheme.



LOBE ROTATOR BLOCK DIAGRAM
FIG. 1

As can be seen in Figure 1, a crystal clock on card 3 provides the timing control of several functions. The 10-bit high-speed counter, common to all three LR generators, counts the clock transitions of the 10.24 MHz oscillator. The MSB of this counter provides the REF output after suitable buffering.

The low speed counter clocks at the frequency output of the 16-bit programmable synthesizer. The count direction of the counter is controlled by the ± input. The clock rate is set by the 16-bit control word f_k. The synthesizer buffer prohibits the low speed counter from clocking during coincidence of phase of the two counter subsystems. In fact, the synthesizer buffer stores the count command from the synthesizer until just after coincidence and then issues a clock pulse to the low speed counter. The low speed counter may be preset to any count upon receipt of an update strobe via the update strobe logic circuit. This preset count represents phase with a resolution of 9 binary bits, the tenth bit of resolution being provided by the set or reset command of $\div$ 2 output flip-flop as issued by the 180° phase initialization logic at update strobe time. This phase initialization is determined by the state of bit 10 of ϕ_k and the command is issued when the high speed counter is in the all 1's state, thereby maintaining the proper time relationship of the phase command.

The coincidence gate compares the phase of the two counters and issues a clock pulse to the output flip-flop at every coincidence of the 9 LSB's of the counters. This output flip-flop provides the LR output after suitable buffering.

The analog phase indicator coupled with a meter provides an indication of the phase that LR leads REF.

As can be appreciated here we have a digital phase and frequency modulation system. Behold, the difference between phase and frequency modulation is apparent from a practical example. The phase modulation port is ϕ_k while the frequency modulation port is f_k. However, the frequency modulation index for this system is very narrow at 0.0005. This may be altered by modifying the ratio of the clock rates of the two counters. Changing either the frequency range of the synthesizer or the clock rate of the high-speed counter will affect this end.

The next section, number 6, is difficult to read and may be skipped if only a general understanding of the system is desired. Section 6 is intended to lead the reader through all of the circuitry in a reasonable order.

6. Long Electronic Description

All schematics referred to in this section may be found in section 11. Much information is contained within these drawings. For example, referring to schematic No. 1, which is a diagram of card 3, we notice that "chip" S (located in the lower left corner of the drawing) is a hex inverter type 8H90. Three of the inverters are tied in parallel via input pins 9, 11, and 13; and output pins 8, 10, and 12, which are also tied to card 3, edge connector output pin 14; the inverse update strobe A ($\overline{\text{UDSA}}$), which is a negative going pulse. Similar notation is used throughout the schematic diagrams. The signal designation lists, section 12, defines the signal names. No timing diagrams are presented (only occasional active pulse symbols throughout the drawings) since it is felt that personal desire of organizations differ and each will probably draw their own, if necessary, with aid of the presented active edge and pulse symbols.

The 10.24 MHz crystal oscillator (upper left corner of schematic 1) provides the clock to the $\div$ 64 counter V and U connected to gates S and T, thus producing two phase clock pulses CLSYN (clock synthesizer) and RASYN and RBSYN (reset synthesizer output pulse flip-flops) to the frequency synthesizer on cards 1 and 2. The crystal oscillator output is also connected to gates W and JJ that function as a super short pulse one shot producing the SCOMP signal (strobe compare) and clock to the high-speed counter system. The SCOMP is a negative going pulse of about 30 percent duty factor, allowing about 30 percent time for the phase comparators of cards 456 to make decisions.

Schematic 2 presents a more detailed sketch of the counter. The counter is synchronous in that all flip-flops are clocked at the same instant. High speed Raytheon III circuits are employed. There are 3 bits per basic high speed counter block as shown in schematic 3. With three basic blocks of 3 bits each and one additional bit, we have a 10-bit high-speed counter producing one 10-bit varying phase input to the phase comparators of cards 456. The unbuffered REF output at card 3, pin 15, is produced from this counter. The unbuffered REF is connected to the analog phase indicators and also to test points for testing purposes. (See test point lists, section 13.) Referring back to schematic 2, it is seen that the 50 ohm buffered REF at pin 16 (schematic 9) is also produced from this counter. This signal is available at two BNC connectors on the front and rear panels.

The 10 second differential update strobe signal (from the sidereal clock repeater) present at B5 and B6 (also pins 5 and 6) are connected to the update strobe logic producing the system reset and update pulses which are used to strobe in the new ϕ_k and also reset the frequency synthesizer output dividers to zero.

Schematic 4 presents the update strobe logic block in greater detail. The 10 sec UDS is available to the input of the differential line receiver MM. The input 1 millisecond low pass is provided to reject noise caused by relay response skew as well as other sources. The 5.1 K resistor corrects for differential offset in the amplifier. Chip KK improves rise time for triggering one shot CC, providing both 1 microsecond senses of the UDS.

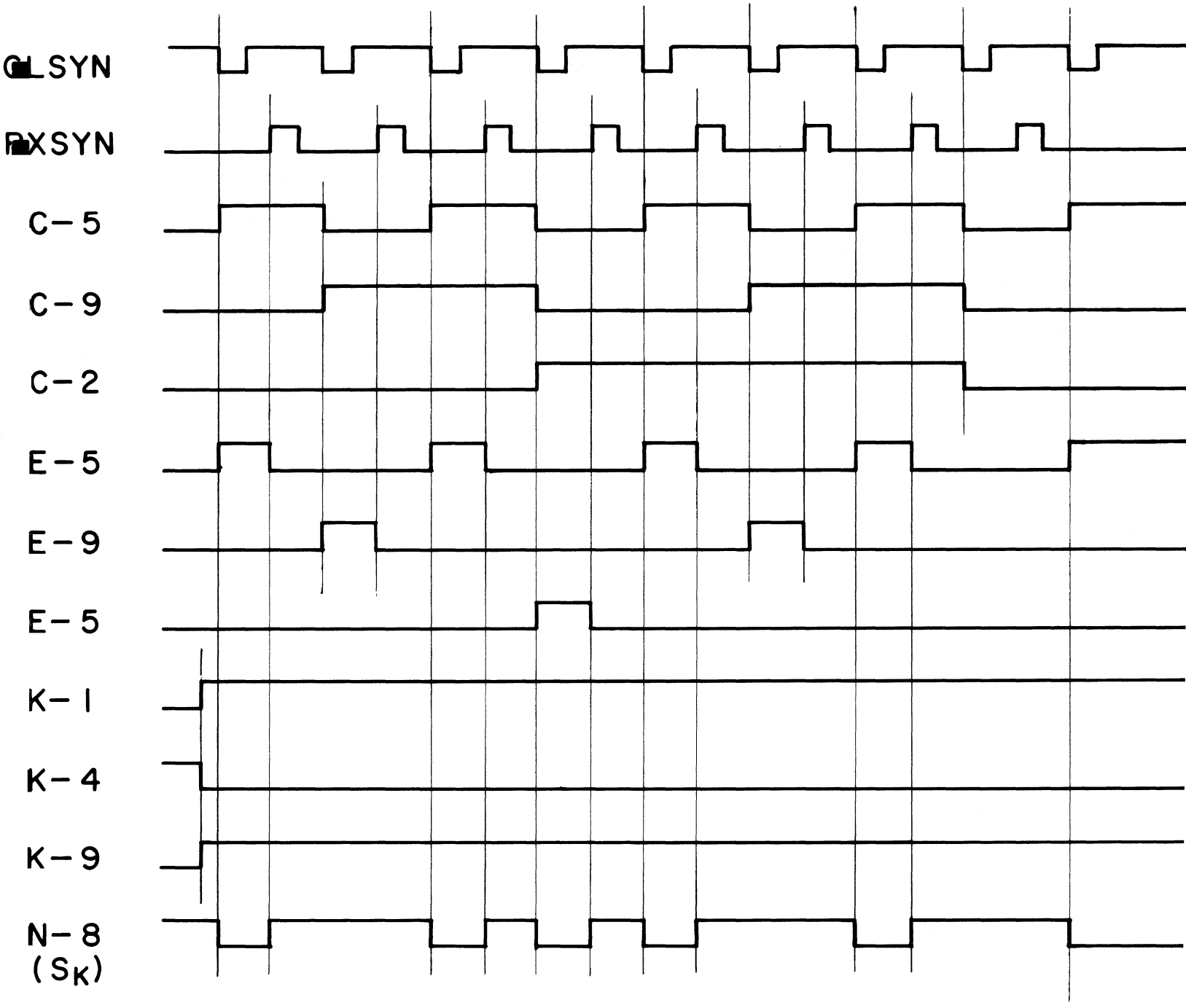
The synthesizer output buffers of card 3 (schematic 2) are presented in greater detail in schematic 5. Pulse trains are present at S_A from card 1 and S_B from card 2 when an all 1's f_k is present from the computer. S_A, representing the 8 MSB's of the synthesizer, is 64 times higher in pulse frequency than S_B, which is the pulse frequency representing the 8 LSB's of the frequency synthesizer.

S_A and S_B pulse frequencies are then summed in NOR gate FF. The nomenclature follows from left to right, top to bottom in schematic 5, for synthesizer buffers 1, 2, and 3. So, for synthesizer 3 the NOR gate is X. This same format designation is used throughout the descriptions. The summed output pulses are divided by 32 in GG and NN, thus producing a square wave output to synchronizer flip-flops AA. These flip-flops store the clock command from the synthesizer and clock the low-speed counter (on card 456 from pin T, synth out, card 3) upon receipt of a coin pulse from card 456. The UDS and $\overline{\text{UDS}}$ inputs, pins 7 and 8, are reset pulses to the synthesizer buffers.

The digital frequency synthesizer cards 12 presented on schematic 6 are clocked and reset by two phase clock pulses CLSYN and RXSYN at a frequency of 160 kHz. The following timing diagram represents the operation of the first three bits of the synthesizer.

The counter C clocks on negative edges while the flip-flops E and F clock on plus edges and reset with RXSYN pulses. Pulses are produced at the flip-flop E and F outputs following plus transitions of the counter C. The pulses out of each flip-flop E and F are not coincident, and when allowed to pass gates K are summed by gate N, thus being present at S_X. With the select lines K-1, K-4, and K-9 programmed according to the timing diagram, the summing gate N adds pulse frequencies of only E-5 and F-5, as shown in the timing diagram for N-8.

TIMING DIAGRAM REPRESENTS THE OPERATION OF THE FIRST THREE BITS OF THE SYNTHESIZER



THE COUNTER C CLOCKS ON NEGATIVE EDGES WHILE THE FLIP-FLOPS E & F CLOCK ON PLUS

Schematic 7 shows the circuits of card 456. In the top-left corner is shown the phase indicator circuit. It is shown in more detail in schematic 8 where gates CC and DD function as a DPDT switch, selecting direct signal paths from inverters CC and DD or paths through ÷ 8 circuits KK and LL, providing the meter range selection logic. The meter high range is 8 times the low range. The outputs CC-13 and DD-13 trigger the set-reset flip-flop Z via one shots X and delay line W. This forms an analog phase comparator indicating relative phase of LR leading REF. A low pass filter FF smooths the flip-flop output forming a pulse width to voltage converter connected to the panel meter. The pulse width is a function of phase of the LR and REF signals.

The outputs of the synthesizer buffers, card 3, are present at cards 4, 5, and 6 on schematic 7 at pin 13 (SYN). Gates B select the up/down count mode of the low speed counter J, K, and L. This is a programmable counter that may be preset to a selected phase by proper input of ϕ_k at pins 3-12, and $\overline{\text{UDSA}}$ pin 14 which loads the phase ϕ_k into the counter. The counter phase is then compared with the phase of the high-speed counter via pins C through N by coincidence gates formed by exclusive-OR gates R, S, and T connected to NOR gates U, further connected to NAND gate V. The strobe compare pulse $\overline{\text{SCOMP}}$ enables this 9-bit coincidence gate at the proper time, eliminating false coincidence conditions. The output of coincidence gate V-8 is connected via delay line M to toggle output flip-flop C-5 with every coincidence pulse. The output of this flop-flop C-5 is connected to the 50 ohm output buffer shown in schematic 9.

In schematic 7, gates H, P, D, and flip-flop C-12 form the 180 degree phase initialization circuit. Gates P and H-3 detect all 1's of the high-speed counter enabling gates D when flip-flop C-12 is set by the update strobe. One of the gates D is selected by the condition of the MSB of ϕ_k, and thus flip-flop C-5 is loaded with the correct phase at the instant when the high-speed counter is all 1's.

7. In Case of Difficulty

It should be possible to repair the lobe rotator digital system in quick time since a "systems" approach in packaging has been employed. The rack contains only 10 card slots with slots 1-6 being active cards, 7 being the card extender, and 8, 9, and 10 are spare cards. Only three spares are required since some redundancy is present. To repair the system it is only necessary to determine which card is defective by some means such as "card snatching".

A more logical approach to troubleshooting the system is to become familiar with the function of each of the three different cards and six slots. A tabulation of this follows.

Card Functions

Quan.	Function	Card No.
2	Frequency synthesizer	12
1	High speed counter, reference generator, oscillator, logic control	3
3	Phase register, low speed counter, phase comparator, LR generator	456

Card Slot Functions

Slot	Function	Output Affected
1.	Most significant half of frequency synthesizers	LR-1, LR-2 LR-3
2.	Least significant half of frequency synthesizers	LR-1, LR-2 LR-3
3.	Master control, oscillator, reference generator	LR-1, LR-2 LR-3, REF
4.	Phase counter and comparator, phase indicator	LR-1
5.	Phase counter and comparator, phase indicator	LR-2
6.	Phase counter and comparator, phase indicator	LR-3
7-10.	Spares	Spares

The following sections are also useful in troubleshooting the system:

Section	Subject
10	Pictures
11	Schematics
12	Signal Designation Lists
13	Test Point Lists
14	Connector Pin Breakout Lists
15	Wiring Lists

A test jig is available to manually control the lobe rotator system without the computer. It comprises of a box of switches and cable connector for connection to the appropriate computer interface control input on the rear of the chassis. The test jig has 16 switches providing manual control of the 16-bit f_k number while another set of 10 switches provide manual control of the 10-bit ϕ_k number. An additional switch provides control of the $\pm f_k$ function while another switch controls the update strobe which must be activated after a change in control setting is made to actually initiate the change. The update strobe switch requires a -6 volt bias that is normally supplied by the computer through the data cables. If all three data cables are removed, then to insure normal operation of the update strobe switch, the -6 bias must be applied to pin V with pin Z being ground through one of the unused control cable connectors.

It may be desirable to test the lobe rotator system using the computer with an observing program. If it is desirable to use a special test program, then the following may be helpful.

Lobe Rotator Computer Control Instructions

OTA 63	f_1
OTA 163	f_2
OTA 263	f_3
OTA 363	ϕ_1 and sign f_1
OTA 463	ϕ_2 and sign f_2
OTA 563	ϕ_3 and sign f_3

16 bit word defines absolute value of f. MSB = Bit 1

LSB = Bit 16

Bit 1 = sign f.

Bit 2 = MSB ϕ_k.

Bit 11 = LSB ϕ_k.

ϕ_k = 10 bit word.

Test Program

```
100   LDA   200
  1   OTA    63
  2   JMP   101
  3   OTA   163
  4   JMP   103
  5   OTA   263
  6   JMP   105
  7   LDA   202
110   OTA   363
  1   JMP   110
  2   OTA   463
  3   JMP   112
  4   OTA   463
  5   JMP   114
  6   HLT
  7   LDA   201
120   OTA    63
  1   JMP   120
  2   OTA   163
  3   JMP   122
  4   OTA   263
  5   JMP   124
  6   LDA   203
  7   OTA   363
130   JMP   127
  1   OTA   463
  2   JMP   131
  3   OTA   563
  4   JMP   133
  5   HLT
  6   JMP   100
  7
```

200	f_k	Control word A
201	f_k	Control word B
202	ϕ_k	Control word A
203	ϕ_k	Control word B

For example:

200	5 2 5 2	$f_k \approx 1/16$ Hz
201	2 5 2 5	$f_k \approx 1/12$ Hz
202	1 2 5 2 4 0	$+f_k$, $\phi_k \approx 115°$
203	5 2 5 0 0	$-f_k$, $\phi_k \approx 240°$

Program repeats every other time that start button is depressed.

For improved strip chart recorder display these values for locations 200 and 201 may be used:

200	4000
201	3400

Using the above test program with the test control words loaded in locations in 200 through 203 and starting at location 100, the first time the start button is pressed, all lobe rotators will be loaded with the control words 200 and 202. While observing the analog phase indicators, an immediate change in f_k will be noted for normal operation but it is necessary to wait until after the 9-0 second transition of the sidereal clock to note a change in phase to about 115°. Pushing the computer start button a second time will cause another change; this time f_k reverses and counts down as indicated by decreasing phase of the indicators. After the 9-0 second clock transition the phase of 240° is initialized. Other values may be stored in locations 200 through 203 for variations in tests.

There are two other ways to observe the changing phase outputs of the lobe rotators for testing. With the REF output connected to one trace of a two trace oscilloscope and an LR output connected to the other trace, synchronizing the scope on trace 1 will yield stationary 10 kHz square wave on trace 1 while trace 2 will be increasing phase (LR leads REF) when movement is to the left and decreasing phase when movement is to the right. The scope may be connected directly to the front panel BNC connectors to observe the 50 ohm outputs going to the local oscillators and filters or connected to corresponding test points 4 to observe the unbuffered wave forms offering steeper rise/fall times.

Another method of observing the lobe rotator output update is to employ a strip chart recorder connected to the analog phase indicator (test point 5) where a ramp wave form will be seen with discontinuities at UDS times. The period of the ramp is a function of f_k while instantaneous voltage out is a function of ϕ_k.

A list of test points may be found in section 12 for additional tests.

8. Conclusion

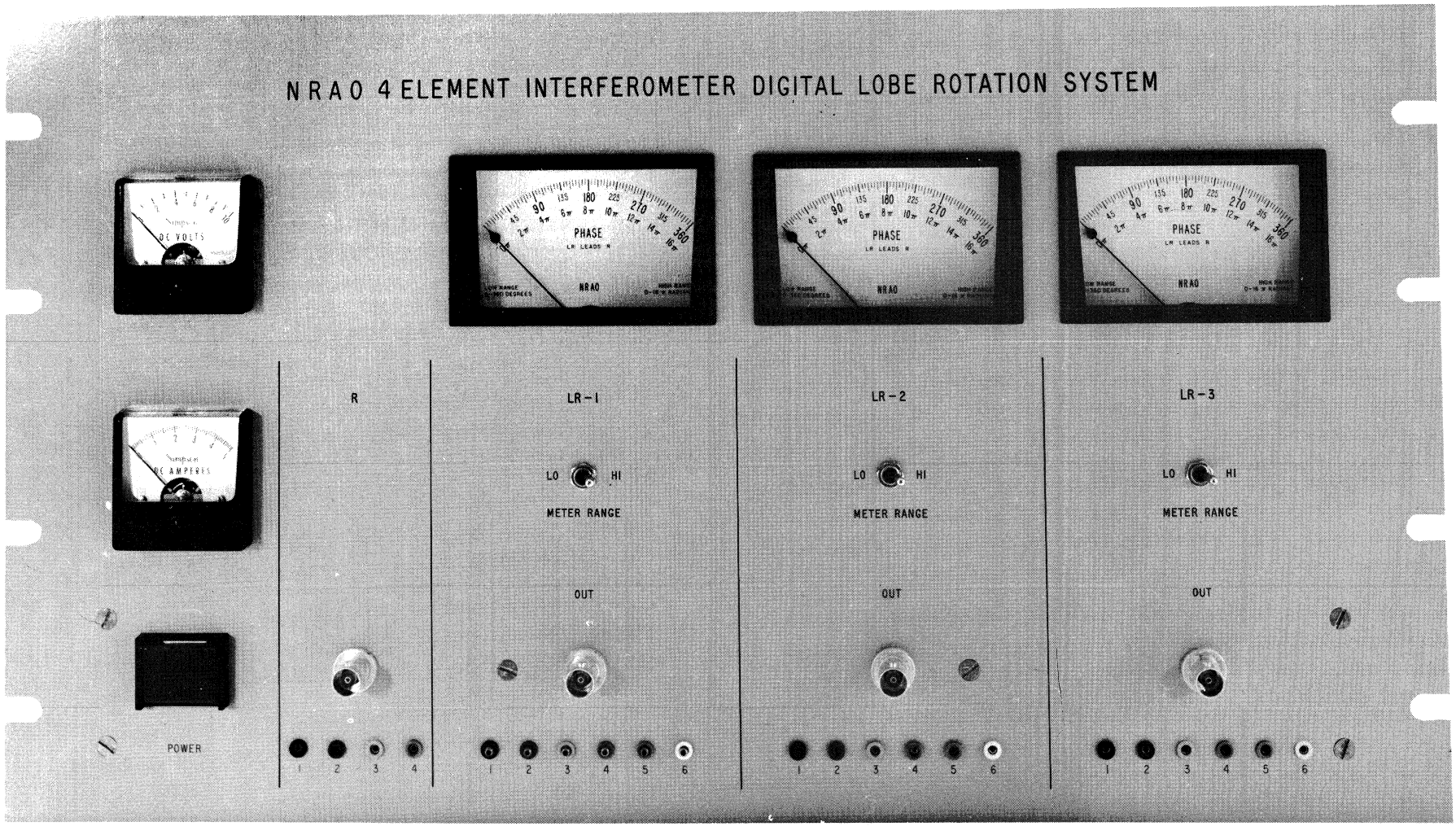
The lobe rotation system described herein is expected to give very reliable service due to the package technique and types of circuits employed. The system was tested with satisfactory performance using a 15 MHz crystal oscillator representing a 150 percent speed margin over the normal 10.24 MHz oscillator. It was found to be important to bring out ground connections from both ends of the card edge connectors, thereby allowing the shortest distances for ground systems. The system speed could probably be doubled with an improved packaging scheme, i.e., locating all circuits on one card, especially those of cards 3, 4, 5 and 6. Also, the coincidence gate limits at about 20 MHz due to skew response in the groups or exclusive OR gates.

Although the basic lobe rotator is digital, we have not completely escaped analog circuits in this design. There are the necessary analog filters and mixing circuits in the local oscillator system, thus allowing some types of analog errors.

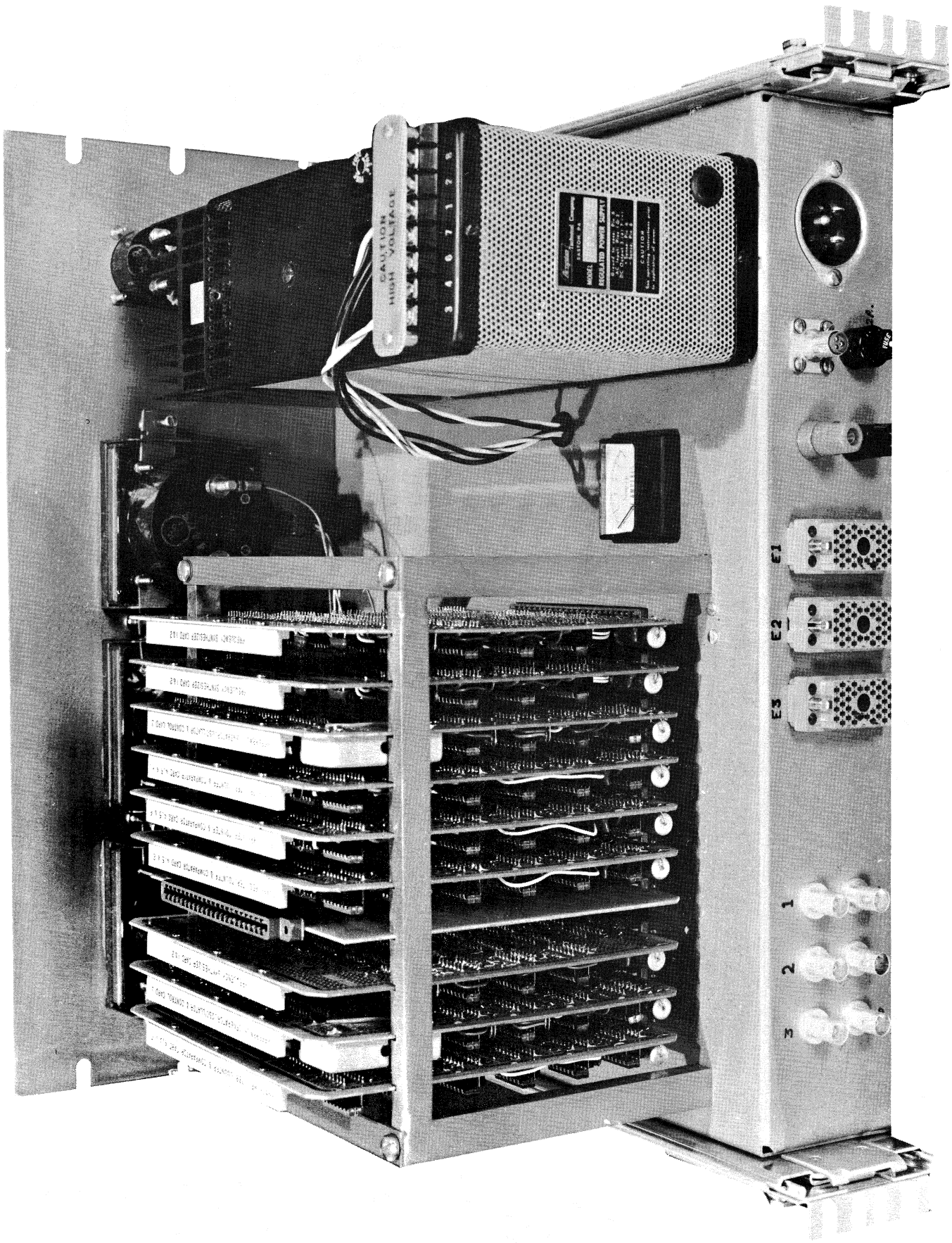
Finally, if the lobe rotator system is operated in a 3-element interferometer system, some advantage is gained by connecting the three local oscillators to the three LR outputs allowing the REF to go unused, some advantages being improved fringe rate (f_k) resolution and range of 9.76566 Hz.

9. Credits

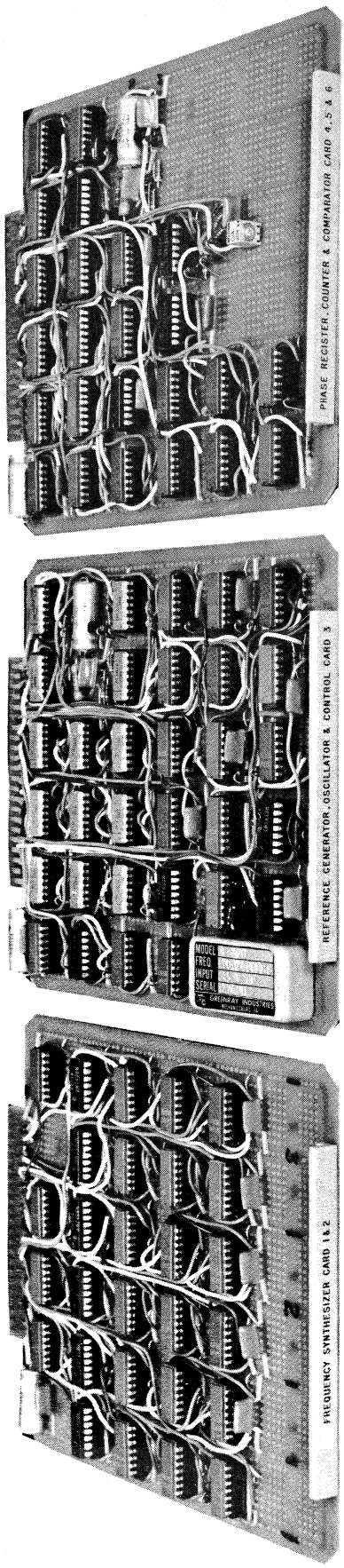
1. S. Weinreb, letter dated February 17, 1970 defining the lobe rotator system.
2. B. G. Clark, suggestion of system principle of operation.
3. R. Hallman, electronic and mechanical design.
4. J. Turner, electronic construction.
5. M. Barkley, mechanical construction.



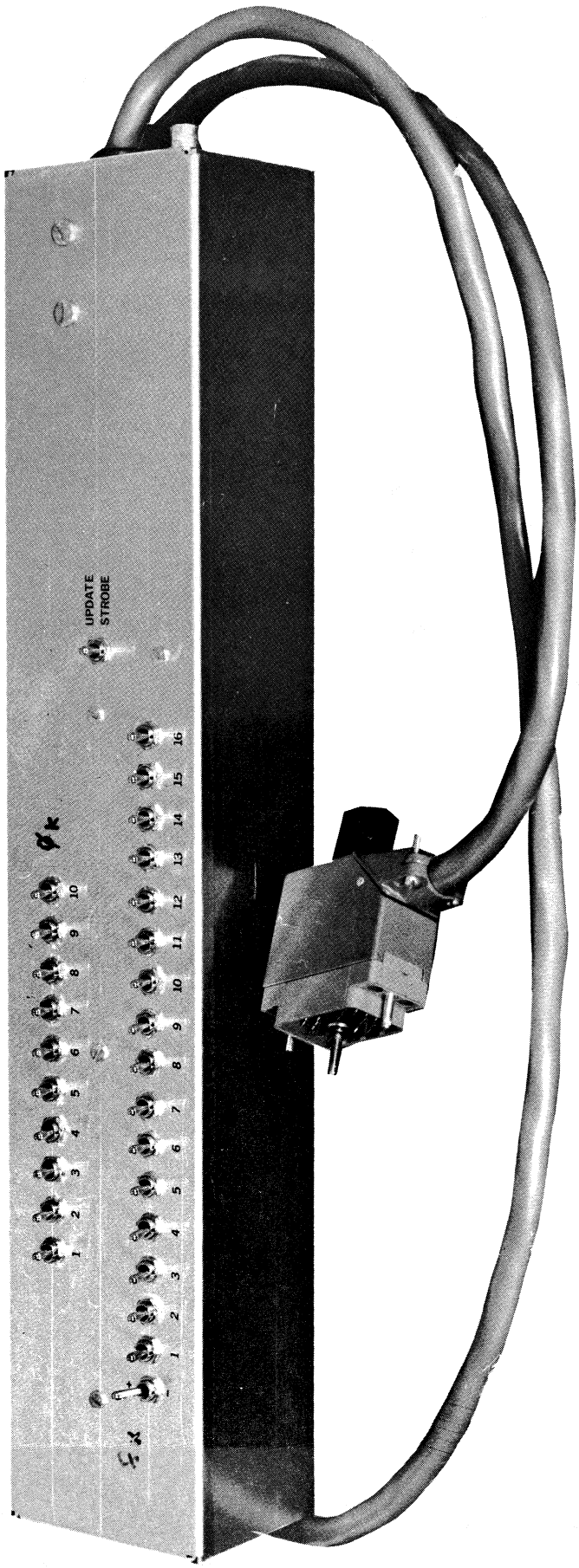
Front View of Lobe Rotator Digital Section



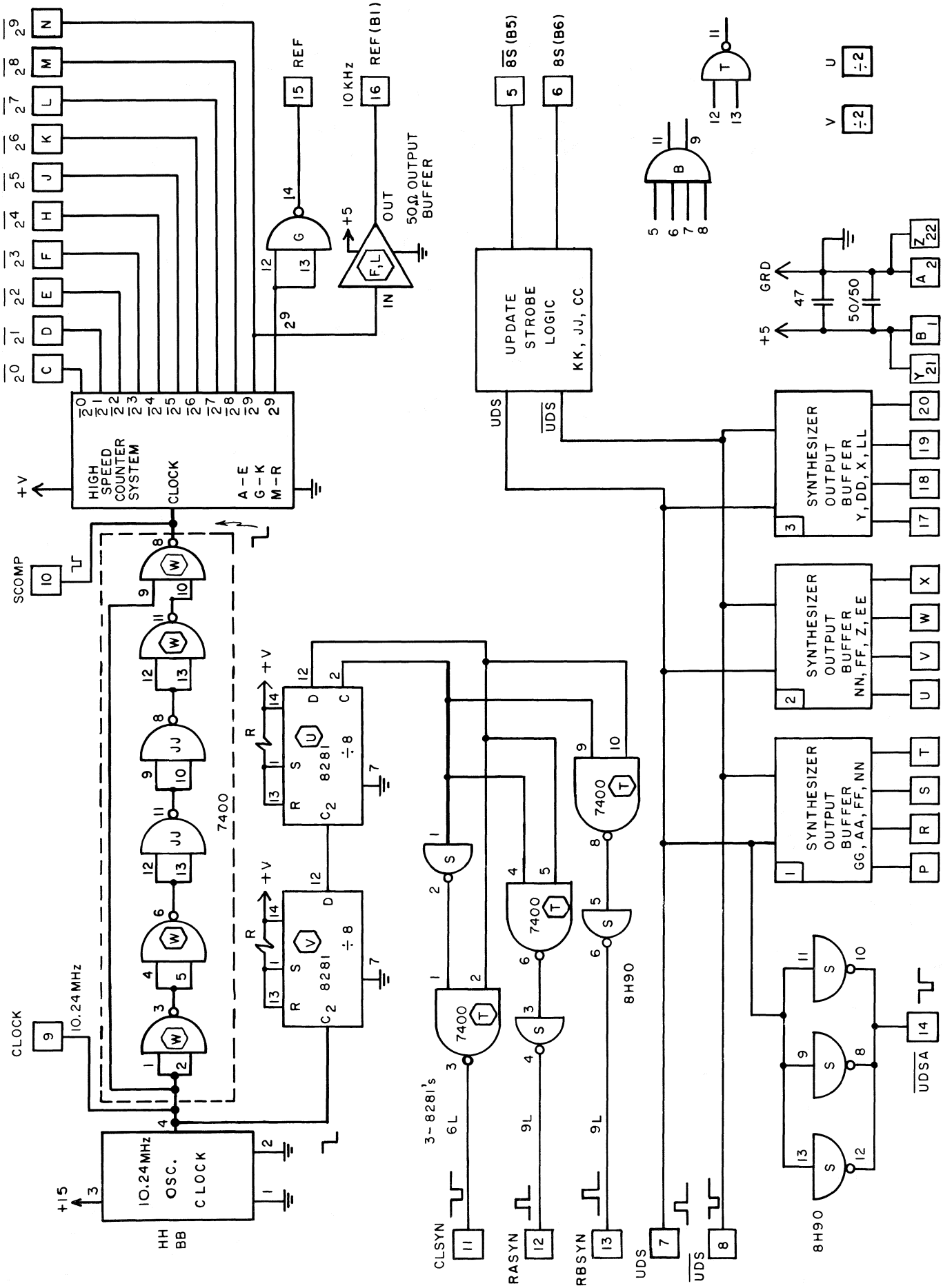
Top-Rear View of Lobe Rotator Digital Section



Lobe Rotator Digital Cards

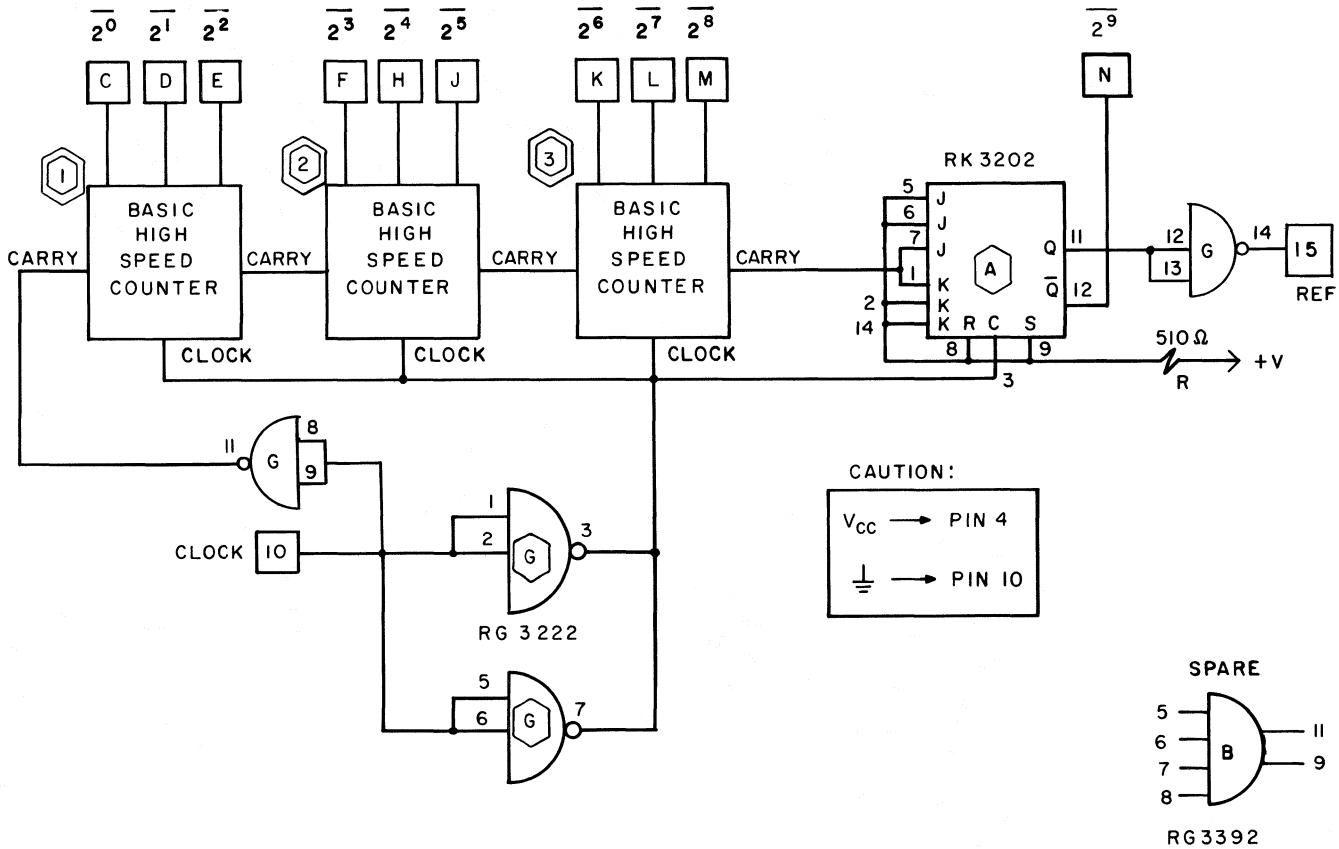


Lobe Rotator Test Jig



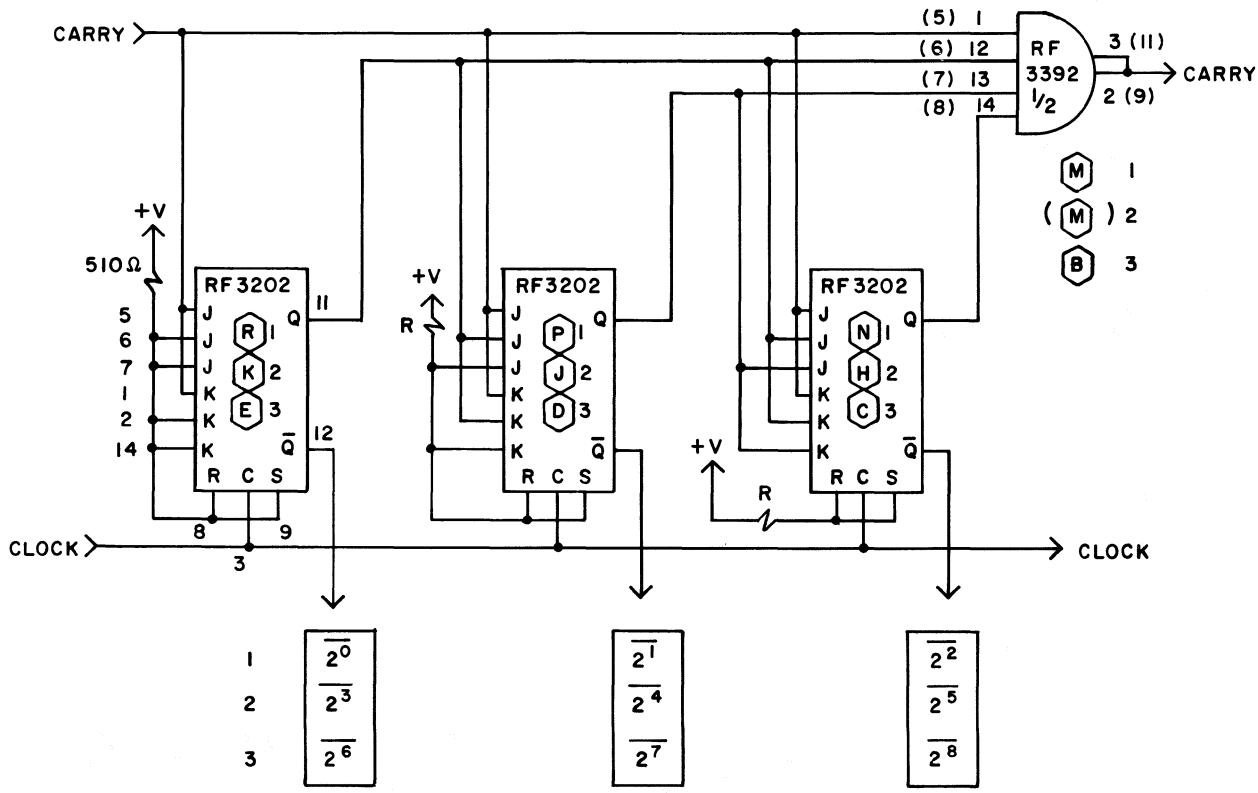
LOBE ROTATOR REF. GEN., OSC., & CONTROL, Card 3

SCHEMATIC # 1.



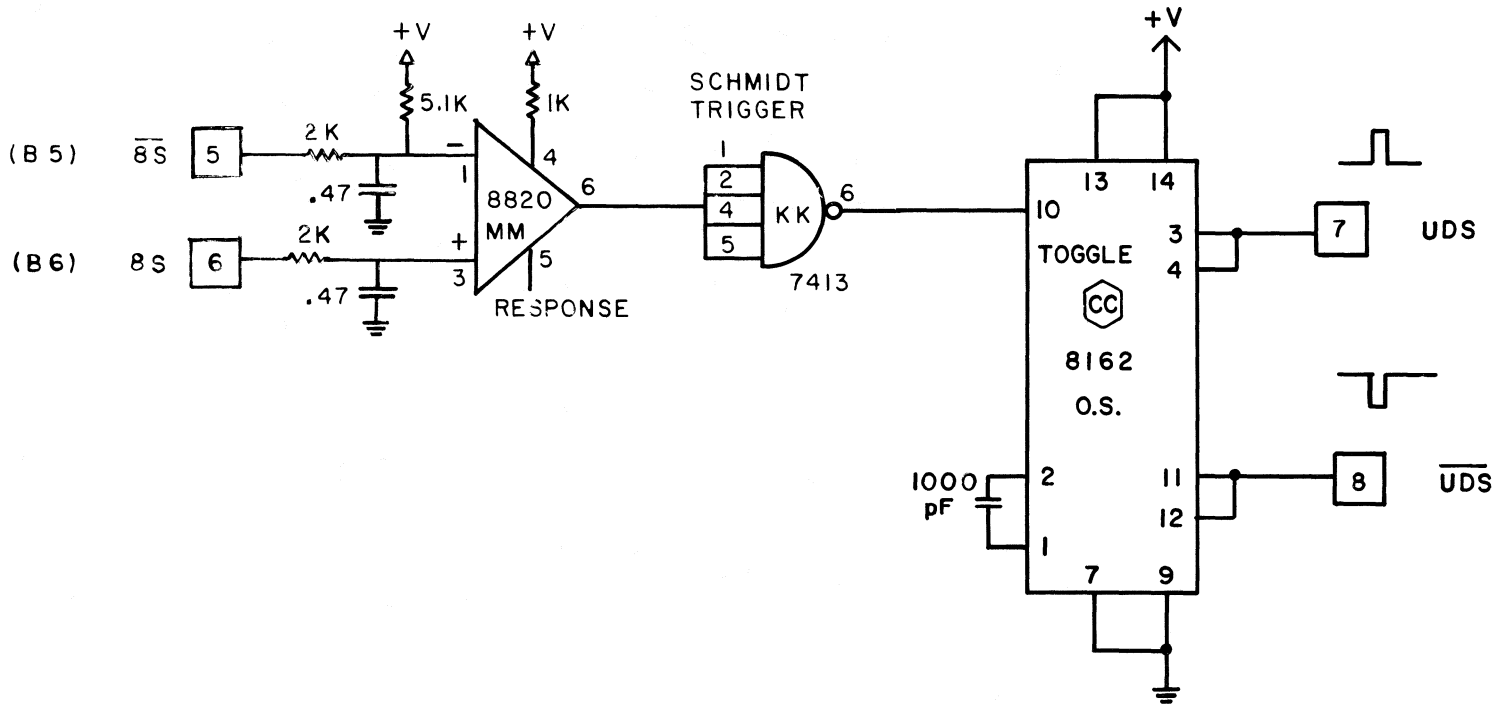
HIGH SPEED COUNTER SYSTEM

SCHEMATIC # 2

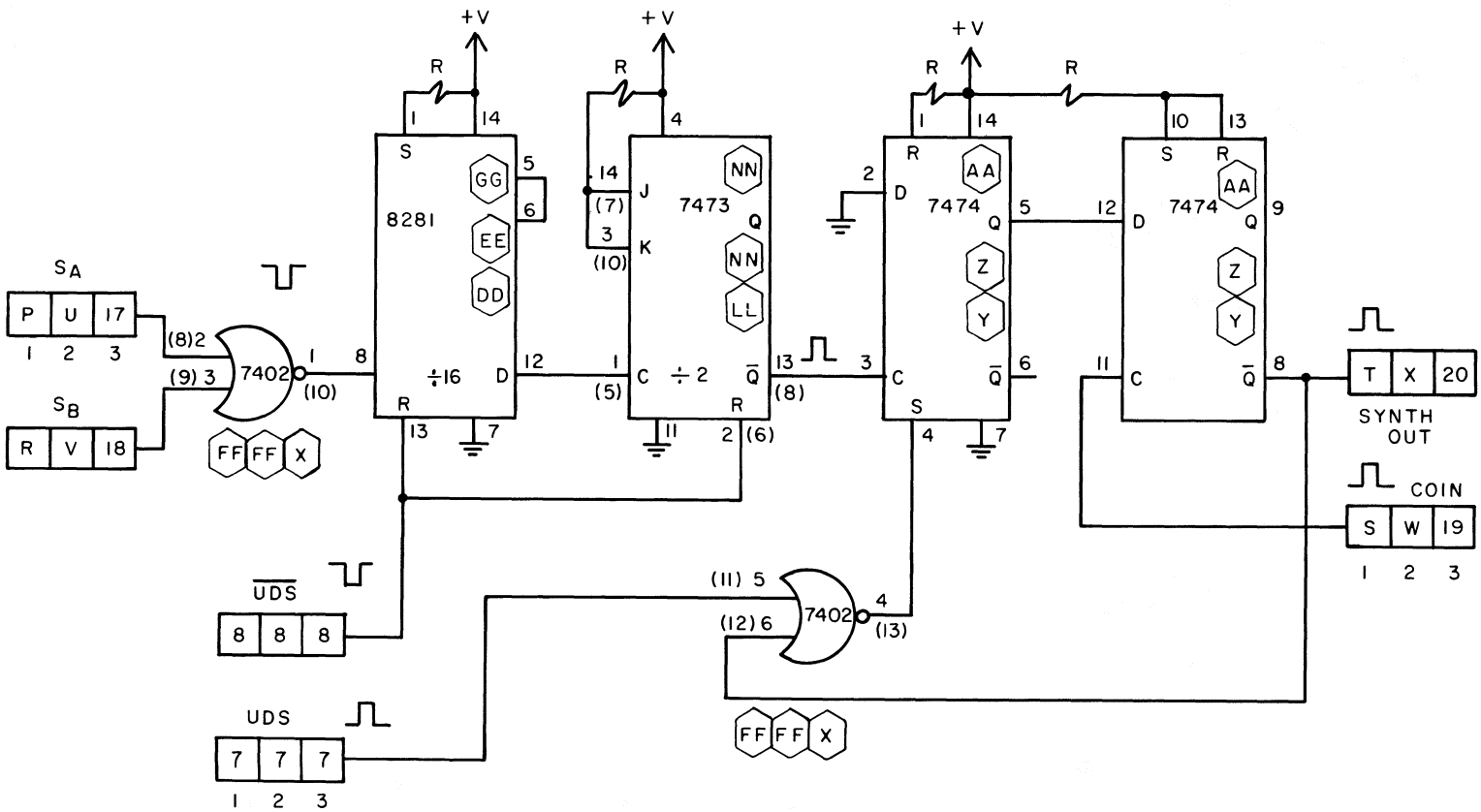


BASIC HIGH SPEED SYNCHRONOUS COUNTER

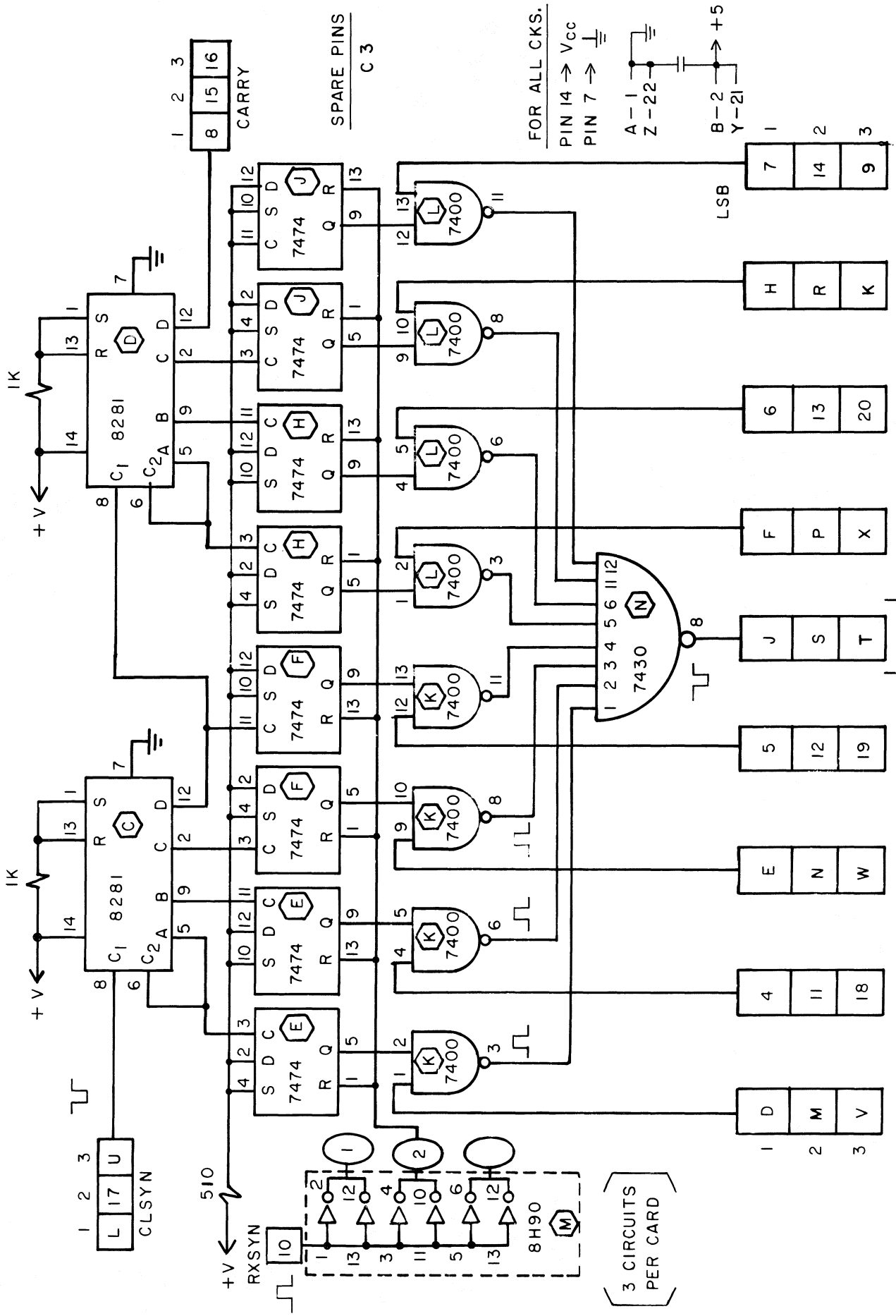
SCHEMATIC # 3

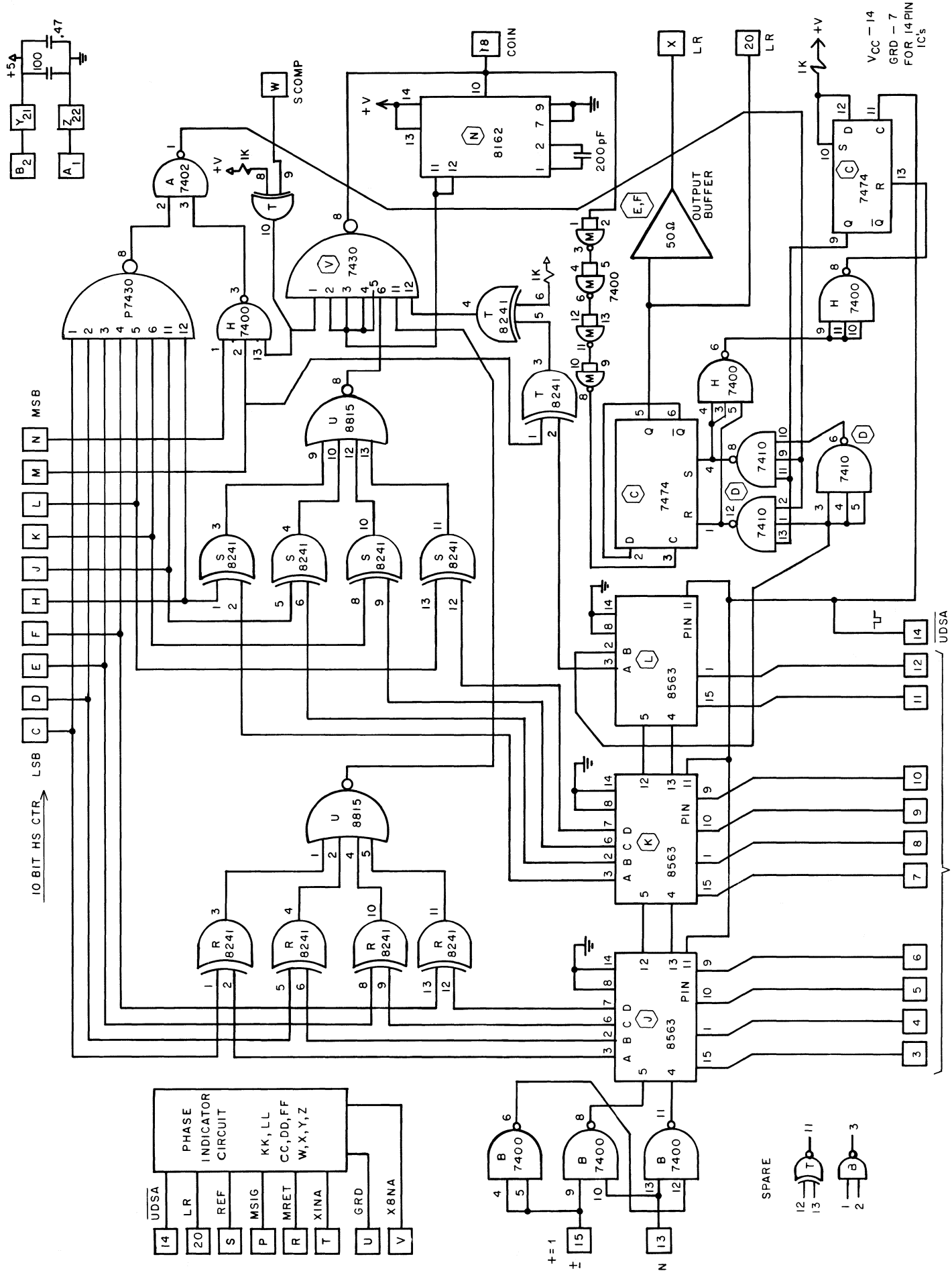


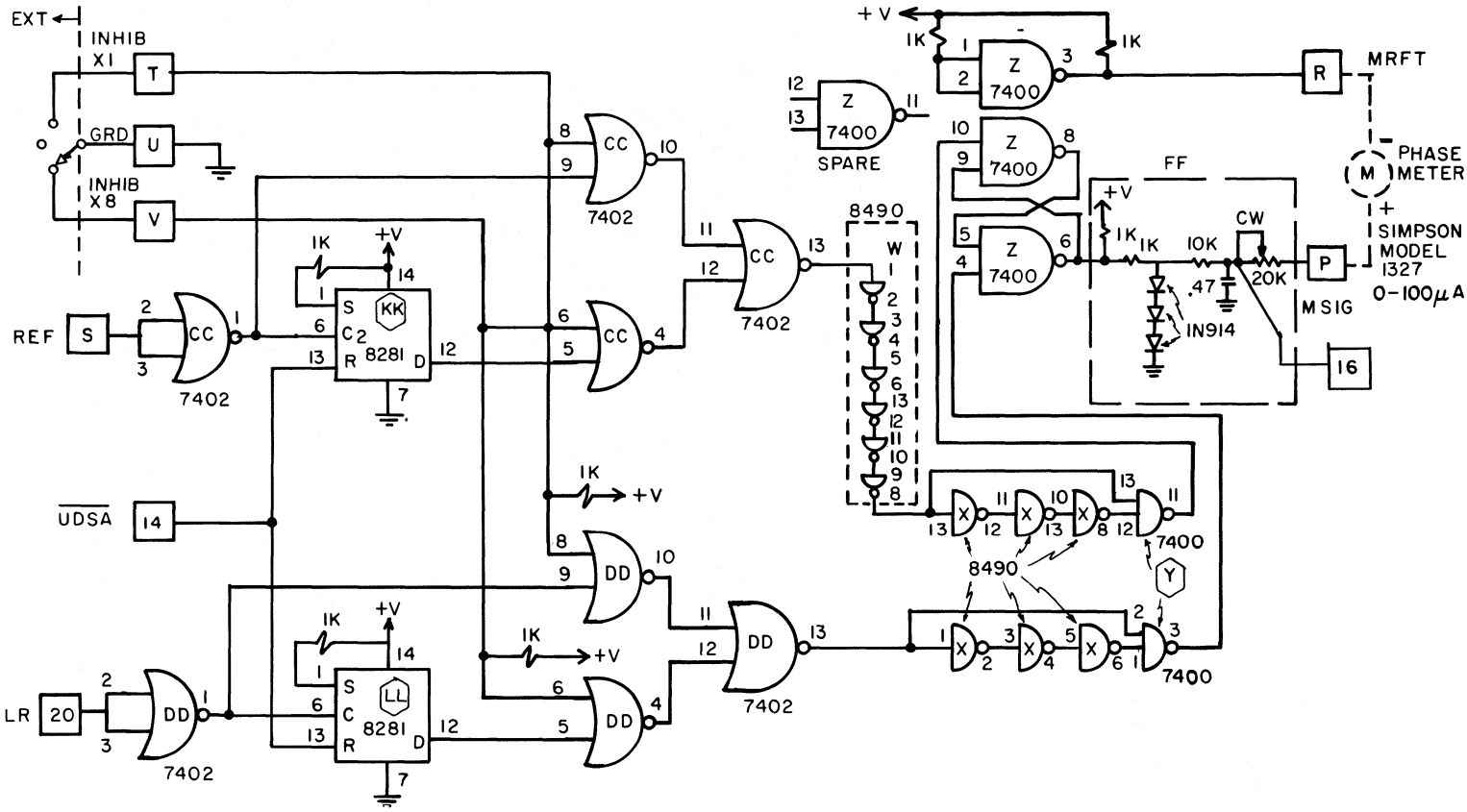
UPDATE STROBE LOGIC
SCHEMATIC # 4



DIGITAL FREQUENCY SYNTHESIZER BUFFER
SCHEMATIC # 5

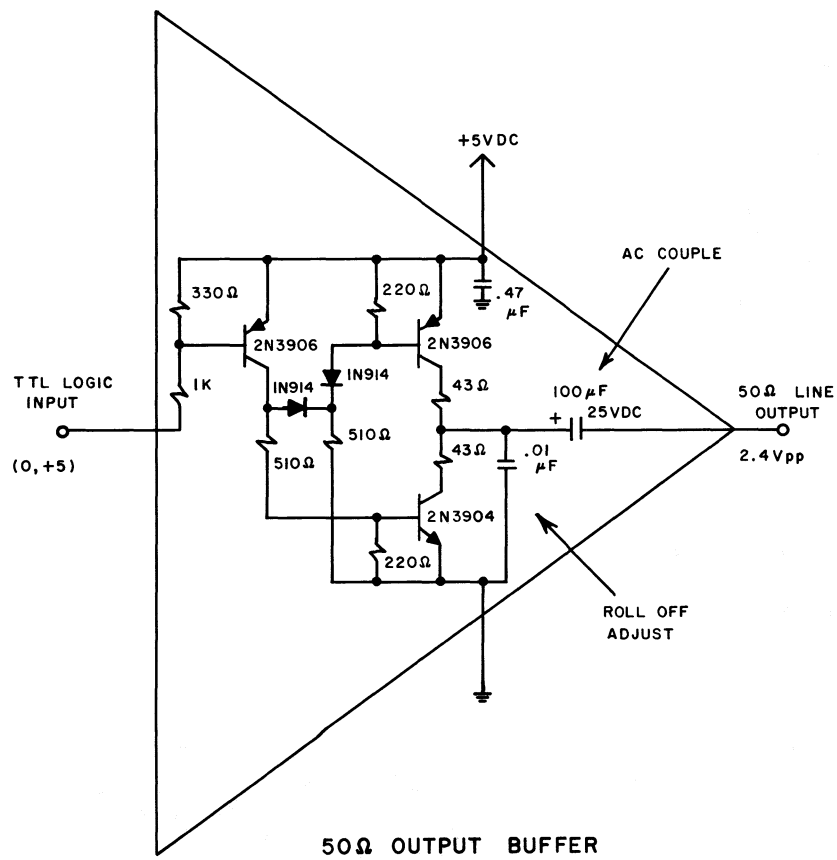

LOBE ROTATOR FREQUENCY SYNTHESIZER Card 1&2
SCHEMATIC # 6
SPARE PINS
C 3
FOR ALL CKS.
PIN 14 → Vcc
PIN 7 → ⏚
A – 1
Z – 22
B – 2
Y – 21
+5
CARRY
LSB
CLSYN
RXSYN
510
1K
+V
8281
7474
7400
7430
8H90
3 CIRCUITS PER CARD
f_K
S_K


LOBE ROTATOR PHASE REG/CTR/COMP Card 4,5,6
SCHEMATIC # 7
10 BIT HS CTR
LSB
MSB
PHASE INDICATOR CIRCUIT
KK, LL
CC, DD, FF
W, X, Y, Z
UDSA
LR
REF
MSIG
MRET
XINA
GRD
XBNA
SPARE
OUTPUT BUFFER
50Ω
COIN
SCOMP
+V
1K
200pF
8162
7402
7430
P7430
7400
8241
8815
8563
7474
7410
V_{CC} – 14
GRD – 7
FOR 14 PIN IC's
ϕK



PHASE INDICATOR CIRCUIT Card 456

SCHEMATIC # 8



50Ω OUTPUT BUFFER

TTL (0,+5) TO 50Ω LINE

SCHEMATIC # 9

12. Signal Designation Lists

8S	The 10 second sidereal clock signal.
Carry	Cascaded count from most significant to least significant.
CLSYN	Clock synthesizer.
COIN	Coincidence output from coincidence gate.
f_k	Fringe frequency.
ϕ_k	Fringe phase.
LR	Lobe rotator generator output.
REF	10 kHz reference phase output.
MSIG	Positive analog phase meter terminal.
MRET	Negative analog phase meter terminal.
RASYN	Reset synthesizer output pulse flops card 1.
RBSYN	Reset synthesizer output pulse flops card 2.
RXSYN	Either RASYN or RBSYN.
S_A	Most significant synthesizer pulse frequency.
S_B	Least significant synthesizer pulse frequency.
SCOMP	Strobe compare.
SYN	Synthesizer buffer output.
UDS	Active high update strobe.
$\overline{\text{UDS}}$	Active low update strobe.
$\overline{\text{UDSA}}$	Active low update strobe A
X1NH	Analog phase indicator low scale inhibit.
X8NH	Analog phase indicator high scale inhibit.

13. Test Point Lists

		Signal from	Signal name
R	1	C3-1	Grd.
	2	C3-9	Clock
	3	C3-7	UDS
	4	C3-15	REF unbuffered
LR-1	1	C4-1	Grd.
	2	C3-J	Syn.
	3	C4-18	Coincidence
	4	C4-20	LR-1 unbuffered
	5	C4-16	Analog phase indicator
	6		
LR-2	1	C5-1	Grd.
	2	C3-X	Syn.
	3	C5-18	Coincidence
	4	C5-20	LR-2 unbuffered
	5	C5-16	Analog phase indicator
	6		
LR-3	1	C6-1	Grd.
	2	C3-20	Syn.
	3	C6-18	Coincidence
	4	C6-20	LR-3 unbuffered
	5	C6-16	Analog phase indicator
	6		

14. Connector Lists

Lobe Rotator - Card 12 Connector Pin Breakout

Pin	Function			Notes
A	Gnd			
B	+5			
C	Spare			
D	Bit 1-9		"F_K"	
E	Bit 3-11			
F	Bit 5-13			
H	Bit 7-15		LR-1	
J	SA-SB	LR-1		Synth out
K	Bit 7-15	LR-3		
L	CLSYN	LR-1		Synth clock
M	Bit 1-9		"F_K"	
N	Bit 3-11			
P	Bit 5-13			
R	Bit 7-15		LR-2	
S	SA-SB	LR-2		
T	SA-SB	LR-3		
U	CLSYN	LR-3		
V	Bit 1-9		F_K	
W	Bit 3-11			
X	Bit 5-13		LR-3	
Y	+5			
Z	Gnd			
1	Gnd			
2	+5			
3	Spare			
4	Bit 2-10		"F_K"	
5	Bit 4-12			
6	Bit 6-14			
7	Bit 8-16		LR-1	
8	Carry	LR-1		Clock carry to pin L card 2
9	Bit 8-16	LR-3		
10	RXSYN			Synth os reset
11	Bit 2-10			
12	Bit 4-12			
13	Bit 6-14			
14	Bit 8-16			
15	Carry	LR-2		To pin 17 - Card 2
16	Carry	LR-3		To pin U - Card 2
17	CLSYN	LR-2		
18	Bit 2-10		F_K	
19	Bit 4-12			
20	Bit 6-14		LR-3	
21	+5			
22	Gnd			

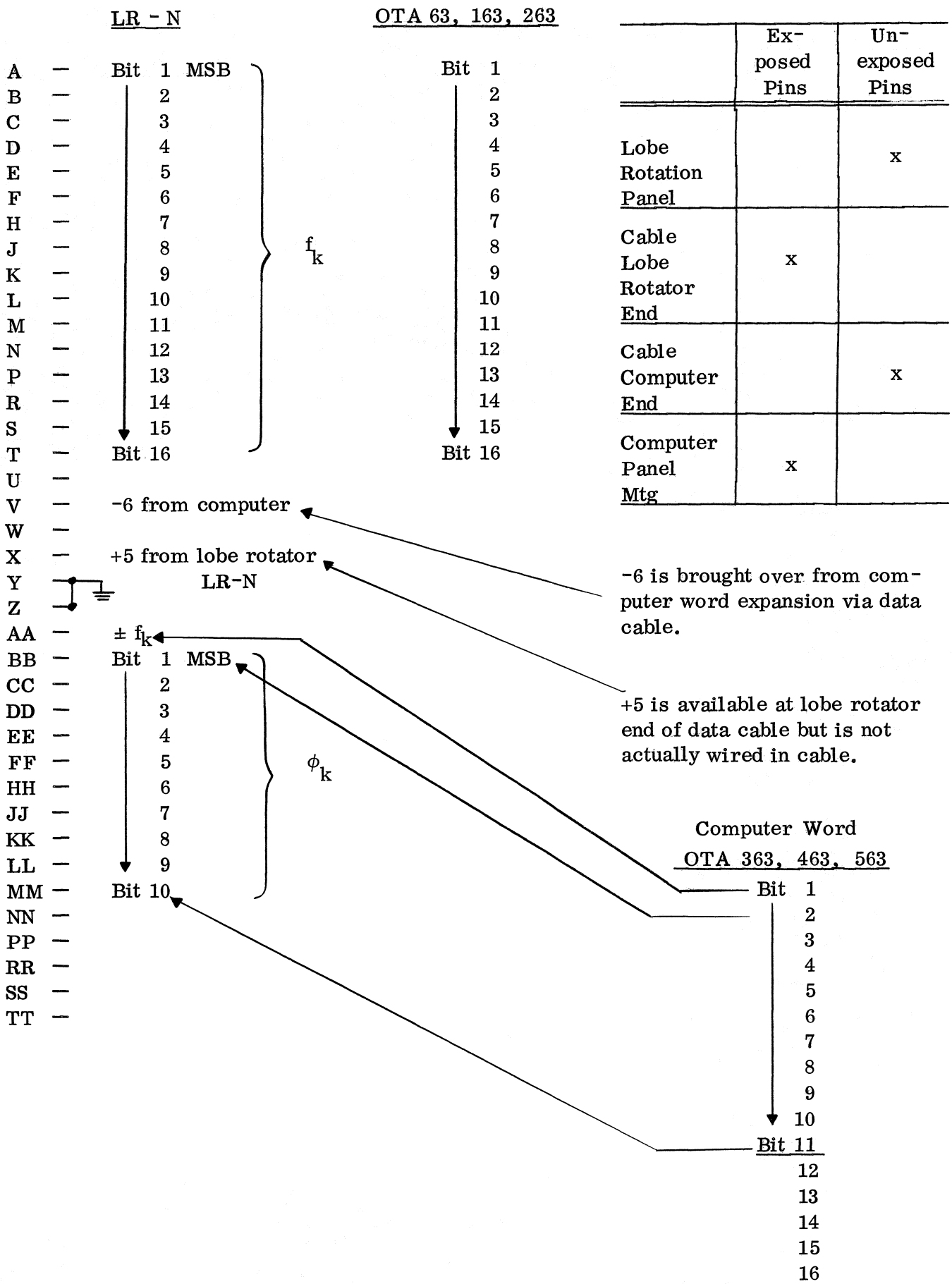
Lobe Rotator - Card 3 Connector Pin Breakout

Pin	Function		Notes
A	Gnd		
B	+5		
C	$\overline{2^0}$	H.S. Counter Out	
D	$\overline{2^1}$		
E	$\overline{2^2}$		
F	$\overline{2^3}$		
H	$\overline{2^4}$		
J	$\overline{2^5}$		
K	$\overline{2^6}$		
L	$\overline{2^7}$		
M	$\overline{2^8}$		
N	$\overline{2^9}$		
P	S_A	LR-1	
R	S_B		
S	Coin		
T	Syn		
U	SA	LR-2	
V	SB		
W	Coin		
X	Syn		
Y	+5		
Z	Gnd		
1	Gnd		
2	+5		
3	$\overline{8S}$		3C Logic Level
4	$\overline{OTP1}$		To pin 14 - card 3
5	$\overline{OTP2}$		
6	$\overline{OTP3}$		
7	UDS		
8	$\overline{UDS}$		
9	Clock		10.24 MHz out
10	SCOMP		
11	CLSYN		
12	RASYN		
13	RBSYN		
14	$\overline{UDSA}$		
15	REF-1		To phase indicator
16	REF		50 ohm output
17	SA	LR-3	
18	SB		
19	Coin		
20	Syn		
21	+5		
22	Gnd		

Lobe Rotator - Card 456 Connector Pin Breakout

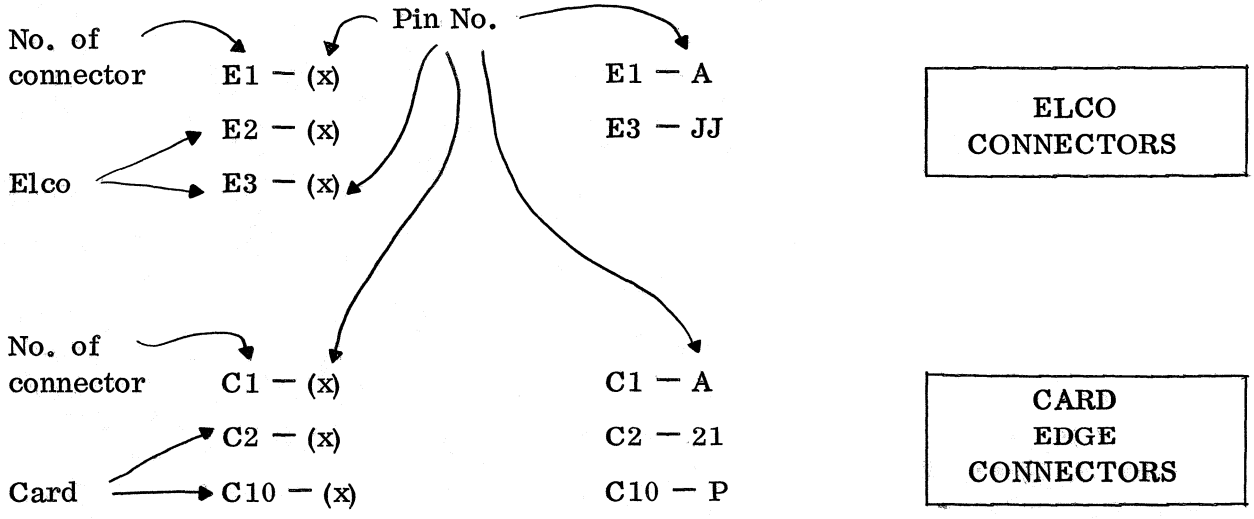
Pin	Function		Notes
A	Gnd		
B	+5		
C	$\overline{2^0}$	To H. S. Counter	
D	$\overline{2^1}$		
E	$\overline{2^2}$		
F	$\overline{2^3}$		
H	$\overline{2^4}$		
J	$\overline{2^5}$		
K	$\overline{2^6}$		
L	$\overline{2^7}$		
M	$\overline{2^8}$		
N	$\overline{2^9}$		
P	MSIG		
R	MRET		
S	REF		To phase indicator
T	X1NH		
U	Gnd		
V	X8NH		
W	SCOMP		
X	LR		50 ohm output
Y	+5		
Z	Gnd		
1	Gnd		
2	+5		
3	Bit 10	LSB	
4	Bit 9		
5	Bit 8		
6	Bit 7		
7	Bit 6		
8	Bit 5	ϕ_k	
9	Bit 4		
10	Bit 3		
11	Bit 2		
12	Bit 1	MSB	
13	Syn		
14	$\overline{\text{UDSA}}$		
15	$\pm f_k$		
16	Analog phase out to test point		
17	Spare		
18	Coin		
19	Spare		
20	LR		To phase indicator
21	+5		
22	Gnd		

Lobe Rotator - Computer Control Cable



	Exposed Pins	Unexposed Pins
Lobe Rotation Panel		x
Cable Lobe Rotator End	x	
Cable Computer End		x
Computer Panel Mtg	x	

Lobe Rotator - Wire List



RT — 1	Test Point 1 "R"
L1T — 3	Test Point 3 "LR-1"
L2T — 6	Test Point 6 "LR-2"
L3T — 4	Test Point 4 "LR-3"

B1
B2
B6

BNC's

Wire power in the usual means through plugs and line fuse 2A SLO BLO.

+5 comes out red and black banana plugs and Deutsch connector through 5 amp meter mounted in back.

+5 to LR's goes through 5 amp meter mounted on panel and power switch.

Lobe Rotator - Wire List

Card 1

From	To	From	To
A	Ground	1	E1-Y, E2-Y, E3-Y E1-Z, E2-Z, E3-Z
B	+5	2	E1-X, E2-X, E3-X
C	NC	3	NC
D	E1-A	4	E1-B
E	E1-C	5	E1-D
F	E1-E	6	E1-F
H	E1-H	7	E1-J
J	C3-P	8	C2-L
K	E3-H	9	E3-J
L	C3-11	10	C3-12
M	E2-A	11	E2-B
N	E2-C	12	E2-D
P	E2-E	13	E2-F
R	E2-H	14	E2-J
S	C3-U	15	C2-17
T	C3-17	16	C2-U
U	C1-L	17	C1-U
V	E3-A	18	E3-13
W	E3-C	19	E3-D
X	E3-E	20	E3-F
Y	+5	21	
Z	Gnd	22	

Card 2

A	Ground	1	—
B	+5	2	—
C	NC	3	NC
D	E1-K	4	E1-L
E	E1-M	5	E1-N
F	E1-P	6	E1-R
H	E1-S	7	E1-T
J	C3-R	8	NC
K	E3-S	9	E3-T
L	—	10	C3-13
M	E2-K	11	E2-L
N	E2-M	12	E2-N
P	E2-P	13	E2-R
R	E2-S	14	E2-T
S	C3-V	15	NC
T	C3-18	16	NC
U	—	17	—
V	E3-K	18	E3-L
W	E3-M	19	E3-N
X	E3-P	20	E3-R
Y	+5	21	+5
Z	Gnd	22	Gnd

Lobe Rotator - Wire List

Card 3

From	To	From	To
A	Ground	1	
B	+5	2	
C	C4-C	3	B-5
D	C4-D	4	C3-5
E	C4-E	5	C3-6
F	C4-F	6	C3-14
H	C4-H	7	NC
J	C4-J	8	NC
K	C4-K	9	RT-2
L	C4-L	10	C4-W
M	C4-M	11	—
N	C4-N	12	—
P	—	13	—
R	—	14	C4-14
S	C4-18	15	C4-S
T	C4-13	16	REF to B-1
U	—	17	—
V	—	18	—
W	C5-18	19	C6-18
X	C5-13	20	C6-13
Y	+5	21	+5
Z	Gnd	22	Gnd

Card 4

	From	To		From	To
	A	Ground		1	
	B	+5		2	
	C	C5-C		3	E1-MM
	D	C5-D		4	E1-LL
	E	C5-E		5	E1-KK
	F	C5-F		6	E1-JJ
	H	C5-H		7	E1-HH
	J	C5-J		8	E1-FF
	K	C5-K		9	E1-EE
	L	C5-L		10	E1-DD
	M	C5-M		11	E1-CC
	N	C5-N		12	E1-BB
	P	+ Term Meter LR-1		13	—
	R	- Term Meter LR-1		14	C5-14
	S	C5-S		15	E1-AA
LO	T	Range		16	NC
Off	U	Switch	LR-1	17	NC
Hi	V	(Meter)		18	NC
	W	C5-W		19	NC
	X	BNC - LR-1 on front and B-2		20	NC
	Y	—		21	+5
	Z	Gnd		22	Gnd

Lobe Rotator - Wire List

Card 5

From		To	From	To
	A	Ground	1	
	B	+5	2	
	C	C6-C	3	E2-MM
	D	C6-D	4	E2-LL
	E	C6-E	5	E2-KK
	F	C6-F	6	E2-JJ
	H	C6-H	7	E2-HH
	J	C6-J	8	E2-FF
	K	C6-K	9	E2-EE
	L	C6-L	10	E2-DD
	M	C6-M	11	E2-CC
	N	C6-N	12	E2-BB
	P	+ Term meter LR-2	13	—
	R	- Term meter LR-2	14	C6-14
	S	C6-S	15	E2-AA
LO	T	Meter	16	NC
Off	U	Range } LR-2	17	NC
Hi	V	Switch	18	NC
	W	C6-W	19	NC
	X	BNC - (LR-2) on front and B-3	20	NC
	Y	—	21	+5
	Z	Gnd	22	Gnd

Card 6

	A	Ground	1	
	B	+5	2	
	C	—	3	E3-MM
	D	—	4	E3-LL
	E	—	5	E3-KK
	F	—	6	E3-JJ
	H	—	7	E3-HH
	J	—	8	E3-FF
	K	—	9	E3-EE
	L	—	10	E3-DD
	M	—	11	E3-CC
	N	—	12	E3-BB
	P	+ Term meter LR-3	13	—
	R	- Term meter LR-3	14	—
	S	—	15	E3-AA
LO	T	Meter	16	—
Off	U	Range } LR-3	17	NC
Hi	V	Switch	18	NC
	W	—	19	NC
	X	BNC - (LR-3) on front and B-4	20	NC
	Y	—	21	—
	Z	—	22	Gnd