Block Diagram of VEGAS

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The overall block diagram of the Versatile GBT Astronomical Spectrometer (VEGAS) is shown in Fig. 1. The analog signals from the converter rack (CR) are fed to the ADCs attached to the ROACH boards after amplification and limiting the bandwidth to 1.5 GHz. The FPGAs in the ROACH board process the signal and send to the high performance computer (HPC) through a 10 GbE switch. The 10 GbE switch in this path will help in (a) maintenance of the system and (b) future development of new observing modes. The HPC consists of 8 (+ 1 spare) independent PCs, with 12 GB RAM and 1 + 1 TB disks connected in raid 0 configuration. It will have a dual port 10 GbE card and a GPU GTX480 card. The GPU will be used for implementing observing modes with bandwidth $\leq$ 250 MHz and the 8 sub-band modes. The internal hard disks in the HPC are used only for system testing and supporting high speed data acquisition ($\sim$ 100 MB/sec) for any test observations. One of the ports of the 10GbE card will receive data from the ROACH boards and the second port will send data to the data storage system. The HPC is connected to the data storage system through the same 10 GbE switch to which the ROACH boards are connected. The data storage system will be a parallel file system (eg. luster) based storage system and will support $>$ 40 TB of disk space. For all the specified observing modes data will be written to this storage system. The GBT users will be accessing data from this storage system through a 1 GbE link as shown in Fig 1.

The monitor and control (M&C) of the whole spectrometer is done through a dedicated computer. The M&C system will obtain data from the ROACH board through a 1 GbE (or 100 MbE) network. The 1 GbE network is connected to the HPCs through a 10 GbE link.

The external 1 PPS signal is connected to the ROACH boards through a commercial distribution system. The 1 PPS is the main synchronization signal for the spectrometer. The internal switching signals are generated by one of the ROACH boards (Switching Master) and will be sent to other ROACH boards through a distribution system. The Switching Master will also accepts external switching signals and re-synchronize them with the FPGA clock and send to other boards through the same distribution board.

The sampling clock is generated using a synthesizer, which is locked to the observatory 10 MHz standard. The output of the synthesizers is amplified and fed to the ROACH board through a 8 way power splitter. Inside the ROACH board there will be a 2 way power splitter to feed the clock to the two ADC boards in the ROACH, which will sample the two polarization of a beam.

The beam based calibration of the GBT data processing pipeline will be implemented in the HPC. The processing of data to make maps with focal plane arrays will be done in a different computer (Arcturus). The data from the HPC after the initial beam based calibration will be sent to Arcturus for making the map.

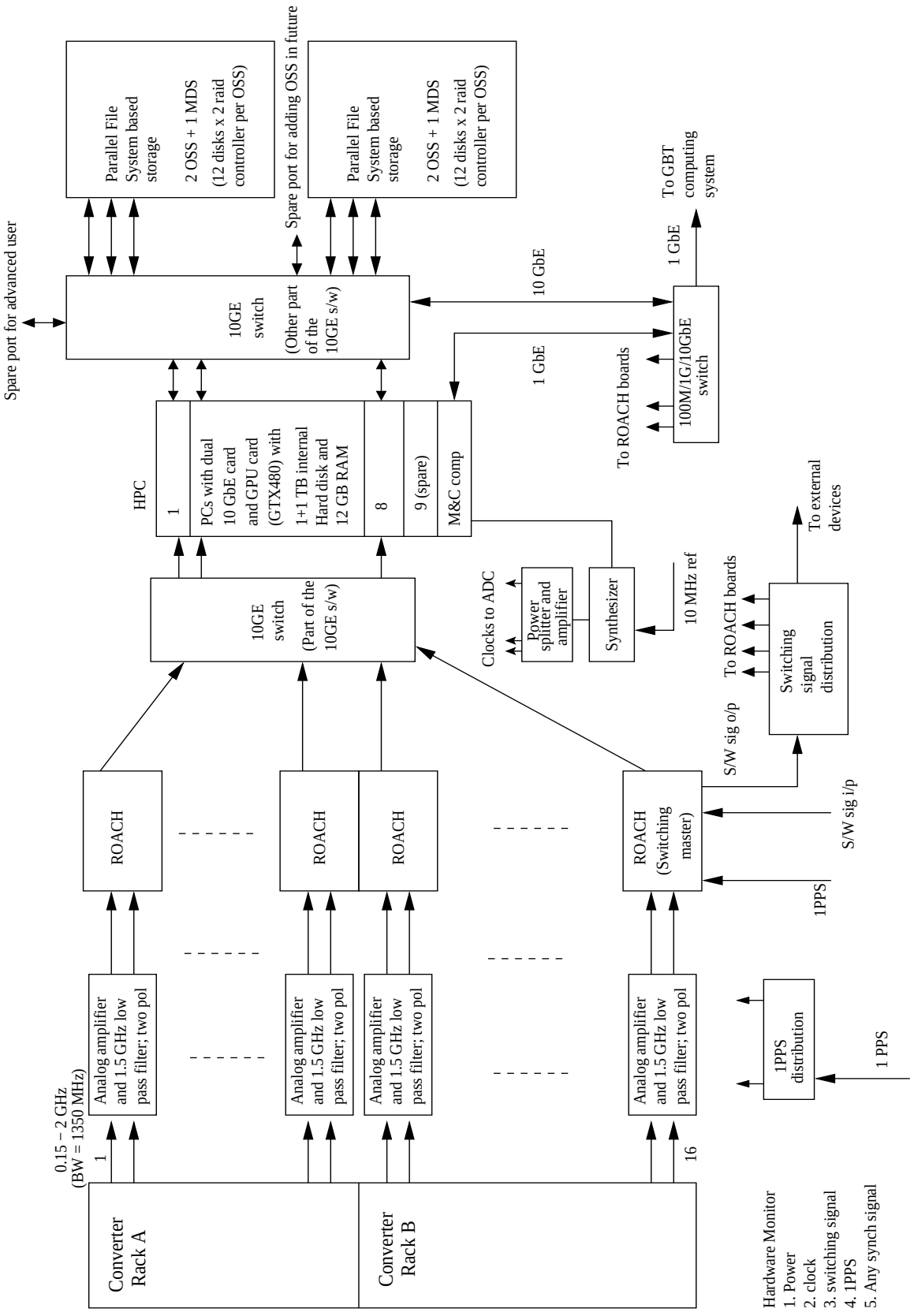

Figure 1: A block diagram of VEGAS