GBT memo

Analog signal conditioning and sampling clock distribution for the GBT spectrometer

Authors: D. Anish Roshi
Affiliation: NRAO, Green Bank.

Date: Oct 13, 2010, (v0.1)

Abstract

Requirements of the analog signal conditioning circuit and sampling clock distribution network are described.

1 Analog signal conditioning

A block diagram of the new GBT spectrometer is shown in Fig. 1. As seen in Fig. 1 there will be 8 spectrometers working in parallel. These spectrometers are connected to the outputs of the Converter Racks (CR) A and B of the GBT. The CR's lower and upper cutoff frequencies are 150 MHz and 2 GHz respectively. The analog-to-digital converters (ADCs) in each of the 8 spectrometer will sample the signal at 3 GHz. Hence the analog bandwidth needs to be filtered (anti-aliasing filter) to 1.5 GHz. In addition, an amplifier may be required to amplify the CR output to the power level required by the ADC. The anti-aliasing filter and amplifier form the analog signal conditioning unit. There will be 16 such units to connect the two polarization signals to the 8 spectrometers. The requirements of the analog signal conditioning unit are given in Table 1 (see also Roshi et al. 2010 for specifications of the spectrometer).

1.1 Intermodulation

The amplifier intermodulation (IM) requirement is obtained as follows. The ADC specification gives an IMD value of 52 dBFS (ADC083000 data sheet 2009). The full-scale value for a single tone corresponds to about +2 dBm at the input of the ADC. For phase locked dual tones, the power per tone that gives ADC full-scale value is -4 dBm. Therefore the IM product power referenced to ADC input is -56 dBm. A 4 dB attenuator is placed at the input of the ADC for impedance matching. Therefore the power levels of the tone and IM product referenced to the output of the amplifier is 0 dBm and -52 dBm respectively. We require the amplifier IM product level 10 dB below this value. So the output IM product power of the amplifier should be < -62 dBm for the per tone amplifier output power of 0 dBm. Thus the output IP3 of the amplifier should be ≥ 31 dBm.

1.2 Isolation

The isolation between analog signal conditioning units is obtained from the requirement of polarization observations. Astronomical sources are polarized typically at 2 % level or less. The Stokes parameters are usually obtained from the measured cross correlation between the two orthogonal

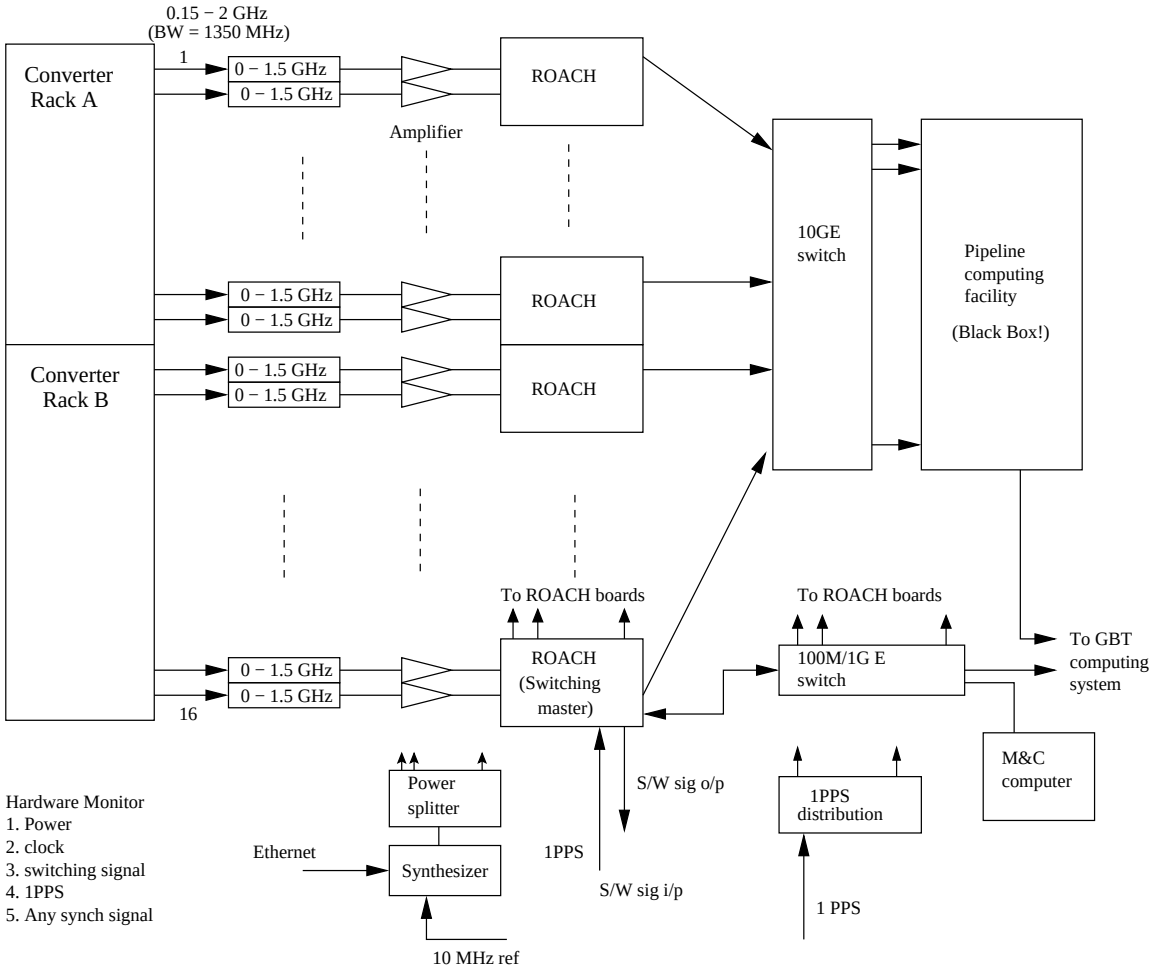

Figure 1: A schematic of the new GBT spectrometer

polarized signals. In such measurement we may require any cross coupling between the signals to be ≤ 0.1 %, which gives an isolation of ≤ 60 dB.

2 Sampling clock distribution

A schematic of the clock distribution is shown in Fig. 2. The specifications for the clock distribution unit are given in Table 2.

2.1 Clock Jitter

The requirement of clock jitter is estimated by comparing the specified SNR of the ADC to that due to sampling clock jitter. The specified SNR for ADC083000 is 42 dB (ADC083000 data sheet 2009) and the clock jitter is then obtained using the equation

$$20log(\frac{1}{2\pi f_{in}\sigma_t}) = 42dB \tag{1}$$

where f_{in} is the input frequency in Hz and σ_t is the RMS jitter in sec. For an operating frequency of $f_{in} = 1.5$ GHz, $\sigma_t \leq 0.84$ ps. The RMS aperture jitter of ADC083000 is 0.55 ps, which implies

Table 1: Analog signal conditioning system specifications

Specifications per unit (see text)	
Anti-aliasing filter	Low pass filter with 3dB cutoff freq 1.5 GHz stop-band rejection $>$ 20 dB Roll-off: 20 dB per 100 MHz $<$ 0.1 dB ripple within the 3dB bandwidth
Analog input power level	+2 dBm for full-scale of the 8 bit ADC -40 dBm for 1 bit fluctuation
Intermodulation ; output IP3	$>$ 31 dBm
Attenuator at ADC input (This is needed for impedance matching)	4 dB
Input connector (Input coming from CR)	SMA female
Output connector (Output going to ADC board)	SMA female
Specifications of the system	
Isolation between the units	$>$ 60 dB

the clock jitter should be $\leq$ 0.61 ps We also calculate $\sigma_t = 3.2$ ps for an effective 5 bits (for most observations the ADC will be operated at this level to avoid saturation due to RFI) and 1.4 GHz (the specified anti-aliasing filter roll-off is 20 dB in 100 MHz). The 'degraded' specification on the clock jitter after removing the contribution from ADC aperture jitter is $\leq$ 3.1 ps

Acknowledgment

I thank Galen Watts for his useful comments on this report.

Reference

Roshi, D. A. et al. 2010, GBT memo.
ADC083000 data sheet, 2009, National Semiconductor website.

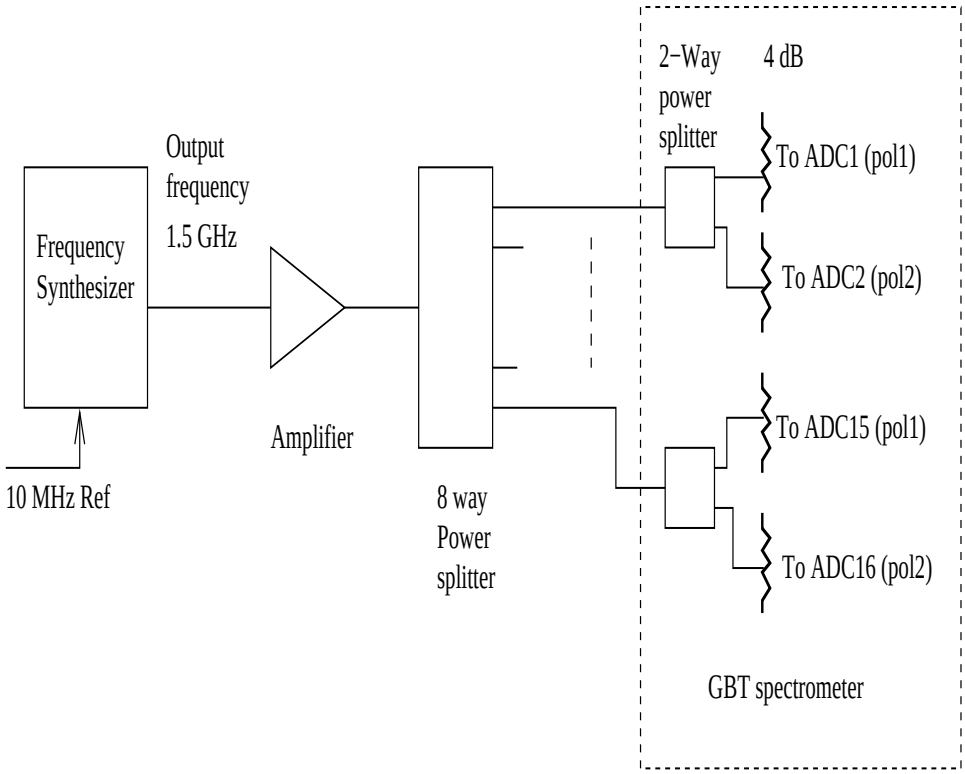

Figure 2: A schematic showing the sampling clock distribution.

Table 2: Clock distribution system specifications

Clock freq Clock waveform	1.5 GHz sine wave
Ref input freq Ref waveform Ref power	10 MHz sine wave 0 dBm
Jitter at the ADC clock input port Jitter (degraded)	$\leq$ 0.61 ps $\leq$ 3.1 ps
Power at ADC clock input port Attenuator at ADC clock input (This is needed for impedance matching)	0 dBm 4 dB
Output connector (Clock outputs to the spectrometer)	SMA female