ELECTRONICS DIVISION TECHNICAL NOTE 195

IPG Continuum Data Collection System

Tim Weadon
8/29/03

The "IPG" Continuum System was designed and built in 1998 by Rick Fisher, Rich Lacasse, Dwayne Schiebel and Tim Weadon. Rick specified the system requirements, Rich designed and built the Filter Amplifier system. Dwayne designed and built the Clock and Switching system and Tim designed and built and specified the computer associated hardware and software. Figure 1 is an over-all block diagram of the system.

The Filter Amplifier has one SMA input and one BNC output. There are three low-pass filters one may choose. The single pole three throw switch (SP3T) allows the user to select either a 50Hz, 500Hz or 5000Hz low-pass filter.

The Clock and Switching system inputs 4 differential signals and routes them, through the ribbon cable, to the computer A/D card. Only one signal was originally requested so the system, presently, only supports one input on the first channel. This system has thumb-wheel switches to set the hardware parameters "sample rate", "switch rate" and "cycles/integration".

The enable/stop switch arms and disarms the system from any spurious signals which could trigger a false start. The thumb-wheel switches should be set when this switch is in the stop position. Once the thumb-wheel switches are set, and the computer system is on and stable, this switch may be set to the enable position. When you wish to begin a new scan the enable/stop switch should be set to stop, the thumb-wheel switches should be set, then the enable/stop switch should be set to enable. The Switch Control LED and the Recording Data LED will be flashing when the clock and switching system is running.

The Clock and Switching system provide an interrupt to the computer A/D for when to sample the data. The computer provides the "go" signal to the Clock and Switching system for when it is to start generating the clock and switching signals.

The Computer and associated hardware provide the user interface for collecting, documenting and analyzing the data. The user enters a filename and description of the data. The number of samples to blank after each switch cycle, the sample rate, switch cycle and cycles/integration. The program generates two files. The first is filename.rfi and the second is filename.rf2. Filename.rfi contains the configuration data such as sample rate, switch cycle, samples/integration, etc. Filename.rf2 contains the raw "streamed" data.

When setting up for a scan the user first sets the thumb-wheel switches and enables the Clock and Switching System. Provisions for reading the thumb-wheel switches were not made or requested so the thumb-wheel positions should be repeated on the computer GUI panel. The total number of A/D conversions (samples) is determined from this data and is used by the program for when to quit sampling, so it is important to set the switches correctly or you will not know how many samples to wait for. Otherwise this data does not affect the collection

of the data but is used by the plotting and analysis software so it is stored for later reference. The Scan Complete "LED" on the GUI screen will turn green when all the data is collected. (If this LED turns green before the Clock and Switching system LEDs stop switching or if it stays black after the Clock and Switching system stops then you know your thumb-wheel switches do not match your GUI settings.)

The GUI panel allows you to collect, load and plot / analyze data which has just been collected or data which was collected sometime in the past. When you specify the filename then press the "Read&Plot" or "Fold&Plot" or "FFT" switches the computer reads the associated filename and performs the appropriate analysis on the data. A picture of the GUI panel is shown below in figure 2.

"Read&Plot" allows the user to plot out all the data collected. The X-axis is sample number and the Y-axis is the amplitude in volts.

"Fold&Plot" averages each "cycle" of data and plots one cycle of the average of all the data.

"FFT" performs an FFT on the data. The X-axis is Hz and the Y-Axis is power.

The boxes labeled "Sig/Ref", "Sig-Ref/Ref", "SIG" and "REF" are the accumulative counts of SIG and REF and the associated equation on that data. It is only filled in when you do the scan, not during post processing.

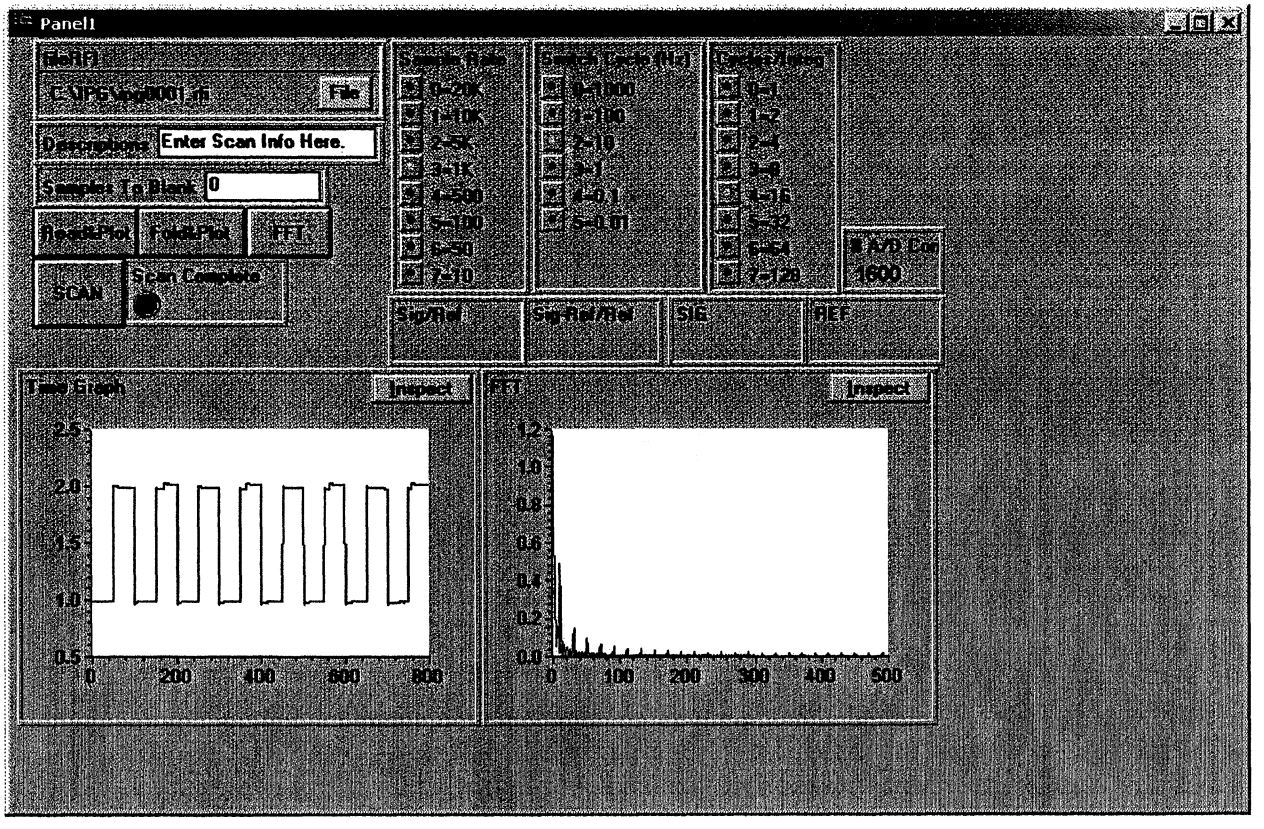
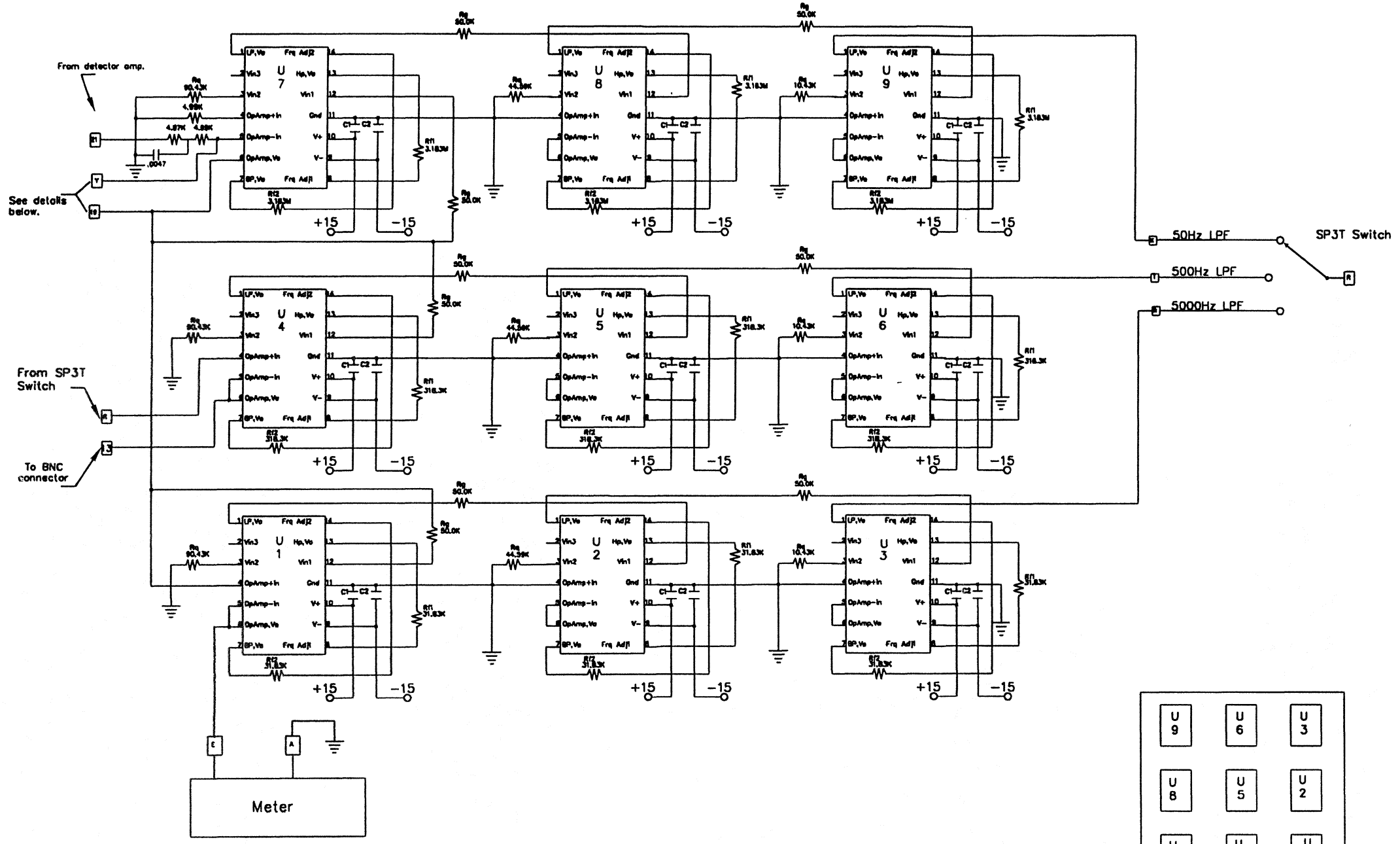
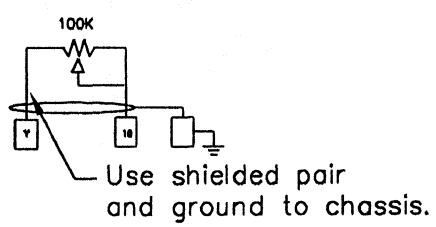


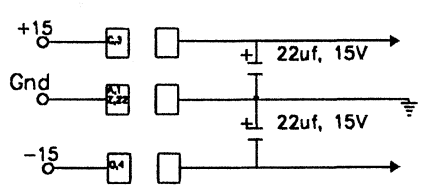
Figure 2

Instructions to run the IPG RFI computer software. (Appendix A)

1. Turn on the computer and associated equipment.
2. Log on to the computer.
3. Double click on the IPG RFI Test Software Icon.
4. Click on the "File" button in the "fileRFI" box.
5. Enter the filename you wish to store your data to or read data from.
6. Fill in the descriptions entry.
7. Set the thumb-wheel switches on the metal box beside the computer to the desired settings and the "Enable/Stop" switch to "Enable".
8. Set the Radio Buttons on the IPG RFI Panel to what you set the thumb-wheel switches to.
9. Press "SCAN" when you are ready to collect data. (Data is presently only collected on input channel 0.)
10. The Scan Complete light will be black during the scan and it will turn to green when the scan is complete.
11. The "Time Graph" will be plotted when the Scan is complete.
12. The data is now in the file you selected in step 5 above.
13. Press "Read&Plot" to read data from the file and plot it in the "Time Graph Window".
14. Press "Folt&Plot" to flod each cycle from the selected file into one cycle and plot the resulting "average" cycle.
15. Press "FFT" to run and plot the FFT on the data in the file selected.







NOTE: C1, C2 are 0.1uf. Each are shown nine places in the schematic. Place these as close to the IC's as possible.

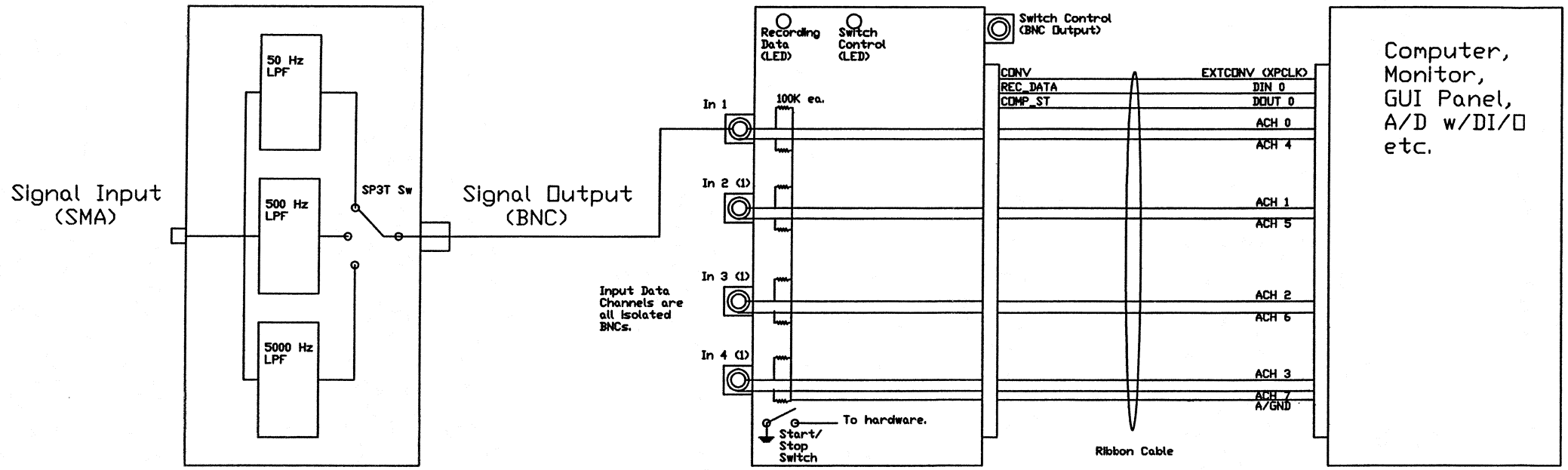
NATIONAL RADIO ASTRONOMY OBSERVATORY P.O. BOX 2, GREEN BANK, WEST VIRGINIA, 24944			TOLERANCES UNLESS OTHERWISE SPECIFIED ANGULAR ±0°30' FRACTIONAL ±1/64 2 PLACE DECIMAL ±.01 3 PLACE DECIMAL ±.005 DIMENSIONS ARE IN INCHES
PROJECT/TITLE: Continuim System Filter Amplifier			
DESIGNED: R.Laccase	DRAWN: J.Nelson	CHECKED: R.Laccase	DATE: 03/03/1999
SCALE:	MATERIAL: Douglas Card	FINISH:	DRAWING NO.: XXXXXXXXXX
FILE: schematic.dwg	SHEET: 1 OF 1	REVISION: 1	

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Continuim
System
Filter
Amplifier
(Lacasse)

Continuim
System
Clock and
Switching Hardware
(Schiebel)

Continuim
System
Computer &
Hardware
(Weadon)



	IPG Continuum System			
Dwg: T. Weadon	SIZE	FSCM NO.	DWG NO. xxxxxxxxxx	REV
Date: 8/29/03	SCALE N/A		SHEET 1/1	

50 Hz

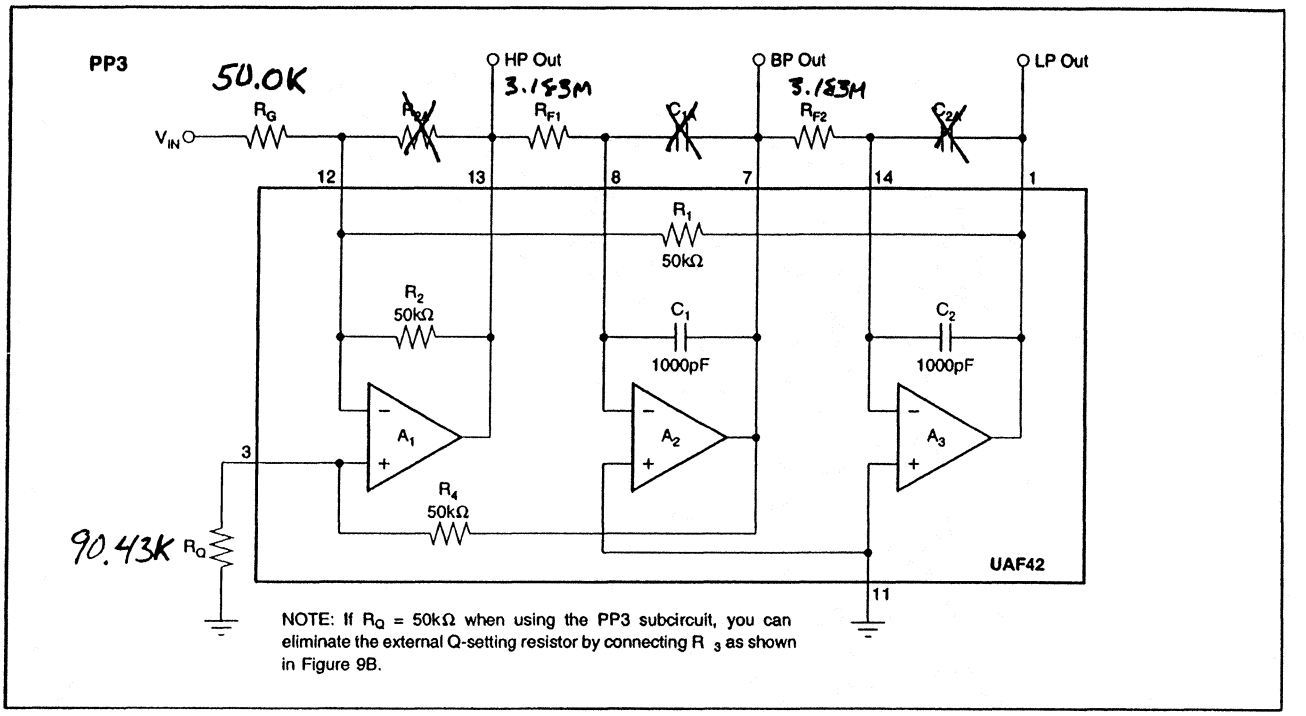


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

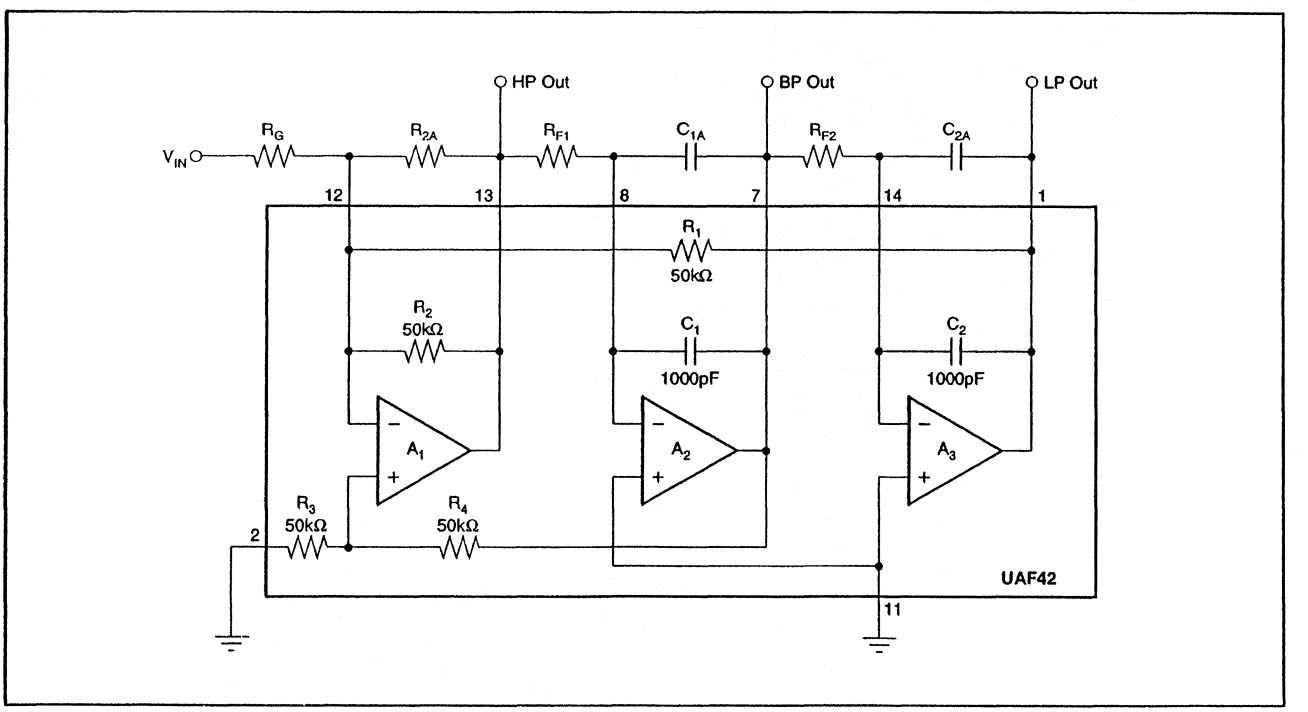


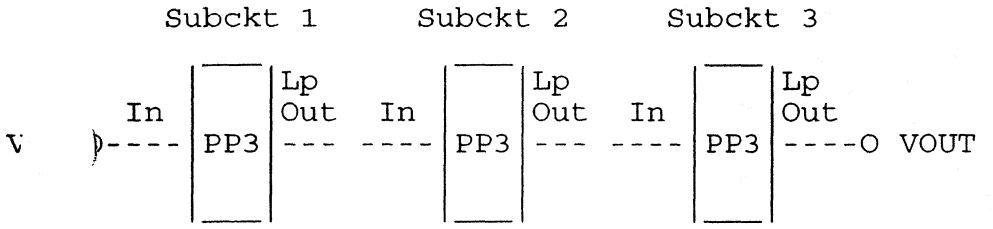
FIGURE 9B. Inverting Pole-Pair Subcircuit Using R_3 to Eliminate External Q-Setting Resistor R_G.

UAF42 Filter Component Values

R nse: Lowpass Topology: Inverting f-3dB : 50.00Hz
Type : Butterworth Order n : 6
Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1,2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3 ----	50.00Hz ----	517.6m ----	---- ----	3.183M ----	90.43k ----	50.00k 1.000	----
Sub Ckt 2	PP3 ----	50.00Hz ----	707.1m ----	---- ----	3.183M ----	44.59k ----	50.00k 1.000	----
Sub Ckt 3	PP3 ----	50.00Hz ----	1.932 ----	---- ----	3.183M ----	10.43k ----	50.00k 1.000	----

Filter Block Diagram



Build this filter by connecting filter subcircuits in order as shown in the 'Filter Block Diagram' above. See Application Bulletin AB-035 for detailed schematics of subcircuits. When no value is shown for a component in the 'Filter Component Values' table, omit the component.

Passband gain : 1.00 V/V (0 dB)
Max Input : 10.00 V (Vs=+-15V)

Freq(Hz)	Gain (DB)	V_{OUT}* insert 1 Vpp
10	0	1
40	-.3	.97
50	-2.85	.72
60	-9.6 db	.33
70	-17	.14
80	-24	.063
90	-30	.032
100	-36	.016

$\frac{V_{out}}{V_{in}}_{db} = 20 \log \frac{V_{out}}{V_{in}}$

$20 \log \frac{V_o}{V_{in}} = \alpha db$

$\log_{10} \frac{V_o}{V_{in}} = \frac{\alpha}{20}$

$\frac{V_o}{V_{in}} = 10^{\frac{\alpha}{20}}$

* V_{in} = 1 volt (p-p or RMS)

500 Hz

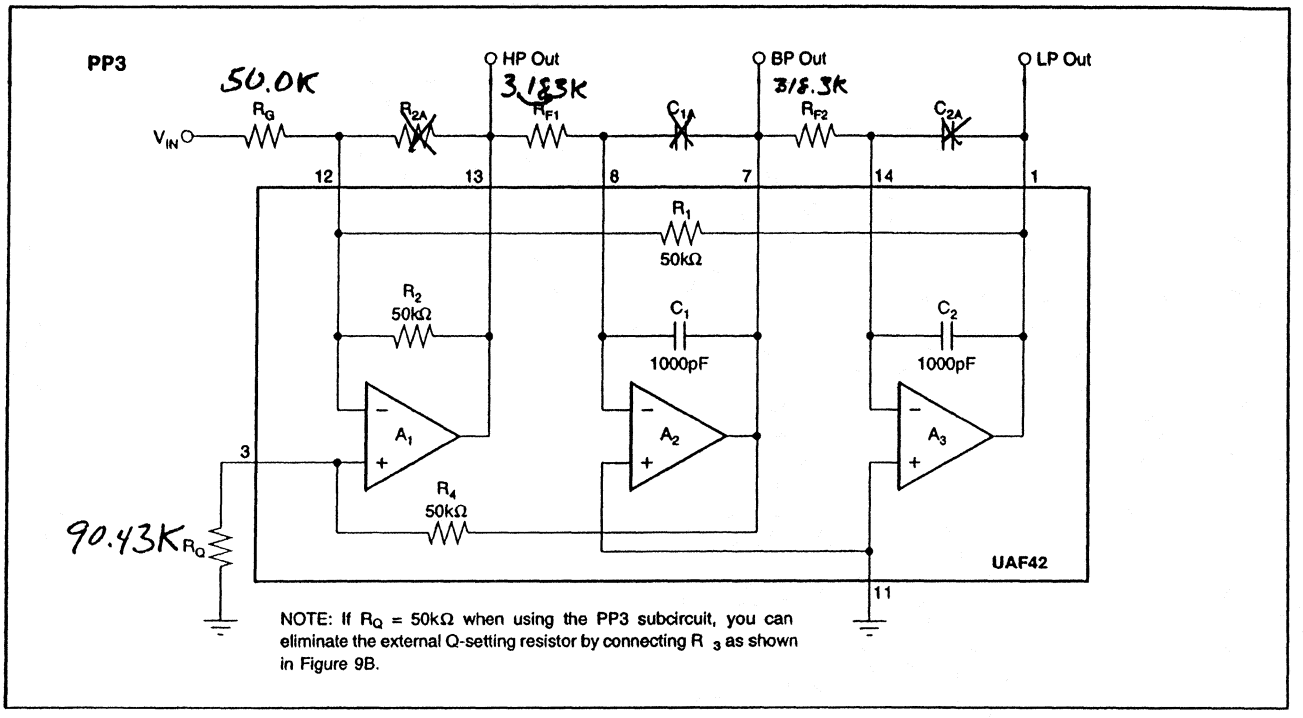


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

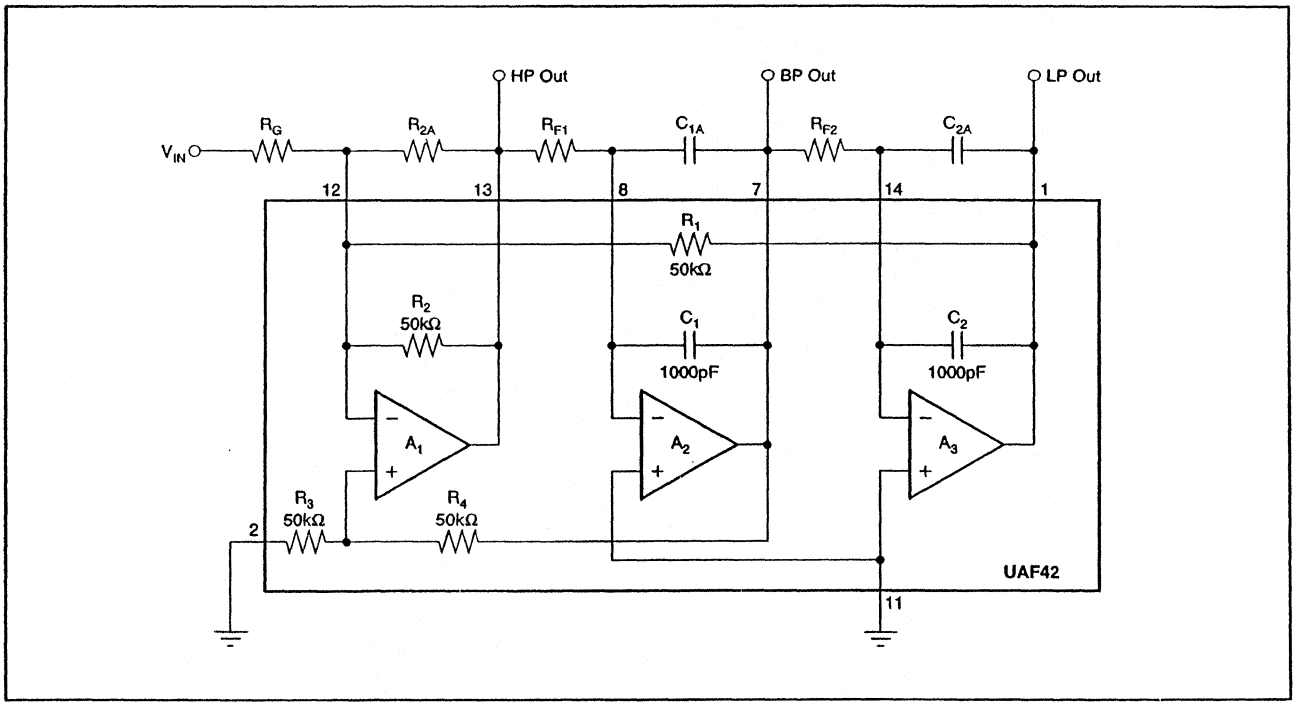


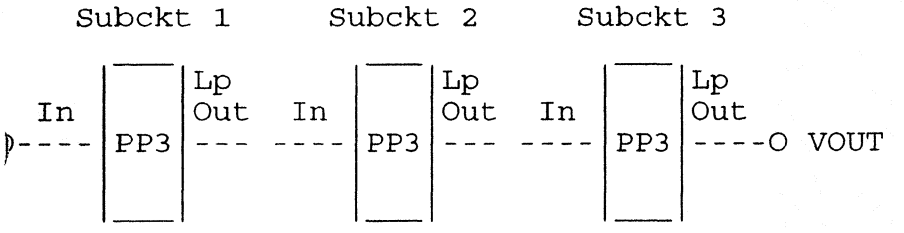
FIGURE 9B. Inverting Pole-Pair Subcircuit Using R_3 to Eliminate External Q-Setting Resistor R_G.

UAF42 Filter Component Values

Response: Lowpass Topology: Inverting f-3dB : 500.0Hz
Type : Butterworth Order n : 6
Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1,2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3 ----	500.0Hz ----	517.6m ----	---- ----	318.3k ----	90.43k ----	50.00k 1.000	----
Sub Ckt 2	PP3 ----	500.0Hz ----	707.1m ----	---- ----	318.3k ----	44.59k ----	50.00k 1.000	----
Sub Ckt 3	PP3 ----	500.0Hz ----	1.932 ----	---- ----	318.3k ----	10.43k ----	50.00k 1.000	----

Filter Block Diagram



Build this filter by connecting filter subcircuits in order as shown in the 'Filter Block Diagram' above. See Application Bulletin AB-035 for detailed schematics of subcircuits. When no value is shown for a component in the 'Filter Component Values' table, omit the component.

Passband gain : 1.00 V/V (0 dB)
Max Input : 10.00 V (Vs=+-15V)

Freq (Hz)	Gain (DB)	VOUT (CALC)	VOUT (MEAS.)
100	0	1	1
400	-.3	.97	.96
500	-2.85	.72	.69
600	-9.6	.33	.33
700	-17	.14	.13
800	-24	.063	.072
900	-30	.032	.043
1000	-36	.016	.021

5000 Hz

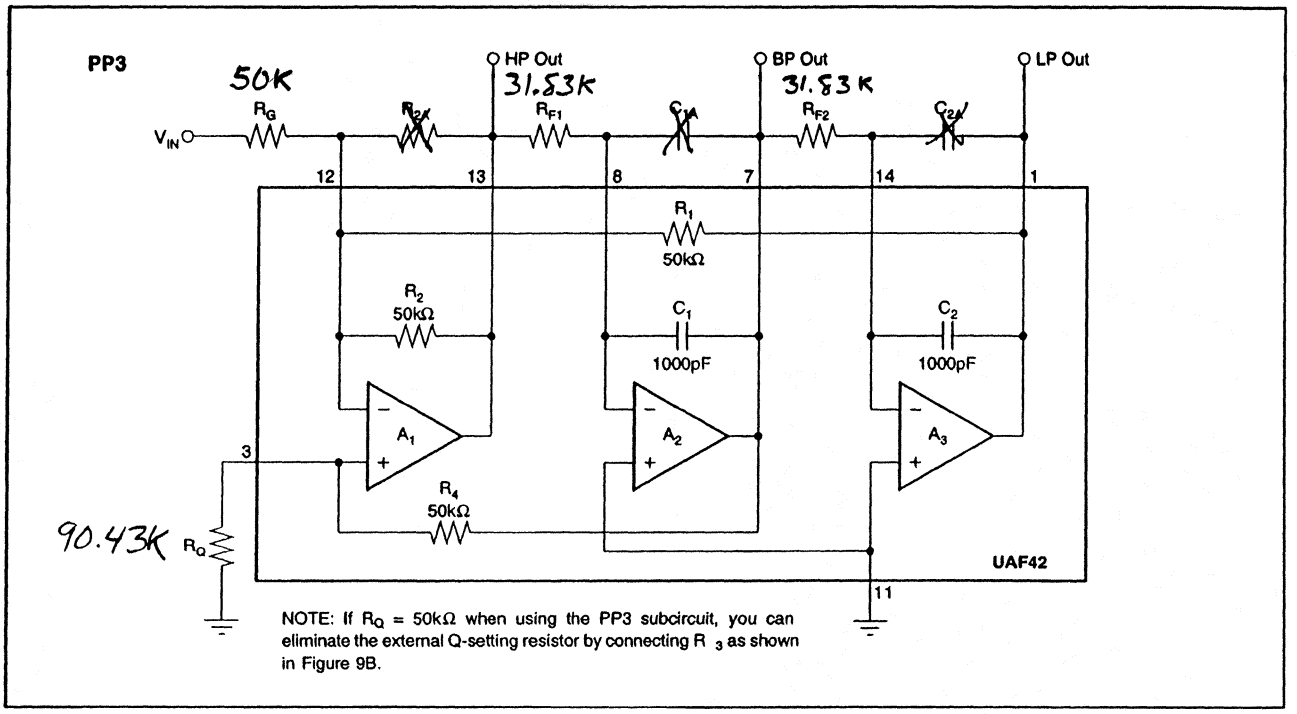


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

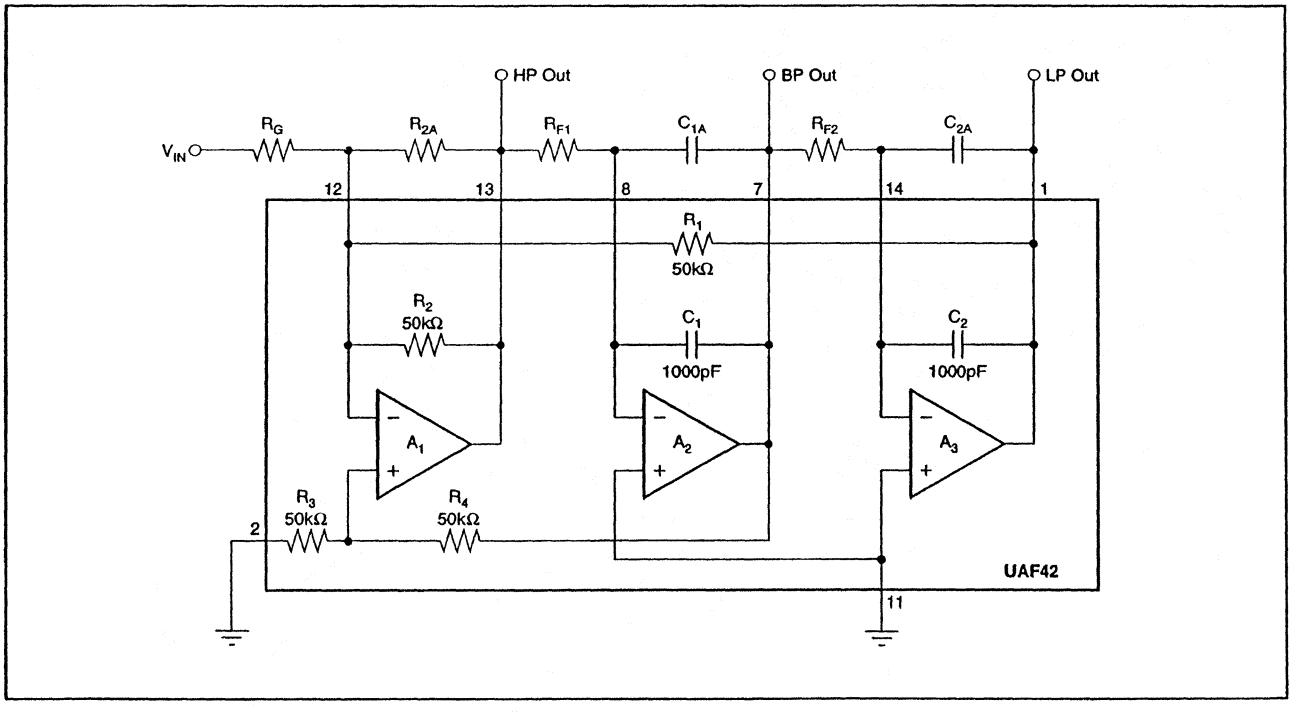


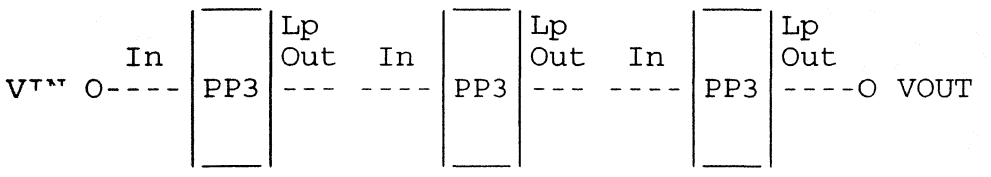
FIGURE 9B. Inverting Pole-Pair Subcircuit Using R_3 to Eliminate External Q-Setting Resistor R_G.

UAF42 Filter Component Values

R· ·onse: Lowpass Topology: Inverting f-3dB : 5.000kHz
T : Butterworth Order n : 6
Resistors : exact

	Subckt C ext	fo Rp	Q Cp	fz Rz1	RF1,2 Rz2	RQ Rz3	RG Ckt-gain	R2A
Sub Ckt 1	PP3 ----	5.000kHz ----	517.6m ----	---- ----	31.83k ----	90.43k ----	50.00k 1.000	----
Sub Ckt 2	PP3 ----	5.000kHz ----	707.1m ----	---- ----	31.83k ----	44.59k ----	50.00k 1.000	----
Sub Ckt 3	PP3 ----	5.000kHz ----	1.932 ----	---- ----	31.83k ----	10.43k ----	50.00k 1.000	----

Filter Block Diagram

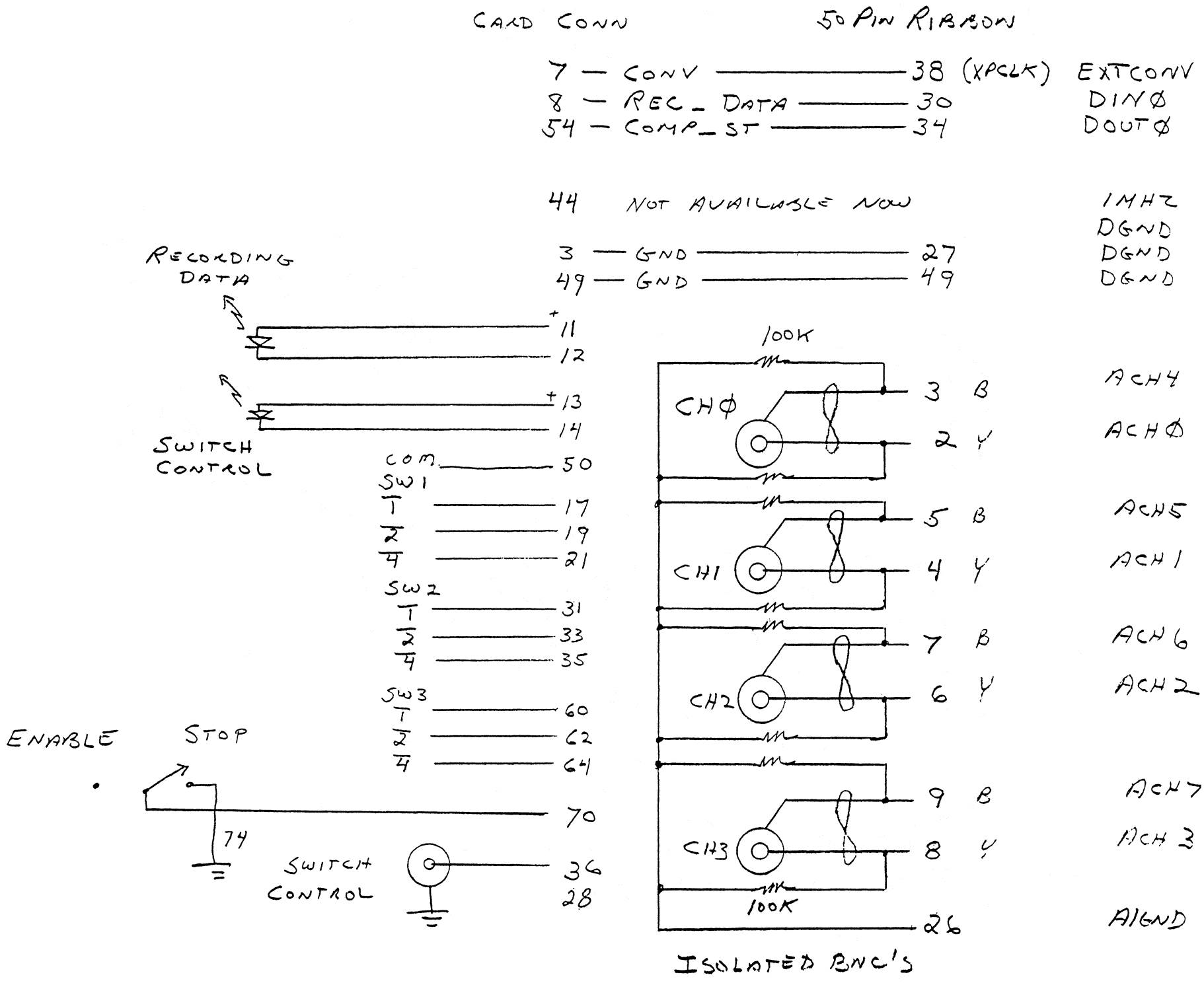


Build this filter by connecting filter subcircuits in order as shown in the 'Filter Block Diagram' above. See Application Bulletin AB-035 for detailed schematics of subcircuits. When no value is shown for a component in the 'Filter Component Values' table, omit the component.

Passband gain : 1.00 V/V (0 dB)
Max Input : 10.00 V (Vs=+-15V)

Freq (Hz) 1080	Gain 0	V_{out} (calc) 1	V_{out} (meas.) 1
4000	-.3	.97	.96
5000	-2.85	.72	.70
6000	-9.1	.33	.33
7000	-17	.14	.13
8000	-24	.063	.066
9000	-30	.032	.031
10000	-36	.016	.020

RFI AID TEST


CARD CONN
50 PIN RIBBON
7 — CONV — 38 (XPCLK) EXTCONV
8 — REC_DATA — 30 DINØ
54 — COMP_ST — 34 DOUTØ
44 NOT AVAILABLE NOW 1MHZ
3 — GND — 27 DGND
49 — GND — 49 DGND
RECORDING DATA
+ 11
12
+ 13
14
SWITCH CONTROL
COM 50
SW1
1 17
2 19
4 21
SW2
1 31
2 33
4 35
SW3
1 60
2 62
4 64
ENABLE
STOP
70
74
SWITCH CONTROL
36
28
100K
CHØ
3 B
2 Y
ACH4
ACHØ
5 B
CH1
4 Y
ACH5
ACH1
7 B
CH2
6 Y
ACH6
ACH2
9 B
CH3
8 Y
ACH7
ACH3
100K
26
AIGND
ISOLATED BNC'S

5/26/98

IN SWITCHING TO A KIETHLY A/D HAVE TO GENERATE A 1MHZ CLOCK SINCE ONE IS NOT AVAILABLE FROM THE A/D. HAVE TO ADD TWO CHIPS U31 & U32.

U31 LS19C

1	C40	14	B40
2	41	13	41
3	42	12	42
4	43	11	43
5	44	10	44
6	45	9	45
7	C46	8	B46

U32 OSC

1	C49	14	B49
2	50	13	50
3	51	12	51
4	52	11	52
5	53	10	53
6	54	9	54
7	C55	8	B55

ADD

U31-14 TO +5
U31-7 TO GND

U32-14 TO +5
U32-7 TO GND

U31-1 TO U31-13
U31-1 TO U30-4

U31-12 TO U31-8

U32-8 TO U31-6

ADD

B40 - B43V
C46 - B47G

B49 - B51V
C55 - B55G

C40 - B41
C40 - L46

B42 - B46

B55 - C45

REMOVE

U5-1 TO PIN 44

REMOVE

C23 - A44

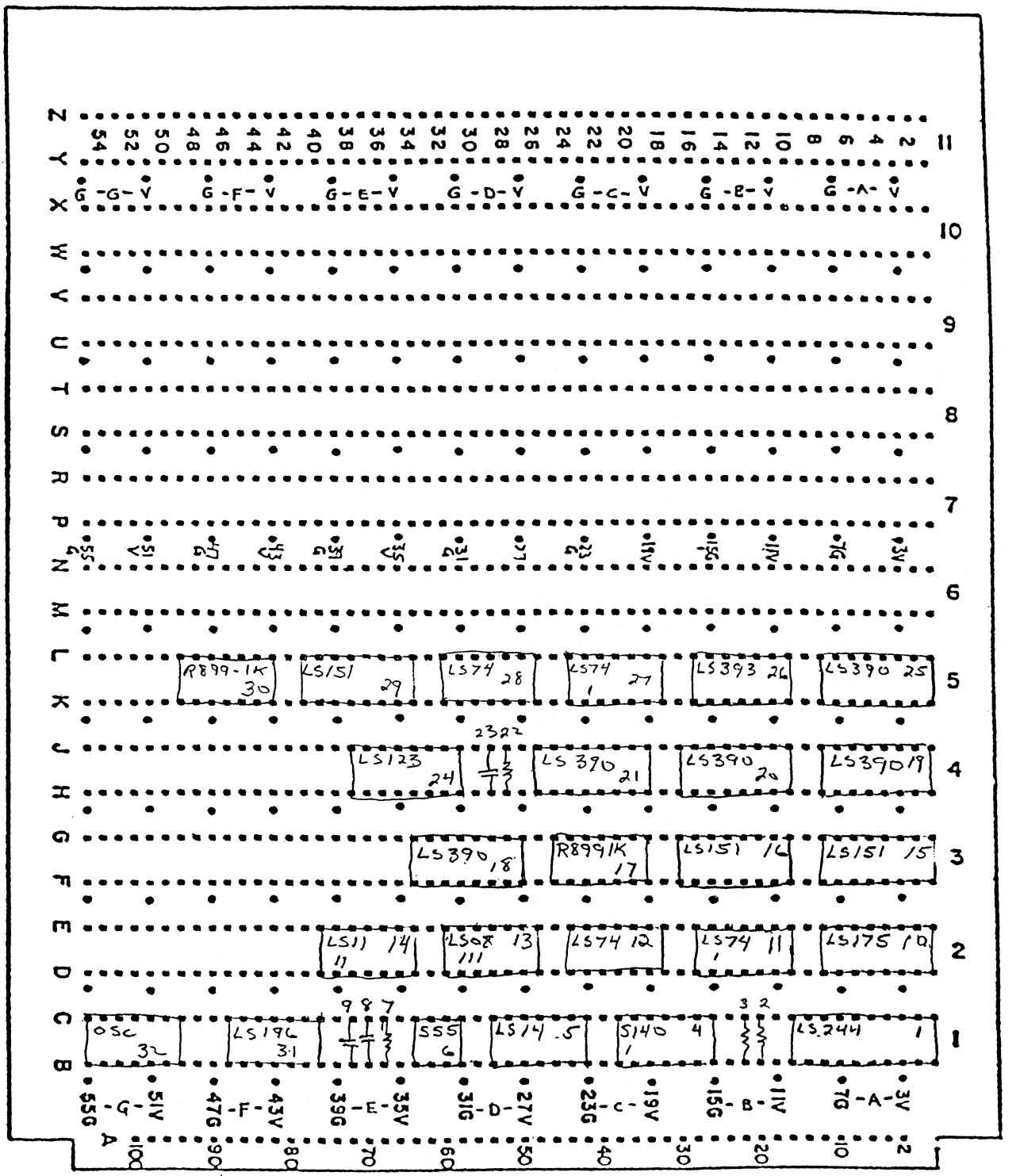
ADD

U5-1 TO U31-5

ADD

C23 - C44

RFI TEST A/D CONTROL

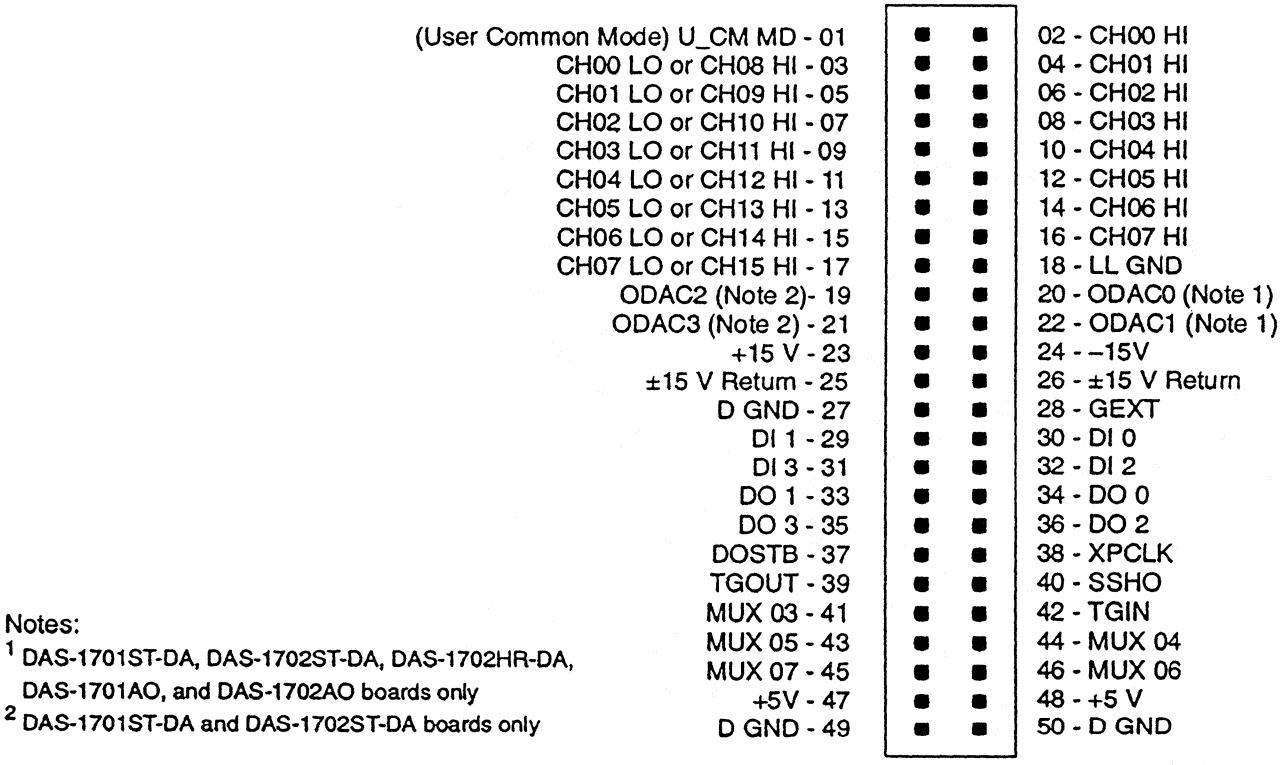


U		
4	S140	1
11	74	1
13	08	111
14	11	11
24	123	1
27	74	1

U2-3 470Ω
U7 1M
U8 1MΩ
U9 .01MΩ
U22 39K
U23 680PF

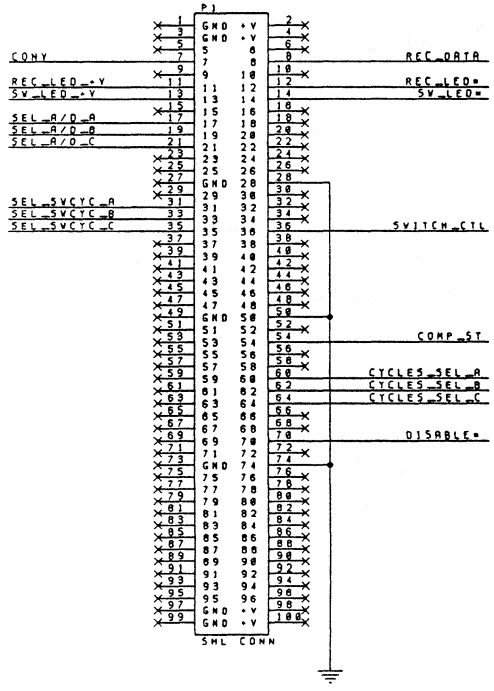
STA-1800U I/O Connectors J1 and J2

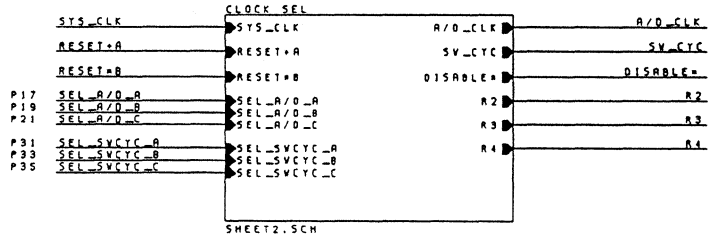
Pin assignments for I/O connectors J1 and J2 of the STA-1800U screw terminal accessory are shown in Figure B-2.

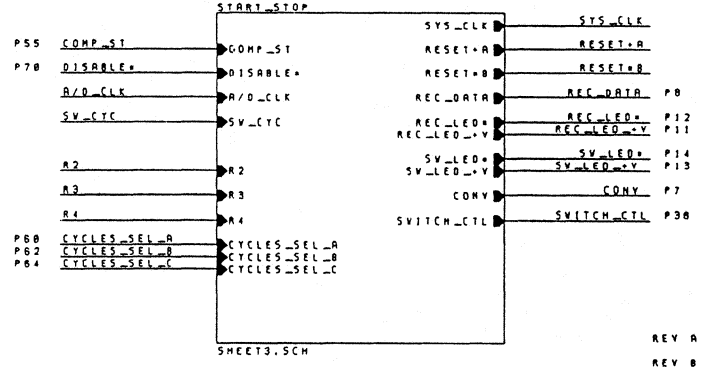


Notes:
[1] DAS-1701ST-DA, DAS-1702ST-DA, DAS-1702HR-DA, DAS-1701AO, and DAS-1702AO boards only
[2] DAS-1701ST-DA and DAS-1702ST-DA boards only

Figure B-2. STA-1800U I/O Connectors J1 and J2







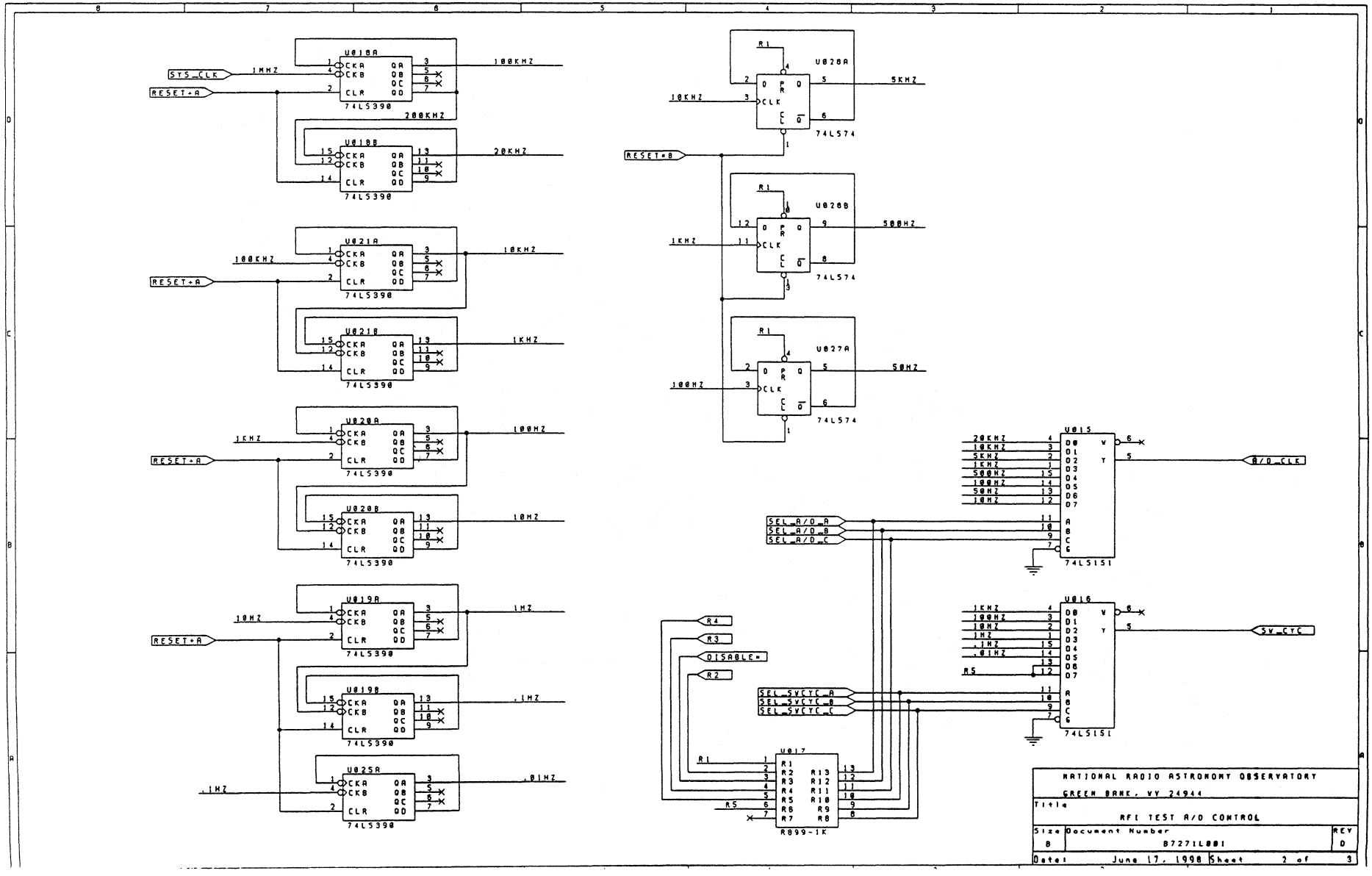
REV A CORRECTED SENSE OF RESET FOR LS390 & 393

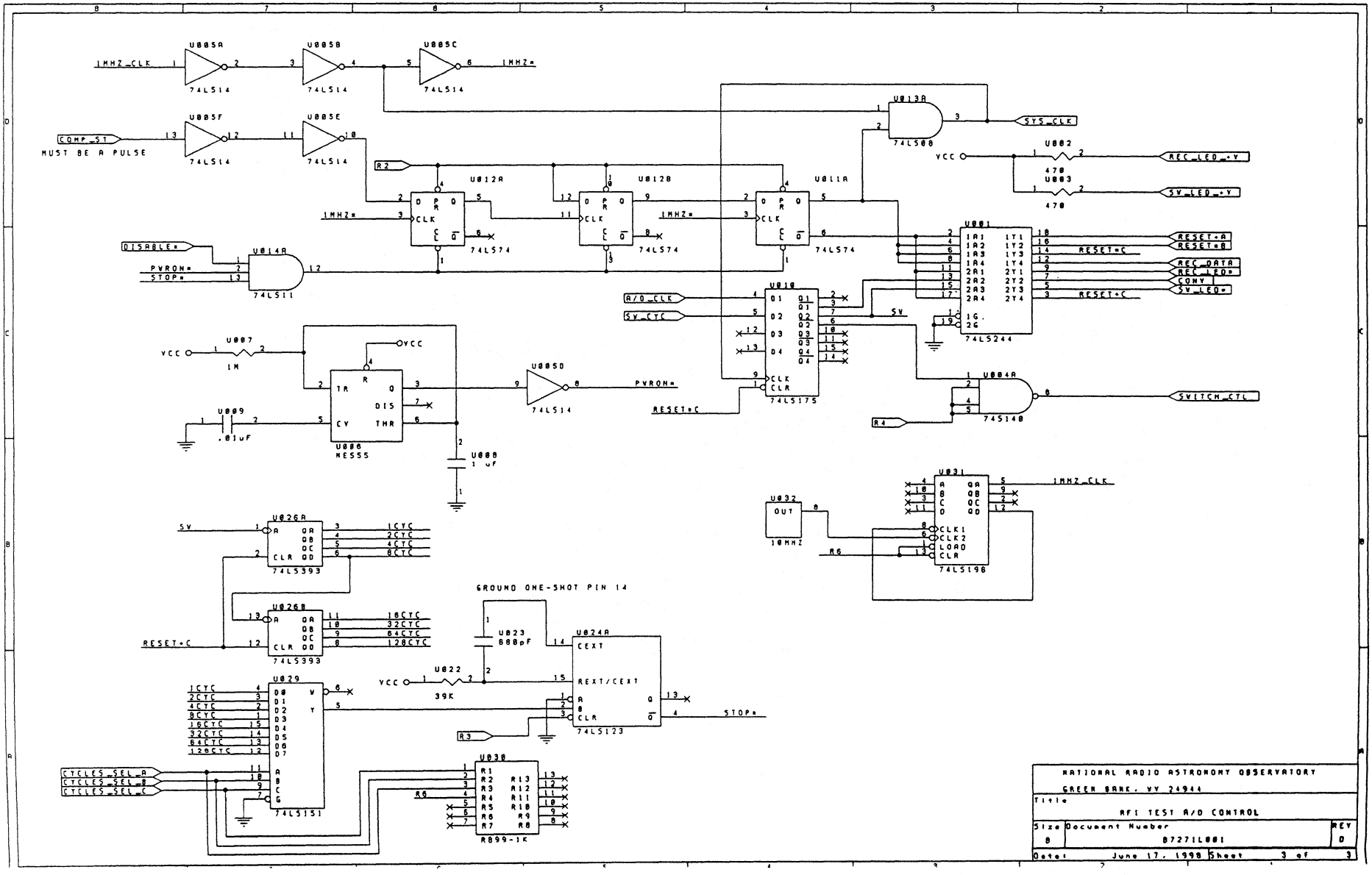
REV B CORRECTED INPUT TO ONE-SHOT U24

REV C REPLACED EXTERNAL 1MHZ CLOCK WITH INTERNAL CLOCK OSCILLATOR

REV D CHANGED THE SENSE OF THE A/D CLOCK TO CLOCK ON THE NEG. EDGE FOR THE KIETHLY A/D

NATIONAL RADIO ASTRONOMY OBSERVATORY GREEN BANK WV, 24944		
Title RFI TEST A/D CONTROL		
Size B	Document Number 87271L001	REV D
Date: June 17, 1998	Sheet 1 of 3	


U018A
SYS_CLK
1MHZ
RESET*A
100KHZ
200KHZ
74LS390
U018B
20KHZ
U021A
10KHZ
U021B
1KHZ
U020A
100HZ
U020B
10HZ
U019A
1HZ
U019B
.1HZ
U025A
.01HZ
U020A
5KHZ
74LS74
U020B
500HZ
U027A
50HZ
U015
74LS151
A/D_CLK
SEL_A/D_A
SEL_A/D_B
SEL_A/D_C
U016
SV_CYC
SEL_SVCYC_A
SEL_SVCYC_B
SEL_SVCYC_C
R4
R3
DISABLE*
R2
R5
R1
U017
R899-1K
NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, WV 24944
Title
RFI TEST A/D CONTROL
Size
B
Document Number
87271L001
REV
D
Date: June 17, 1998 Sheet 2 of 3



NATIONAL RADIO ASTRONOMY OBSERVATORY		
GREEN BANK, WV 24944		
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Date: June 17, 1998	Sheet 3 of 3	