NATIONAL RADIO ASTRONOMY OBSERVATORY
Charlottesville, Virginia

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Title: **140-ft MODCOMP CONTROL COMPUTER DATA OUTPUT**

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140-FT MODCOMP CONTROL COMPUTER DATA OUTPUT

Ronald B. Weimer

Introduction

The control computer at the 140-ft telescope collects observing data, stores it on the disk and does some preliminary data reduction. The data comes from the autocorrelator, digital standard receiver, or A/D converter. Log information is also included along with the data. At the present time a copy of the stored data is sent over a 16-bit wide data channel to the analysis Modcomp. In order to improve the data analysis at the telescope we needed to make the data available in real time to a more modern computer system. No ethernet interface to the Modcomp computers is available. Changing the programs to handle a new interface would be difficult. What we tried to do is develop an interface that would be transparent to the current program and hardware. It turned out that Bob Vance, Ron Maddalena, and Allen Farris modified the data transmission program slightly to make synchronization easier. The original intent was to pipe the data to a Sun model 3/60 workstation. It would accept the data, convert Modcomp floating point numbers to standard numbers, store the data on disk, and make it available for reduction either on itself or over the ethernet loop to a remote terminal. We got the data link running but had trouble with missing data when the Sun got busy doing data reduction. As a consequence, the system was modified so that the data is first piped to an Apple Mac II which modifies the numbers and sends it over ethernet to the Sun. This report describes the electronics in the Modcomp that captures the control computer to analysis computer data stream and transmits it to the Mac II.

Description of Electronics

The Modcomp link was built on a General Purpose Controller by Dwayne Schiebel. The signals of interest are: 16 bits of data (OUT1N to OUT16N), an output data strobe (OUDCM), a transfer initiate signal (XFERN), and Master Clear (ICBFB). A 5 MHz clock (CLKFBN) was brought in but was not used. The input data word is broken up into two 8-bit bytes, stored in a first in/first out (FIFO) memory and then sent to the Mac II over an RS-232 serial-data link.

The maximum buffer size was around 5000 16-bit words. The FIFO will handle 12 K bytes--3 each 4 K x 9 bits.

Figure 1 schematic. The FIFO's are cleared by Master Clear or by the start of a new Modcomp transfer (6G). Data input is bussed thru the 74LS240 (9C, 9D) into the input of the FIFO's (11A, 11B, 11C). A 4.90 MHz crystal oscillator (8D) is used for local clocks and the baud rates for the serial data links. A data sheet is included on the IDT 7204 used as a FIFO.

Figure 2 schematic. An OUDCMN pulse starts a sequence of loading 2 bytes into the FIFO input (7F, 7E). $\overline{\text{OEMS}}$ and $\overline{\text{OELS}}$ selects which byte is to be loaded, and $\overline{\text{W}}$ signal strobes the data into the FIFO. The FIFO output buss Q0 thru Q7 is used on page 3. EF signal (6F, 6A) is high if all 3 chips are empty.

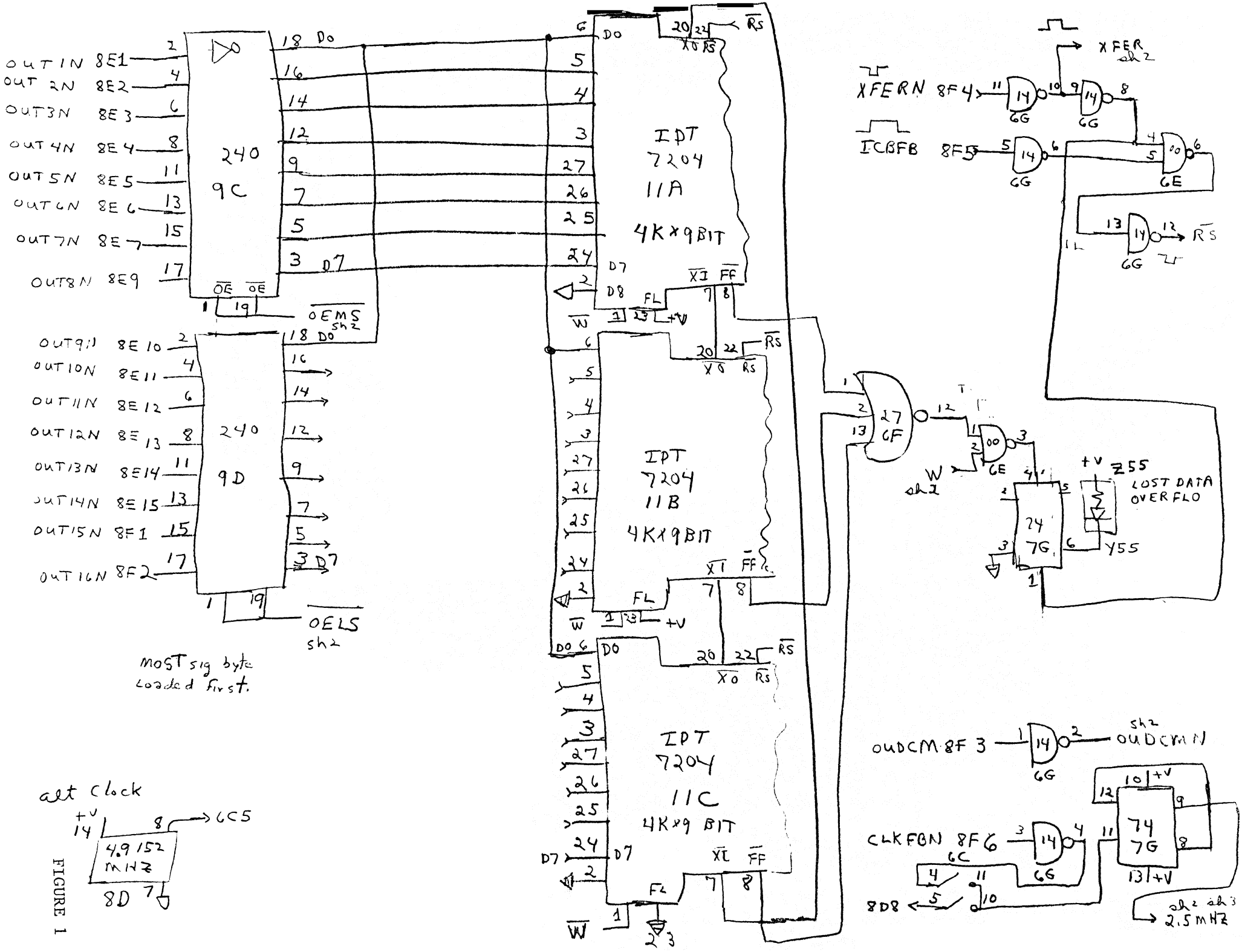
Figure 3 schematic. Chip 6D divides the crystal oscillator clock down to provide baud rate clocks. Note: A switch is shown for baud rate select but only 9600 should be used. $\overline{EF}$ is gated with either DTR or the XON/XOFF signal (sheet 5) to initiate the serial data out. DTR is not used in the Mac II link. Chips 7B, 7C, 7D, and 8B generate the signals to read a byte out of the FIFO, load it in a shift register, and shift the data out. Chips 7A and 8A form the data shift register. The chip in 1B shifts the TTL level to RS-232 signal levels. A data sheet for this chip is also included. One TTL to RS-232 circuits is not used. The same chip shifts RS-232 levels back to TTL. One circuit is used for the DTR signal and one for the receive data on page 5.

Figure 4 schematics. These circuits are for test only. To use, the ribbon cables from the GPC are removed and test jumpers from 4F and 4G to 8E and 8F are plugged in. A dip carrier holding two switches is then plugged into slot 4A. The jumpers and switches are in the brown folder for the circuits. Pressing the reset switch simulates a transfer initiate; then pressing the start switch loads 5 K words into FIFO, which starts the serial data output sequence.

Figure 5 schematics. This is the XON/XOFF circuit added. Receive data is level shifted by the 232 chip and fed to a UART (1D). XON/XOFF is decoded (3F, 3C) and sets or resets a flip flop (3D). A data sheet for the CDP 1854 is included. (UART is the courtesy of Ed Childers.)

Physical Layout

The circuit was constructed on a Shalloway card, mounted in an empty slot in the same page as the Modcomp to Modcomp link transmitter. Two 16-pin ribbon cables connect from the GPC to the Shalloway card. Data link connections are via the edge connector as well as +5 V power supply. A male DB 25 connector is mounted on the back of the PCI. The Mac II cable ended up with three conductor, ground and two data. A copy of the card layout is included (Figures 6 and 7). Also, a wire list from the GPC is included (Figure 8). Wirewrap lists are not included. They are in the brown folder.


OUT 1N 8E1
OUT 2N 8E2
OUT 3N 8E3
OUT 4N 8E4
OUT 5N 8E5
OUT 6N 8E6
OUT 7N 8E7
OUT 8N 8E9
240
9C
OE OE
OEMS sh2
OUT 9N 8E10
OUT 10N 8E11
OUT 11N 8E12
OUT 12N 8E13
OUT 13N 8E14
OUT 14N 8E15
OUT 15N 8F1
OUT 16N 8F2
240
9D
OELS sh2
most sig byte loaded first.
IDT 7204 11A 4K x 9 BIT
IDT 7204 11B 4K x 9 BIT
IDT 7204 11C 4K x 9 BIT
XFERN 8F4
ICBFB 8F5
XFER sh2
RS
OUDCM 8F3
OUDCMN sh2
CLKFBN 8F6
8D8
74 7G
sh2 sh3 2.5 MHZ
W sh2
LOST DATA OVERFLO
Y55
alt Clock
4.9152 MHZ
8D 7
GC5
FIGURE 1

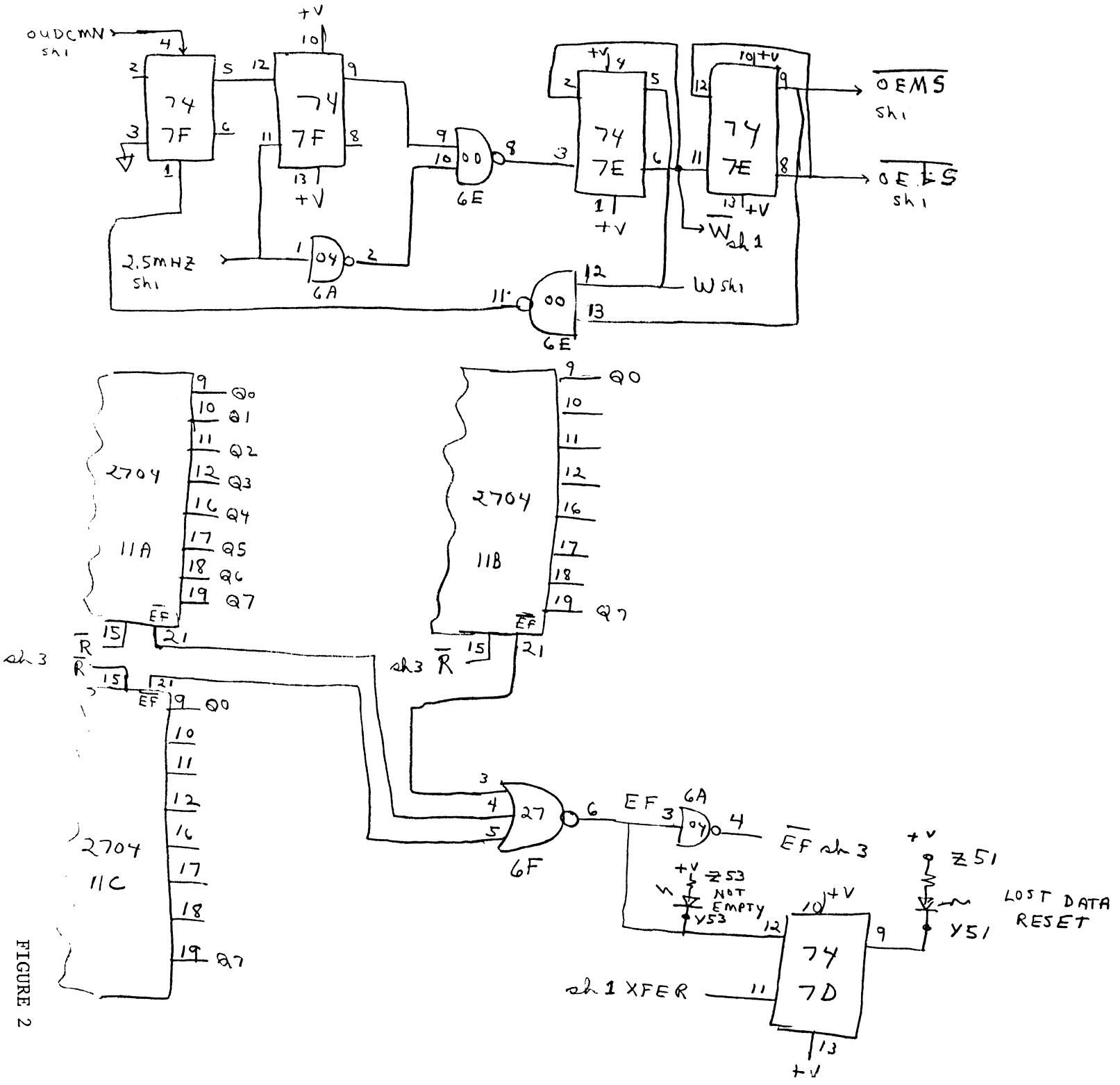

OUDCMN sh1
74 7F
74 7F
74 7E
74 7E
74 7D
00
04
2.5MHZ sh1
+V
6E
6A
W sh1
W sh 1
OEMS sh1
OES sh1
2704 11A
2704 11B
2704 11C
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
EF
R
sh3 R
sh3
27
6F
EF 6A
EF sh 3
Z53 NOT EMPTY
Y53
Z51
Y51
LOST DATA RESET
sh 1 XFER

FIGURE 2

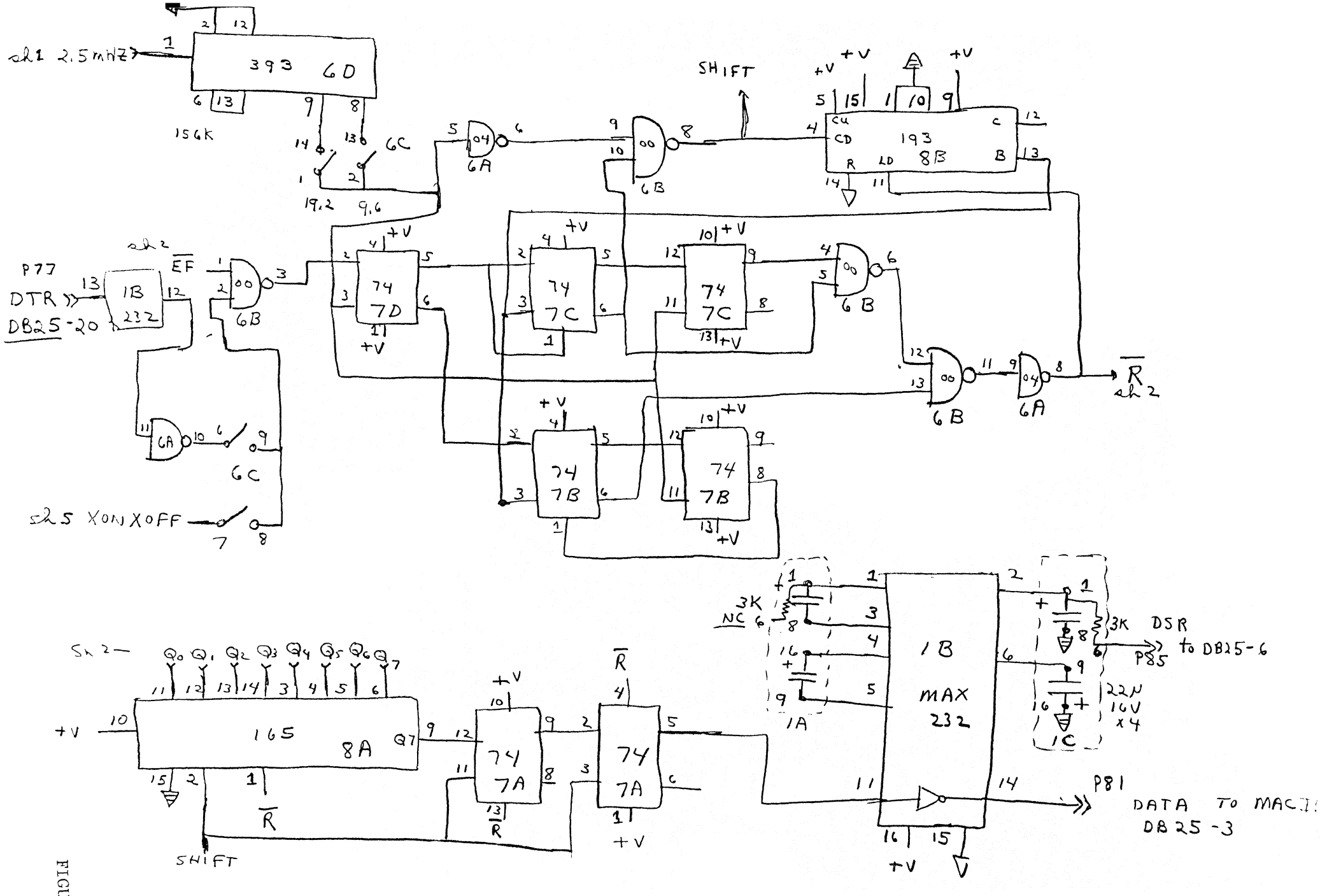
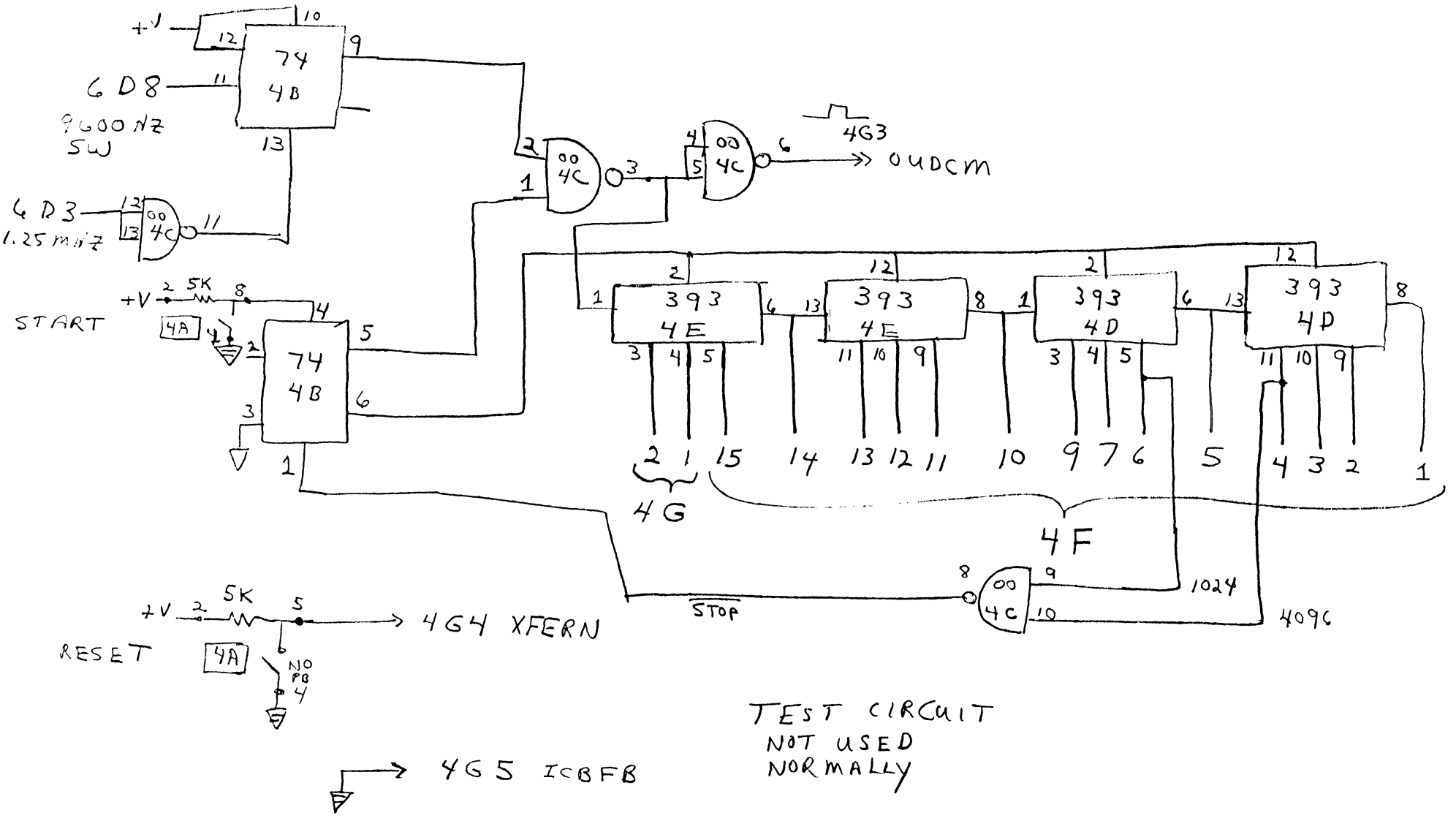

clk 2.5mHZ
393 6D
156K
SHIFT
+V
193 8B
6A
6B
P77
DTR
DB25-20
1B 232
EF
74 7D
74 7C
74 7B
6C
clk 2
XON XOFF
3K NC
1A
1B MAX 232
3K DSR
P85
to DB25-6
22N 16V x4
1C
165 8A
74 7A
SHIFT
P81
DATA TO MAC II
DB 25 -3

FIGURE 3


+V
6D8
9600 NZ
SW
74
4B
6D3
1.25 MHZ
00
4C
START
5K
4A
RESET
NO
PB
4
393
4E
393
4E
393
4D
393
4P
4G3
OUDCM
2 1 15 14 13 12 11 10 9 7 6 5 4 3 2 1
4G
4F
1024
STOP
4096
4G4 XFERN
4G5 ICBFB
TEST CIRCUIT
NOT USED
NORMALLY
5K 1/8
5K 1/8

4A

FIGURE 4

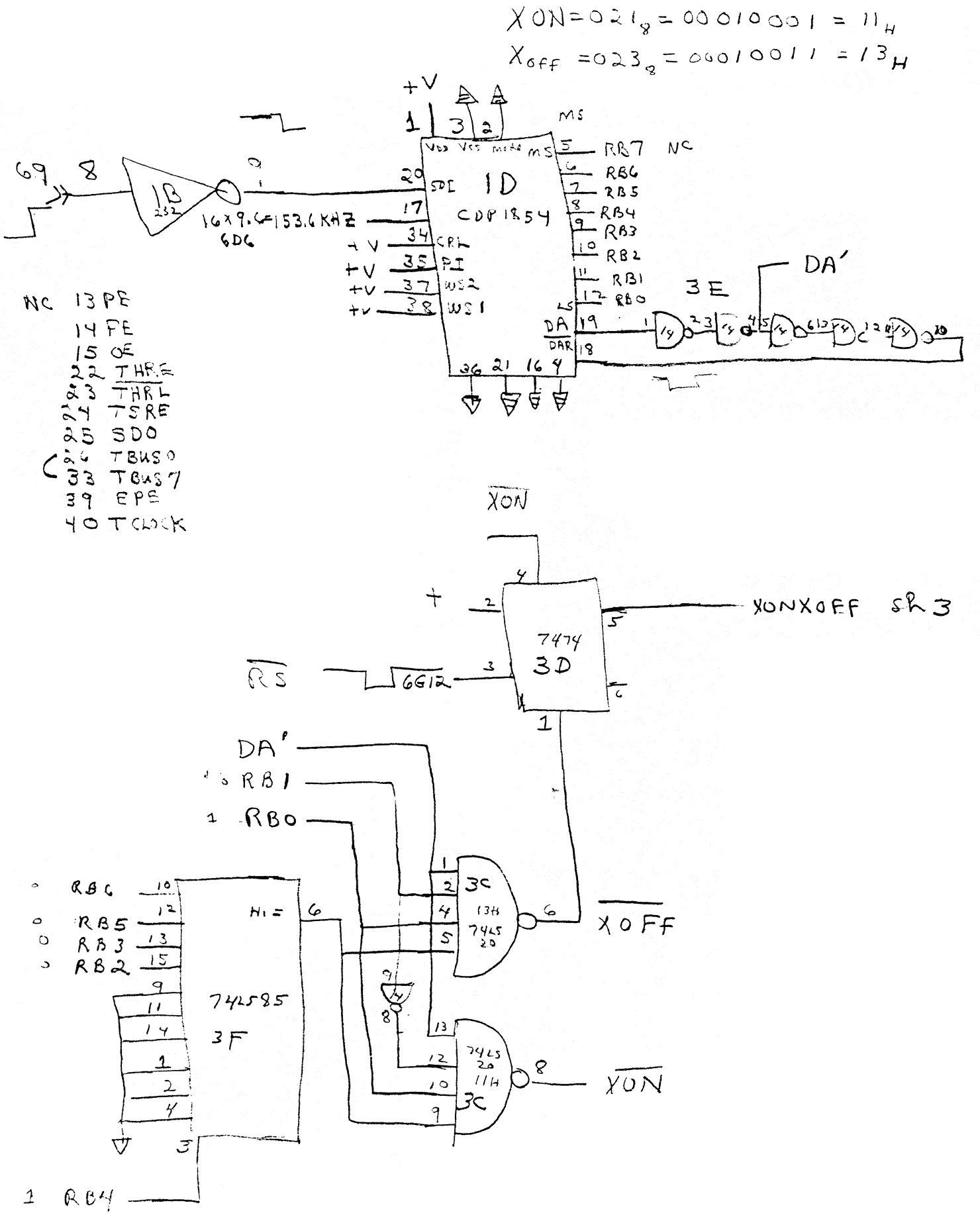

XON = 021₈ = 00010001 = 11H
XOFF = 023₈ = 00010011 = 13H
+V
MS
1D
CDP1854
RB7 NC
RB6
RB5
RB4
RB3
RB2
RB1
RB0
SDI
CRL
PI
WS2
WS1
DA
DAR
16x9.6=153.6 KHZ
6DG
1B
232
3E
DA'
NC 13 PE
14 FE
15 OE
22 THRE
23 THRL
24 TSRE
25 SDO
TBUS0
33 TBUS7
39 EPE
40 TCLOCK
XON
7474
3D
XONXOFF SH 3
RS
6G12
DA'
RB1
RB0
RB6
RB5
RB3
RB2
HI=
74LS85
3F
3C
13H
74LS20
XOFF
11H
XON
RB4

FIGURE 5

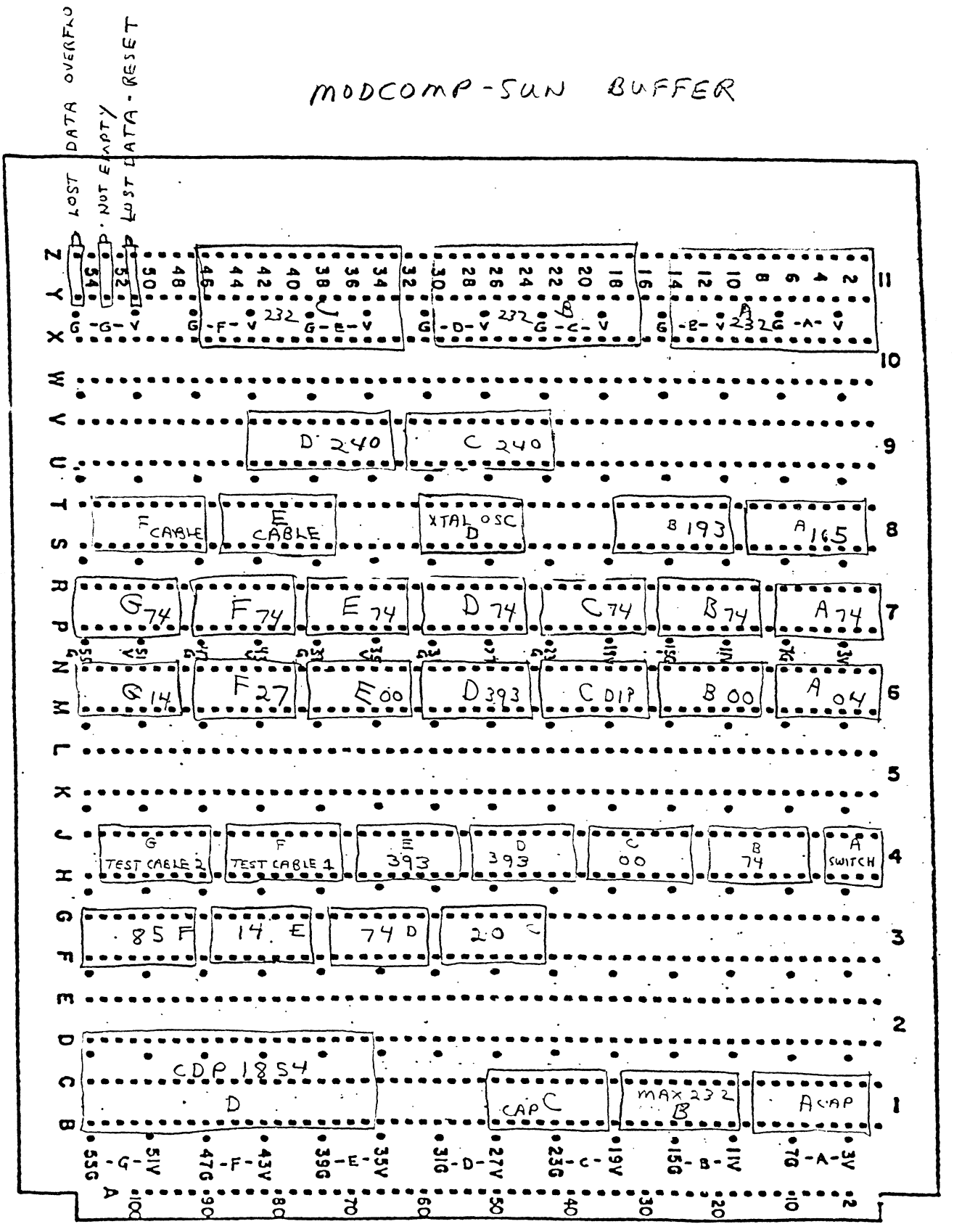
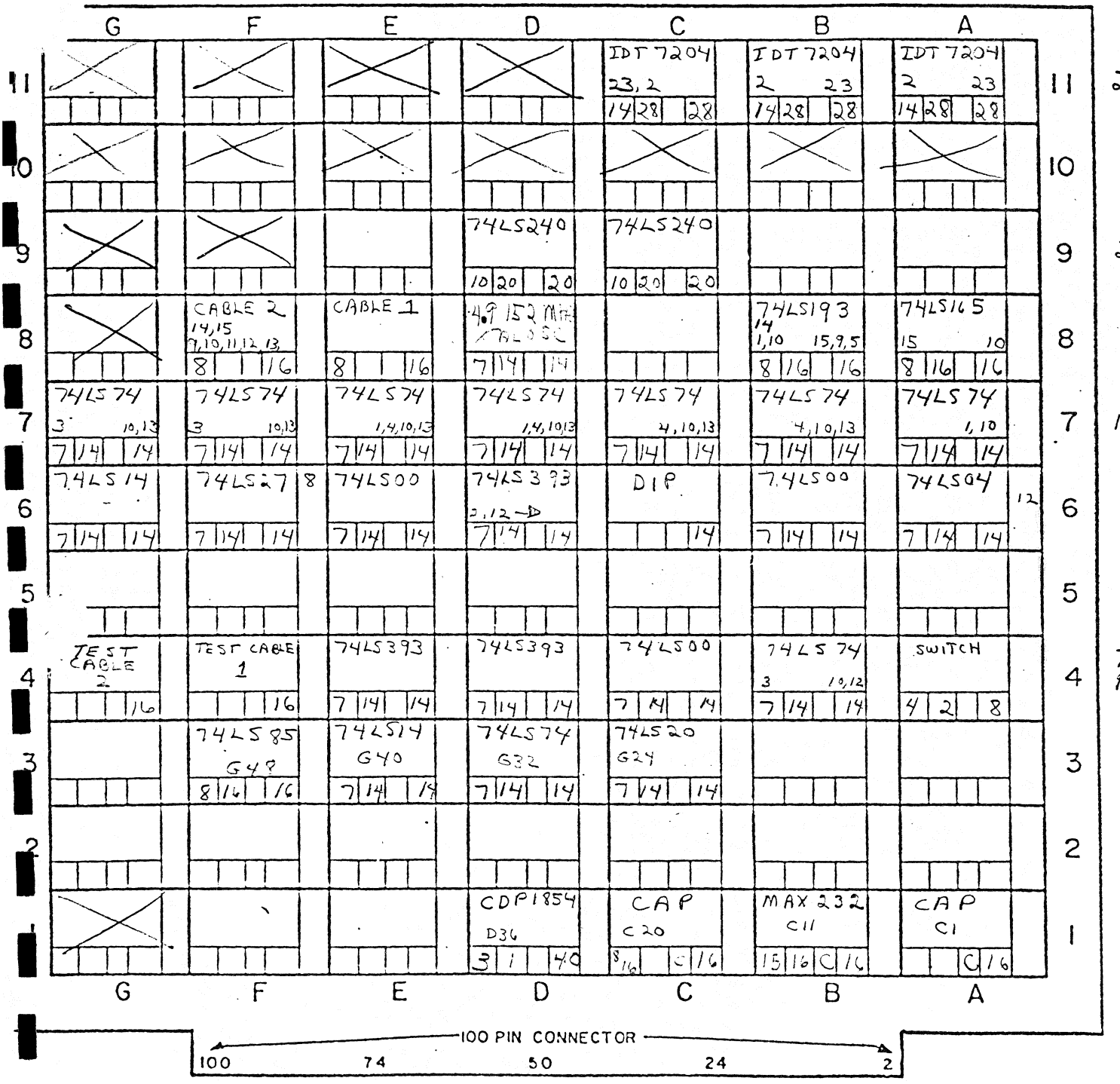

MODCOMP-SUN BUFFER
LOST DATA OVERFLO
NOT EMPTY
LOST DATA - RESET
232
232
232
D 240
C 240
F CABLE
E CABLE
XTAL OSC
D
B 193
A 165
G 74
F 74
E 74
D 74
C 74
B 74
A 74
G 14
F 27
E 00
D 393
C DIP
B 00
A 04
G TEST CABLE 2
F TEST CABLE 1
E 393
D 393
C 00
B 74
A SWITCH
85 F
14 E
74 D
20 C
CDP 1854
D
CAP C
MAX 232
B
A CAP

FIGURE 6

MODCOMP-SUN BUFFER

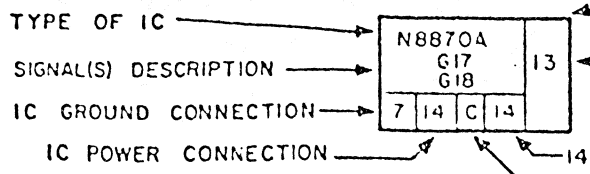
NRAO LOCATION

BY RBW CABLE 1 8E to VGT CABLE 2 8F to VGS DATE 4/15/88



NOTES:

1. SAMPLE BOX



VIEW, COMPONENT SIDE OF BOARD

THIS COLUMN NOT AVAILABLE

4. VCC CONNECTOR PINS: P2,4,98,100 - GND. CONNECTOR PINS: P 1, 3, 27, 49, 73, 97, 99

FIGURE 7

MODCOMP - MODCOMP XMIT GPC

1 6 2 15 3 14

U1S 2	VGT 1	OUT IN
U1S5	VGT2	
U1S7	VGT 3	
U1S 10	VGT 4	
U1S 12	VGT5	
U1S 15	VGT6	
U1T 2	VGT7	
U1T5	VGT9	
U1T7	VGT 10	
U1T 10	VGT11	
U1T 12	VGT12	
U1T 15	VGT13	
U1U 2	VGT14	
U1U5	VGT15	
U1U7	VGS1	
U1U 10	VGS2	OUT 16 N
U2U 10	VGS3	OUDCM
U1R 11	VGS4	XFERN
U3D 6	VGS5	ICBFB
U2D 12	VGS6	CLKFBN 5mHz
	VGS7	
GND	VGS8	hard wired
GND	VGS9	
GND	VGS10	
GND	VGS11	
GND	VGS12	
GND	VGS13	
GND	VGS14	
GND	VGS15	
+VCC	16	hardwired
GND	VGT8	hard wired
+VCC	VGT16	hard wired

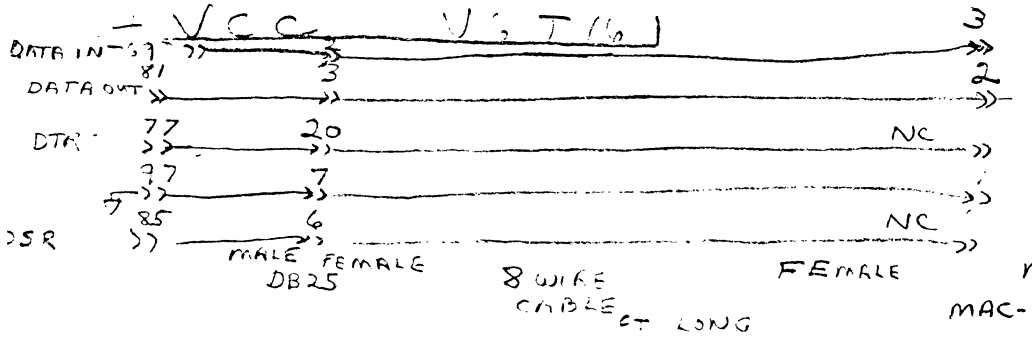


FIGURE 8

TSC232 Dual RS-232 Transmitter/Receiver

General Description

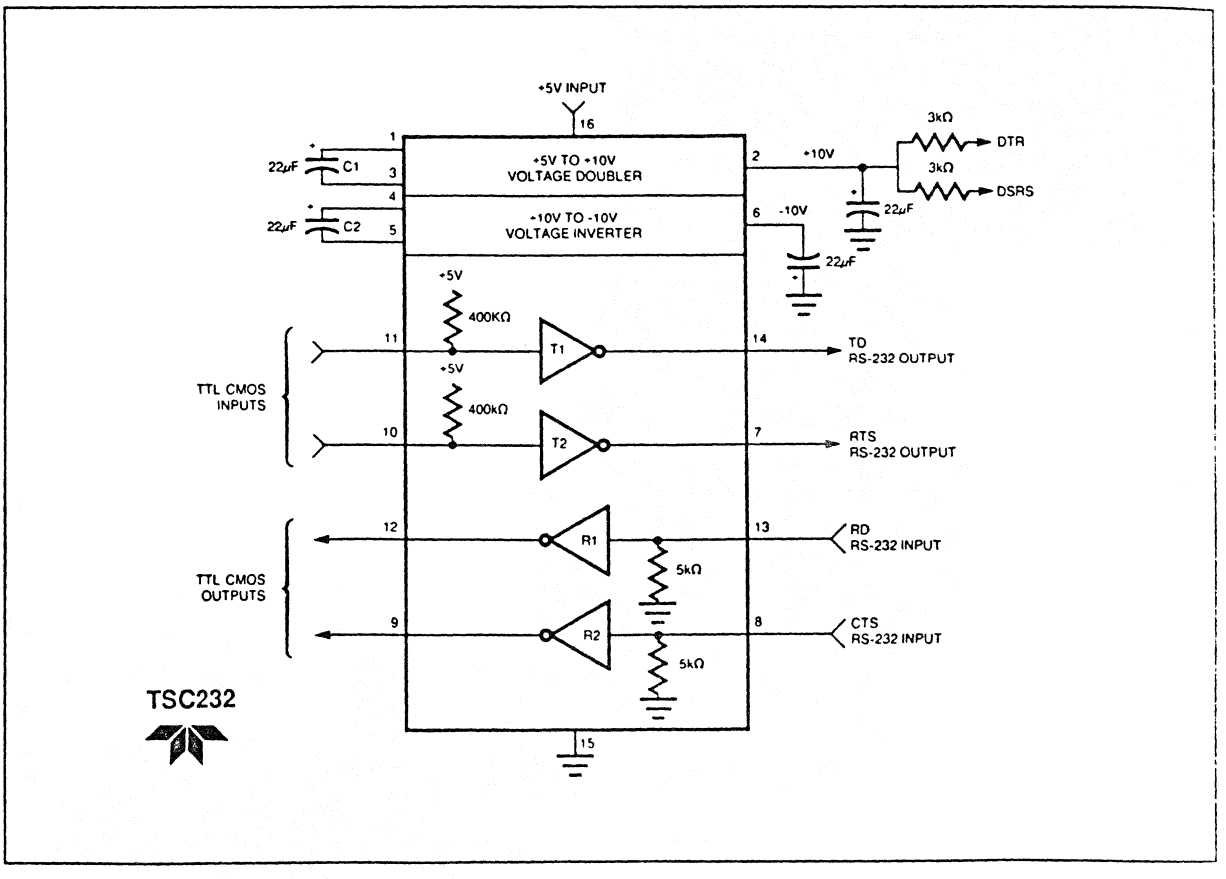
The TSC232 from Teledyne Semiconductor is a dual RS-232 transmitter/receiver that complies with EIA RS-232C guidelines and is ideal for all RS-232C communication links. This device has a 5 V power supply and two charge pump voltage converters that produce +10 V/-10 V power supplies.

The TSC232 has four level translators. Two are RS-232 transmitters that convert TTL/CMOS input levels to 9 V RS-232 outputs. The other two translators are RS-232 receivers that convert RS-232 inputs to 5 V TTL/CMOS output levels. The receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5 V, and can operate with up to ±30 V inputs.

Features

- **Meets all RS-232C Specifications**
- **Operates from Single 5 V Power Supply**
- **2 Drivers and 2 Receivers**
- **Onboard Voltage Quadrupler**
- **±30 V Input Levels**
- **±9 V Output Swing with +5 V Supply**
- **Low Power CMOS: 5 mA**

Functional Diagram



3-21-88

6 each - 7204 5120 P @ 48.60 each!

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

PRELIMINARY
IDT7203S/L
IDT7204S/L

Integrated Device Technology, Inc.

FEATURES:

- First-In, First-Out dual port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  —Active: 660mW (max.)
  —Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201/02
- IDT7204 allows 4096 word structure without expansion
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ II technology
- Available in DIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

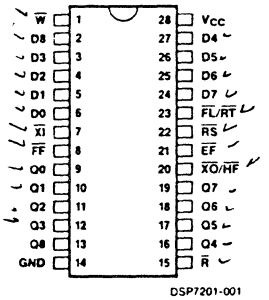
The IDT7203/7204 is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

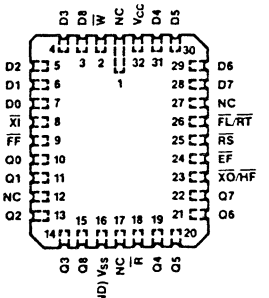
The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

The IDT7203/7204 is fabricated using the high-speed CEMOS™ II, 1.5 micron technology and is available in DIP and LCC screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

PIN CONFIGURATIONS

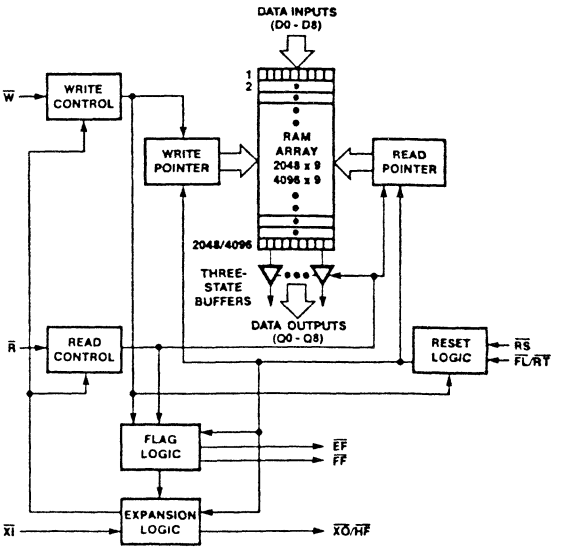


DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0 - D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset. HALF FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual purpose output. In the Multiple Device Mode, this pin is grounded to indicate that it is the first device loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7203/4 can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EXPANSION OUT/HALF FULL FLAG ($\overline{XO}/\overline{HF}$)

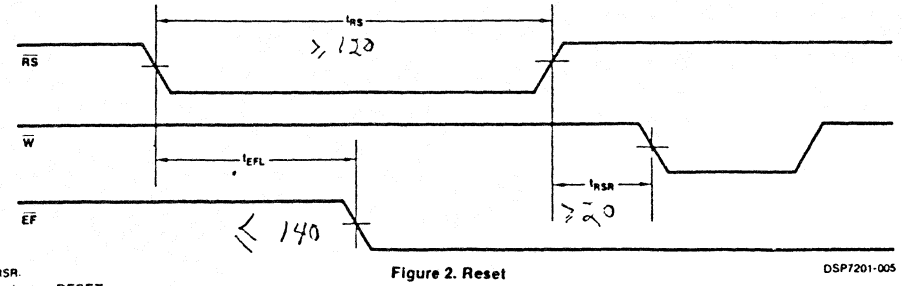
This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Multiple Device Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0 - Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

Figure 2. Reset

DSP7201-005

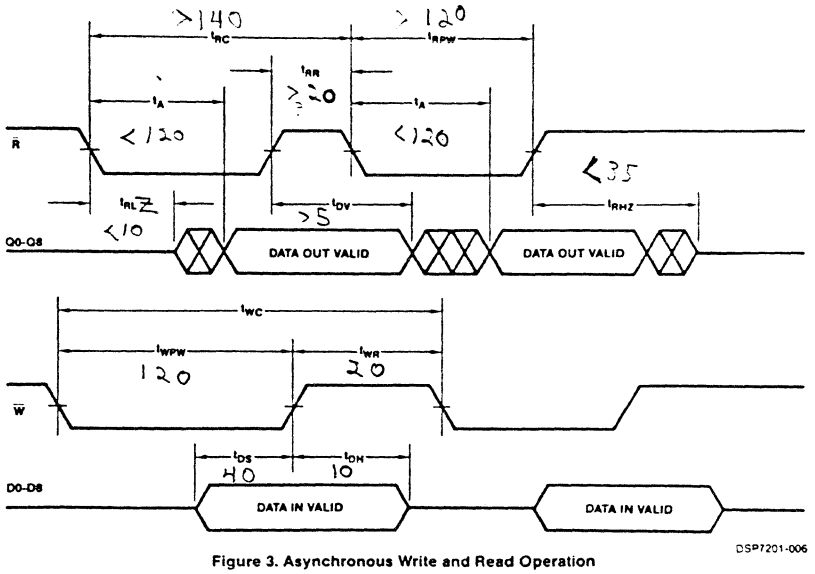


Figure 3. Asynchronous Write and Read Operation

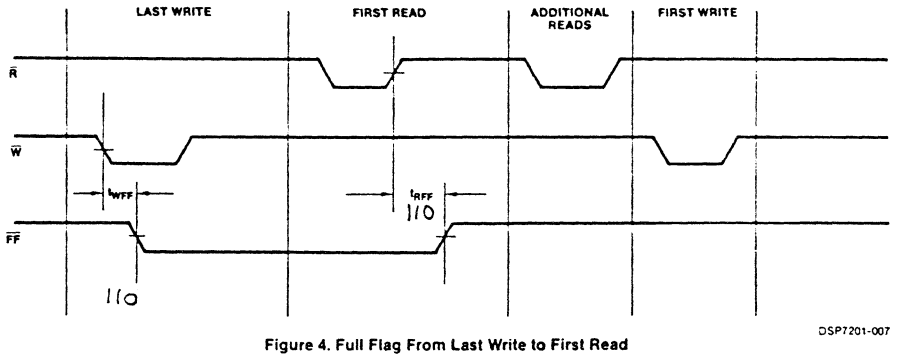


Figure 4. Full Flag From Last Write to First Read

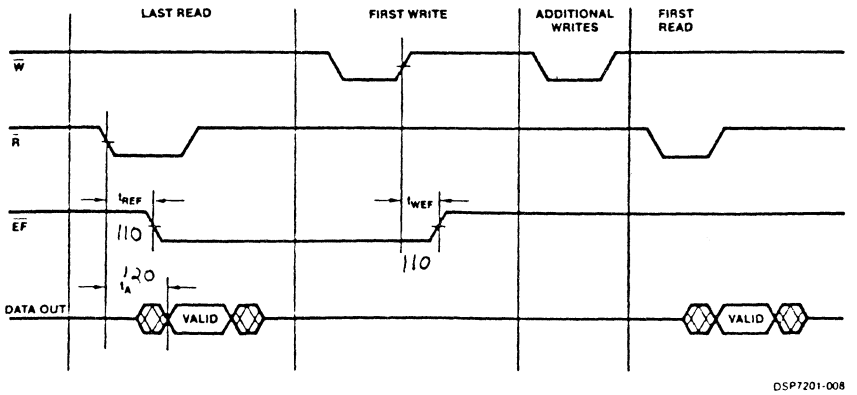


Figure 5. Empty Flag From Last Read to First Write

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7203/4 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/4 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 10.) In this mode the HALF FULL FLAG ($\overline{HF}$), which is an active low output, is shared with EXPANSION OUT ($\overline{XO}$).

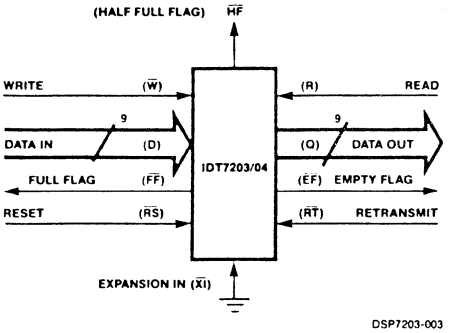
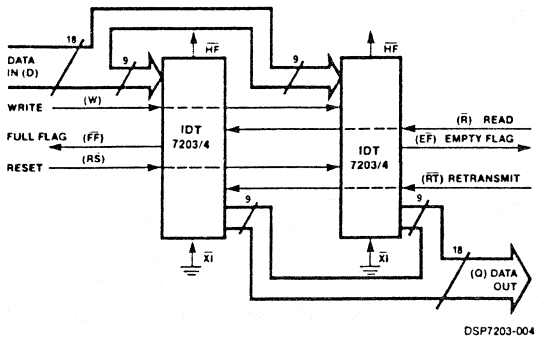


Figure 10. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 11 demonstrates an 18-bit word width by using two IDT7203/4s. Any word width can be attained by adding additional IDT7203/4s.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 11. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7203/4 can easily be adapted to applications when the requirements are for greater than 2048/4906 words. Figure 12 demonstrates Depth Expansion using three IDT7203/4s. Any depth can be attained by adding additional IDT7203/4s. The IDT7203/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other device must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 12.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s. (I.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 12.
5. The RETRANSMIT ($\overline{RT}$) function and HALF FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 13.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7203/4s as is shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (I.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW THRU MODES

Two types of flow through modes are permitted with the IDT7203/7204. A read flow through and write flow through mode. For the read flow through mode (Figure 15), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow through mode (Figure 16), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

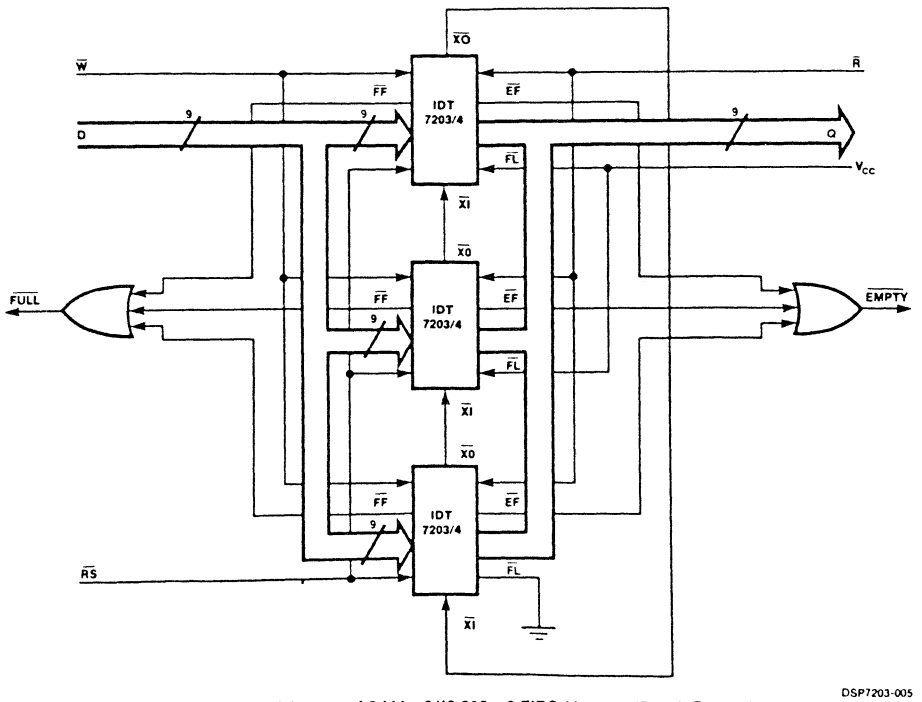
MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

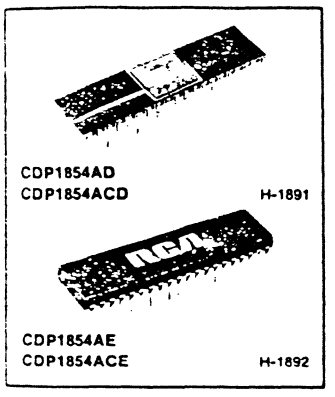
NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12
$\overline{RS}$ = Reset Input, $\overline{FL}$/$\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.



DSP7203-005

Figure 12. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)

CDP1854A, CDP1854AC



Programmable Universal Asynchronous Receiver/Transmitter (UART)

Features:

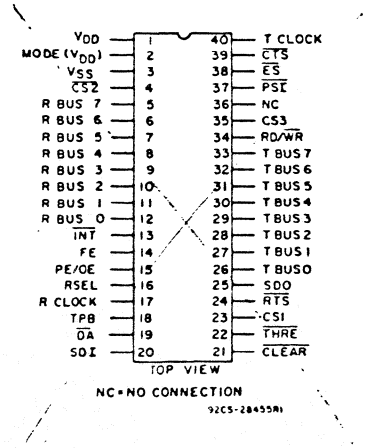
- *Two operating modes: Mode 0-functionally compatible with industry types such as the TR1602A Mode 1-interfaces directly with CDP1800-series microprocessors without additional components*
- *Full- or half-duplex operation*
- *Parity, framing, and overrun error detection*
- *Baud rate-DC to 200 K bits/sec @ V_{DD}=5 V DC to 400 K bits/sec @ V_{DD}=10 V*
- *Fully programmable with externally selectable word length (5-8 bits), parity inhibit, even/odd parity, and 1, 1½, or 2 stop bits*
- *False start bit detection*

The RCA CDP1854A and CDP1854AC are silicon-gate CMOS Universal Asynchronous Receiver/Transmitter (UART) circuits. They are designed to provide the necessary formatting and control for interfacing between serial and parallel data. For example, these UARTs can be used to interface between a peripheral or terminal with serial I/O ports and the 8-bit CDP1800-series microprocessor parallel data bus system. The CDP1854A is capable of full duplex operation, i.e., simultaneous conversion of serial input data to parallel output data and parallel input data to serial output data.

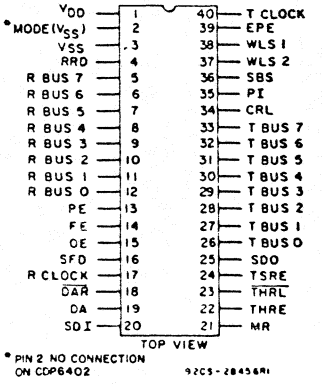
The CDP1854A UART can be programmed to operate in one of two modes by using the mode control input. When the mode input is high (MODE=1), the CDP1854A is directly compatible with the CDP1800-series microprocessor system without additional interface circuitry. When the mode input is low (MODE=0), the device is functionally compatible with industry standard UART's such as the TR1602A. It is also pin compatible with these types, except that pin 2 is used for the mode control input instead of a V_{GG}=−12 V supply connection.

The CDP1854A and the CDP1854AC are functionally identical. The CDP1854A has a recommended operating-voltage range of 4-10.5 volts, and the CDP1854AC has a recommended operating-voltage range of 4-6.5 volts.

The CDP1854A and CDP1854AC are supplied in hermetic 40-lead dual-in-line ceramic packages (D suffix) and in 40-lead dual-in-line plastic packages (E suffix). The CDP1854AC is also available in chip form (H suffix).



Mode 1
Terminal Assignment



Mode 0
Terminal Assignment

CDP1854A, CDP1854AC

Functional Definitions for CDP1854A Terminals Standard Mode 0

SIGNAL: FUNCTION

V_{DD}:
Positive supply voltage.

MODE SELECT (MODE):
A low-level voltage at this input selects Standard Mode 0 Operation.

V_{SS}:
Ground.

RECEIVER REGISTER DISCONNECT (RRD):
A high-level voltage applied to this input disconnects the Receiver Holding Register from the Receiver Bus.

RECEIVER BUS (R BUS 7 - R BUS 0):
Receiver parallel data outputs.

PARITY ERROR (PE):
A high-level voltage at this output indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE (EPE) control. This output is updated each time a character is transferred to the Receiver Holding Register. PE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

FRAMING ERROR (FE):
A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

OVERRUN ERROR (OE):
A high-level voltage at this output indicates that the DATA AVAILABLE (DA) flag was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bused together since an output disconnect capability is provided by the STATUS FLAG DISCONNECT (SFD) line.

STATUS FLAG DISCONNECT (SFD):
A high-level voltage applied to this input disables the 3-state output drivers for PE, FE, OE, DA, and THRE, allowing these status outputs to be bus connected.

RECEIVER CLOCK (RCLOCK):
Clock input with a frequency 16 times the desired receiver shift rate.

DATA AVAILABLE RESET ($\overline{DAR}$):
A low-level voltage applied to this input resets the DA flip-flop.

DATA AVAILABLE (DA):
A high-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):
Serial data received at this input enters the receiver shift register at a point determined by the character length. A high-level voltage must be present when data is not being received.

MASTER RESET (MR):
A high-level voltage at this input resets the Receiver Holding Register, Control Register, and Status Register, and sets the serial data output high.

TRANSMITTER HOLDING REGISTER EMPTY (THRE):
A high-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

TRANSMITTER HOLDING REGISTER LOAD ($\overline{THRL}$):
A low-level voltage applied to this input enters the character on the bus into the Transmitter Holding Register. Data is latched on the trailing edge of this signal.

TRANSMITTER SHIFT REGISTER EMPTY (TSRE):
A high-level voltage at this output indicates that the Transmitter Shift Register has completed serial transmission of a full character including stop bit(s). It remains at this level until the start of transmission of the next character.

SERIAL DATA OUTPUT (SDO):
The contents of the Transmitter Shift Register (start bit, data bits, parity bit, and stop (bit(s)) are serially shifted out on this output. When no character is being transmitted, a high-level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):
Transmitter parallel data inputs.

CONTROL REGISTER LOAD (CRL):
A high-level voltage at this input loads the Control Register with the control bits (PI, EPE, SBS, WLS1, WLS2). This line may be strobed or hardwired to a high-level input voltage.

PARITY INHIBIT (PI):
A high-level voltage at this input inhibits the parity generation and verification circuits and will clamp the PE output low. If parity is inhibited the stop bit(s) will immediately follow the last data bit on transmission.

STOP BIT SELECT (SBS):
This input selects the number of stop bits to be transmitted after the parity bit. A high-level selects two stop bits, a low-level selects one stop bit. Selection of two stop bits with five data bits programmed selects 1.5 stop bits.

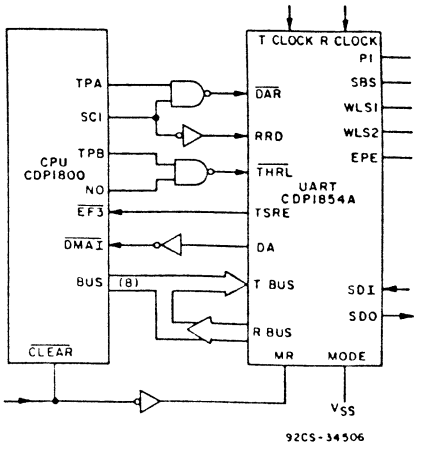


Fig. 8 - Mode 0 connection diagram.

CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 9.

CHARACTERISTIC		V_{DD} (V)	LIMITS CDP1854A Typ.†	CDP1854A Max.*	CDP1854AC Typ.†	CDP1854AC Max.*	UNITS
Interface Timing — Mode 0							
Minimum Pulse Width: CRL	t_{CRL}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Pulse Width: MR	t_{MR}	5	200	400	200	400	ns
		10	100	200	—	—	
Minimum Setup Time: Control Word to CRL	t_{CWC}	5	40	80	40	80	ns
		10	20	50	—	—	
Minimum Hold Time: Control Word after CRL	t_{CCW}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: SFD High to SOD	t_{SFDH}	5	200	300	200	300	ns
		10	100	150	—	—	
SFD Low to SOD	t_{SFDL}	5	75	120	75	120	ns
		10	40	60	—	—	
RRD High to Receiver Register High Impedance	t_{RRDH}	5	200	300	200	300	ns
		10	100	150	—	—	
RRD Low to Receiver Register Active	t_{RRDL}	5	100	150	100	150	ns
		10	50	75	—	—	

†Typical values are for T_A=25°C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.

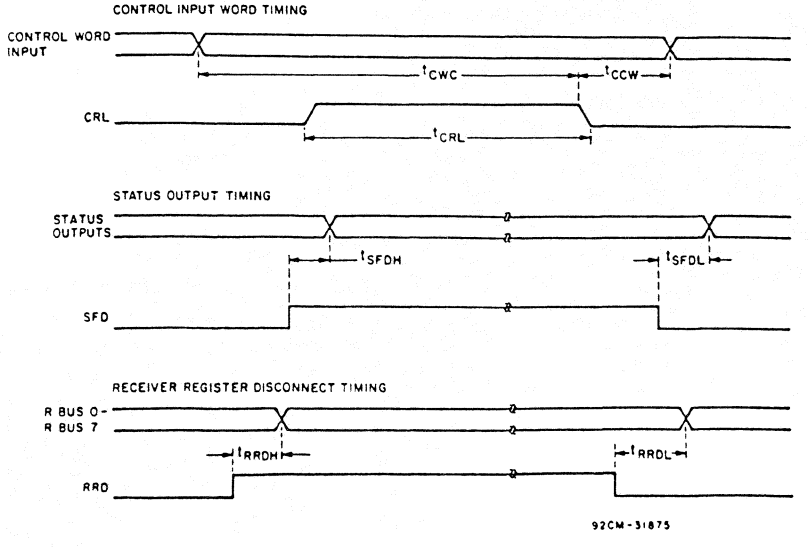


Fig. 9 - Mode 0 interface timing diagram.

CDP1854A, CDP1854AC

WORD LENGTH SELECT 2 (WLS2):
WORD LENGTH SELECT 1 (WLS1):
These two inputs select the character length (exclusive of parity) as follows:

WLS2	WLS1	Word Length
Low	Low	5 Bits
Low	High	6 Bits
High	Low	7 Bits
High	High	8 Bits

EVEN PARITY ENABLE (EPE):
A high-level voltage at this input selects even parity to be generated by the transmitter and checked by the receiver. A low-level input selects odd parity.

TRANSMITTER CLOCK (TCLOCK):
Clock input with a frequency 16 times the desired transmitter shift rate.

Description of Standard Mode 0 Operation (Mode Input=V_{SS})

1. Initialization and Controls

The MASTER RESET (MR) input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting the SERIAL DATA OUTPUT (SDO) signal high. Timing is generated from the clock inputs, Transmitter Clock (TCLOCK) and Receiver Clock (RCLOCK), at a frequency equal to 16 times the serial data bit rate. When the receiver data input rate and the transmitter data output rate are the same, the TCLOCK and RCLOCK inputs may be connected togetner. The CONTROL REGISTER LOAD (CRL) input is pulsed to store the control inputs PARITY INHIBIT (PI), EVEN PARITY ENABLE (EPE), STOP BIT SELECT (SBS), and WORD LENGTH SELECTs (WLS1 and WLS2). These inputs may be hardwired to the proper voltage levels (V_{SS} or V_{DD}) instead of being dynamically set and CRL may be hardwired to V_{DD}. The CDP1854A is then ready for transmitter and/or receiver operation.

2. Transmitter Operation

For the transmitter timing diagram refer to Fig. 10. At the beginning of a typical transmitting sequence the Transmitter Holding Register is empty (THRE is HIGH). A character is transferred from the transmitter bus to the Transmitter holding Register by applying a low pulse to the $\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$ ($\overline{\text{THRL}}$) input causing THRE to go low. If the Transmitter Shift Register is empty (TSRE is HIGH) and the clock is low, on the next high-to-low transition of the clock the character is loaded into the Transmitter Shift Register preceded by a start bit. Serial data transmission begins 1/2 clock period later with a start bit and 5-8 data bits followed by the parity bit (if programmed) and stop bit(s). The THRE output signal goes high 1/2 clock period later on the high-to-low transition of the clock. When THRE goes high, another character can be loaded into the Transmitter Holding Register for transmission beginning with a start bit immediately following the last stop bit of the previous character. This process is repeated until all characters have been transmitted. When transmission is complete, THRE and Transmitter Shift Register Empty (TSRE) will both be high. The format of serial data is shown in Fig. 12. Duration of each serial output data bit is determined by the transmitter clock frequency (f_{CLOCK}) and will be 16/f CLOCK.

3. Receiver Operation

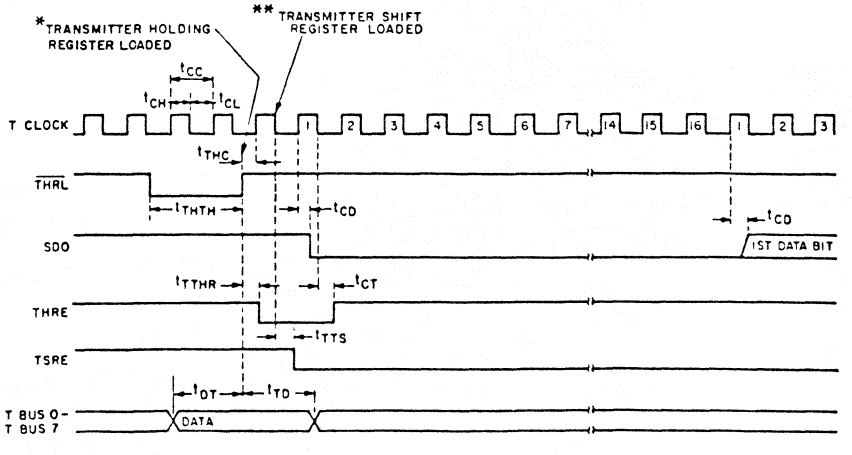
The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After the detection of a high-to-low transition on the SDI line, a divide-by-16 counter is enabled and a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed), and stop bit(s) are shifted into the Receiver Shift Register at clock pulse 7-1/2 in each bit time. If programmed, the parity bit is checked, and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output voltage level) are loaded into the unused most significant bits. If DATA AVAILABLE (DA) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) signal is raised. One-half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) signals become valid for the character in the Receiver Holding Register. The DA signal is also raised at this time. The 3-state output drivers for DA, OE, PE and FE are enabled when STATUS FLAG DISCONNECT (SFD) is low. When RECEIVER REGISTER DISCONNECT (RRD) goes low, the receiver bus 3-state output drivers are enabled and data is available at the RECEIVER BUS (R BUS 0 - R BUS 7) outputs. Applying a negative pulse to the $\overline{\text{DATA AVAILABLE RESET}}$ ($\overline{\text{DAR}}$) resets DA. The preceding sequence of operation is repeated for each serial character received. A receiver timing diagram is shown in Fig. 11.

CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 10.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Transmitter Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
$\overline{THRL}$	t_{THTH}	5	100	150	100	150	ns
		10	50	75	—	—	
Minimum Setup Time: $\overline{THRL}$ to Clock	t_{THC}	5	175	275	175	275	ns
		10	90	150	—	—	
Data to $\overline{THRL}$	t_{DT}	5	20	50	20	50	ns
		10	0	40	—	—	
Minimum Hold Time: Data after $\overline{THRL}$	t_{TD}	5	80	120	80	120	ns
		10	40	60	—	—	
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5	300	450	300	450	ns
		10	150	225	—	—	
Clock to THRE	t_{CT}	5	200	300	200	300	ns
		10	100	150	—	—	
$\overline{THRL}$ to THRE	t_{TTHR}	5	200	300	200	300	ns
		10	100	150	—	—	
Clock to TSRE	t_{TTS}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25°C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.



* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF $\overline{THRL}$

** THE TRANSMITTER SHIFT REGISTER, IF EMPTY, IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD+t_{THC} AFTER THE TRAILING EDGE OF $\overline{THRL}$, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER

92CM-31876R1

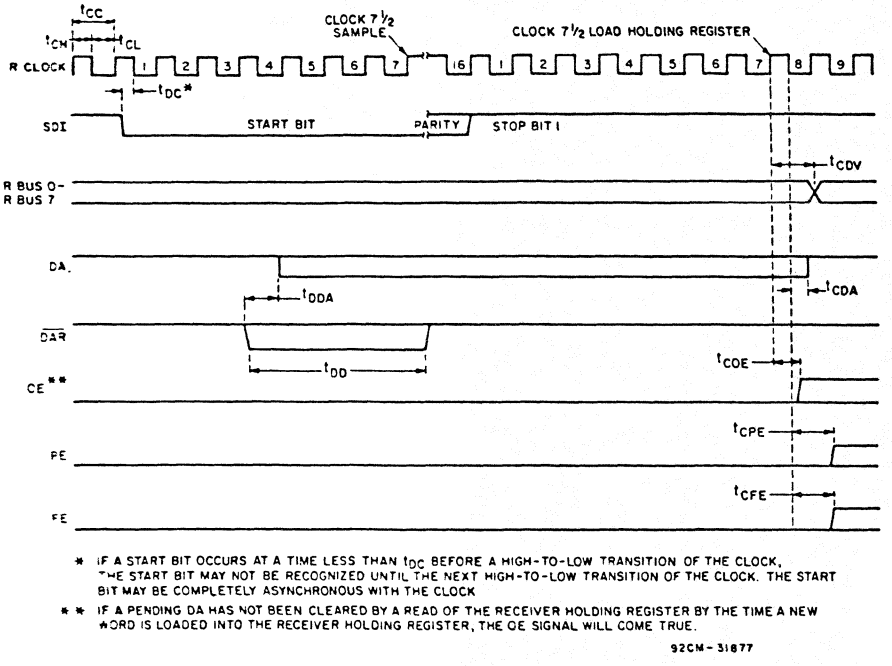
Fig. 10 - Mode 0 transmitter timing diagram.

CDP1854A, CDP1854AC

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = -40 to +85°C, V_{DD} ±5%, t_r,t_f=20 ns, V_{IH}=0.7 V_{DD}, V_{IL}=0.3 V_{DD}, C_L=100 pF, see Fig. 11.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP1854AC		
			Typ.†	Max.*	Typ.†	Max.*	
Receiver Timing — Mode 0							
Minimum Clock Period	t_{CC}	5	250	310	250	310	ns
		10	125	155	—	—	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	100	125	100	125	ns
		10	75	100	—	—	
Clock High Level	t_{CH}	5	100	125	100	125	ns
		10	75	100	—	—	
$\overline{\text{DATA AVAILABLE}}$ RESET	t_{DD}	5	50	75	50	75	ns
		10	25	40	—	—	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	100	150	100	150	ns
		10	50	75	—	—	
Propagation Delay Time: $\overline{\text{DATA AVAILABLE}}$ RESET to Data Available	t_{DDA}	5	150	225	150	225	ns
		10	75	125	—	—	
Clock to Data Valid	t_{CDV}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Data Available	t_{CDA}	5	225	325	225	325	ns
		10	110	175	—	—	
Clock to Overrun Error	t_{COE}	5	210	300	210	300	ns
		10	100	150	—	—	
Clock to Parity Error	t_{CPE}	5	240	375	240	375	ns
		10	120	175	—	—	
Clock to Framing Error	t_{CFE}	5	200	300	200	300	ns
		10	100	150	—	—	

†Typical values are for T_A=25°C and nominal voltages.
*Maximum limits of minimum characteristics are the values above which all devices function.



* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK. THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK

** IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL COME TRUE.

92CM-31877

Fig. 11 - Mode 0 receiver timing diagram.

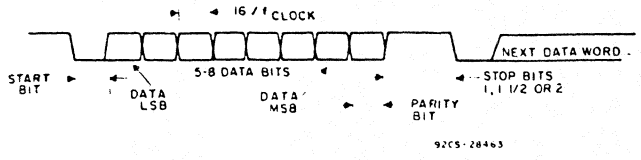


Fig. 12 - Serial data word format.