ERRATUM: In accordance with the standardized nomenclaure adopted at NRAO, the term "instrumental meridian" should now be "instrumental equator".

NATIONAL RADIO ASTRONOMY OBSERVATORY
Green Bank, West Virginia

Electronics Division Internal Report No. 41

NRAO INTERFEROMETER: THE DELAY SWITCHING COMPUTER

Nigel J. Keen

NOVEMBER 1964

NUMBER OF COPIES: 75

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ABSTRACT

Continuous source-tracking with the NRAO interferometer requires short incremental delays to be switched into or out of the IF paths in a programmed way. The purpose of this report is to describe the computer designed, constructed and used at NRAO.

THEORY

The electrical parameters of the NRAO interferometer give a reduction in response of approximately 2 percent for the sixteenth fringe on either side of the interferometer response maximum [1]. This was arbitrarily chosen as the maximum permissible reduction in response, and hence IF delay switching occurs every 32 fringes. (In fact, the choice of 32 fringes was not quite arbitrary, since a pulse is developed for every fringe, and the computer uses a chain of binary counters). A typical compressed interferometer response record is shown in Figure I: this record was taken in the region of interferometer meridian transit (zero IF delay).

The number of fringes away from the instrumental meridian is given by

$$n = \frac{D}{\lambda}[\sin d \sin \delta + \cos d \cos \delta \cos (H - h)]$$

and the number of delays (away from the instrumental meridian) by

$$N = \frac{D}{32\lambda}[\sin d \sin \delta + \cos d \cos \delta \cos (H - h)$$

where d = declination of interferometer pole (for $H \lesssim 6$ hours)

δ = source declination

H = source hour angle

h = hour angle of pole

D = baseline length

and λ = operating wavelength.

Since the value of N gives the position of the response maximum, the Nth delay should be switched in when

$$N - \frac{1}{2} = \frac{D}{32\lambda} [\sin d \sin \delta + \cos d \cos \delta \cos (H - h)] \qquad (1)$$

which corresponds to 16 fringes before maximum response. Equation (1) is used to compute the initial setting of N, since the computed switching sequence actually depends on $\frac{dN}{dt}$

$$\text{i.e.,} \quad \frac{dN}{dt} = -\frac{D}{32\lambda} \cdot \frac{dH}{dt} \cos d \cos \delta \sin (H - h) \qquad (2)$$

$$\text{where} \quad \frac{dH}{dt} = \frac{2\pi}{24 \times 3600} \text{ (sidereal radians per sidereal second)}$$

If a given source is being tracked, all terms but sin (H - h) are constant during the track. Hence

$$\frac{dN}{dt} = k \sin (H - h) \qquad (3)$$

Since a digital computer is more accurate than a mechanical analog computer, a "sine encoder" gave a 10-bit value of the sine of the angle through which the encoder shaft had rotated (from the encoder zero). The encoder is driven by a stepping motor and reduction gear, so that 1 pulse per sidereal second (from the NRAO sidereal clock) causes one rotation of the encoder in one sidereal day. Since the stepping motor can be driven in either direction, faster pulses are applied ($\sim$180 p.p.s.) to reset the encoder prior to tracking another source. The stepping motor also drives an hour angle clock, so that the correct initial value of H allows the correct values of sin (H - h) throughout the new track, and also allows the initial value of N to be set.

So far, we have considered the methods of setting the initial value of N (from equation (2)), and of continuously generating sin (H - h). We must now consider the generation of k sin (H - h) pulses per sidereal second (equation (3)), and the method by which these pulses control the delays. Further, we have to provide for a variation of k as

various source declinations and baseline lengths are required. The next section discusses the computer used for these purposes.

THE COMPUTER

A block diagram of the delay switching equipment is shown in Figure II. In this section we shall be concerned only with the computer. A function diagram of the computer is shown in Figure III. Detailed logic and relay diagrams may be obtained from the NRAO Electronics Division (digital section).

The output of the Baldwin sine encoder is in Gray code, in order to eliminate errors greater than 1 bit (1 in 1023). The complement of the Gray-to-binary converter output is set on the "sine counters", so that when the gate is opened by a command level the number on the sine counters is $1023 \times 1 - \sin (H - h)$. Hence the number of 1 MHz clock pulses which is required to fill the sine counters is $1023 \sin (H - h)$. The next pulse gives a "gate close" pulse to the command flip-flop (FF), which in turn closes the gate. Since the pulses passing through the gate also go to the "counter-divider", the counter-divider receives $1024 \sin (H - h)$ pulses every time the gate opens. The "control counter" defines that the gate is opened once every 2^{11} microseconds. Hence the counter divider receives

$$\frac{1024 \times 10^6}{2^{11}} \sin (H - h) \text{ p.p.s.}$$

$$\text{i.e.,} \quad 5 \times 10^5 \sin (H - h) \text{ p.p.s.}$$

The function of the counter-divider is to produce pulses at a rate proportional to $k \sin (H - h)$. Suppose that the maximum possible count on the counter-divider is M, and the number pre-set (before counting starts) is N. Hence the number to be counted is M - N. However, since $5 \times 10^5 \sin (H - h)$ p.p.s. arrive at the counter input, the counter divider will be filled

$$\frac{5 \times 10^5 \sin (H - h)}{M - N}$$

times per second, and each time the counter-divider is filled the number N is reset and

one pulse is obtained. This method produces a slight irregularity in the counter-divider output pulse sequence, since

$$\frac{5 \times 10^5 \sin (H - h)}{M - N}$$

is not, in general, an integer. However, since these pulses are sent through a count-down sequence before being used as switching pulses, these irregularities are smoothed out in one switching interval. In fact, 2^{10} output pulses from the counter-divider are required for each switching interval. Hence the delay switching rate is

$$\frac{5 \times 10^5 \sin (H - h)}{2^{10} (M - N)} = k \sin (H - h)$$

Hence

$$M - N = \frac{10^6 \times 2^{-11} \times 32\lambda \times 24 \times 3600}{2\pi D \cos d \cos \delta}$$

$$= \frac{2.7 \times 10^9}{\pi D \cos d \cos \delta}$$

The sense of all counter-divider switches is actually reversed so that N is "pre-counted" and (M - N) remains to be counted: this means that the number to be set is proportional to sec δ , which is useful for checking switching rates from source to source.

Since continuous tracking requires delays to be switched out on one side of the correlator, and then switched in on the other side, the following system is used:

A flip-flop is set (by the "set FF" switch) to activate a relay so that delays are in the eastern arm of the interferometer. A multicontact relay is simultaneously set in such a way that the complement of the selected number of delays is set on the delay-counters, but the connections from the delay counters to the delay switches are reversed. Hence the correct number of delays will be set in the eastern interferometer arm, but an up-count in the delay-counters results in a down-count in the delays. Once all delays

have been switched out (i.e., all delay-counters are filled), the next delay count reverses the flip-flop, which in turn sets the counters, restores the normal mode of delay switching (i.e., delay-switching follows delay-counting), and switches delays into the western interferometer arm. It is essential that counter setting switches all be set to zero during this "crossover". Normal delay counting now proceeds until (H - h) = 0, when reverse counting is required. However, the computer cannot automatically reduce delays in the western arm: such delay switching has to be performed manually.

One unit of the computer remains to be described: this is the "pulse-sequence generator". The purpose of this unit is to provide pulses in the correct sequence, for sine encoder-interrogation, Gray-to-binary conversion and counter setting and clearing. No further details will be given here.

The "check encoder setting" switch gives a binary readout of the encoder setting on the "encoder setting" lamps. The switch should not be depressed for too long, since normal counting is inhibited when it is depressed.

REFERENCE

[1] Keen, N. J., Electronics Division Internal Report No. 40, "NRAO Interferometer: Design, Operation, and Early Results"(November 1964).

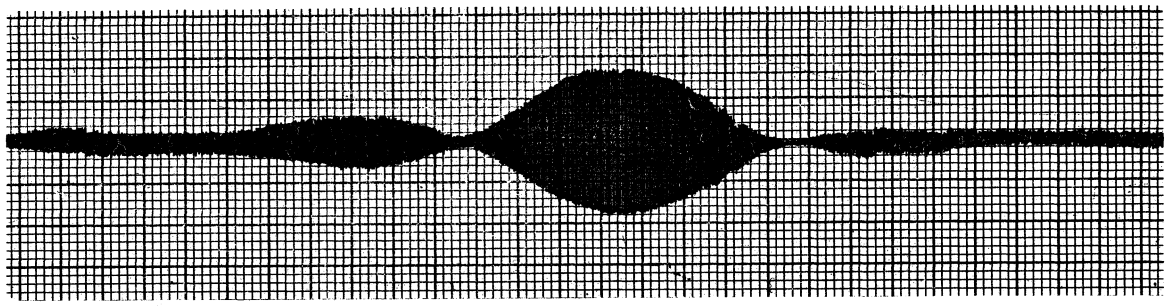

Fig. I

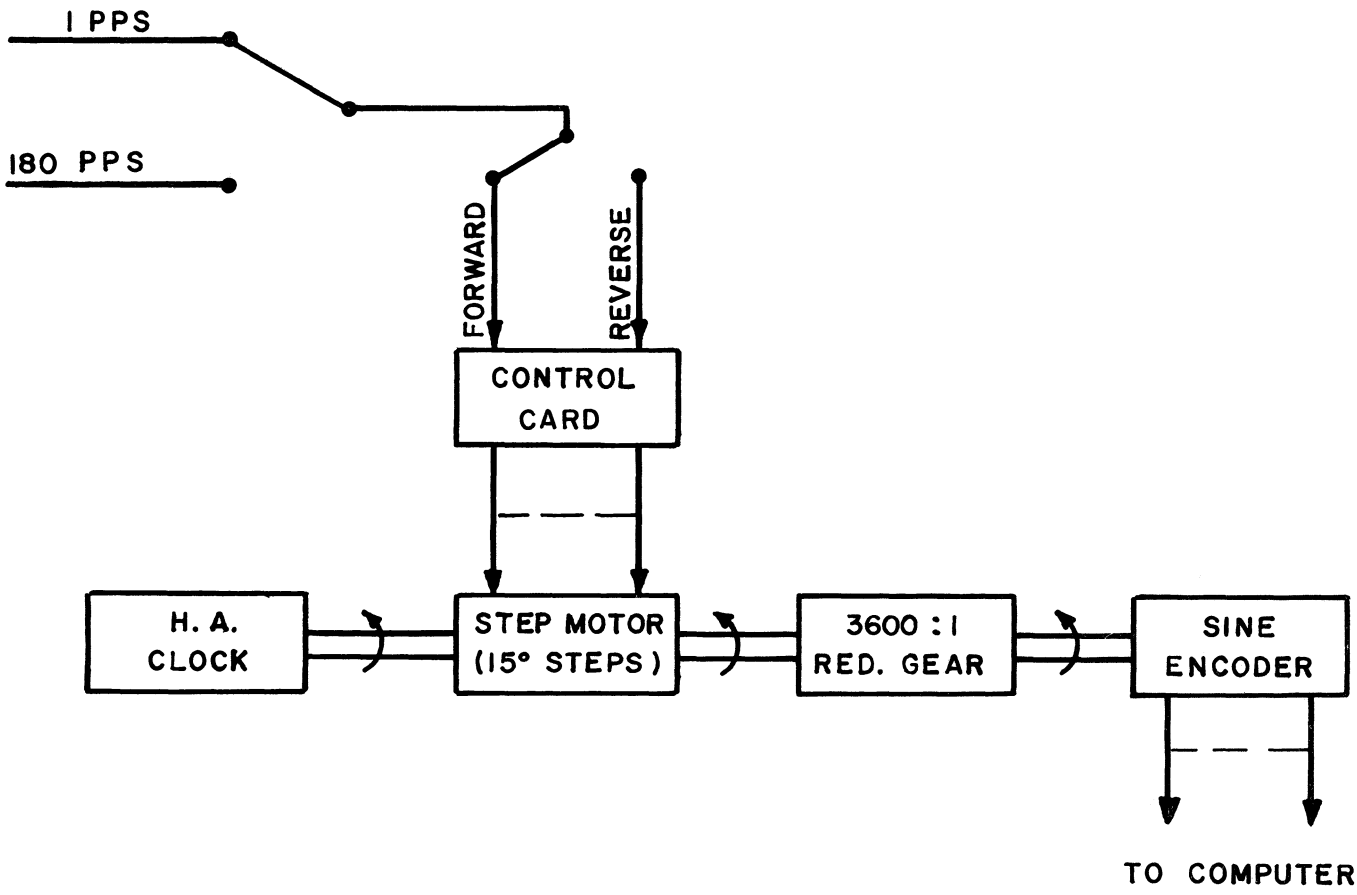
1 PPS
180 PPS
FORWARD
REVERSE
CONTROL CARD
H. A. CLOCK
STEP MOTOR (15° STEPS)
3600 : 1 RED. GEAR
SINE ENCODER
TO COMPUTER

Fig. II

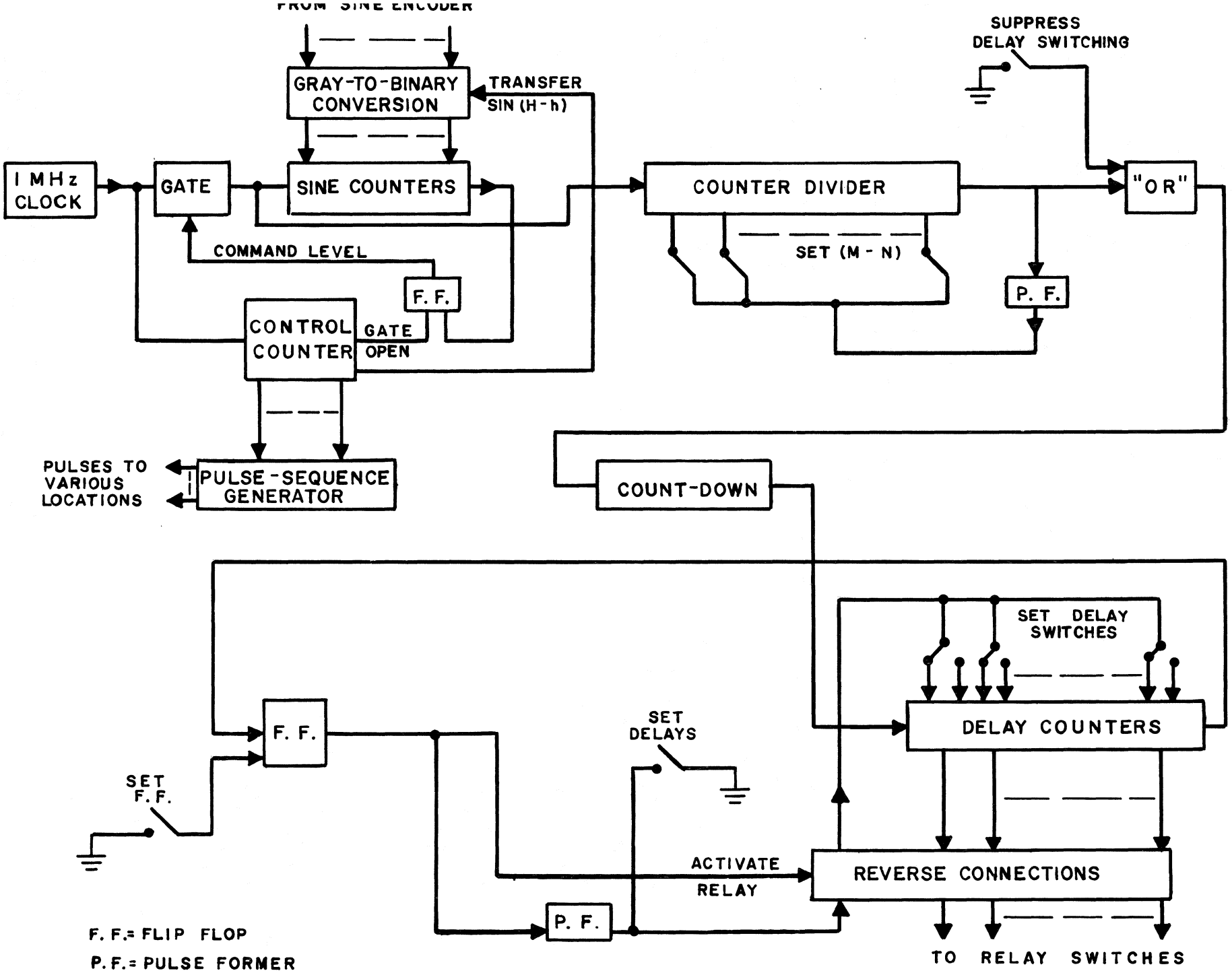
FROM SINE ENCODER
GRAY-TO-BINARY CONVERSION
TRANSFER
SIN (H-h)
SUPPRESS DELAY SWITCHING
1 MHz CLOCK
GATE
SINE COUNTERS
COUNTER DIVIDER
"OR"
COMMAND LEVEL
F. F.
SET (M - N)
P. F.
CONTROL COUNTER
GATE OPEN
PULSES TO VARIOUS LOCATIONS
PULSE-SEQUENCE GENERATOR
COUNT-DOWN
SET DELAY SWITCHES
DELAY COUNTERS
F. F.
SET DELAYS
SET F. F.
ACTIVATE RELAY
REVERSE CONNECTIONS
P. F.
TO RELAY SWITCHES
F. F.= FLIP FLOP
P. F.= PULSE FORMER

Fig. III