LOW-NOISE, 4.8 GHz, COOLED GaAs FET AMPLIFIER

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February 1986

Number of Copies: 150
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2.605-837-001 DC Block Stub
2.605-836-xxx Endplates

(ii)
I. Introduction

This report describes the design procedure, construction, and testing of a microwave transistor amplifier that operates at a physical temperature of 15 Kelvin. The amplifier was designed to operate reliably on a closed-cycle refrigerator in various radio astronomy receiving systems. Approximately twenty of these amplifiers have now been constructed and tested at the NRAO - Green Bank laboratories. The frequency range of interest is 4.6 to 5.1 GHz and the amplifiers typically provide 31 to 34 dB of gain with minimum noise temperature of 15 to 18 Kelvin (Figure 1). A photograph of a completed amplifier is shown in Figure 2.

The construction technique used in this amplifier is similar to that used in amplifiers at higher frequencies by the NRAO Central Development Labs [1], [2], [3]. The major characteristics of the design are:

1) The three-stage amplifier uses commercially available, packaged, GaAs field-effect-transistors.
2) An input isolator and a flange mounted output attenuator are incorporated to improve the amplifier match and stability.
3) A coaxial geometry with a round center conductor in a square outer conductor is used. Tuning of the amplifier performance is achieved by adjusting the position of low impedance slugs.
on a 50 ohm center conductor and by adjusting the length of small
diameter wires used as series inductors. Input and output DC
blocks are formed by quarter-wave reentrant transmission lines,
and chip capacitors are used for interstage DC blocks.

II. Design Process

The first step in the design of this amplifier was to select
a transistor. Based on results at the NRAO CDL, three transistor
types were selected for testing and evaluation at cryogenic
temperatures: the Nippon Electric NE75083, the Mitsubishi MGF1412,
and the Fujitsu FSC10FA. Samples of each of these types were
mounted in a single-stage amplifier such that the impedance
presented to the transistor gate and drain could easily be adjusted
[3]. The minimum noise temperature was then measured for at
least five values of the real part of the impedance seen by the
FET gate, and at several bias points. From this data, and an
accurate circuit model, the transistor noise parameters can be
calculated [2]. Figures 3, 4, and 5 show the variation of minimum
noise temperature versus generator resistance for one of each of
the transistor types, at 13 Kelvin. Figure 6 shows the performance
of a Mitsubishi FET at 300 Kelvin. The room temperature and
cryogenic performance of the three types of transistors is summarized
in Table 1.

In order to do the curve fitting illustrated in Figures 3
through 6, and to calculate the noise parameters given in Table
1, it was necessary to develop an accurate model of the amplifier
matching and bias networks. Figure 7 shows the model used for the input and output networks. In this model, XF1 is the quarter-wavelength tuning slug, XF2 is the variable length 50 ohm line, XF3 is the open-circuited quarter-wavelength DC block, XF4 is the high impedance line used to realize a series inductor, and XF5 is the quarter-wavelength bias choke. C1, C2, C3, and C4 are fringing capacitances, and C5 is a chip bypass capacitor. A closed form approximation formula was used to calculate the values of the fringing capacitances [4]. Analysis of the circuit model was accomplished using the NRAO microwave circuit analysis program, FARANT.

Based on the results in Table 1, it was initially decided to use the NE75083 FET for the first stage of the three stage amplifier. At 13 Kelvin, $R_{opt}$ is higher and $G_n$ is lower than the other two FETs, desirable because the amplifier noise response will be broader in frequency. The NEC FET costs three times as much as the other FETs, so it was decided to use it only in the amplifier first stage. Since the MGF1412 has been used in many NRAO cooled amplifiers, we decided to use it for the second and third stages. The early design work was done and several amplifiers built with this configuration. However, a later batch of NEC FETs purchased had much poorer performance, and later we found that NEC had discontinued manufacturing the NE75083, so we then redesigned the amplifier using the MGF1412 in all three amplifier stages. The design information in this report is for that, three MGF1412, configuration.
A circuit model for the FET was required in order to do the multi-stage amplifier simulations using FARANT. The starting point was a model used at NRAO - CDL (Figure 8) and element values obtained by M. Pospieszalski [2] from manufacturer's data on the FSC10FA FET. Figure 9 shows $S_{11}$ and $S_{22}$ plotted from manufacturer's data for the MGF1412 and calculated from Model 1. As expected, they do not match well, so we then proceeded to reoptimize the element values using the MGF1412 data.

The optimization procedure used was to minimize the difference between the magnitude and angle of the S-parameters calculated from Model 1 and the manufacturer's data. Equation 1 was used as the FARANT error function, summed over the 2 - 6 GHz frequency range at 2 GHz increments.

$$
\sum_{\text{freq}} \sum_{i} \sum_{j} \left[ \left| S_{ij}^{\text{manuf}} - S_{ij}^{\text{model}} \right| + \left| \frac{\angle S_{ij}^{\text{model}} - \angle S_{ij}^{\text{manuf}}}{180} \right| \right] \quad (1)
$$

First $S_{11}$ and $S_{22}$ were optimized, starting with the element values given in column (a) of Table 2, and letting elements 2, 4, 7, 18, and 20 vary. The results of this optimization were used as initial values while $S_{12}$ and $S_{21}$ were optimized, letting elements 1, 3, 5, 6, 8, 9, 17, and 19 vary. During the optimizations, it was found to be to some advantage to add resistances in series with the gate-source and gate-drain capacitances, yielding Model 2 (Figure 10). A final optimization of all four S-parameters was then done, letting all model elements vary. The
final element values are shown in column (b) of Table 2 and the resulting calculated $S_{11}$ and $S_{22}$ plotted in Figure 11. Agreement with $S_{12}$ and $S_{21}$ was also quite good. This model was used in all subsequent FARANT simulations.

Figure 12 shows the calculated and experimental performance of a single-stage amplifier. This figure illustrates the strong effect of any source lead inductance. The experimental data doesn't match the calculated data as well as desired, but if the experimental gain were increased uniformly by about 1 dB, then the match to a calculated curve would be fairly good for source inductance somewhere between 0.01 and 0.1 nH. During the multistage simulations, source inductance of 0.05 or 0.1 nH was used. The noise curves in Figure 12 agree fairly well, but the experimental curve is somewhat narrower than the calculated curve. The square-law detector used in the noise measurements tended to saturate at frequencies where the amplifier had both high gain and high noise, and this may account for the rapid increase in noise below 4.5 GHz. Another factor that should be pointed out is the way that the FARANT programs simulate the variation in the noise parameters with frequency. Because of the time involved, we usually measure the noise parameters only near the center of the frequency range of interest and use equations 2 through 5 to estimate the parameter variation with frequency.
Most of the work at NRAO-CDL has used $a = 1$. Based on my measurements here on transistors at 3.2 GHz and 4.8 GHz, $a = 0.5$ seems to fit better (at 13 Kelvin), and that is what was used in the simulations.

Figure 13 shows the interstage network model used in the FARANT multistage simulations. XF1 and XF6 are the high impedance lines used as tuning inductors, XF2 and XF4 are short lengths of 50 ohm line, and XF3 is the low impedance tuning slug. XF5 and C5 simulate the DC blocking capacitor, and C1 through C4 fringing capacitances.

The FARANT optimization routines were used to design the three-stage amplifier. Starting with the models described above, a two-stage amplifier was optimized. The output matching network
was fixed as that which had been selected experimentally. The following parameters of the input matching network were allowed to vary: the length and impedance of XF1, and the length of XF4.

The following parameters of the interstage network were allowed to vary: the length and impedance of XF3, and the lengths of XF1 and XF6. The error function minimized was:

$$\text{ERROR} = \sum_{\text{freq}} \left[ \left( \frac{T_{\text{MIN}}}{10} \right)^2 + e^{10(1-K)} \right]$$

This function tends to minimize the amplifier noise and maximize the gain while forcing the stability factor to stay greater than one. Once the two-stage performance was satisfactory, work began on optimizing the second interstage of a three-stage amplifier. The error function used was:

$$\text{ERROR} = \sum_{\text{freq}} \left[ \left( \frac{T_{\text{MIN}}}{10} \right)^2 + e^{10(1-K)} + (V - \text{GAIN})^2 + \frac{34}{V} \right]$$

$T_{\text{MIN}}$, the amplifier noise achievable with an ideal input matching network, was used in the first term rather than $T_N$, the actual amplifier noise, because the amplifier input matching network dominates $T_N$ and hides the effect of the interstage networks. $V$ was one of the optimization variables. The third term in eq. 7 forces the gain to be constant over the frequency range, and the fourth term attempts to maximize that constant. The numerator of the fourth term was selected to equal the nominal value of $V$. Once a satisfactory second interstage network was found, an iterative process was started, where each of the matching networks
was re-optimized using the most recent values for the remaining networks. Only a couple of iterations were required, and Figure 14 shows the calculated performance of the optimized three-stage amplifier. At this point, the first three-stage amplifier was constructed, using the optimized networks. The construction process is described in the next section.

III. Amplifier Construction

Drawings and a bill of materials for the amplifier are appended to this report. The 3-stage amplifier body is milled from OFHC copper stock and is plated with 80 μin gold. The following instruments are needed for assembly:

1) 700°F soldering iron with narrow tip.
2) Low power microscope.
3) Temperature variable hot plate.
4) Ersin solder, type SN62, .062 inch diameter.
5) Assorted tweezers.

The construction procedure is as follows:

1) Check all chip capacitors with a capacitance meter.
2) Heat amplifier body (B53205M101) on a hot plate to 375-425°F (190-220°C). Tin all capacitor locations and ground post holes with solder. Place ground posts and chip capacitors in their proper locations and allow the assembly to cool. Clean amplifier body with flux remover. Check mechanical stability of the chip capacitors and re-check values with meter.
3) With the 700°F soldering iron, solder the 50 ohm chip resistors, bias resistors, and protection diodes into place.
4) Heat output endplate (2.605-856-001) on the hot plate to 375-425°F (190-220°C). Solder the DC bias connector into the endplate and allow to cool. Clean with flux remover.

5) Using a small soldering iron, solder #30 AWG enameled copper wire into DC connector. Bolt output endplate to amplifier body and solder bias wires to chip capacitors and the ground wire to the ground pole.

6) Mill .025 inch off tip of two transistor straps (2.605-838-001). Overall length of transistor strap should now be .215 inch. Prepare two pieces of .001 inch thick Kapton by cutting into a .075 inch square.

TABLE 3
(All dimensions in inches.)

<table>
<thead>
<tr>
<th>Stage</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>MGF1412-11-08</td>
<td>MGF1412-11-08</td>
<td>MGF1412-11-08</td>
</tr>
<tr>
<td>Gate</td>
<td>.050</td>
<td>.010</td>
<td>.010</td>
</tr>
<tr>
<td>Drain</td>
<td>.010</td>
<td>.010</td>
<td>.050</td>
</tr>
<tr>
<td>Source</td>
<td>.175</td>
<td>.175</td>
<td>.175</td>
</tr>
</tbody>
</table>

7) Cut leads of the transistor for stage one to dimensions given in Table 3.

8) Place Kapton under each source lead and clamp the first stage FET using the modified transistor straps.

9) Prepare the transistors for stages 2 and 3 by trimming to dimensions given in Table 3. Place two .097 inch diameter ferrite beads on the source leads of FET #3. Mount FET's in amplifier by clamping with the standard transistor straps.
10) Using a small soldering iron, solder the .031 inch diameter DC blocking stub to the gate of FET 1 and to the drain of FET 3.

11) Stretch a 1 inch length of #22 thin wall Teflon tubing over a .035 inch diameter drill rod. Use a heat gun and tweezers for this procedure. Place the stretched tubing over the .031 inch diameter DC blocking stubs. The teflon should extend approximately .030 inch over the end of the DC blocking stubs. NOTE: The actual length of the stubs and the tubing are determined during testing.

12) Press one teflon support bead (BOM item 5) into input end plate (2.605-856-002) and one into output end plate (2.605-856-001).

13) Prepare and mount the 50 ohm input and output lines in each endplate. Mount the selected tuning slugs on these lines. Slide the teflon covered DC blocking stubs into the input and output 50 ohm lines. Also mount the 1st and 2nd interstages in the amplifier.

14) Using a small soldering iron, solder a 4.7 pF chip capacitor onto the end of each interstage 50 ohm line.

15) Cut six lengths of 36 AWG enameled wire to .60 inch. Remove .015 to .020 inches of insulation from each end of each wire. Wind four complete turns on a #73 (.024 inch dia.) drill rod. Solder the coil between the 4.7 pF bias capacitor and the gate and drain of each FET.

16) Place a .070 inch diameter ferrite bead on the drain lead of FET 2.

17) Solder 28 AWG wire between the FET's and the interstages with SN62 solder. Lengths are selected during testing.

18) Clean entire amplifier body with flux remover. Using a low power microscope, inspect the entire amplifier to insure there are no poor or cold solder joints. Also, verify correct component placement.

19) To hold ferrite beads in place, apply a small amount of Duco cement or equivalent.
The ferrite beads mounted on the drain of the second FET and the source leads of the third FET serve to suppress high frequency oscillations. The Kapton under the source leads of the first FET is used to increase the source lead inductance of that stage, found to reduce the amplifier gain below 4 GHz and increase the amplifier stability. The .031 inch diameter DC blocking stub is formed from half-hard brass wire, copper and gold plated. The 36 AWG wire forms the bias coils and the 28 AWG wire forms the series tuning inductors.

A mechanical outline drawing and electrical schematic for this amplifier are included in the drawings appended to this report.

IV. Results

When the first amplifier was assembled, we found it necessary to adjust the lengths of the tuning inductors. Evidently a simple transmission line is not an adequate model for them. Some experimentation with the impedances and lengths of the interstage tuning slugs was also done, but the final values are very close to the FARANT optimization results. On most of the subsequent units only the position of the tuning slugs is adjusted, with the rare case where the lengths of the tuning inductors must be trimmed. The amplifiers constructed with three MGF1412 transistors seem to be repeatable, even when the lot number of the transistors change.

The output 1 dB compression point of these amplifiers is typically greater than 0 dBm. Figure 16 shows the typical input and output return loss at 13 Kelvin. Figure 17 shows the measured
amplifier noise temperature versus ambient temperature, and the same with the effect of the input isolator removed.

V. Future Work

Additional work should be done on the computer models. Relying on the manufacturer's data for the transistors is adequate for fairly narrowband amplifiers, but to achieve better modeling results, we should attempt to measure some actual transistor S-parameters. Careful noise measurements on a single FET at several widely spaced frequencies should be done to try to determine the variation in noise parameters with frequency more accurately. We would like to design a more complex input matching network to provide wider bandwidth in the amplifier noise temperature response. Finally, when HEMT devices become available, we hope to incorporate one of these extremely low noise transistors in the amplifier first stage.

VI. Acknowledgements

We would like to express our thanks to R. Bradley for his work on the transistor model and to the Green Bank machine shop personnel for their excellent work. Special thanks go to S. Weinreb for helping duplicate his test stations and for getting us started in this work. R. Harris taught us how to assemble a reliable cryogenic amplifier and M. Pospieszalski has many excellent suggestions.
REFERENCES


FIGURE 1. Noise temperature and gain of a typical amplifier without the input isolator. The isolator will increase the noise by about 3 Kelvin.
FIGURE 2. A completed amplifier assembly. The input isolator with cold strap is on the left and the output attenuator and DC connector are on the right.
FIGURE 3. Experimentally determined noise parameters of FSC1054A, Lot PT02, at 13 Kelvin.

FIGURE 4. Experimentally determined noise parameters of NE75083, Lot 72A, at 13 Kelvin.

FIGURE 5. Experimentally determined noise parameters of MGF 1412, Lot 3YAJ8, at 13 Kelvin. Drain voltage 3 V.

FIGURE 6. Experimentally determined noise parameters of MGF 1412, Lot 3YAJ8, at 300 Kelvin. Drain voltage 3 V.
FIGURE 7. Input and output matching network model.
FIGURE 8. GaAs FET Model 1
FIGURE 9. $S_{11}$ and $S_{22}$ plotted from manufacturer's data for the MGF 1412 and from Model 1.
FIGURE 10. GaAs FET Model 2 with resistors added in series with the gate-source and gate-drain capacitors.
FIGURE 11. $S_{11}$ and $S_{22}$ plotted from manufacturer’s data for the MGF 1412 and from Model 2.
FIGURE 12. Calculated performance of a single-stage amplifier using FET Model 2 and input/output matching networks illustrated in Figure 7, and for three values of source lead inductance. Dashed lines show performance of an amplifier measured in the lab.
FIGURE 13. Model of the amplifier interstage networks. The bias networks are identical to those in Figure 7.
FIGURE 14. Calculated three stage amplifier performance. See Figures 7 and 13 for circuit model topologies.

### Input Matching Network
- \( Z_1(q) \) Len(in) \( \varepsilon_r \)

| \( X \) | \( 24.5 \) | .427 | 2.1 |
| \( X \) | \( 50.0 \) | .050 | 1.0 |
| \( X \) | \( 18.0 \) | .460 | 2.0 |
| \( X \) | \( 101.0 \) | .147 | 1.0 |
| \( X \) | \( 211.0 \) | .600 | 1.0 |

### Output Matching Network
- \( Z_1(q) \) Len(in) \( \varepsilon_r \)

| \( X \) | \( 34.5 \) | .427 | 2.1 |
| \( X \) | \( 50.0 \) | .050 | 1.0 |
| \( X \) | \( 18.0 \) | .460 | 2.0 |
| \( X \) | \( 101.0 \) | .147 | 1.0 |
| \( X \) | \( 211.0 \) | .600 | 1.0 |

### Interstage 1
- \( Z_1(q) \) Len(in) \( \varepsilon_r \)

| \( X \) | \( 154.0 \) | .135 | 1.0 |
| \( X \) | \( 50.0 \) | .050 | 1.0 |
| \( X \) | \( 15.2 \) | .290 | 2.1 |
| \( X \) | \( 50.0 \) | .050 | 1.0 |
| \( X \) | \( 154.0 \) | .100 | 1.0 |

### Interstage 2
- \( Z_1(q) \) Len(in) \( \varepsilon_r \)

| \( X \) | \( 154.0 \) | .500 | 1.0 |
| \( X \) | \( 50.0 \) | .050 | 1.0 |
| \( X \) | \( 19.1 \) | .300 | 2.1 |
| \( X \) | \( 50.0 \) | .040 | 1.0 |
| \( X \) | \( 154.0 \) | .210 | 1.0 |
FIGURE 15. The amplifier during construction.
(a) With the RF lines ready to be mounted.
(b) A completed amplifier.
FIGURE 16. Amplifier input (a) and output (b) return loss at 13 Kelvin.
FIGURE 17. Amplifier noise temperature versus ambient temperature.
(a) Measured.
(b) After subtracting the effect of the input isolator.
### TABLE 1
Comparison of FET's at 4.8 GHz

<table>
<thead>
<tr>
<th>FET</th>
<th>V\text{DS} (V)</th>
<th>I\text{DS} (mA)</th>
<th>R\text{opt} (Ω)</th>
<th>X\text{opt} (Ω)</th>
<th>g\text{n} (mmho)</th>
<th>T\text{min} (K)</th>
<th>Assoc. Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MGF1412-3YAJ8-M015</td>
<td>3.0</td>
<td>7.5</td>
<td>17.8</td>
<td>53</td>
<td>7.9</td>
<td>57.8</td>
<td>10</td>
</tr>
<tr>
<td>FSC 10-PT02-F004</td>
<td>3.0</td>
<td>12.5</td>
<td>25.9</td>
<td>47</td>
<td>4.5</td>
<td>75.1</td>
<td>10</td>
</tr>
<tr>
<td>NEC 750-72A-N001</td>
<td>3.0</td>
<td>10.0</td>
<td>21.7</td>
<td>65</td>
<td>6.0</td>
<td>51.6</td>
<td>12</td>
</tr>
<tr>
<td><strong>Ambient Temperature – 13 K</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MGF1412-3YAJ8-M015</td>
<td>3.0</td>
<td>7.5</td>
<td>10.7</td>
<td>53</td>
<td>2.9</td>
<td>9.9</td>
<td>12</td>
</tr>
<tr>
<td>FSC 10-PT02-F004</td>
<td>3.0</td>
<td>12.5</td>
<td>9.6</td>
<td>47</td>
<td>3.3</td>
<td>11.9</td>
<td>11</td>
</tr>
<tr>
<td>NEC 750-72A-N001</td>
<td>3.0</td>
<td>10.0</td>
<td>15.0</td>
<td>65</td>
<td>1.8</td>
<td>10.0</td>
<td>13</td>
</tr>
</tbody>
</table>
### TABLE 2

Element Values for GaAs FET Models

(a) Model plotted in Figure 9.
(b) Model plotted in Figure 11.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>(a) Model 1</th>
<th>(b) Model 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gate Resistor (Ω)</td>
<td>6.3</td>
<td>0.0548</td>
</tr>
<tr>
<td>2</td>
<td>Gate/Source Cap (pF)</td>
<td>0.22</td>
<td>0.5389</td>
</tr>
<tr>
<td>3</td>
<td>Gate/Drain Cap (pF)</td>
<td>0.039</td>
<td>0.0467</td>
</tr>
<tr>
<td>4</td>
<td>Drain/Source Cap (pF)</td>
<td>0.18</td>
<td>0.2655</td>
</tr>
<tr>
<td>5</td>
<td>Source Resistor (pF)</td>
<td>1.2</td>
<td>16.1528</td>
</tr>
<tr>
<td>6</td>
<td>Source Inductor (nH)</td>
<td>0.10</td>
<td>0.1433</td>
</tr>
<tr>
<td>7</td>
<td>Drain/Source Resistor (Ω)</td>
<td>157.0</td>
<td>199.1638</td>
</tr>
<tr>
<td>8</td>
<td>Transconductance</td>
<td>30.0</td>
<td>85.0097</td>
</tr>
<tr>
<td>9</td>
<td>Phase Delay (ps)</td>
<td>0.0</td>
<td>0.2118</td>
</tr>
<tr>
<td>10</td>
<td>Drain Resistor (Ω)</td>
<td>0.0</td>
<td>0.4579</td>
</tr>
<tr>
<td>11</td>
<td>G/D Fringing Resistor (Ω)</td>
<td>-</td>
<td>798.6768</td>
</tr>
<tr>
<td>12</td>
<td>Gate and Channel Resistor (Ω)</td>
<td>-</td>
<td>3.2906</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Package Gate Inductor (nH)</td>
<td>0.83</td>
<td>0.9159</td>
</tr>
<tr>
<td>18</td>
<td>Package Gate Capacitor (pF)</td>
<td>0.26</td>
<td>0.3794</td>
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<tr>
<td>19</td>
<td>Package Drain Inductor (nH)</td>
<td>0.69</td>
<td>1.0037</td>
</tr>
<tr>
<td>20</td>
<td>Package Drain Capacitor (pF)</td>
<td>0.26</td>
<td>0.2072</td>
</tr>
<tr>
<td>Qty.</td>
<td>Req.</td>
<td>Description</td>
<td>Designation</td>
</tr>
<tr>
<td>------</td>
<td>------</td>
<td>--------------------------------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>1.</td>
<td>1</td>
<td>Circulator</td>
<td>CTB-1107</td>
</tr>
<tr>
<td>2.</td>
<td>1</td>
<td>Termination, SMA Male, 50 ohm</td>
<td>4112P</td>
</tr>
<tr>
<td>3.</td>
<td>1</td>
<td>SMA Connector, Jack</td>
<td>6540</td>
</tr>
<tr>
<td>4.</td>
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<td>SMA Connector/Attenuator, 6 dB</td>
<td>7406</td>
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<td>Teflon Support Bead</td>
<td>6400-00-3</td>
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<td>6.</td>
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<td>Amplifier Body</td>
<td>B53205M101</td>
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<td>B53205M102</td>
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<td>8.</td>
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<td>Endplates, Input and Output</td>
<td>2.605.856</td>
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<td>Tuning Slug, Input</td>
<td>B53205M103</td>
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<td>Tuning Slug, Interstage 1</td>
<td>B53205M103</td>
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<td>Tuning Slug, Interstage 2</td>
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<td>12.</td>
<td>1</td>
<td>Tuning Slug, Output</td>
<td>B53205M103</td>
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<td>13.</td>
<td>2</td>
<td>50 Ohm Input/Output Line (Select Length in Test)</td>
<td>B53205M104</td>
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<td>14.</td>
<td>2</td>
<td>50 Ohm Interstage Line</td>
<td>B53205M104</td>
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<td>Transistor Strap II</td>
<td>2.605-838</td>
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<td>16.</td>
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<td>Circulator Cold Strap</td>
<td>A53205M106</td>
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<td>18.</td>
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<td>Transistor Lead Extensions (Select Length in Test)</td>
<td>2.605-837</td>
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<td>19.</td>
<td>AR</td>
<td>28 AWG Solid Copper Wire, Tuning Coils</td>
<td>8054</td>
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<tr>
<td>20.</td>
<td>REF</td>
<td>FET Mounting Detail 2</td>
<td>B53205M105</td>
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<tr>
<td>Item</td>
<td>Qty</td>
<td>Description</td>
<td>Designation</td>
</tr>
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<td>21.</td>
<td>1</td>
<td>DC Connector, Solder Mount</td>
<td>ER-7S-4</td>
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<td>22.</td>
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<td>DC Connector, Mating</td>
<td>EP-7S-1</td>
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<td>24.</td>
<td>3</td>
<td>Gallium Arsenide FET</td>
<td>MGF-1412-11-08</td>
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<td>25.</td>
<td>1</td>
<td>Ferrite Bead, .070&quot; Dia.</td>
<td>T7-6</td>
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<td>26.</td>
<td>2</td>
<td>Ferrite Bead, .097&quot; Dia.</td>
<td>T10-6</td>
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<td>27.</td>
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<td>28.</td>
<td>6</td>
<td>680 pF Chip Capacitor</td>
<td>ATC700B</td>
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<td>681KP50</td>
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<td>22 pF Chip Capacitor</td>
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<td>220JP50X</td>
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<td>4.7 pF Chip Capacitor</td>
<td>ATC100A</td>
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<td>4R7DP50X</td>
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<td>33.</td>
<td>6</td>
<td>50 ohm Chip Resistor</td>
<td>WA-13PG-500J-S</td>
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<td>34.</td>
<td>6</td>
<td>Diode, Zener</td>
<td>1N821</td>
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<td>35.</td>
<td>6</td>
<td>Diode, Zener</td>
<td>1N4099</td>
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<td>37.</td>
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<td>Resistor, Metal Film, 1 K ohm</td>
<td>RLR05C-1001FS</td>
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<td>38.</td>
<td>3</td>
<td>Resistor, Metal Film, 49.9 ohm</td>
<td>RLR05C-49R9FS</td>
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<td>38.</td>
<td>AR</td>
<td>30 AWG Solid Copper Wire, Bias Input</td>
<td>8055</td>
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<td>40.</td>
<td>AR</td>
<td>#22 Teflon Tubing</td>
<td>TFT 400</td>
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<tr>
<td>Item</td>
<td>Qty</td>
<td>Description</td>
<td>Designation</td>
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<td>41.</td>
<td>AR</td>
<td>36 AWG Solid Enamed Copper Wire</td>
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<tr>
<td>42.</td>
<td>6</td>
<td>2-56 x 3/8 Socket Head Cap Screws</td>
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<tr>
<td>43.</td>
<td>4</td>
<td>2-56 x 1/4 Socket Head Cap Screws</td>
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<tr>
<td>44.</td>
<td>11</td>
<td>#2 Flat Washers</td>
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<td>45.</td>
<td>13</td>
<td>#2 Lock Washers</td>
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<tr>
<td>46.</td>
<td>2</td>
<td>2-56 x 3/16 Socket Head Cap Screws</td>
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<tr>
<td>47.</td>
<td>2</td>
<td>2-56 x 5/8 Flat Head Screws</td>
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<td>48.</td>
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<td>4-40 x 3/8 Socket Head Cap Screws</td>
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<td>50.</td>
<td>10</td>
<td>#4 Flat Washers</td>
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<td>51.</td>
<td>10</td>
<td>#4 Lock Washers</td>
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<td>52.</td>
<td>5</td>
<td>Ground Poles</td>
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<td>54.</td>
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<td>0-80 x 3/16 Socket Head Cap Screws</td>
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<td>55.</td>
<td>6</td>
<td>#0 Flat Washers</td>
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<tr>
<td>56.</td>
<td>AR</td>
<td>Ersin SN62 Rosin Core solder</td>
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<td>57.</td>
<td>AR</td>
<td>Kaptan Film, 1 mil thick</td>
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<tr>
<td>58.</td>
<td>REF</td>
<td>Interface Drawing</td>
<td></td>
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<td>59.</td>
<td>REF</td>
<td>Schematic</td>
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<td>60.</td>
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</tbody>
</table>
S/N STAMPED ON CASE.
"H" SUFFIX IF HEMT DEVICE USED.

RF OUT
(SMA FEMALE)

1.120 DIA MOUNTING HOLES THRU
(4 PLACES)

RF IN
(SMA FEMALE)

* ON AMPLIFIERS WITH HEMT DEVICES, CENTER PIN IS LED POWER. GROUND OBTAINED THRU CONNECTOR BACKSHELL. OTHERWISE, CENTER PIN IS GROUND.

PROJ: 4.8 GHz
TITLE: COOLED FETAMP INTERFACE DRAWING
MATERIAL:
FINISH:
SCALE:

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
ANGLES:
1. PLACE DEC.
2. PLACE DEC.
3. PLACE DEC.
.427 LONG 24.5 JL (TEFLON)
.670 LONG .073 DIA (50 L)
.047 DIA X .53 LONG DRILL FOR DC BLOCK (TYPICAL)
.630 LONG .073 DIA (50 L)
.380 LONG .073 DIA (50 L)
.300 LONG 19.1 JL (TEFLON)
.047 LONG 1.073 DIA (50 JL)
4.7 pF
4.7 pF
.050 LONG #28 WIRE
.100 LONG #28 WIRE
.100 LONG #28 WIRE
.300 LONG 19.1 JL (TEFLON)
.350 LONG .073 DIA (50 JL)
.100 LONG .073 DIA (50 JL)
.135 LONG #28 WIRE
.290 LONG 15.2 JL (TEFLON)
.427 LONG 34.8 JL (TEFLON)
.300 LONG 19.1 JL (TEFLON)
.350 LONG .073 DIA (50 JL)
.100 LONG #28 WIRE
.100 LONG #28 WIRE
.380 LONG .073 DIA (50 L)
.300 LONG 19.1 JL (TEFLON)
.047 LONG 1.073 DIA (50 JL)
4.7 pF
4.7 pF
.050 LONG #28 WIRE
.100 LONG #28 WIRE
.300 LONG 19.1 JL (TEFLON)
.350 LONG .073 DIA (50 JL)
.100 LONG .073 DIA (50 JL)
.135 LONG #28 WIRE
.290 LONG 15.2 JL (TEFLON)
.427 LONG 34.8 JL (TEFLON)
.630 LONG .073 DIA (50 L)
.047 DIA X .53 LONG DRILL FOR DC BLOCK (TYPICAL)
.600 LONG #36 WIRE TYP.

DC CONNECTOR

CONNECT C TO ANODE OF LED IN HEMT AMPS, GROUND OTHERWISE.

VIEW FROM INSIDE AMP CASE

STAGES 2 AND 3 BIAS NETWORKS IDENTICAL TO STAGE 1.
NOTE: SEE Dwg B53207M105 FOR DETAILS OF FLY MOUNTING AREAS.
.120 DIA THRU
(4 PLACES)

SOLDER IN PLACE
CONTACT STRIPS: CAT NO. 97-221-A
INSTRUMENT SPARITIES, INC
DELANAEE WATER GAP, PA

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W.VA. 24944
.073 DIA TAPER (REAM) SHOULD BE A SNUG SLIP FIT ON .073 DIA ROO AFTER PLATING. CONTACT AT ENDS IMPORTANT.

MATERIAL - BRASS

DIA TOL .001
**MATERIAL:**

- **FINISH:**
  - **/A**
  - **/C**

**APPROVE BY:**

**NUMBER:**

**SHEET DRAWING NUMBER:**

**DATE:**

**SCALE:**

**TOOL:**

**INTERSTAGE LINE**

**DIA TOL = ±0.001**

**NATIONAL RADIO ASTRONOMY OBSERVATORY**

**GREEN BANK, W. VA. 24944**
Mill to .025 depth

A — 2-56 TAP THRU

B — 2-56 CLEARANCE THRU
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES:
1 PLACE DEC.(ax) = .003
2 PLACE DEC.(ax) = .005
3 PLACE DEC.(ax) = .010

NATIONAL RADIO ASTRONOMY OBSERVATORY
GREEN BANK, W. VA. 24944

PROJ.
FET DEV
TITLE.
TRANSISTOR STRAP II

MATERIAL:
1/2 HARD BRASS

DRAWN BY:
RDN
DATE: 5/22/91

DESIGNED BY:
DATE:

APPROVED BY:
DATE:

FINISH:
GOLD PLATE

PLATE

APPROVED:
DATE:

SHEET:
VI
DRAWING NUMBER: 2605-83B-001

REV:
SCALE:
1/0.1/
NOTE 1: DIVIDING LINE. ENDPLATE IS MADE IN TWO PARTS.

-001
OUTPUT ENDPLATE

-002
INPUT ENDPLATE

NRAO
GREEN BANK, WV

DRAWN BY
ENDPLATES
2.605-856-001, 002