NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VIRGINIA

ELECTRONICS DIVISION INTERNAL REPORT NO. 213

INSTRUMENTATION INTERFACE FOR HP 9845A DESKTOP COMPUTER

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INSTRUMENTATION INTERFACE

FOR HP9845A DESKTOP COMPUTER

I. Introduction

This report describes an HP9845A interface which provides two 6-digit resolution integrating (V/F and Counter) analog inputs, two high resolution analog outputs, and four TTL logic level outputs; a block diagram of the unit is shown in Figure 1. The purpose of the interface is to allow the computer to make noise temperature, gain and other measurements upon microwave amplifiers and mixers. To accomplish this the computer must control noise sources, microwave switches, movable shorts, voltage-controlled oscillators and measure output power (via a square-law detector or power meter). The next two sections describe hardware and software operation and should give the reader sufficient knowledge to use the interface. Additional sections treat subjects which are needed for repair or modification.

II. Hardware Operation

The interface is composed of 2 parts, the 16-bit HP interface card (HP98032A) and the interface module. The interface card plugs directly into the backplane of the HP9845. This card is an input/output port to the HP9845 and connects to the interface module via a 4-foot cable and 50-pin connector. The interface module has been given the title, "I/O 2" due to the fact that its address has been designated the number 2.

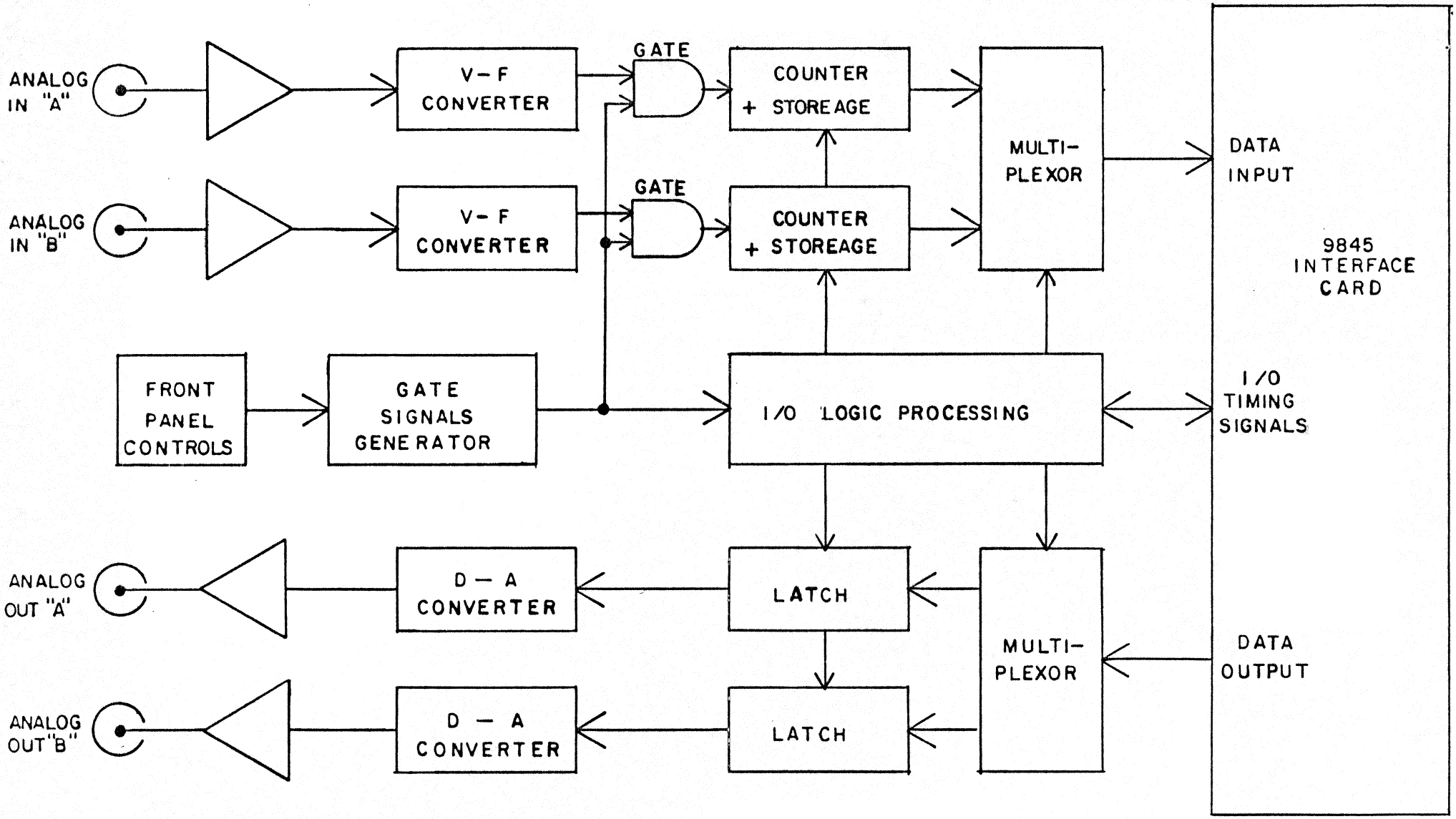


Fig. 1. Interface Block Diagram

This module is intended to be plugged into a standard VLA Bin. A power supply furnishes I/O 2 with +5V, -15V, +15V via a cable and 34-pin connector. A photograph of the front panel of I/O 2 is shown in Figure 2 and internal layout is shown in Figure 3.

The front-panel components of I/O 2 are as follows:

Analog Inputs - The two analog inputs, designated "A" and "B," allow voltages to be read by the computer ranging from 0V to 10V with $\pm$ 1 mV accuracy. These inputs have 1000 meg ohm input impedance and have overload protection of $\pm$ 30V for infinite durations and $\pm$ 150V for short duration. These inputs feed 1 MHz voltage-to-frequency (V/F) converters. The outputs of these converters are counted by 6-digit, BCD counters. This makes it possible to take the average voltage of a signal over a period of time selected with the CYCLE and BLANK digi-switch to be described.

Analog and Digital Outputs - The two analog outputs provide voltage ranging from 0V to 9.999V with an accuracy of $\pm$ 1 mV. These outputs have 100 ohm output impedance and are protected against short circuits. The digital outputs are TTL levels (0 - 3.5V) and can sink a 30 mA source when low (0V) and drive 40 uA when high. LED's on the front panel indicate the state of these outputs; a logic "1" (3.5V) is represented by an illuminated LED.

Cycle/Blank - A 4-digit block of thumbwheel switches control the duration of each measurement CYCLE and the fraction of each measurement cycle, denoted as BLANK, which is not integrated by the voltage/frequency converters. The left-most three (3) digits represent the CYCLE time. The right-most

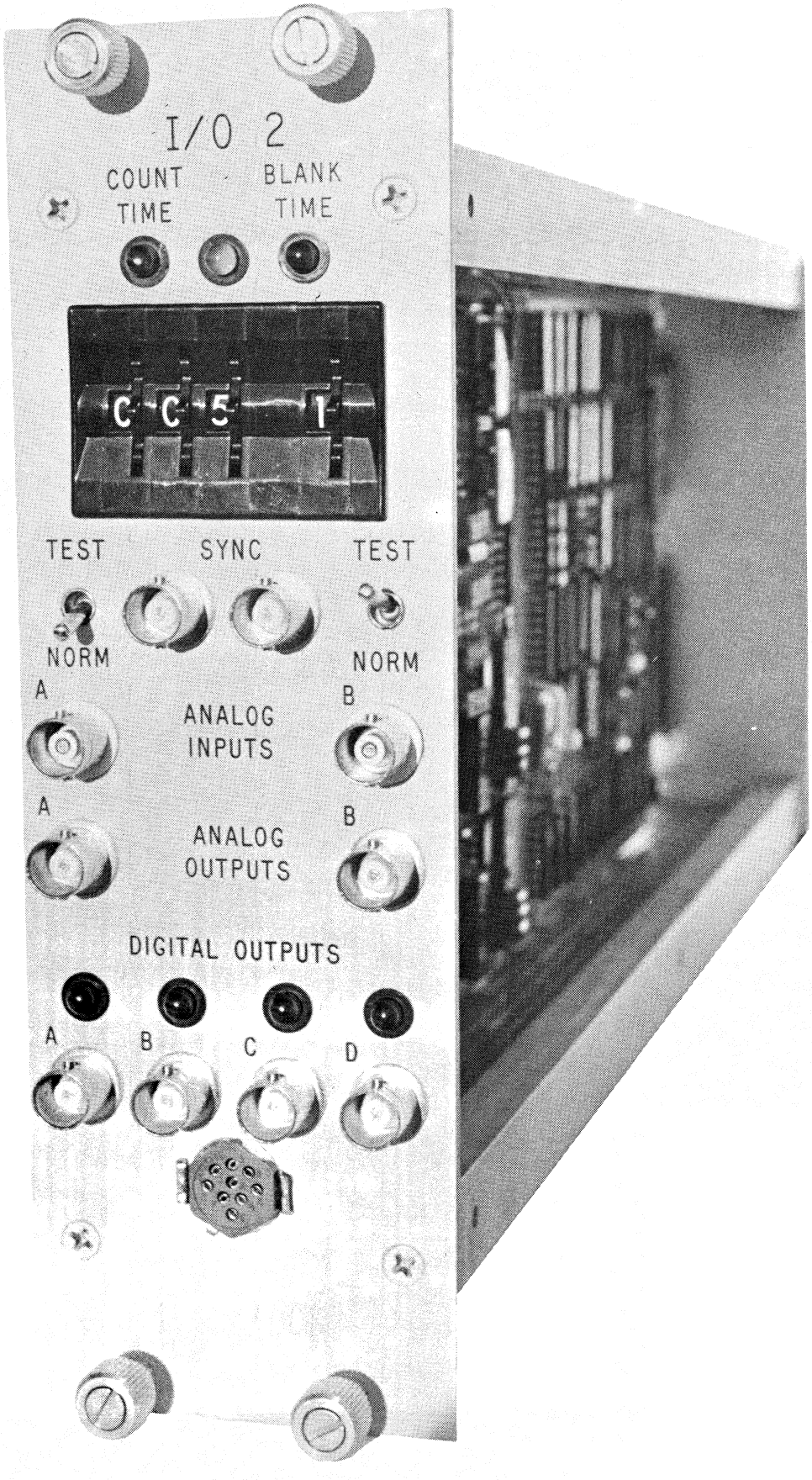


Fig. 2. Interface Front-Panel

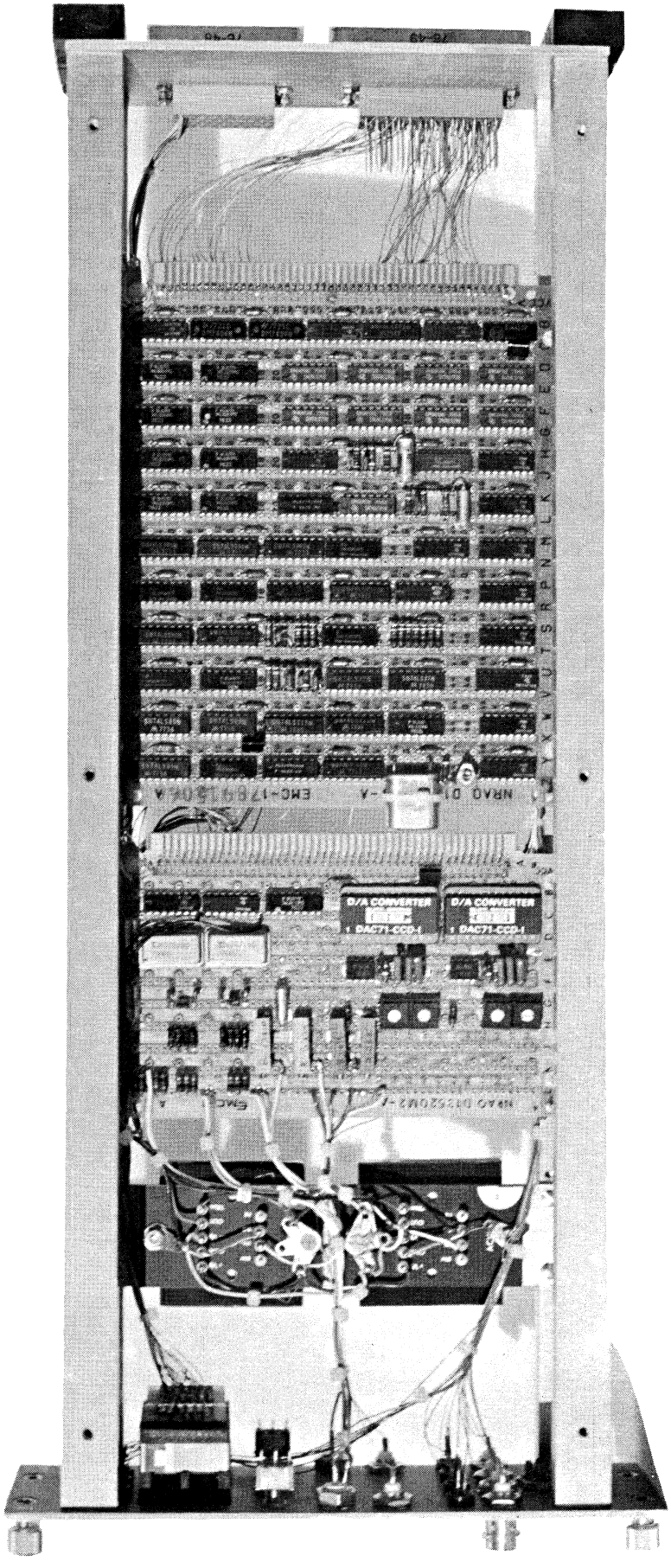


Fig. 3. Interface Side-View

digit represents BLANK time as a fraction of the cycle time. The CYCLE time ranges from 0.01 to 9.99 seconds. The BLANK time setting ranges from .1 to .9 and determines the duration of BLANK time as a fraction of the CYCLE time. A BLANK setting of .1 means 1/10th of the CYCLE time is allowed for settling of analog input signals before valid data is present. The difference between the BLANK time and CYCLE time is the COUNT time during which V/F converters are counted.

Two TTL logic signals, COUNT and BLANK, are provided through front panel BNC jacks. COUNT is high during COUNT time; BLANK is high during BLANK time.

Front Panel LED's - The 3 LED's located at the top of the front panel have the following description:

1) Color: Red
   Label: "COUNT TIME"
   Location: Left upper panel
   Characteristics: This LED indicates whether I/O 2 is in a BLANK mode or COUNT mode (illuminated).
   Significance: This LED indicates that power is applied to I/O 2 (will blink) and timing circuits are operating properly.

2) Color: Green
   Label: None
   Location: Center upper panel
   Characteristics: This LED illuminates for .5 seconds after a variable is transferred (input or output).

Significance: This LED indicates whether the program is actually inputting or outputting data.

3) Color: Red

Label: "BLANK TIME" (erroneous); should be "MISSED DATA"

Location: Most right upper panel

Characteristics: This LED illuminates for .5 seconds if the computer does not output during a CYCLE. This LED should flicker when a program isn't running.

Significance: This LED helps adjusting the CYCLE/BLANK switches according to the length of the program I/O loop (elaborated in Software section).

9-Pin Connector - Located at the bottom of the front panel with the following pin designation:

I/O 2 Module: Front Panel 9-Pin Connector

Pin	Description
A	Digital Output A (LSB)
B	Digital Output B
C	Analog Input A +
D	Analog Input A -
E	Digital Output D (MSB)
F	Analog Input B -
H	Analog Input B +
J	Digital Output C
K	Digital Ground

III. Software Operation

All analog input/outputs on I/O 2 are controlled by software from the HP9845. There are many statements available for manipulating I/O 2, yet only the following statements are required:

```
RESET 2
ENTER 2 WHS NOFORMAT; Var 1, Var 2
OUTPUT 2 WHS NOFORMAT; Var 1, Var 2
```

RESET 2 - The RESET statement/command resets the I/O 2 multiplexers. If the multiplexers lose synchronization, the HP9845 will misread and miswrite data. RESET 2 is necessary at the beginning of all I/O programs; it can be executed from the keyboard.

Short Precision Variables - The OUTPUT and ENTER statements are followed by Short Precision variables which have 6-digit mantissa and an exponent ranging from -99 to 99. A variable can be declared to be short precision by the use of a SHORT statement (This is done once and usually near the beginning of the program).

ENTER - The ENTER statement can input either one or two variables. These variables are equal to the V/F converter counts plus 800,000. The 800,000 is necessary in order to cancel a "dummy bit" needed in transferring the variables from I/O 2 to the HP9845. The result (after subtracting 800,000) is proportional to the input voltage with the proportionality constant dependent upon COUNT time, the V/F converter outputs 1 MHz for a 10 volt input.

I/O 2 alternates between A and B inputs. One cannot input from Port A twice (successively) without inputting from Port B. After the RESET

statement is executed, Port A is available for input. The following example shows two methods of inputting data from the two input ports. Example 2 is more efficient and uses less time.

Example #1

```
10  SHORT A, B                  ! Declares variables SHORT precision
20  RESET 2                     ! Now Port "A" is available for input
30  ENTER 2 WHS NOFORMAT; A     ! Port "A" input is put into Variable A
40  ENTER 2 WHS NOFORMAT; B     ! Port "B" input is put into Variable B
                                  Note:  Port "A" is now available for
                                         input
50  A = A - 800000              ! A is now a voltage derived from the input BNC.
60  B = B - 800000
```

Example #2

```
10  SHORT A, B                  ! See above.
20  RESET 2                     ! See above.
30  ENTER 2 WHS NOFORMAT; A, B  ! Variable A & B receive inputs from
                                  Ports "A" & "B" respectively
40  A = A - 800000
50  B = B - 800000              ! See above.
```

OUTPUT - In nature, the output statement is very similar to the ENTER statement. The output statement controls both the analog outputs and the 4 digital outputs. These voltages and digital states are coded into SHORT precision variables placed at the end of the OUTPUT statement. Outputs to Port "A" or "B" alternate as described for inputs.

A variable written to either analog output Port "A" or "B" specifies a voltage between 0 and 9.999V in the units of millivolts (5000 represents 5V). One must specify an integer. (An output of 123.5 does not represent 123.5 mV.) One must add 800,000 to all written variables in order to set a dummy bit required in transferring data. The following example program will produce a saw-tooth wave on both analog output ports. Port "A" will be inverted in relation to the Port "B" output.

```
 10   RESET 2                          ! One must set count time to 0.00
 20   SHORT A, B
 30   For X = 0 to 9999 Step 200       ! 2 Hz saw tooth wave
 40   Y = 9999 - X
 50   A = Y + 800000
 60   B = X + 800000
 70   OUTPUT 2 WHS NOFORMAT; A, B
 80   Next X
 90   GO TO 30
100   END
```

Digital Output Control - The control of the digital outputs is coded into the variable which is written to Analog Port "B". Encoding is done by adding certain numbers to this variable (in addition to 800,000) to represent certain digital outputs. In order to make digital output "A" go high, add 10,000 to the variable which is written to Analog Port "B". The following table shows what number must be added to set a certain bit high:

Number added to Short Precision variable which is written to Analog output Port "B".	Digital output bit set high
10,000	A
20,000	B
40,000	C
100,000	D

The following are examples of several output variables and the effects they produce:

	Status of Digital Ports				
Variable, B	A	B	C	D	Output Voltage, B
809999	0	0	0	0	9.999V
800001	0	0	0	0	.001V
815555	1	0	0	0	5.555V
835555	1	1	0	0	5.555V
934321	1	1	0	1	4.321V
979999	1	1	1	1	9.999V

The following example program makes all digital outputs square-wave. Digital outputs A and C are 180° out of phase with digital outputs B and D:

```
10  RESET 2
20  SHORT A, B1, B2
30  B1 = 850000
40  B2 = 920000
50  OUTPUT 2 WHS NOFORMAT; A, B1
```

```
60  WAIT 250
70  OUTPUT 2 WHS NOFORMAT; A, B2
80  WAIT 250
90  GO TO 50
```

Special Output Considerations

1) An output voltage of 10,000 is considered to be Ø, not 10V. Only the first 4 digits apply.

2) One cannot place a number (instead of a variable) at the end of an OUTPUT statement, i.e.,

```
OUTPUT 805432
```

is forbidden. The reason for this restriction is that numbers are not written in SHORT precision.

3) One cannot place an expression at the end of an OUTPUT statement, i.e.,

```
OUTPUT 2 WHS NOFORMAT; (A + 800000), (B + 800000)
```

is forbidden. The HP 9845 will interpret the preceding example as ASCII characters requesting to be transferred.

4) Always output integers. One cannot output numbers such as 800100.5 and 800000.753.

IV. Synchronization

The COUNT/BLANK signals control the timing between the HP9845 software and I/O 2. The following rules govern this synchronization between I/O 2 and the HP9845:

1) The computer can only output during BLANK time. When the computer executes an OUTPUT statement during COUNT time, I/O 2 will cause the computer to WAIT until BLANK time occurs. When BLANK time begins, the transfer of data will occur.

2) The computer cannot output more than 2 variables during a BLANK period. If the computer attempts to OUTPUT a third variable, it will be put into a WAIT state until a new BLANK begins (as in Rule #1).

3) The computer cannot input more than 2 variables during a CYCLE (BLANK time + COUNT time). If it attempts to input a third variable, it will be put into a WAIT state until a new CYCLE begins.

4) The right-most red LED on the front panel will illuminate for .5 seconds if the computer fails to output during a BLANK period. The illumination of this LED indicates an error in a fully synchronized system.

The following program illustrates both OUTPUT and ENTER commands and synchronization. It is a test program which measures the error in an output-input loop. Analog output ports "A" and "B" are connected to analog input ports "A" and "B" respectively. The program prints out the average error on both ports every 100 readings:

```
10 ! G.Weinreb       1/9/81     "TESTAB"
20 ! THIS PROGRAM WILL DETERMINE THE AVERAGE ERROR FROM OUTPUTTING TO THE INPUTS
     100 TIMES. THE ERROR SHOULD BE LESS THAN 3.000 mV.
100 Adjust=.1
110 SHORT Ai,Bi,Ao,Bo
120 RESET 2
130 PRINT "PLEASE SET CYCLE TIME TO 0.20 SECONDS AND BLANK TO .5."
140 PRINT "CONNECT THE 'A' ANALOG OUTPUT TO THE 'A' ANALOG INPUT."


143 PRINT "CONNECT THE 'B' ANALOG OUTPUT TO THE 'B' ANALOG INPUT."
146 PRINT
150 PRINT "ARE YOU READY?          (TYPE 'Y' , THEN HIT 'CONT')"
160 INPUT A$
170 PRINT "THE PROGRAM IS NOW RUNNING. IN 20 SECONDS YOU WILL RECEIVE DATA."
180 PRINT
200 FOR X=0 TO 9999 STEP 99              ! LAST OUTPUT OF 9999 mV. HAS NO CORRESPO
NDING INPUT.
210  Ao=Bo=X+800000
220   OUTPUT 2 WHS NOFORMAT;Ao,Bo
230   ENTER 2 WHS NOFORMAT;Ai,Bi
240    IF X=0 THEN 300                   ! IF THE FIRST OUTPUT HAS JUST BEEN ENICI
ATED THEN WE MUST WAIT A CYCLE BEFORE VALID DATA CAN BE INPUTTED.
250     Ai=(Ai-800000)*Adjust            ! THE INPUT IS ADJUSTED TO "mV."
260     Bi=(Bi-800000)*Adjust
270      Ao=Bo=Ao-99-800000              ! THE CURRENT OUTPUT IS ADJUSTED TO CORRE
SPOND TO THE LATEST INPUT.
280    Aerror=Aerror+ABS(Ao-Ai)          ! THE ERROR IS CALCULATED AND ADDED TO AN
ERROR ACCUMULATING VARIABLE.
290    Berror=Berror+ABS(Bo-Bi)
300  NEXT X
310   Aerror=Aerror/100                 ! THE AVG. ERROR IS FIGURED.
320   Berror=Berror/100
330  PRINT "AVG. 'A' ERROR =";Aerror;"mV    AVG. 'B' ERROR =";Berror;"mV"
340 Aerror=Berror=0
350 GOTO 200                             ! THE PROGRAM DOES IT AGAIN UNTIL THE
'STOP' KEY IS HIT.
1000 END
```

TABLE 1. "TESTAB" PROGRAM

Special Considerations

1) The HP9845 can go into a WAIT state for a maximum of ∿9.8 seconds, assuming there is nothing wrong with the system.

2) If one tries to either OUTPUT or ENTER while I/O 2 is not properly set-up (power on, cables not attached, etc.), the HP9845 will go into a WAIT state until these problems are fixed. After several minutes of waiting, an error 163 will appear.

3) Everytime one changes the CYCLE/BLANK setting switches, the new CYCLE/BLANK signals are delayed several seconds.

V. HP 16-bit I/O Interface Card

The Hewlett Packard 16-bit input/output card (Model No. 98032A) plugs directly into the main frame of the HP9845. This card makes it possible to input and output 16-bit words in parallel fashion. The card comes equipped with 16 data input lines and 16 data output lines (open collector outputs). All data used in conjunction with the input and the output lines is in negative true logic. In other words, 0 volts represents a logic 1 and 4 volts represents a logic 0.

There are many control lines associated with the interface card. Most of these lines can be complemented by inserting jumpers on the P.C. board of the interface card. There is a line referred to as the PRESET line which pulses high when the "RESET" command is executed from the computer. Other interface lines not used with I/O 2 include two control input lines (STIO and ST11), two control output lines (CTLO and CTL1), the I/O line (direction of transfer), the EIR line (External Interupt Request) and the PSTS line (Peripheral status).

When inputting or outputting a 16-bit word, the peripheral and the interface card must execute a procedure called a handshake. There are two handshake lines (PFLG and PCTL) which govern all transfers for input and output operations. The following description of handshake logic assumes that jumper 3 is installed, in the interface card used with I/O 2 (Jumper 3 complements the logic sense of the PCTL line). The PCTL is an output of the interface card and the PFLG is an input to the interface card. The following explains how a handshake is performed:

When the computer wishes to execute an input or output transfer (one 16-bit word), it will begin the handshake by checking if the peripheral is busy (PFLG will be high if the peripheral is busy). If the PFLG is low, it will proceed by driving the PCTL high. The peripheral will then respond by setting the PFLG high (Signaling to the computer that it is ready for data). The PFLG will automatically drive the PCTL low. The peripheral will keep the PFLG high until it is ready for new data or until it wishes to end the transfer. If one did not require a handshake, he could tie these two lines together (the PCTL would drive the PFLG producing a handshake).

All interface card lines enter the interface module via a 50-pin connector. From the connector (in the module) the lines are connected to the input/output pins on a wirewrap card. The following table shows all interface lines with their associated connector pins and input/output pins (on the wirewrap card):

Interface Line	Connector Pin	Wirewrap Card I/O Pin
Data Input 0	A	6
DI_1	B	8
DI_2	C	10
DI_3	D	12
DI_4	E	14
DI_5	F	16
DI_6	H	18
DI_7	J	20
DI_8	K	22
DI_9	L	24
DI_{10}	M	26
DI_{11}	N	28
DI_{12}	P	30
DI_{13}	R	32
DI_{14}	S	34
DI_{15}	T	36
STI_0	U	40
STI_1	V	42
GND	W	GND
GND	X	GND
GND	Y	GND
GND	Z	GND
I/O	a	43
PRESET	b	45
PCTL	c	47
PFLG	d	51
PSTS	e	53
EIR	f	55
GND	h	GND
CTL_0	n	60
CTL_1	p	62
Data Output 0	r	66
DO_1	s	68
DO_2	t	70
DO_3	u	72
DO_4	v	74
DO_5	w	76
DO_6	x	78
DO_7	y	80
DO_8	z	82
DO_9	AA	84
DO_{10}	BB	86
DO_{11}	CC	88
DO_{12}	DD	90
DO_{13}	EE	92
DO_{14}	FF	94
DO_{15}	HH	96

TABLE 2. INTERFACE LINES

The following is a list of the jumpers which have been installed in the interface card associated with I/O 2:

Jumper	Function When Installed
3	Complements logic sense of PCTL
7	Allows calculator to actuate DMA
A	Clocks the high input byte at the time the calculator reads the register
B	Selects word input mode
C	Clocks the low input byte at the time the calculator reads the register
F	Selects word input mode

Mounted on the interface card there is a switch which selects which address the card is located at on the HP9845 HP-1B bus. The address, called the "select code" can be between 0 and 16. The interface card used with I/O 2 is set for Select Code 2. All software controlling this interface card must specify its select code. The following contains a table of the select codes which are occupied:

TABLE 3. SELECT CODES

Select Code	Device
0	keyboard, printer
2	I/O 2
13	graphics
14	tape drive
15	tape drive
16	CRT

VI. HP9845 Variable Formats

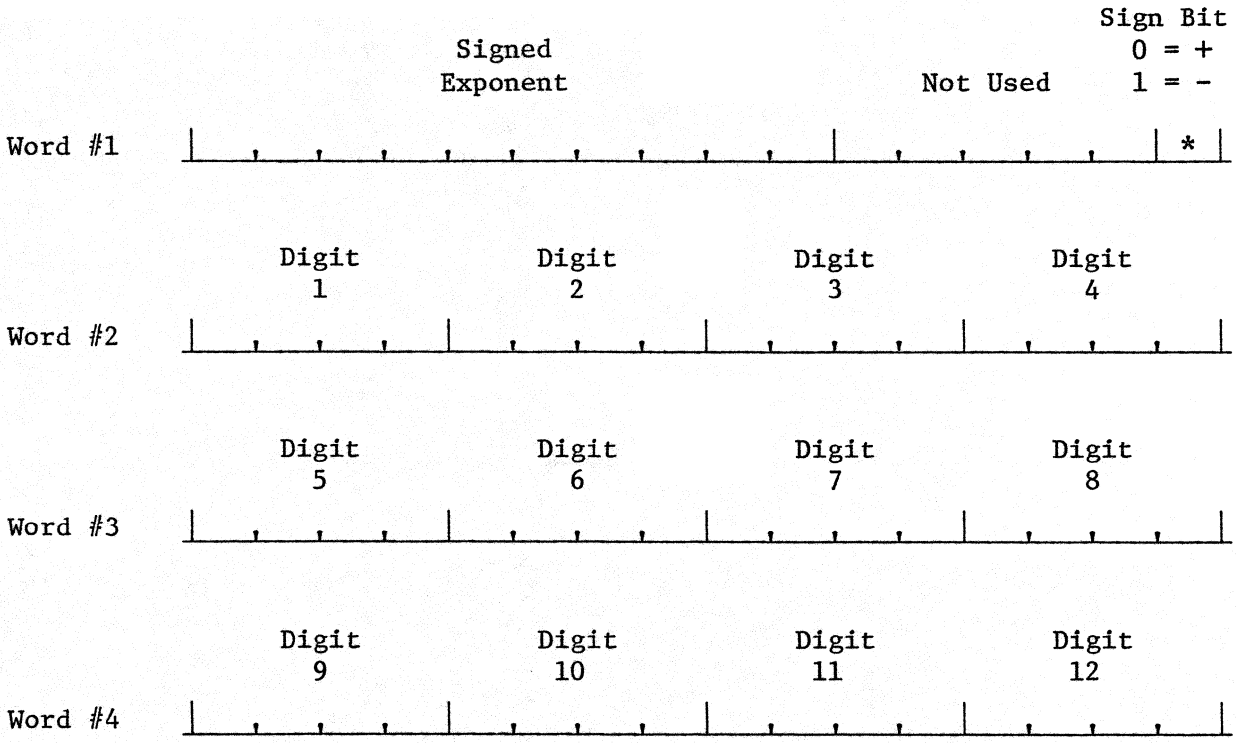
INTEGER

The integer precision variable requires one 16-bit word of memory and can denote an integer between -32768 and 32767. The variable is stored in binary. Data bus line No. 0 pertains to the LSB of the binary word. The numbers 0 to 32767 are stored using standard binary; negative integers are stored in complement form as shown in the following examples:

INTEGER	BIT PATTERN
$+32767_{10}$	0111 1111 1111 1111
$+ \quad 5_{10}$	0000 0000 0000 0101
$+ \quad 1_{10}$	0000 0000 0000 0001
0	0000 0000 0000 0000
$- \quad 1_{10}$	1111 1111 1111 1111
$- \quad 5_{10}$	1111 1111 1111 1011
-32768_{10}	1000 0000 0000 0000

FULL PRECISION

The full precision variable can accomodate up to 12 digits and the exponent is between -512 and 511. This method requires four 16-bit words. The 12 digits are stored in binary-coded-decimal (BCD) and the exponent is stored in binary. Each digit requires 4 bits and the exponent requires 10 bits. Another bit pertains to the sign of the number (+/-). The following figure illustrates the architecture of the full precision variable:



16-Bit Word

Fig. 4. Architecture of Full Precision Variable

(Word #1 is the first word transferred)

SHORT PRECISION

A short precision variable can accomodate up to 6 digits and the exponent can denote a number between -64 and 63. The short precision variable requires two 16-bit words of memory to store its contents. Like the full precision variable, the digits are stored in BCD (4 bits per digit) and the exponent is stored in binary using 7 bits. The last bit pertains to the sign of the number (logic "0" = positive/logic "1" = negative). The following figure illustrates how a short-precision variable is set up:

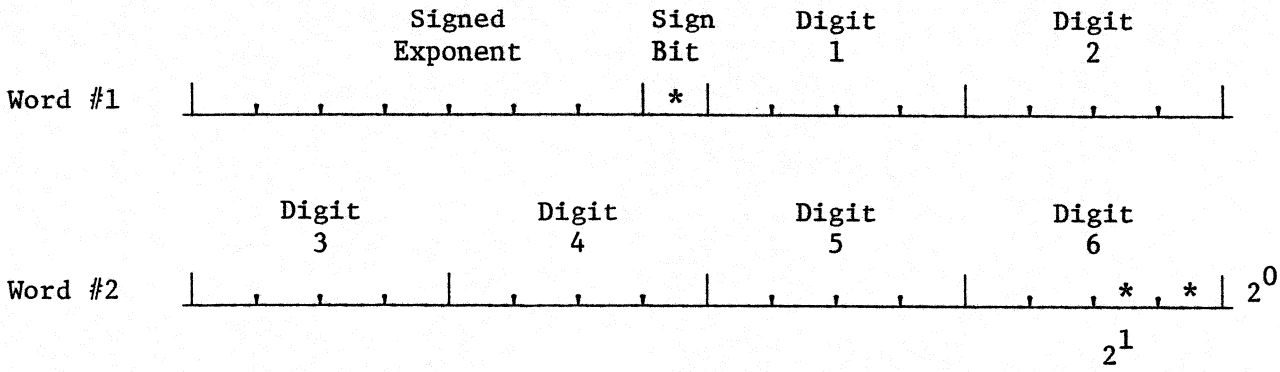


Fig. 5. Architecture of a Short Precision Variable

Between Digit 1 and Digit 2 there is an imaginary fixed decimal. Independent of the number of digits in a short precision variable, the most significant digit will always be placed in the space referred to as "Digit 1". This means that Digit 1 could denote the 1's place or the 100,000's place depending on the exponent. The rest of the digits will fall into their place respectively. This may be referred to as a stacking procedure. All the digits of a variable (in the mantissa) are stacked against Digit 1. The following table shows some examples of how a short precision variable is stored:

	Imaginary Fixed Decimal							
Number	Digit 1	2	3	4	5	6	7 Bits Exponent	Sign Bit
10	1_{10}	0	0	0	0	0	1_{10}	0
100	1_{10}	0	0	0	0	0	2_{10}	0
156.7	1_{10}	5_{10}	6_{10}	7_{10}	0	0	2_{10}	0
1567	1_{10}	5_{10}	6_{10}	7_{10}	0	0	3_{10}	0
-1567	1_{10}	5_{10}	6_{10}	7_{10}	0	0	3_{10}	1
.1	1_{10}	0	0	0	0	0	-1_{10}	0
.123456	1_{10}	2_{10}	3_{10}	4_{10}	5_{10}	6_{10}	-1_{10}	0
.000123	1_{10}	2_{10}	3_{10}	0	0	0	-4_{10}	0

← All digits are stacked in this direction.

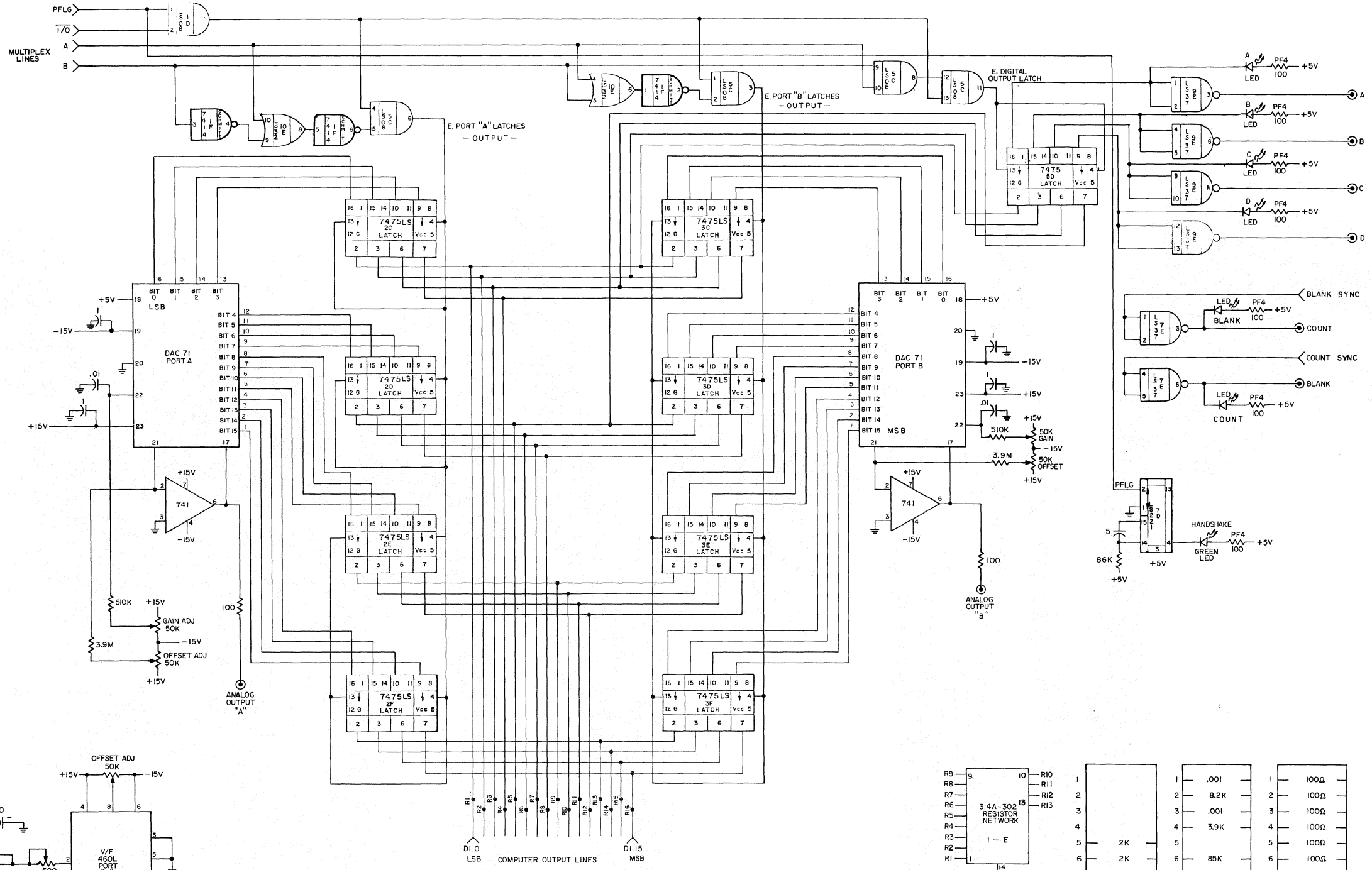
TABLE 4. SHORT PRECISION VARIABLE INTERNAL FORMAT

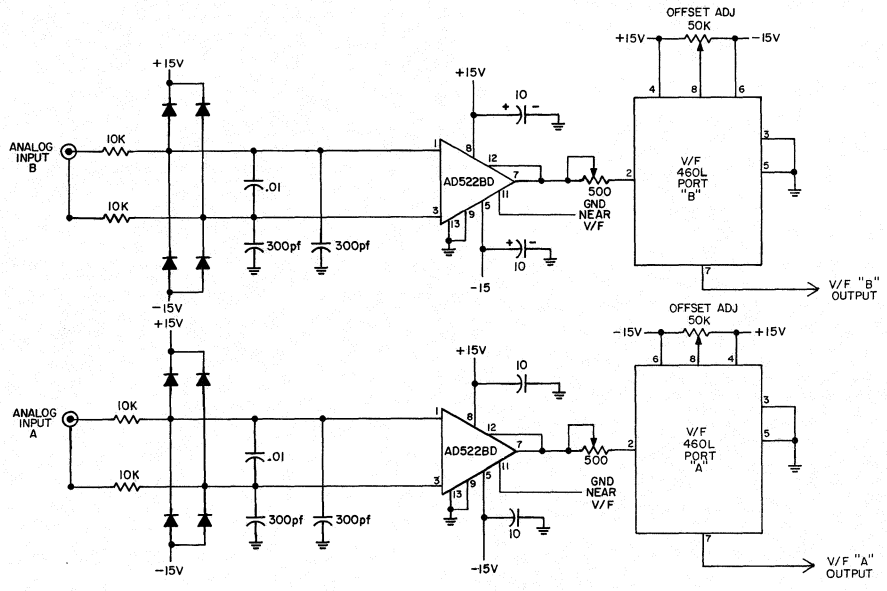
It is possible to input a number from the interface in a manner producing an illegal format. The following illustrates an example of this:

	Fixed Decimal							
Number	Digit 1	2	3	4	5	6	Exponent	Sign Bit
1234	0_{10}	0_{10}	1_{10}	2_{10}	3_{10}	4_{10}	5	1

Illegal Format for Short Precision Variable

Note that Digits 1 and 2 are both zero. This is in violation of the stacking procedure: the most significant digit (1_{10}) is not in the space referred to as "Digit 1". Suppose this inputted into short precision variable "A". When a "Print A" statement is executed, the computer will not catch the illegal format and print out "1234"; however, a "PRINT (A+1)" statement would print an erroneous value.





MULTIPLEX LINES A	MULTIPLEX LINES B	WORD ON DATA OUT LINES	PORT ENABLED
L	L	4th	ANALOG B
H	L	1st	
L	H	2nd	ANALOG A
H	H	3rd	DIGITAL A,B,C,D

ALL CAPACITANCE VALUES ARE IN MICROFARDS

Appendix 1.A.
- 26 -

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

SIZE: I/O 2

TITLE: ANALOG OUTPUT

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA 22901

DRAWN BY: W. R. BOND	DATE: 3-5-80
DESIGNED BY: GLENN WEINREB	DATE:
APPROVED BY	DATE:

Sh 1 of 3 | SHEET NUMBER | DRAWING NUMBER | REV. | SCALE

MULTIPLEX LINES A	MULTIPLEX LINES B	WORD ON DATA-IN LINES	PORT ENABLED
0	0	4th	"B"– least sig. word
1	0	1st	"A"– most sig. word
0	1	2nd	"A"– LSW
1	1	3rd	"B"– MSW

TO COMPUTER DATA INPUT LINES

DI 15 (MSB) DI 12 DI 11 DI 8 DI 7 DI 4 DI 3 DI 0 (LSB)

CLOCK FOR COUNTER LATCHES "U" 15 u.s.

COUNTERS CLEAR INPUT

COUNTER "A"

COUNTER "B"

dummy bits

MULTIPLEXER LINES A B

COUNTER "A" INPUT

COUNTER "B" INPUT

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

I/O 2

DRAWN BY W.R. BOND 2-28-80
DESIGNED BY GLENN WEINREB 7-10-79
APPROVED BY DATE

COUNTER MULTIPLEXER LOGIC DIAGRAM

SIZE | DRAWING NUMBER | SHEET NUMBER 2 of 3 | REV. | SCALE

	PF 1	PF 2	PF 5
	9C	8C	5E
1	220Ω	3K	2.2K
2	470Ω	.001 mfd	.01 mfd
3	.01 mfd	500Ω	220Ω
4	3K	10 pf	
5	.001 mfd	2K	
6	4K	2K	56K
7	100pf	2K	5.6 mfd

1 MHz
5-50PF
74S124 7D
1 MHz
100 KHz
10 KHz
1 KHz
LS390 6D DECADE COUNTER
LS390 8A DECADE COUNTER
LS390 11B DECADE COUNTER
LS390 8D DECADE COUNTER
DIGI SWITCH 23011 D-3
23011 D-2
23011 D-1
4 BIT COMPARATOR
+5V
GOES H WHEN DIGI-SWITCH = THE COUNTER
2us PULSE TO CLEAR COUNTER SO ANOTHER CYCLE CAN BE GENERATED FOR THE TIMING FREQ.
PF2 3K
PF2 .001
CLEAR
1 KHz CLOCK
TIMING FREQ.- BETWEEN 1000 Hz AND .999 Hz depending ON THE SETTING OF THE DIGI-SWITCHES
- 10 CYCLES OF THIS FREQ.= THE COUNT TIME
LS162 IID DECADE COUNTER
DIGI SWITCH 23011 D — 4
LS793 4D 4 2 4
LS157 9B 2-IN MUX
LS393 8D BINARY COUNTER
3K-PF1
.001 PF1
STARTS BLANK TIME WITH A 2.5us
ENDS BLANK TIME WITH A PULSE
4K-PF1
100 pf PF1
220 PF1
FROM CALCU. PRESET
A B TO MULTIPLEXOR CONTROL LINES
H. WHEN BLANKING
L. WHEN BLANKING
PULSES BEFORE EVERY WORD TRANSFER
I/O
L IF OK
H IF NOT OK
H IF OK
100Ω
LED UNSUCCESSFUL CYCLE COMPLETION
56K PF5
FROM CALCULATOR PIN 47 PCTL
DISALLOWS COMPUTER TO OUTPUT > 2 VARIABLES IN ONE CYCLE
H WHEN BLANKING
2us
470-PF1
.01 PF1
23K PF5
.01
TO COUNTERS "A" AND "B" CLEAR
BLANK SYNC
CLOCK FOR COUNTER LATCHES
1.6 ms
4.5ms
.001
4K PF3
8K PF3
COUNT SYNC
FROM CALCULATOR I/O
FROM V/F "A" OUTPUT
TO COUNTER "A"
TO COUNTER "B"
FROM V/F "B"
TO CALCULATOR-PIN 51 PFLG

Appendix 1.C.
- 28 -

REV.	DATE	DRAWN BY	APPRV'D BY	DESCRIPTION

SIZE C — I/O 2

TITLE: FREQ. COUNTERS GATE CONTROL AND MULTIPLEX CONTROL OVER I/O OPERATIONS

NATIONAL RADIO ASTRONOMY OBSERVATORY
CHARLOTTESVILLE, VA. 22901

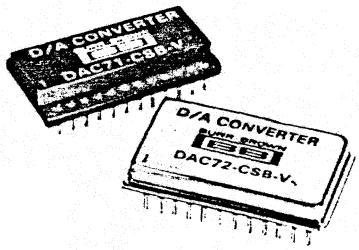
DRAWN BY	W.R. BOND	DATE	2-26-80
DESIGNED BY	G. WEINREB	DATE	7-26-79
APPROVED BY		DATE	

SHEET NUMBER	DRAWING NUMBER	REV.	SCALE
Sh 3 of 3			

Appendix 2. Manufacturers Data

Appendix 2.A. Consists of pages 1-4 of an eleven-page report. The complete report can be obtained from Burr-Brown Research Corporation, P. O. Box 11400, Tucson, Arizona 85734.

BURR-BROWN

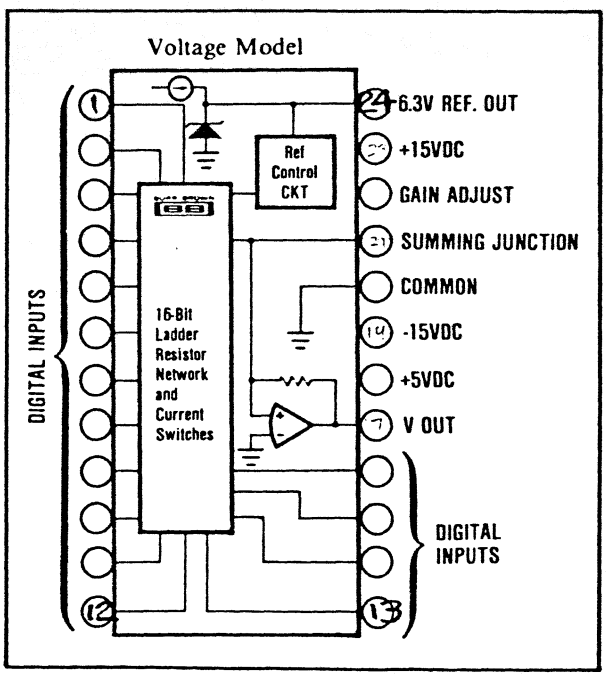


DAC71
DAC72

High Resolution
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 16-BIT, 4-DIGIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±5ppm/°C (DAC72)
- AVAILABLE IN TWO TEMPERATURE RANGES:
  0°C to +70°C
  -25°C to +85°C
- CURRENT AND VOLTAGE MODELS
- LOW COST



DESCRIPTION

The DAC71/72 are high quality 16-bit hybrid IC D/A converters available in 24-pin DIP compatible ceramic and metal packages.

DAC71/72C with internal reference and optional output amplifier offers a maximum linearity error of ±0.003% of FSR at room temperature and a maximum gain drift of ±15ppm/°C over a temperature range of 0°C to +70°C. The DAC72 offers a maximum linearity error of ±0.003% of FSR at room temperature and a gain drift of ±5ppm/°C over a temperature range of -25°C to +85°C.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes.

Packaged within the DAC71/72 are fast-settling switches and stable laser-trimmed thin-film resistors that let you select output voltages 0 to 10V (CSB and CCD) or ±10V (COB) and output currents of ±1mA or 0 to -2mA. Input power is ±15VDC and +5VDC.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-409 Printed in U.S.A. October, 1978

SPECIFICATIONS

ELECTRICAL

T_A = 25°C and rated power supplies unless otherwise noted.

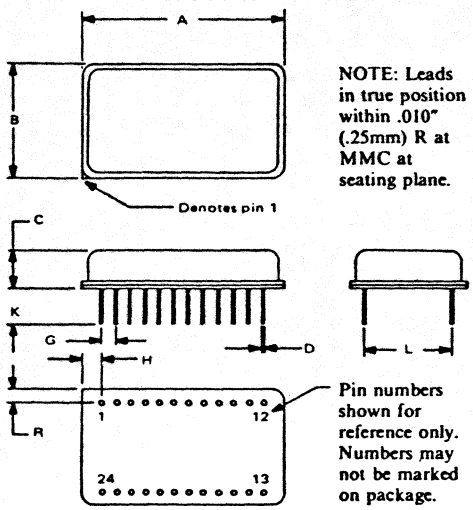
MODEL	DAC71/72C			DAC72			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT							
DIGITAL INPUT							
Resolution, CCD		4			4		Digits
CSB, COB		16			16		Bits
Logic Levels (TTL-Compatible)[1]							
Logical "1" (at +40μA)	+2.4		+5.5	+2.4		+5.5	VDC
Logical "0" (at -1.0mA)	0		+0.4	0		+0.4	VDC
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at 25°C, CCD			±0.005			±0.005	% of FSR[2]
COB, CSB			±0.003			±0.003	% of FSR
Gain Error[3], Voltage		±0.01	±0.05		±0.01	±0.05	%
Current		±0.05	±0.25		±0.05	±0.25	%
Offset Error[3], Voltage, Unipolar		±0.1	±1		±0.1	±1	mV
Voltage,Bipolar			±2			±2	mV
Current, Unipolar			±1			±1	μA
Current, Bipolar			±5			±5	μA
Monotonicity Temp. Range (14-bits)	0		+50	0		+70	°C
DRIFT(Over specified temp. range)							
Total Bipolar Drift (includes gain, offset, and linearity drift)[4], Voltage		±7	±15		±5	±8	ppm of FSR/°C
Current		±15	±50		±10	±40	ppm of FSR/°C
Total Error over Temp. Range[5]							
Voltage, Unipolar			±0.083			±0.045	% of FSR
Bipolar			±0.071			±0.05	% of FSR
Current, Unipolar			±0.23			±0.24	% of FSR
Bipolar			±0.23			±0.24	% of FSR
Gain, Voltage			±15			±5	ppm/°C
Current			±45			±35	ppm/°C
Offset							
Voltage, Unipolar		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±5	ppm of FSR/°C
Current, Unipolar			±1			±1	ppm of FSR/°C
Bipolar			±40			±35	ppm of FSR/°C
Differential Linearity over Temperature			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step		5	10		5	10	μsec
1LSB Step[6]		3	5		3	5	μsec
Slew Rate		20			20		V/μsec
Current Models (to ±0.003% of FSR)							
Output: 2mA step 10Ω to 100Ω Load			1			1	μsec
1kΩ Load			3			3	μsec
Switching Transient		500			500		mV
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges - CSB, CCD		0 to +10			0 to +10		V
COB		±10			±10		V
Output Current	±5			±5			mA
Output Impedance (DC)		0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common		
Current Models							
Ranges - CSB, CCD		0 to -2			0 to -2		mA
COB		±1			±1		mA
Output Impedance - Unipolar		15			15		kΩ
Bipolar		4.4			4.4		kΩ
Compliance			±2.5			±2.5	V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current[7]			±200			±200	μA
Temp. Coeff. of Drift			±10			±5	ppm/°C

MODEL	DAC71/72C			DAC72			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY							
Unipolar Offset							
±15VDC		±0.0001			±0.0001		% of FSR/% V_S
+15VDC		±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset							
±15VDC		±0.0004			±0.0004		% of FSR/% V_S
+5VDC		±0.0001			±0.0001		% of FSR/% V_S
Gain							
±15VDC		±0.001			±0.001		% of FSR/% V_S
+5VDC		±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS							
DAC71/72	±14.5, +4.75	±15, +5	±15.5, +5.25	±14.5, +4.75	±15, +5	±15.5, +5.25	VDC
Supply Drain, ±15VDC (no load)		±25	±35		±25	±35	mA
+5VDC (logic supply)		+20	±30		±20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Operating (double above Drift Specs)	-25		+85	-55		+100	°C
Storage	-55		+100	-55		+110	°C

NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility.
2. FSR means Full Scale Range and is 20V for ±10V range, 10V for ±5V range, etc.
3. Adjustable to zero with external trim potentiometer.
4. See "Computing Total Accuracy over Temperature".
5. With gain and offset errors adjusted to zero at 25°C.
6. LSB is for 14-bit resolution.
7. Maximum with no degradation of specifications.

MECHANICAL
DAC72 & DAC72C



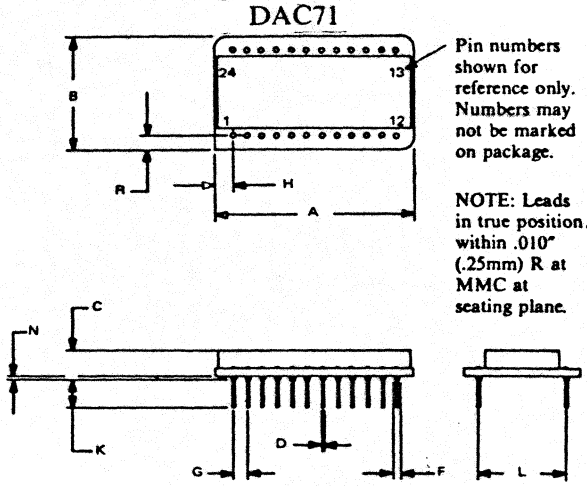
NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

CASE: Nickel Plated Kovar
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (gross leak).

MECHANICAL
DAC71



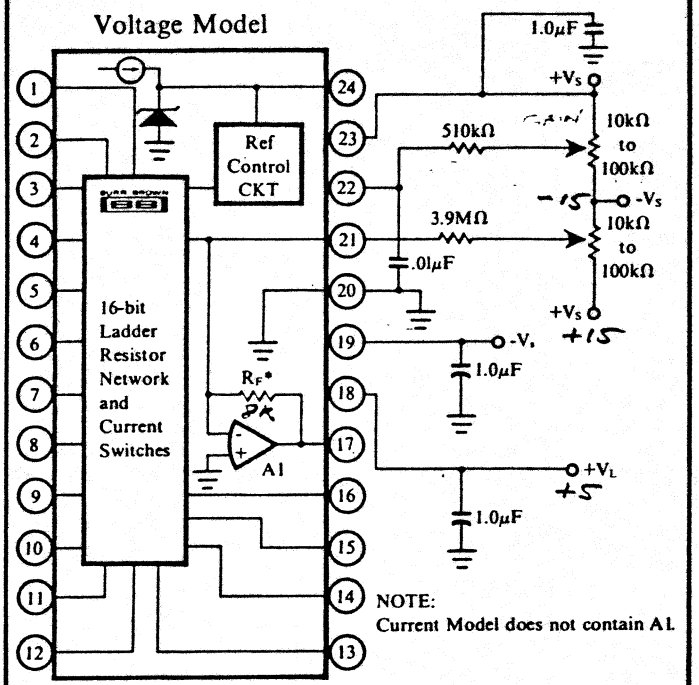
Pin numbers shown for reference only. Numbers may not be marked on package.

NOTE: Leads in true position, within .010" (.25mm) R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	0.85	.105	2.16	2.67

CASE: Black Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderabiltiy) of Mil-Std-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 Condition C Step 1 (fluorocarbon) of Mil-Std-883 (gross leak).

CONNECTION DIAGRAM



PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

*R_F = 5kΩ (CSB), 10kΩ (COB), 8kΩ (CCD).

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC71/72 accepts complementary digital input codes in either binary (CSB, COB) or decimal (CCD) format. The COB model may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES					
		MSB LSB	CSB	COB	CTC*
			Compl. Straight Binary	Compl. Offset Binary	Compl. Two's Complement
CSB, COB MODELS	All bits ON	0000...000	+Full Scale	+Full Scale	-1LSB
	Mid Scale	0111...111	+1/2 Full Scale	Zero	-Full Scale
	All bits OFF	1111...111	Zero	-Full Scale	Zero
		1000...000	Mid Scale -1LSB	-1LSB	+Full Scale
			CCD		*Invert the MSB of the COB code with an external inverter to obtain CTC code.
			(Complementary Coded Decimal) 4 Digits		
CCD MODELS	F.S. bits ON	0110...0110	+Full Scale		
	All bits OFF	1111...1111	Zero		

ACCURACY

LINEARITY

This specification describes one of the truest measures of D/A converter accuracy. As defined it means that the analog output will not vary by more than ±0.003% max (CSB, COB) or ±0.005% max (CCD) from a straight line drawn through the end points (all bits ON and all bits OFF) at +25°C.

DIFFERENTIAL LINEARITY

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can be anywhere from 1/2LSB to 3/2LSB when the input changes from one adjacent input stage to the next.

MONOTONICITY

Monotonicity over 0°C to +50°C (DAC71/72C) and 0°C to +70°C (DAC72) is guaranteed in the DAC71/72. This insures that the analog output will increase or remain the same for increasing 14-bit input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (see Figure 1). Gain Drift is established by: 1) testing the end point differences for each DAC71/72 model at +25°C and the appropriate specification temperature extremes; 2) calculating the gain error with respect to the +25°C value; and 3) dividing by the

ANALOG DEVICES

High Accuracy, 100kHz and 1MHz Voltage to Frequency Converters

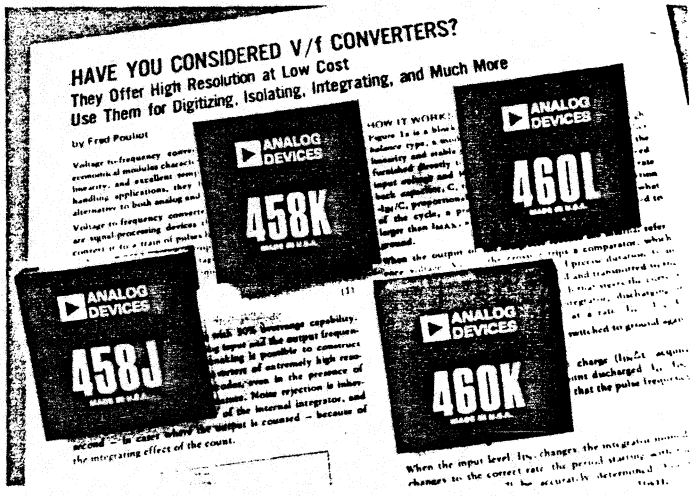
MODELS 458 and 460

FEATURES

High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
Low Nonlinearity: 100ppm max, Model 458
150ppm max, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL or CMOS/HNIL Compatible Output

APPLICATIONS

Fast Analog-to-Digital Converter
High Resolution Optical Data Link
Ratiometric Measurements
2-Wire High Noise Immunity Digital Transmission
Long Term Precision Integrator



GENERAL DESCRIPTION

Models 458 and 460 are high performance, differential input, voltage to frequency modular converters designed for analog to digital applications requiring accuracy and fast data conversion. Model 458 offers a 100kHz full scale frequency, guaranteed nonlinearity of ±0.01% maximum over five decades (1Hz to 100kHz) of operation and guaranteed low maximum gain drift in three model selections; model 458L: 5ppm/°C max; model 458K: 10ppm/°C max; and model 458J: 20ppm/°C max. Model 460 offers a 1MHz full scale frequency, guaranteed maximum nonlinearity of ±0.015% over six decades (1Hz to 1MHz) of operation and guaranteed low maximum gain drift in three selections; model 460L: 15ppm/°C max; model 460K: 25ppm/°C max; and model 460J: 50ppm/°C max. Model 460L is the industries' first 1MHz V/F converter to offer 15ppm/°C maximum gain drift.

The differential input stage of models 458 and 460 provide the versatility of either direct interface to off-ground 0 to +11V input signals with common mode voltages (CMV) to ±10V, as well as ground referenced positive, 0 to +11V or negative, 0 to -11V signals. Both models also accept positive current signals: 0 to +0.5mA, model 458; 0 to +1mA, model 460 for current to frequency (I/F) applications.

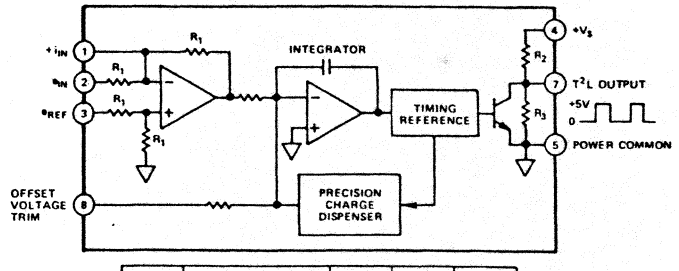
The rated performance of both models 458 and 460 is achieved without the need for external components or adjustments. Optional adjustments are available for trimming full scale frequency and the input offset voltage.

WHERE TO USE MODELS 458 AND 460

The combination of low gain drift, low nonlinearity and the versatility of a differential input with both high speed (100kHz/1MHz) models, offer excellent solutions to a wide variety of demanding applications; in high speed remote data acquisition systems — two wire data transmission over long wires; in 5½ digit DVM's — featuring high resolution A/D conversion, monotonic performance, no missing codes and high noise rejection; in strain gage bridge weighing applications — accurate ratiometric measurements over wide dynamic range.

DESIGN APPROACH - PRECISION CHARGE BALANCE

Models 458 and 460 incorporate a superior charge balance design that result in high linearity and temperature stability - see Figure 1. Both models accept unipolar, single-ended voltage or current input signals directly. By offsetting the input using the current terminal, models 458 and 460 will accept bipolar input voltages up to ±5V.



MODEL	FULL SCALE OUTPUT	R_1	R_2	R_3
458	100kHz	20kΩ	10kΩ	4.7kΩ
460	1MHz	10kΩ	2kΩ	910Ω

Figure 1. Block Diagram - Models 458, 460

P.O. Box 280; Norwood, Massachusetts 02062 U.S.A.
Telex: 924491 Cables: ANALOG NORWOODMASS

SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise noted)

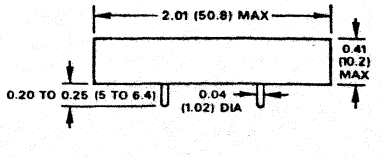
MODEL	100kHz Full Scale 458 J | K | L	1MHz Full Scale 460 J | K | L
TRANSFER FUNCTION		
Voltage Input	$f_{OUT} = (10^4 Hz/V)\ e_{IN}$	$f_{OUT} = (10^5 Hz/V)\ e_{IN}$
Current Input	$f_{OUT} = (2 \times 10^5 Hz/mA)\ i_{IN}$	$f_{OUT} = (10^6 Hz/mA)\ i_{IN}$
ANALOG INPUT		
Configuration	Differential	Differential
Voltage Signal Range		
e_{IN} Terminal (e_{REF} = 0)	0 to +10V dc min	0 to +10V dc min
e_{REF} Terminal (e_{IN} = 0)	0 to -10V dc min	0 to -10V dc min
Differential ($e_{IN} - e_{REF}$)	0 to +10V dc min	0 to +10V dc min
Overrange	+10% min	+10% min
Current Signal Range (i_{IN})	0 to +0.5mA min	0 to +1mA min
Common Mode Voltage	±10V	±10V
Common Mode Rejection	40dB	40dB
Impedance, e_{IN} Terminal	20kΩ	10kΩ
e_{REF} Terminal	40kΩ	20kΩ
i_{IN} Terminal	0Ω	0Ω
Max Safe Input	$\pm V_S$	$\pm V_S$
ACCURACY		
Warm Up Time	5 Seconds to 0.01%	2 Minutes to 0.02%
Nonlinearity, e_{IN} = +0.1mV to +11V	±0.01% of Full Scale, max	±0.015% of Full Scale, max
e_{IN} = -0.1mV to -11V	±0.01% of Full Scale	±0.015% of Full Scale
Full Scale Error[1]	+0.1% to +2%, max	+0.1% to +2%, max
Gain vs. Temperature (0 to +70°C)	±20ppm/°C max | ±10ppm/°C max | ±5ppm/°C max	±50ppm/°C max | ±25ppm/°C max | ±15ppm/°C max
vs. Supply Voltage	±15ppm/%	±25ppm/%
vs. Time	±10ppm/day	±10ppm/day
Input Offset Voltage[2]	±10mV max	±10mV max
vs. Temperature (0 to +70°C)	±30μV/°C max	±30μV/°C max
vs. Supply Voltage	±10μV/%	±10μV/%
vs. Time	±20ppm/day	±10ppm/day
RESPONSE		
Settling Time, ±0.01% +10V Step	3 Output Pulses Plus 2μs	2 Output Pulses Plus 2μs
Overload Recovery Time	10ms	1ms
FREQUENCY OUTPUT[3]		
Waveform	TTL/DTL Compatible Pulses	TTL/DTL Compatible Pulses
Pulse Width	5μs	500ns
Rise and Fall Time	300ns/50ns	60ns/50ns
Pulse Polarity	Positive	Positive
Logic "1" (High) Level	+2.4V min	+2.4V min
Logic "0" (Low) Level	+0.4V max	+0.4V max
Capacitive Loading	500pF max	200pF max
Fan Out Loading	10 TTL Loads min	10 TTL Loads min
Impedance	3kΩ (High State)	670Ω (High State)
POWER SUPPLY[4]		
Voltage, Rated Performance	±15V dc	±15V dc
Voltage, Operating	±(13 to 18)V dc	±(13 to 18)V dc
Current, Quiescent	(+25, -8)mA	(+25, -8)mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	0 to +70°C
Operating	-25°C to +85°C	-25°C to +85°C
Storage	-55°C to +125°C	-55°C to +125°C
MECHANICAL		
Case Size	2" x 2" x 0.4"	2" x 2" x 0.4"
Weight	45 Grams	45 Grams
Mating Socket	AC1016	AC1016

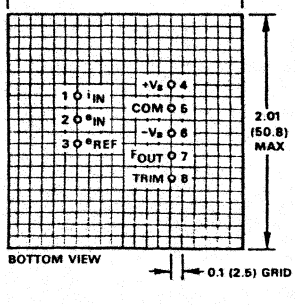
[1] Adjustable to zero using 500Ω potentiometer.
[2] Adjustable to zero using 50kΩ potentiometer.
[3] Protected for continuous short-circuits to ground and momentary (less than 1 sec) shorts to the $+V_S$ supply. Output is not protected for shorts to the $-V_S$ supply.
[4] Recommended power supply, ADI model 904, ±15V @ 50mA output.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).





Applying the Voltage to Frequency Converter

VOLTAGE TO FREQUENCY OPERATION

Models 458 and 460 provide accurate conversion of analog signals into a train of constant width and constant amplitude pulses at a rate directly proportional to the analog signal amplitude. The output continuously tracks the input signal, responding directly to changes in the input signal; external clock synchronization is not required. The output pulse train is TTL/DTL compatible, permitting direct interface to digital processing circuits. Adding a resistor from the output terminal, pin 7, to the +15V supply (1.2kΩ model 458; 820Ω model 460), shifts the output swing from 0 to +5V to 0 to +12V, providing a 4V noise immunity for driving high noise immunity logic (HNIL) and CMOS logic.

BASIC V/F HOOK-UP AND OPTIONAL TRIMS

Models 458 and 460 can be applied directly to achieve rated performance without external trim potentiometers or other components. Figures 2, 3 and 4 below illustrate the basic wiring connections for either V/F converter model. Using the basic hookup without trims, full scale (e_{IN} = 10V) accuracy is +0.1% to +2% and the input offset voltage is ±10mV max. The full scale and input offset voltage errors can be eliminated by using the FINE TRIM PROCEDURE.

FINE TRIM PROCEDURE

Connect the optional trims as shown in Figure 2, 3 or 4 and allow a five minute warm-up after initial power turn-on.

V/F INTERCONNECTIONS

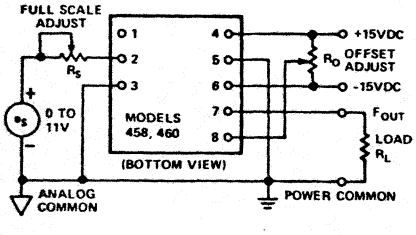


Figure 2. Positive Input Signal

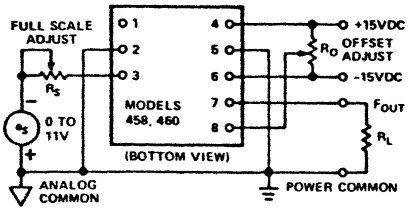


Figure 3. Negative Input Signal

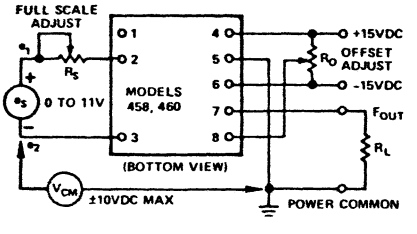


Figure 4. Floating Input Signal

EXTERNAL CONNECTIONS FOR VOLTAGE TO FREQUENCY OPERATION, WITH OPTIONAL INPUT OFFSET VOLTAGE AND FULL SCALE FREQUENCY ADJUSTMENTS

R_S = FULL SCALE ADJUSTMENT; 500Ω (Use low T.C. Cermet, < 50ppm/°C or equivalent)
R_O = INPUT OFFSET ADJUSTMENT; 50kΩ (Use low T.C. Cermet, < 50ppm/°C or equivalent)

CAUTION: DO NOT SHORT OUTPUT TERMINAL TO -15V

Using a precision, stable voltage source, set the input voltage, e_S, to 10mV. Adjust the OFFSET trim, R_O, for an output pulse interval of 0.1 sec (model 458) or 0.01 sec (model 460). Set the input voltage to +10.000V and adjust the FULL SCALE trim for an output pulse frequency of 100kHz (model 458), or 1MHz (model 460). The V/F converter may now be used without further adjustment.

DIFFERENTIAL INPUT

The e_{IN} and e_{REF} input terminals represent a true differential input capable of accepting a signal from a strain gage bridge, a balanced line, or a signal source sitting at a common mode voltage. The differential input eliminates the need for a differential amplifier to handle these signals.

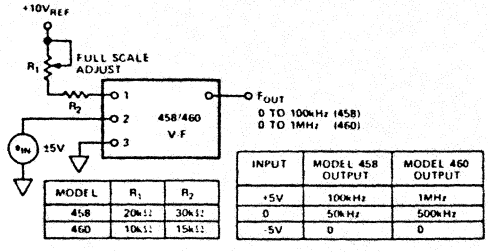
To apply the 458 or 460 voltage inputs differentially, the e_{IN} pin must always be positive with respect to the e_{REF} pin as shown in Figure 4. The differential signal source may be completely floating with common mode voltages up to ±10V max. For differential inputs the output frequency is:

$$F_{OUT} = \left[\underbrace{(e_1 - e_2)}_{\text{INPUT SIGNAL}} + \underbrace{\left(\frac{e_1 + e_2}{2}\right) \times \left(\frac{1}{CMR}\right)}_{\text{CMR ERROR}} \right] K_g$$

K_g = 10^4 Hz/V; model 458
10^5 Hz/V; model 460

OFFSETTING INPUT FOR BIPOLAR INPUTS

The input summing terminal, $+i_{IN}$, may be used to improve dynamic response as well as scale the output frequency to directly convert bipolar input voltages. An offset current is fed through an external resistor from a stable voltage reference. As shown in Figure 5, input voltages of ±5V min can be converted directly.

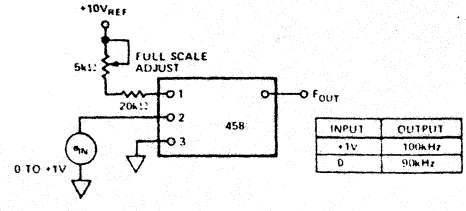


MODEL	R_1	R_2
458	20kΩ	30kΩ
460	10kΩ	15kΩ

INPUT	MODEL 458 OUTPUT	MODEL 460 OUTPUT
+5V	100kHz	1MHz
0	50kHz	500kHz
-5V	0	0

Figure 5. Offsetting Input to Accept ±5V Bipolar Inputs

The output may also be scaled up so that low amplitude signals, such as 1V will give full scale output frequency; 100kHz model 458 or 1MHz model 460. By scaling the output frequency for low level signals, the step response will significantly improve. As shown in Figure 6 for model 458, the step response for a 1 volt input decreases from 200μs before input scaling, to 20μs with scaling.



INPUT	OUTPUT
+1V	100kHz
0	90kHz

Figure 6. Offsetting Input to Achieve Improved Dynamic Response for Small Signal Inputs

PERFORMANCE SPECIFICATIONS

Nonlinearity: Nonlinearity error is specified as a % of 10V full scale input and is guaranteed over the 0.1mV to 11V operating signal range; ±0.01% max, models 458J/K/L, ±0.015% max, models 460J/K/L. Typical nonlinearity performance is illustrated in Figure 7.

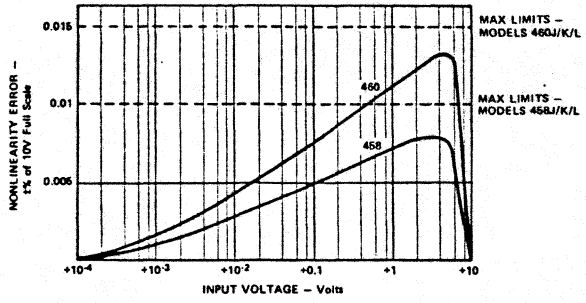


Figure 7. Nonlinearity Error Versus Input Voltage

Gain Temperature Stability: Gain drift is specified in ppm of output signal and is guaranteed for each model over the 0 to +70°C temperature range; 5ppm/°C (458L), 10ppm/°C (458K), 20ppm/°C (458J), 15ppm/°C (460L), 25ppm/°C (460K) and 50ppm/°C (460J) max.

LONG TERM PRECISION INTEGRATOR

In critical measurement applications, such as pollution monitoring where it is required to integrate for periods greater than 1 hour with overall accuracy of 0.05%, the V/F converter offers a superior low cost approach when compared to the traditional operational integrator circuit. As shown in Figure 8, the analog signal is applied to a precision input amplifier, model 52K and then to the V/F input. The V/F output is connected to a large capacity counter and display, operating as a totalizer. The total pulse count is equal to the time integral of the analog input signal. Since the output displayed is an accumulated pulse count, there is no integrator drift error. A feature of this approach is the infinite hold capability without errors due to time drift, since the counter may be held at any time without affecting the output reading.

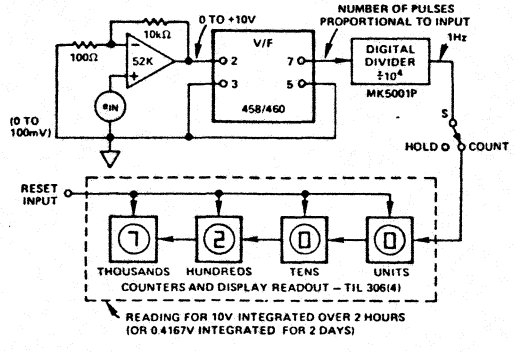


Figure 8. Models 458/460 as Long Term Integrator with Arbitrary Display Calibration. Frequency Division Ratio can Otherwise be Chosen to Provide Direct Readout in any Desired Units

RATIOMETRIC MEASUREMENTS

The circuit shown in Figure 9 illustrates a simple and inexpensive way of using two 100kHz V/F converters to achieve ratiometric measurements with less than 0.1% error over a dynamic range of 10,000 to 1. One converter is used as the input V/F to a digital counter and display, while a second converter, with a digital divide-by-N circuit is used as the time base for the counter. The counting time is one half the output period of the divide-by-N circuit, resulting in an output count of $2NV_1/V_{REF}$.

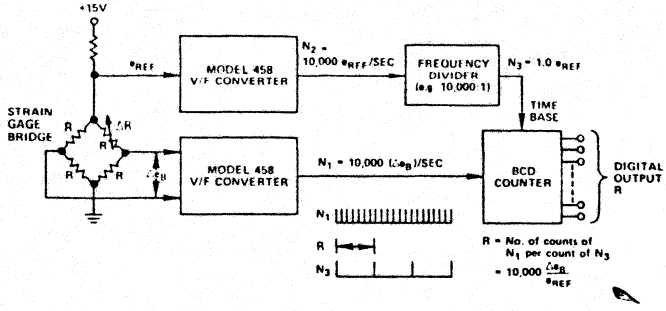


Figure 9. High Resolution, Wide-Range Ratiometer Using Model 458 V/F Converter

PRECISION HIGH CMV ANALOG ISOLATOR

By combining the V/F converter with a floating power supply and optical isolator as shown in Figure 10, accurate low level measurements in the presence of high common mode voltages may be achieved. Only the CMV rating of the optical isolator and the breakdown rating of the power supply limit the CMV rating. Using this approach for isolating transducers, ground loop problems are eliminated. Cost and complexity are minimized since only a single optical isolator is required to couple the serial pulse output from the V/F to the digital readout.

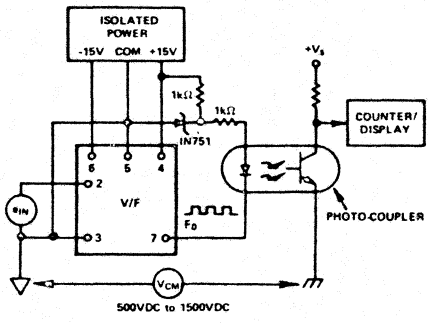


Figure 10. Optical Isolation Using LED Photo Isolator to Provide Up to 1500VDC CMV Isolation

APPLICATION IN DATA ACQUISITION SYSTEMS

High Noise Immunity Data Transmission: A method of accurately transmitting analog data through high noise environments is illustrated in Figure 11. This approach utilizes the self clocking output of models 458 and 460 and eliminates the need for costly additional twisted pair for external synchronization. Model 610 amplifies the low level differential transducer signal up to the 10V full scale V/F input level. A differential line driver is used to drive a twisted pair cable. The differential line driver and receiver offer high noise immunity to common mode noise signals.

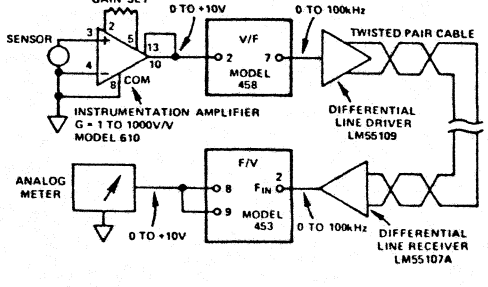


Figure 11. Application of Model 458 V/F Converter in a High Performance, High Noise Rejection Two-Wire Data Transmission System