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RESISTANCE ASSOCIATED WITH FET GATE METALLIZATION

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Abstract

The resistance of the metallization of a FET gate stripe has the effect of placing a non-linear resistance R(I) in series with the gate junction. A simple means of calculating R(I) is developed, and a curve of the drop across R(I) at milliampere forward biases is given.

RESISTANCE ASSOCIATED WITH FET GATE METALLIZATION

The resistance of the metallization of the short, wide gate stripe of a FET, together with the gate junction, can evidently be modelled as a ladder containing incremental series resistances and shunt Schottky diodes. The terminal behavior of the entire stripe/junction ladder can be further modelled as a single non-linear resistance R(I) in series with the junction, i.e., in series with the parallel combination of all of the diodes in the ladder. For small forward currents or for reverse bias, R(I) approaches R(0), which has been shown by Wolf [1] to be equal to 1/3 of the end-to-end resistance of the gate stripe metallization. R(0) detracts appreciably from the performance of the FET as a microwave amplifier, so an accurate determination is desirable. In microwave measurements at the FET terminals, R(0) is masked by the high reactance of the gate-to-source capacitance and also by impedances produced by feedback through various parasitic elements. Weinreb [2] finds that these masking effects severely limit the accuracy of the determination of R(0) from S-parameter data.

An alternative approach is to determine R(0) from d-c measurements, as is suggested by Fukui [3], and then to calculate -- or even to neglect -- the typically small correction for skin effect at r-f: The resistance correction for an aluminum gate stripe 0.7μm thick is less than 1% at 5 GHz. The essence of the d-c measurements is that the stripe/junction is forward-biased strongly enough so that the drop across R(I) is a measurable

fraction of the Schottky junction voltage. This junction voltage, extrapolated from measurements at lesser forward currents, is subtracted from the total stripe/junction voltage, leaving the drop across R(I). The strong forward bias needed to measure R(I) requires gate currents in the 1-20ma range that place the non-linear character of R(I) in evidence. One purpose of this letter is to relate R(I), measured with strong forward bias, to R(0), its value when the FET is normally biased as an amplifier. Now if the total voltage were measured from gate to source, the drop remaining after the above subtraction would include comparable drops across other more-or-less current-independent resistances in the FET model. Except for the last paragraph, it will be supposed in this letter that such additional drops have been accounted for, perhaps by the methods of [3], leaving only the gate stripe metallization and junction to be dealt with here.

The ladder model of the stripe/junction is suggested by Figure 1 for current flow across the width of the stripe. The differential equations for this distributed structure read

$$\frac{\partial V}{\partial x} = - rI \tag{1}$$

$$\frac{\partial I}{\partial x} = - c(e^{V/v_o} - 1) \simeq - ce^{V/v_o}, \tag{2}$$

in which

r = metallization resistance per unit width of stripe

$c(e^{V/v_o} - 1)$ = diode current per unit width of stripe

v_o = barrier potential of each incremental Schottky diode.

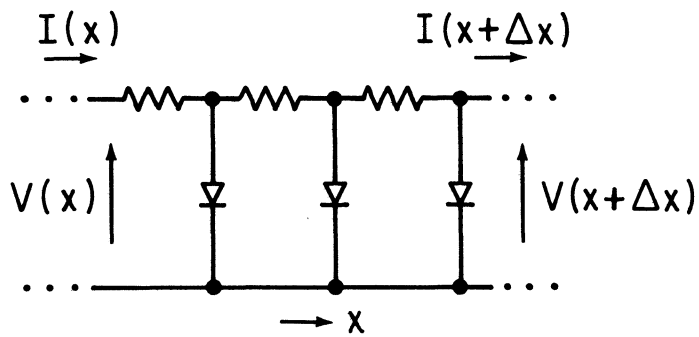

Figure 1. Model of junction and metallization resistance.

Measurements will be made at forward gate currents far in excess of the saturation current, as is suggested by the approximation in (2). With the change of variable $y \equiv V/v_o$ and the introduction of $a \equiv rc/v_o$, (1) and (2) can be simplified and combined to read

$$\frac{d^2y}{dx^2} = ae^y.$$

With $\dot{y} \equiv \frac{dy}{dx}$, so that

$$\frac{d^2y}{dx^2} = \frac{d\dot{y}}{dx} = \frac{d\dot{y}}{dy}\frac{dy}{dx} = \dot{y}\frac{d\dot{y}}{dy} = a\,e^y,$$

the equation separates to produce

$$\dot{y}d\dot{y} = a\,e^y\,dy$$

$$\tfrac{1}{2}\dot{y}^2 = a\,e^y - 2k^2$$

$$\dot{y} = \frac{dy}{dx} = -\sqrt{2a\,e^y - 4k^2}.$$

The negative sign has been chosen for the radical because V(x) and hence y(x) will certainly diminish as the distance x from the point of gate current application increases. It turns out that the constant of integration $2k^2$ must be positive if there is to be an end of the stripe where I = 0; k itself will also be taken to be positive. The last integration is most easily performed using y = ln t, so that

$$\frac{dy}{dx} = \frac{1}{t}\frac{dt}{dx} = -\sqrt{2at - 4k^2}$$

$$\frac{dt}{t\sqrt{2at - 4k^2}} = -\,dx$$

$$\frac{1}{k}\tan^{-1}\sqrt{\frac{2at - 4k^2}{4k^2}} = w - x.$$

Solved for t, this yields

$$V(x) = v_o \ln t = v_o \ln\left(\frac{2k^2}{a \cos^2 k(w-x)}\right) \tag{3}$$

$$I(x) = -\frac{1}{r}\frac{\partial V}{\partial x} = \frac{2kv_o}{r} \tan k(w - x). \tag{4}$$

The last constant of integration w is evidently the width of the gate stripe: Gate current enters the metallization at x = 0 and falls to zero at x = w.

The terminal behavior -- V ≡ V(0); I ≡ I(0) -- of this resistor-diode ladder can be expressed as

$$I = \frac{2v_o}{\rho} \cdot \theta \tan \theta \tag{5}$$

$$V = v_o \ln\left(\frac{2v_o}{\alpha \rho} \cdot \frac{\theta^2}{\cos^2 \theta}\right) = v_o \ln\left(\frac{2v_o}{\alpha \rho} \theta \tan \theta \cdot \frac{\theta}{\sin\theta \cos\theta}\right)$$

$$= v_o \ln\left(\frac{2v_o}{\alpha \rho} \theta \tan \theta \cdot \frac{2\theta}{\sin 2\theta}\right)$$

$$= v_o \ln(I/\alpha) + v_o \ln\left(\frac{2\theta}{\sin 2\theta}\right) \tag{6}$$

by using the convenient parameters

$\theta = kw$, contains the still-to-be-determined constant of integration k.

$\rho = rw = 3\,R(0)$ = end-to-end resistance of stripe metallization

$\alpha = cw$ = total junction saturation current.

Given the gate current I, it seems necessary to solve the transcendental equation (5) for θ -- which will lie in the range $0 \leq \theta \leq \pi/2$ -- in order to determine the stripe/junction voltage V. Using the normalized gate current

$$u = \frac{\rho I}{2v_o} = 3/2 \frac{IR(0)}{v_o} = \theta \tan \theta , \qquad (7)$$

the required solution is completed efficiently by the three iterative steps of the following algorithm:

Radians

n = 0

$\theta = \tan^{-1}\sqrt{u}$

n = n + 1

$b = u/(\theta^2 + u^2 + u)$

$\theta = b\theta + (1-b) \tan^{-1} (u/\theta)$

If n < 3 then

End

In this algorithm, (7) is iterated in such a way that convergence is guaranteed for all $u > 0$. The parameter b is chosen to force quadratic convergence, and b is updated at each step. As described so far, the algorithm is weakest for small u, so the initial estimate of θ is chosen to be particularly good for small u. When executed by a floating point calculator with 12 digits of mantissa and 2 of exponent, θ is determined for $10^{-49} < u < 10^{49}$ with error mostly confined to the last mantissa digit.

Returning to the metallization resistance question, the term

$$E = v_o \ln(I/\alpha) \tag{8}$$

in (6) is the junction voltage in the absence of any stripe resistance. The gate stripe metallization and junction can therefore be modelled as the junction itself in series with the single non-linear resistance

$$R(I) = \frac{V - E}{I} = \frac{\rho}{2} \cdot \frac{\ln\left(\frac{2\theta}{\sin 2\theta}\right)}{\theta \tan \theta}$$

$$= \frac{\rho}{3}\left(1 - \frac{1}{5}\theta^2 - \frac{31}{945}\theta^4 - \ldots.\right), \tag{9}$$

from (5), (6), and (8). Note that as I, and hence θ, vanishes, R(I) rises to Wolf's $R(0) = \rho/3$. Most of a higher gate current tends to be carried by the first few diodes in the ladder, so R(I) falls as gate current increases.

By dealing with the small difference between $\pi/2$ and θ at high gate currents, it can be shown that the log I vs. V characteristic of the stripe/junction has a second high-current asymptote having half the slope of the low-current asymptote produced by the junction itself. The two asymptotes intersect at $I = 2v_o/\rho$ -- or $u = 1$ -- which is typically within, but near the top of the range to which prudence limits d-c measurements. The fillet between the two asymptotes is drawn as the solid curve of Figure 2, which is a semi-log plot of u, the normalized gate current of (7), against

$$v = \frac{V - E}{v_o}, \tag{10}$$

the normalized drop across R(I). By extrapolating $E \simeq V$ from its values at lower forward currents, $V - E$, v_o, and I are determined. The curve is

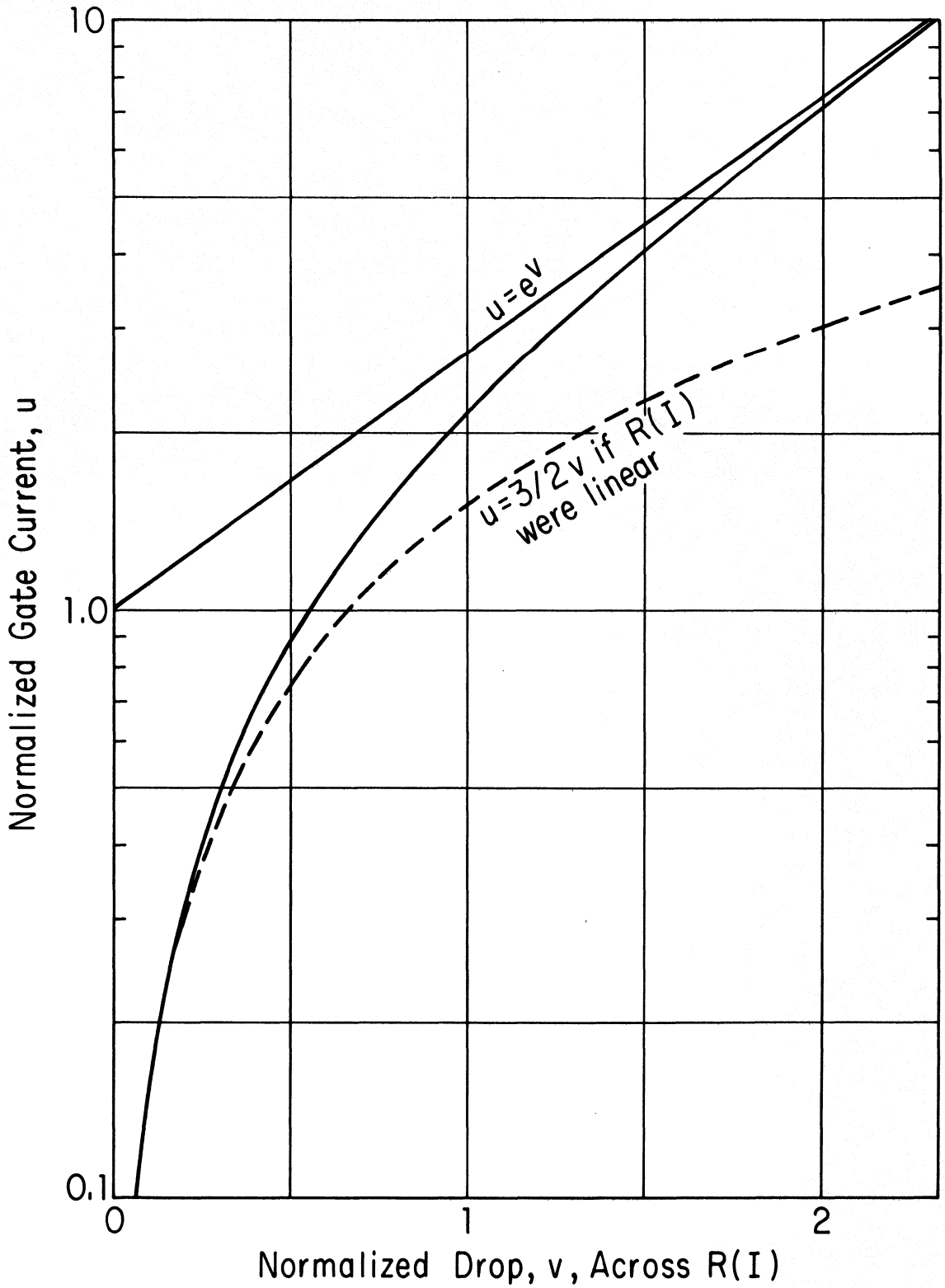

Figure 2. The volt-ampere characteristic of R(I).

entered with v, u is read, and R(0) is calculated from (7). The dashed curve is a plot of u = 3/2 v, which would apply if R(I) = R(0) for all I. Clearly, one must account for the non-linearity of R(I) in reducing the data from d-c measurements.

If much of the constant resistance from the FET model remains in the measured volt-ampere characteristic, the determination of R(0) from Figure 2 will not yield consistent results at different gate currents. When much data is to be reduced or when there is doubt about the presence of constant resistance, it is recommended that a model that also includes some fixed resistance be least-squares fitted to a complete set of data. From (5) and from (6) modified to include the fixed resistance, say R_{ext}, it will be noted that the conditions for minimization of the sum of squared errors can be made linear in the variables v_o, $v_o \ln\alpha$, and R_{ext}. If the linear conditions are imposed first, there remains a non-linear minimization in only the single variable $2v_o/\rho$.

ACKNOWLEDGMENT

I am indebted to S. Weinreb for exposing me to this problem and for convincing me that it deserved further work.

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[1] P. Wolf, "Microwave Properties of Schottky-barrier Field-effect Transistors", IBM Journal of Research and Development, v. 14, pp. 125-141, March 1970.

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