GBT 3mm Receiver
Monitor and Control Specification

1. Introduction

This document provides the reader with a brief description of the GBT 3mm receiver hardware (section 2), and follows with a specification for the monitor and control functions (sections 3, 4, and 5).

Basic monitor and control functions that do not have critical timing requirements, such as the monitoring of cryogenic temperatures, are handled by the Standard Interface Board on the MCB. These functions are defined in Sections 3 and 4 of this document. A separate subsystem, called the Thermal Calibration Optics, will be monitored and controlled via a separate network connection, independent from the MCB. The requirements for the Thermal Calibration Optics are given in section 5. Finally, a concise summary of all MCB specifications is given in tabular form in Appendix A, and a list of motor control commands for the Thermal Calibration Optics system in Appendix B.

2. Receiver Hardware Description

The GBT 3mm receiver operates in the frequency range of 68-92 GHz with two feeds, designated beams 1 and 2, viewing the sky at the same elevation. Each beam is dual polarized (linear) producing a total of four RF signal paths. The feed horns are designed for operation at the Gregorian focus of the GBT, are cooled to cryogenic temperatures inside the receiver dewar and view the sky through a shared, low-loss impedance-matched quartz vacuum window. Opposing polarizations from each beam are combined in hybrid-T junctions creating two dual path differencing assemblies. Each path of the differencing assembly contain phase switches that, when actuated, introduce a 180° phase shift in the signal in that path. The pairs of differencing paths are recombined with a second set of hybrid-T junctions resulting in four output channels. Each output channel is split into a full bandwidth channel for spectrometry and a channel divided into three frequency sub-bands for continuum detection and processing with such instruments as the California Institute of Technology Continuum Back End (CCB).

A noise calibration system, comprised of a single diode noise source followed by a two-way splitter, provides for injection of noise into the vertical polarization of each of the two feeds. Coupling of the noise into the RF path is achieved by means of crossguide couplers located just after the feed horns and polarizers.

The local oscillator (LO) signal for the GBT 3mm Receiver is obtained by frequency multiplying the LO1 synthesizer output by a factor of four (X4). The LO1 frequency will typically be set to 16.5 GHz, giving a final LO frequency of 66.0 GHz. Note that the LO frequency is on the low side of the RF band. As such, the RF spectrum will NOT be

inverted, as viewed at the first IF which covers 2-26 GHz. LO power level will be monitored at the input to the X4 frequency multiplier.

A Note on Amplifier Designation:
This receiver is a differencing receiver and as such has no polarity distinction at the amplifier stages. Amplifiers are designated according to Beam 1 or Beam 2 and Sum or Difference. In addition, this receiver has two cascaded amplifiers in each arm of the differencing assembly, which will be designated “a” and “b”. Therefore, each amplifier has a 3-character designator scheme – indicating its beam number (1 or 2), path (Sum or Difference), and order (a or b). For example: the first amplifier in the Beam 1 Sum path is designated 1Sa, and the second amplifier in the Beam 2 difference path is designated 2Db.

3. System Control, MCB

Control is accomplished by writing a code to a specified control relative address. This data is latched and may be verified by a read to the same relative address. Note that the LOCAL/MCB switch on the receiver local control box (located on the front-end) must be in the MCB position before MCB control of certain receiver functions (the noise cal sources and the phase switch polarity) is possible. In addition, the cryogenic control switch on the manual control box must be in the CPU position before MCB control of the cryogenics state is possible. Both of these switches may be monitored via the MCB (see Table III).

Control of the receiver may be divided into four categories, cryogenic state control, calibration signal control, phase modulator switch control, and cryogenic amplifier control.

Each explanation of the relative monitor or control address contains bit level control descriptions.

The MCB ID number for the 3mm Receiver is TBD.

3.1 Cryogenic State Control, Relative Address 48h.

Three Bits, X, C and not-H allow control of the receiver's refrigerator and heater. The cryogenic state may be set by writing the desired code to the Cryo Control address, relative address 48h. The cryogenic control code description is shown here:

b_2 (X)	b_1(H')	b_0(C)	Decimal	Name	
1	1	0	6	OFF	No refrigerator or heater power.
1	1	1	7	COOL	Normal cooled operation.
1	0	1	5	HEAT	Fast warm up of dewar with 33 watts of heat added. PUMP REQ becomes high when dewar vacuum is greater than 10 microns.
0	0	1	1	PUMP	No refrigerator or heater power. PUMP REQ high.

The cryogenic state control is not absolute. The circuitry within the receiver will not execute a command which will cause damage to the receiver. In order for the refrigerator to start the vacuum of the dewar must be sufficiently low. The circuitry used in controlling this receiver is the same used in VLBA receivers and is described in VLBA Technical Report No. 1. One exception is that this receiver has a manually operated vacuum valve rather than a solenoid operated unit.

MCB Interface pins:
b_0: P13-1 b_1: P13-2 b_2: P13-3

Bit 3 is not used. This is a 4 bit address.

3.2 Calibration Signal Control Select, Relative Addresses 49h and 4Ah.

Relative address 49h, bits 0, 1, and 4, give the user several options for control of the noise diode's state; the noise diode may be toggled on/off using any one of four control inputs: the CAL signal (originating from backends such as the DCR), the CalTech Continuum Backend (CCB), the manual toggle switch on the receiver, or by selecting the appropriate button on a CLEO user interface. Control is assigned by writing to RA 49h, bits 0 and 1 as follows:

b_1 b_0
0 0 : LOCAL manual control via a switch on the receiver control box.
0 1 : EXT Cal input to the receiver through BNC connector J31.
1 0 : Control of noise source by the MCB, via b_4 (see below).
1 1 : Control of noise source by the CCB.

b_4 Controls the diode noise source for beams 1 & 2 with the MCB. When bit 4 is set HIGH the noise source is OFF.

When in the EXT control mode (bit 0 is high, and bit 1 low), a TTL low signal at connector J31 turns both noise sources ON; TTL high turns them OFF.

Relative address 4Ah, bits 0 and 1 are used to enable the EXT input to the noise sources over as follows:

b_0 - Controls the diode noise source for beams 1 & 2 with the EXT input, J31. When bit 6 is set LOW, the noise source is ON when EXT is LOW.

b_1 - Controls the diode noise source for beams 3 & 4 (future use) with the EXT input, J31. When bit 7 is set LOW the noise source is ON when EXT is LOW.

MCB Interface Pins:
[RA49, b_0: P13-5, b_1: P13-6, b_4: P13-9] [RA4A, b_0: P13-13, b_1: P13-14]

Bits 2 and 3 are not used.

3.3 Phase Modulator Control Select, Relative Address 4Dh.

Similar to the noise calibration signal control, the phase switches may be controlled from a variety of sources. Selection of the appropriate source is implemented through RA 4Dh as follows:

b_1 b_0
0 0 : LOCAL manual control via switches on the receiver control box.
0 1 : Control of phase switches individually by the SIG/REF-EXT PHASE Input.
1 0 : Control of phase switches individually by the MCB via RA 4Ah.
1 1 : Control of phase switches individually by the CCB.

MCB Interface Pins:
b_0: P13-33 b_1: P13-34

Bits 2 - 7 are not used.

3.4 Cryogenic Amplifier Bias On/Off, Relative Address 4Bh.

Relative address 4Bh provides control of the bias voltage for each of the eight cryogenic low-noise HFET amplifiers, according to the following table:

Amplifier Bias:

b_0	Beam 1 Sum, a (1Sa)
b_1	Beam 1 Sum, b (1Sb)
b_2	Beam 1 Difference, a (1Da)
b_3	Beam 1 Difference, b (1Db)
b_4	Beam 2 Sum, a (1Sa)
b_5	Beam 2 Sum, b (1Sb)
b_6	Beam 2 Difference, a (1Da)
b_7	Beam 2 Difference, b (1Db)

3.5 Phase Modulator Switch Control, Relative Address 4Ah

The phase switches are controlled by relative address 4Ah if 4Dh: b_1=1, b_0=0.

When a bit is set HIGH the modulator switch current is POSITIVE.

b_0 - Beam 1 sum (1S).
b_1 - Beam 1 difference (1D).
b_2 - Beam 2 sum (2S).
b_3 - Beam 2 difference (2D).

MCB Interface Pins:
b_0: P13-16 b_1: P13-17 b_2: P13-18 b_3: P13-19

This is a 4 bit address.

3.6 Cryogenic Amplifier Bias Level Control, Relative Addresses 40h-43h

Relative addresses 40h-47h allow trimming the bias of the final two stages of each cryogenic HFET amplifier. D/A converters have their outputs connected to trim the gate bias of the last stage of cryogenic amplification, enabling the gain to be varied over about a 2 dB range. Address assignments are:

RA, hex	**Amplifier**
40	1Sa
41	1Sb
42	1Da
43	1Db
44	2Sa
45	2Sb
46	2Da
47	2Db

The digital control code used to set the D/A converters is offset binary where

4095 gives +10 volts,
2048 gives 0 volts,
0 gives -10 volts.

Control software should default to 2048 giving 0 volts D/A output.

4. System Monitor, MCB

The contents of the registers at all control addresses can be read by monitor command to the control address. Additional monitor points are also provided here.

4.1 Digital Monitor

The cryogenic state, phase switch condition, noise switch condition, MCB/CCB control and external cal/sig ref signals are all monitored at points closer to the actual hardware for fault detection within the control circuitry.

4.1.1 Cryogenic and Local/MCB Status Monitor, Relative Address 50h

Bits at relative address 50h are used to monitor the status of the dewar cryogenic control system, and Local/MCB hardware switches. Details are shown below.

Cryogenic Control State

b_2	b_1	b_0	Decimal	State	MCB Pin
X	H	C			
1	1	0	6	OFF	
1	1	1	7	COOL	
1	0	1	5	HEAT	
0	0	1	1	PUMP	

b_3, Pump Request, MCB Interface Pin P12-4
This bit indicates the state of the Control card Pump Request bit. Logic 1 indicates the dewar vacuum is higher than normal.

b_6, Refrigerator CPU Monitor, Pin P12-7
This bit is logic 1 when the Refrigerator Control rotary switch on the receiver local control box is in the CPU position. Logic 0 indicates RA 48 does NOT have control of the cryogenic state.

b_7, Cal Local Monitor, Pin P12-8
This bit is logic 1 when the MCB/Local control toggle switch on the receiver local control box is in the Local position. In this condition, RA 49, 4A and 4B do NOT have control of the noise cal sources, MCB/CCB control grant or phase switches.

b_4 and b_5 are not used.

MCB Interface Pins:

b_0: P12-1	b_1: P12-2	b_2: P12-3	b_3: P12-4
b_4: P12-5	b_5: P12-6	b_6: P12-7	b_7: P12-8

4.1.2 Receiver Identification Monitor, Relative Address 51h

The identification of the receiver can be read at relative address 51h. Bits 0 through 6 return the seven bit MCB ID Byte for this device. Bit 7 is an odd parity bit for the ID Byte. Bits 8, 9, and 10 are designated for the receiver serial number. Bits 11, 12, and 13 give the modification level of the receiver. For the 3mm Receiver, decimal TBD is assigned as the MCB ID number.

MCB Interface Pins:

b_0 - b_{13}: P12-9 - P12-22

4.1.3 Calibration and SIG/REF Status Monitor, Relative Address 52h

The Calibration Status address, relative address 52h, monitors the Cal Control Select signals, the external CAL control signal, the state of the calibration noise sources and the Cal control signals from the CCB. This eight bit monitor is defined as follows:

b_0 Monitors the CAL Control Select signal on RA49h-b_1

b_1 Monitors the CAL Control Select signal on RA49h-b_0

b_2 Monitors the EXT CAL control signal supplied to the dewar on connector J31. Logic 0 on bit 0 indicates logic 0 on J31.

b_3 Monitors the present state of the SIG/REF signal in slot 11.

b_4 Monitors the present state of noise source for beams 1 & 2. Logic 0 indicates ON; logic 1 indicates OFF.

b_5 Monitors the present state of noise sources for beams 3 & 4 (future use). Logic 0 indicates ON; logic 1 indicates OFF.

b_6 Monitors the Beams 1 & 2 cal control signal supplied by the CCB. Logic 1 indicates Cal On.

b_7 Monitors the Beams 3 & 4 cal control signal (future use) supplied by the CCB. Logic 1 indicates Cal On.

MCB Interface Pins:

b_0: P12-23 b_1: P12-24 b_2: P12-25 b_3: P12-26
b_4: P12-27 b_5: P12-28 b_6: P12-29 b_7: P12-30

4.1.4 Phase Modulator Status Monitor, Relative Address 53h

The status of the PMOD control select state and individual switches are monitored with relative address 53h. Individual switch monitor bits may be changing at rates in excess of 10 kHz while the switches are under control of the CCB.

b_0 Monitors the PMOD Control Select signal on RA4Dh-b_0.

b_1 Monitors the PMOD Control Select signal on RA4Dh-b_1.

b_2 Not used.

b_3 Not used.

b_4 Monitors the present state of the phase switch for beam 1, sum (1S).

b_5 Monitors the present state of the phase switch for beam 1, difference (1D).

b_6 Monitors the present state of the phase switch for beam 2, sum (2S).

b_7 Monitors the present state of the phase switch for beam 2, difference (2D).

MCB Interface Pins:

b_0: P12-31 b_1: P12-32 b_2: P12-33 b_3: P12-34
b_4: P12-35 b_5: P12-36 b_6: P12-37 b_7: P12-38

4.2 Analog Monitor Table

Note: The 12-bit A/D Counts value is returned by the SIB in two's complement form, with the MSB in bit position 15. Hence the returned value must be bit shifted right 4 positions and converted to a decimal float value before applying the formula below to obtain the Display value. The units of Counts * 4.8828e-3 is volts. The value of Mult and the resulting units are given below for each analog monitor point. Display = Mult * Counts * 4.8828e-3

RA	Description	Mult.	Units	Range	Digits	
00	LED Voltage 1Sab	2	Volts	0-10	x.xxx	
01	LED Voltage 1Dab	2	Volts	0-10	x.xxx	
O2	LED Voltage 2Sab	2	Volts	0-10	x.xxx	
O3	LED Voltage 2Dab	2	Volts	0-10	x.xxx	
O4	15K Temp	100	Kelvin	0-360	x.x	
O5	50K Temp	100	Kelvin	0-360	x.x	
O6	300 K Temp	100	Kelvin	0-360	x.x	
07	Dewar Vacuum	1000	mV	0-9999	x.	
08	Pump Vacuum	1000	mV	0-9999	x.	
09	+15 Supply Mon	2	Volts	0-20	x.xxx	
0A	-15 Supply Mon	2	Volts	-20-0	x.xxx	
0B	+5 Supply Mon	1	Volts	0-10	x.xxx	
0C	+28 Supply Mon	1/0.249	Volts	0-40	x.xxx	
Cryogenic Amplifiers:						
0D	1Sa, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
0E	1Sa, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
0F	1Sa, gate 1 voltage	2	Volts	-20-0	x.xxx	
10	1Sb, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
11	1Sb, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
12	1Sb, gate 1 voltage	2	Volts	-20-0	x.xxx	
13	1Da, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
14	1Da, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
15	1Da, gate 1 voltage	2	Volts	-20-0	x.xxx	
16	1Db, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
17	1Db, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
18	1Db, gate 1 voltage	2	Volts	-20-0	x.xxx	
19	2Sa, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
1A	2Sa, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
1B	2Sa, gate 1 voltage	2	Volts	-20-0	x.xxx	
1C	2Sb, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
1D	2Sb, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
1E	2Sb, gate 1 voltage	2	Volts	-20-0	x.xxx	
1F	2Da, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
20	2Da, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
21	2Da, gate 1 voltage	2	Volts	-20-0	x.xxx	
22	2Db, gate 5,6 voltage	2	Volts	-20-0	x.xxx	
23	2Db, gate 2, 3, 4 voltage	2	Volts	-20-0	x.xxx	
24	2Db, gate 1 voltage	2	Volts	-20-0	x.xxx	
25	Not used.					
26	Not used.					
27	Not used.					
28	Cal 1 current					
29	Cal 1 voltage					
2A	Phase switch, 1S, current					
2B	Phase switch, 1D, current					
2C	Phase switch, 2S, current					
2D	Phase switch, 2D, current					
2E	Phase switch, 3S, current					
2F	Phase switch, 3D, current					
30	Phase switch, 4S, current					
31	Phase switch, 4D, current					

5. Thermal Calibration Optics

The GBT 3mm Receiver has a thermal calibration system that requires controlled motion of hardware, using two independent stepper motors and associated programmable controllers.

The motor controllers are connected to the telescope control system through a multi-drop RS-485 serial port. This serial port is located on the receiver room Reset Box (gbtrbrc), on port XY. The port uses an external RS-232 to RS-485 converter. This port should be configured for:

ABCD Baud
X Stop bits
XYZ parity

The command set for the motor controllers may be found in Appendix B of this document.

Appendix A

Summary of MCB RA Assignments

Analog Control Table

Relative addresses 40h-47h allow trimming the bias of the final two stages of each cryogenic HFET amplifier. D/A converters have their outputs connected to trim the gate bias of the last stage of cryogenic amplification, enabling the gain to be varied over about a 2 dB range. Address assignments are

RA, hex	
40	1Sa
41	1Sb
42	1Da
43	1Db
44	2Sa
45	2Sb
46	2Da
47	2Db

Digital Relative Address Table

RA (Hex)	Description
Digital Control	
48	Cryogenic State Control
49	Calibration Control
4A	Phase Modulator MCB Control and EXT CAL Select
4B	Cryogenic Amplifier Bias ON/OFF
4D	Phase Modulator Control Select
Digital Monitor	
50	Cryogenic and Local/MCB Status Monitor
51	Receiver Identification
52	Calibration and SIG/REF Status Monitor
53	Phase Modulator Status Monitor

Analog Inputs, P10

PIN	NAME	RA	FUNCTION
1	AIN 1A	00	LED voltage 1Sab (beam 1, SUM channel, amplifiers a & b)
2	AIN 2A	01	LED voltage 1Dab
3	AIN 3A	02	LED voltage 2Sab
4	AIN 4A	03	LED voltage 2Dab
5	AIN 5A	04	15K temperature
6	AIN 6A	05	50K temperature
7	AIN 7A	06	300K temperature
8	AIN 8A	07	Dewar vacuum
9	AIN 1B	08	Pump vacuum
10	AIN 2B	09	+15V supply mon
11	AIN 3B	0A	-15Vsupply mon
12	AIN 4B	0B	+5V supply mon
13	AIN 5B	0C	+28V supply mon
14	AIN 6B	0D	Cryo LNA 1Sa, gate 5,6 voltage
15	AIN 7B	0E	Cryo LNA 1Sa, gate 2, 3, 4 voltage
16	AIN 8B	0F	Cryo LNA 1Sa, gate 1 voltage
17	AIN 1C	10	Cryo LNA 1Sb, gate 5,6 voltage
18	AIN 2C	11	Cryo LNA 1Sb, gate 2, 3, 4 voltage
19	AIN 3C	12	Cryo LNA 1Sb, gate 1 voltage
20	AIN 4C	13	Cryo LNA 1Da, gate 5,6 voltage
21	AIN 5C	14	Cryo LNA 1Da, gate 2, 3, 4 voltage
22	AIN 6C	15	Cryo LNA 1Da, gate 1 voltage
23	AIN 7C	16	Cryo LNA 1Db, gate 5,6 voltage
24	AIN 8C	17	Cryo LNA 1Db, gate 2, 3, 4 voltage
25	AIN 1D	18	Cryo LNA 1Db, gate 1 voltage
26	AIN 2D	19	Cryo LNA 2Sa, gate 5,6 voltage
27	AIN 3D	1A	Cryo LNA 2Sa, gate 2, 3, 4 voltage
28	AIN 4D	1B	Cryo LNA 2Sa, gate 1 voltage
29	AIN 5D	1C	Cryo LNA 2Sb, gate 5,6 voltage
30	AIN 6D	1D	Cryo LNA 2Sb, gate 2, 3, 4 voltage
31	AIN 7D	1E	Cryo LNA 2Sb, gate 1 voltage
32	AIN 8D	1F	Cryo LNA 2Da, gate 5,6 voltage
33	AIN 1E	20	Cryo LNA 2Da, gate 2, 3, 4 voltage
34	AIN 2E	21	Cryo LNA 2Da, gate 1 voltage
35	AIN 3E	22	Cryo LNA 2Db, gate 5,6 voltage
36	AIN 4E	23	Cryo LNA 2Db, gate 2, 3, 4 voltage
37	AIN 5E	24	Cryo LNA 2Db, gate 1 voltage
38	AIN 6E	25	
39	AIN 7E	26	
40	AIN 8E	27	
41	AIN 1F	28	Cal 1 current
42	AIN 2F	29	Cal 1 voltage
43	AIN 3F	2A	Phase switch, 1S, current
44	AIN 4F	2B	Phase switch, 1D, current
45	AIN 5F	2C	Phase switch, 2S, current
46	AIN 6F	2D	Phase switch, 2D, current
47	AIN 7F	2E	Phase switch, 3S, current
48	AIN 8F	2F	Phase switch, 3D, current
49	AIN 1G	30	Phase switch, 4S, current
50	AIN 2G	31	Phase switch, 4D, current

Analog Inputs and Outputs, P11

PIN	NAME	RA	FUNCTION
1	AIN 3G	32	Noise source, current, module 1 68-92 GHz
2	AIN 4G	33	Noise source, voltage, module 1 68-92 GHz
3	AIN 5G	34	Noise source, current, module 2 90-115 GHz
4	AIN 6G	35	Noise source, voltage, module 2 90-115 GHz
5	AIN 7G	36	LO detector voltage, module 1 68-92 GHz
6	AIN 8G	37	LO detector voltage, module 2 90-115 GHz
7	NOT USED		
8	NOT USED		
9	NOT USED		
10	NOT USED		
11	NOT USED		
12	NOT USED		
13	NOT USED		
14	NOT USED		
15	+5V		+5 VOLT SUPPLY
16	+5V		+5 VOLT SUPPLY
17	+5V		+5 VOLT SUPPLY
18	+5V		+5 VOLT SUPPLY
19	+5V		+5 VOLT SUPPLY
20	+5V		+5 VOLT SUPPLY
21	+5V		+5 VOLT SUPPLY
22	+15V		+15 VOLT SUPPLY
23	+15V		+15 VOLT SUPPLY
24	+15V		+15 VOLT SUPPLY
25	-15 V		-15 VOLT SUPPLY
26	-15 V		-15 VOLT SUPPLY
27	-15 V		-15 VOLT SUPPLY
28	GND		CHASSIS GROUND, AND DC RETURNS
29	GND		CHASSIS GROUND, AND DC RETURNS
30	GND		CHASSIS GROUND, AND DC RETURNS
31	GND		CHASSIS GROUND, AND DC RETURNS
32	GND		CHASSIS GROUND, AND DC RETURNS
33	GND		CHASSIS GROUND, AND DC RETURNS
34	GND		CHASSIS GROUND, AND DC RETURNS
35	AOUT 3E	40	Gain adjust, cryo LNA 1Sa
36	AOUT 4E	41	Gain adjust, cryo LNA 1Sb
37	AOUT 5E	42	Gain adjust, cryo LNA 1Da
38	AOUT 6E	43	Gain adjust, cryo LNA 1Db
39	AOUT 7E	44	Gain adjust, cryo LNA 2Sa
40	AOUT 8E	45	Gain adjust, cryo LNA 2Sb
41	AOUT 1F	46	Gain adjust, cryo LNA 2Da
42	AOUT 2F	47	Gain adjust, cryo LNA 2Db
43	NOT USED		
44	NOT USED		
45	NOT USED		
46	NOT USED		
47	NOT USED		
48	NOT USED		
49	NOT USED		
50	NOT USED		

Digital Monitor, P12

PIN	NAME	RA	FUNCTION
1	RA50-DM0	50	C
2	RA50-DM1		Not-H
3	RA50-DM2		X
4	RA50-DM3		Pump req.
5	RA50-DM4		
6	RA50-DM5		
7	RA50-DM6		CPU monitor
8	RA50-DM7		Manual/MCB control select
9	RA51-DM0	51	Bit 0 7-bit ID, ODD PARITY
10	RA51-DM1		Bit 1
11	RA51-DM2		2
12	RA51-DM3		3
13	RA51-DM4		4
14	RA51-DM5		5
15	RA51-DM6		6
16	RA51-DM7		Parity bit
17	RA51-DM8		Serial number, bit 0
18	RA51-DM9		Serial number, bit 1
19	RA51-DM10		Serial number, bit 2
20	RA51-DM11		Mod #, bit 0
21	RA51-DM12		Mod #, bit 1
22	RA51-DM13		Mod #, bit 2
23	RA52-DM0	52	CAL Control Select, bit 1
24	RA52-DM1		CAL Control Select, bit 0
25	RA52-DM2		Ext cal monitor
26	RA52-DM3		Ext SIG/REF mon
27	RA52-DM4		
28	RA52-DM5		
29	RA52-DM6		CCB cal monitor beam 1
30	RA52-DM7		CCB cal monitor beam 2
31	RA53-DM0	53	Phase con stat mon b0
32	RA53-DM1		Phase con stat mon b1
33	RA53-DM2		
34	RA53-DM3		
35	RA53-DM4		1S phase sw state
36	RA53-DM5		1D phase sw state
37	RA53-DM6		2S phase sw state
38	RA53-DM7		2S phase sw state
39	RA54-DM0	54	3S phase sw state
40	RA54-DM1		3D phase sw state
41	RA54-DM2		4S phase sw state
42	RA54-DM3		4S phase sw state
43	RA54-DM4		
44	RA54-DM5		
45	RA54-DM6		
46	RA54-DM7		
47	RA55-DM0	55	
48	RA55-DM1		
49	RA55-DM2		
50	RA55-DM3		

Digital Control, P13

PIN	NAME	RA	FUNCTION
1	RA48-DM0	48	C
2	RA48-DM1		not-H
3	RA48-DM2		X
4	N.C.		
5	RA49-DC0	49	Cal control select b0
6	RA49-DC1		Cal control select b1
7	RA49-DC2		
8	RA49-DC3		
9	RA49-DC4		MCB: cal 1 control
10	RA49-DC5		MCB: cal 2 control
11	N.C.		
12	N.C.		
13	RA4A-DC0	4A	Ext cal select B6
14	RA4A-DC1		Ext cal select B7
15	RA4A-DC2		
16	RA4A-DC3		MCB: 1S phase switch control
17	RA4A-DC4		MCB: 1D phase switch control
18	RA4A-DC5		MCB: 2S phase switch control
19	RA4A-DC6		MCB: 2D phase switch control
20	RA4A-DC7		
21	RA4B-DC0	4B	Cryo LNA 1Sa bias ON/OFF
22	RA4B-DC1		Cryo LNA 1Sb bias ON/OFF
23	RA4B-DC2		Cryo LNA 1Da bias ON/OFF
24	RA4B-DC3		Cryo LNA 1Da bias ON/OFF
25	RA4B-DC4		Cryo LNA 2Sa bias ON/OFF
26	RA4B-DC5		Cryo LNA 2Sa bias ON/OFF
27	RA4B-DC6		Cryo LNA 2Db bias ON/OFF
28	RA4B-DC7		Cryo LNA 2Da bias ON/OFF
29	RA4C-DC0	4C	
30	RA4C-DC1		
31	RA4C-DC2		
32	RA4C-DC3		
33	RA4D-DC0	4D	Phase switch control select b0
34	RA4D-DC1		Phase switch control select b1
35	RA4D-DC2		
36	RA4D-DC3		
37	RA4D-DC4		
38	RA4D-DC5		
39	RA4D-DC6		
40	RA4D-DC7		
41	RA4E-DC0	4E	Cryo LNA 3Sa bias ON/OFF
42	RA4E-DC1		Cryo LNA 3Sb bias ON/OFF
43	RA4E-DC2		Cryo LNA 3Da bias ON/OFF
44	RA4E-DC3		Cryo LNA 3Da bias ON/OFF
45	RA4E-DC4		Cryo LNA 4Sa bias ON/OFF
46	RA4E-DC5		Cryo LNA 4Sa bias ON/OFF
47	RA4E-DC6		Cryo LNA 4Da bias ON/OFF
48	RA4E-DC7		Cryo LNA 4Da bias ON/OFF

Analog Monitor	56 12-bit channels, -10 to +10 VDC	
Analog Control	8 12-bit channels, -10 to +10 VDC @ 5mA maximum	
Digital Monitor	IC = 74LS244	
	High level input voltage	2 to 5 volts
	Low level input voltage	0.8 Volts maximum
	High level input current	-15 mA maximum*
	Low level input current	23 mA maximum
	4 8-bit addresses	
	1 14-bit address	
	1 4-bit address	
Digital Control	IC = 74LS273	
	High level output voltage	2.7 Volts minimum
	Low level output voltage	0.5 Volta maximum
	High level output current	-800 microamps maximum
	Low level output current	16 mA maximum

*Current flowing out of a terminal is given as a negative value.

Appendix B

Summary of Motor Commands for the Thermal Calibration Optics

Command Set for Microstepping Motor Driver

Command Name	Function	Mnemonic	ASCII	Type
ESC	Abort	Esc	27	Immediate, global
@	Soft stop	@	64	Immediate, global, program
^C	Software reset	^C	03	Immediate, global
A	Port read/write	(name)A	65	Immediate, program
B	Set jog speeds	(name)B	66	Default, immediate, program
C	Clear and restore	(name)C	67	Immediate
D	Divide resolution	(name)D	68	Default, immediate, program
F	Find home	(name)F	70	Immediate, program
G	Go	(name)G	71	Immed, program, hardware
I	Initial velocity	(name)I	73	Immediate, default, program
K	Ramp slope	(name)K	75	Immediate, default, program
M	Move at fixed velocity	(name)M	77	Immed, program
O	Set origin	(name)O	79	Immed, program
P	Program mode	(name)P	80	Immediate
Q	Query stored program	(name)Q	81	Immediate
R	Relative index	(name)R	82	Immed, program
S	Store parameters	(name)S	83	Immediate
V	Slew velocity	(name)V	86	Immediate, default, program
+	+ Index	(name)+	43	Immediate, program
-	- Index	(name)-	45	Immediate, program
f	Find encoder index mark	(name)f	102	Immediate, program
o	Set origin	(name)o	111	Default
Z	Read encoder position	(name)z	122	Immediate